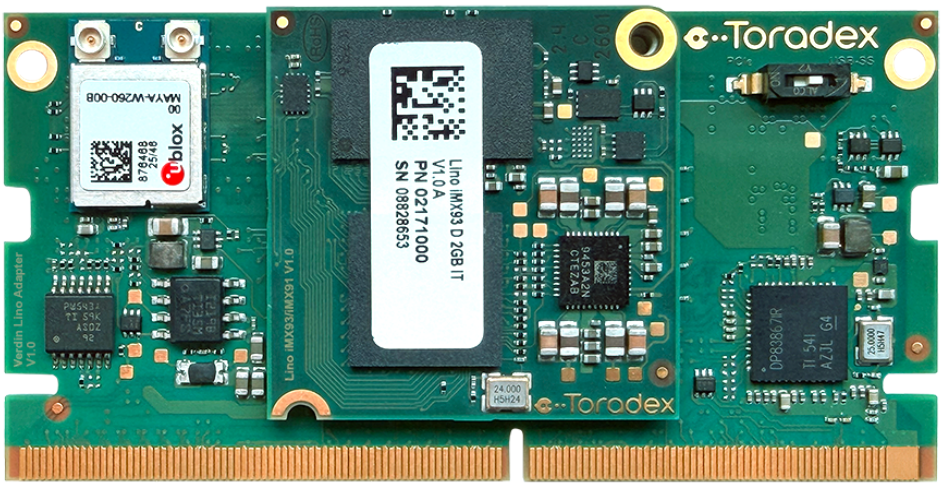
Toradex
Swiss. Embedded. Computing.

Lino-Verdin Adapter

Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
09-Mar-2026	Rev. 0.1	V1.0	Initial documentation
01-Jul-2026	Rev. 0.2	V1.1	Update documentation to reflect new product version

Contents

1 Introduction **7**
1.1 Purpose of the Datasheet . . . 7
1.2 Lino to Verdin Adapter Overview . . . 7

2 Architecture Overview **8**
2.1 Block Diagram . . . 8
2.2 Power Architecture . . . 10
2.3 System Control and Debug . . . 10
2.4 Physical Drawing . . . 11
2.4.1 Top Side Connectors . . . 11

3 Connectors **12**
3.1 Mating Connector (Adapter Board) . . . 12
3.2 Pin Assignment . . . 12

4 Interfaces Description **26**
4.1 Ethernet PHY . . . 26
4.2 PCIe / USB SuperSpeed Switching Circuit . . . 28
4.2.1 Signal Mapping . . . 28
4.2.2 Power and Decoupling . . . 28
4.2.3 Design Considerations . . . 28
4.3 Wi-Fi and Bluetooth PHY . . . 28

5 Test Points **31**

6 Operating Conditions **33**

7 Product Compliance **34**

8 Device and Documentation Support **35**
8.1 Trademarks . . . 35

List of Tables

1 Edge connector pin assignment (X1) . . . 13
2 Ethernet transceiver to Lino . . . 26
3 Ethernet transceiver to edge connector . . . 27
4 PCIe USB switch . . . 28
5 Wi-Fi/Bluetooth transceiver to Lino . . . 29
6 Wi-Fi/Bluetooth transceiver to edge connector . . . 29
7 Test points . . . 31
8 Absolute maximum ratings . . . 33

List of Figures

1 Lino-Verdin Adapter Block Diagram 9
2 Lino-Verdin Adapter top side connectors (top view) 11

Abbreviations

Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
BTB	Board To Board
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.

Continued on next page

Abbreviations (Continued)

Abbreviation	Explanation
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1 Introduction

1.1 Purpose of the Datasheet

This document describes the **hardware characteristics, functionality, and integration details** of the **Lino to Verdin Adapter**. The adapter enables **Lino System-on-Modules (SoMs)** to operate with **carrier boards designed for the Toradex Verdin family**, allowing developers to evaluate and prototype Lino-based systems using the existing Verdin ecosystem.

The **Lino to Verdin Adapter** translates the **mechanical and electrical interfaces** of the Lino module to the **Verdin connector architecture**, enabling compatibility with Verdin carrier boards. This allows developers to reuse **existing Verdin carrier board designs and development infrastructure**, accelerating system bring-up and early product development.

This document serves as a reference for **hardware designers, system integrators, and software developers** working with the **Lino to Verdin Adapter**. It provides the information required to understand the adapter architecture, interface mapping, and system integration considerations.

Supporting design resources for the adapter, including **schematic files and related hardware documentation**, are provided in the Developer Website[1].

1.2 Lino to Verdin Adapter Overview

The **Lino to Verdin Adapter** is a hardware interface board that enables **Lino System-on-Modules** to operate with **carrier boards designed for the Toradex Verdin family**. By adapting the Lino module interfaces to the Verdin connector layout, the adapter allows developers to leverage the **existing Verdin ecosystem**, including carrier boards, accessories, and development tools.

To maintain compatibility with the Verdin carrier board architecture, the adapter integrates additional supporting components and interface circuitry. These components provide system functionality typically expected by Verdin carrier boards, including networking and wireless connectivity.

The adapter integrates the following key hardware resources:

- **Ethernet PHY**, enabling Ethernet connectivity through standard Verdin carrier board network interfaces
- **Wi-Fi and Bluetooth connectivity**, providing wireless communication capabilities compatible with Verdin platform designs
- **Power management and supporting circuitry**, enabling proper power sequencing and signal conditioning between the Lino SoM and the Verdin platform

These integrated components allow the **Lino SoM** to operate on **Verdin carrier boards** with networking and peripheral capabilities aligned with the Verdin ecosystem.

The **Lino to Verdin Adapter** is primarily intended for **evaluation, development, and prototyping purposes**. For production systems, it is recommended to design a **custom carrier board for the Lino module**, ensuring optimal performance, cost efficiency, and system integration.

[1] https://developer.toradex.com/hardware/lino-som-family/add-ons/lino-verdin-adapter

2 Architecture Overview

This section provides an overview of the **hardware architecture of the Lino-Verdin Adapter** and the main functional building blocks that enable interoperability between **Lino System-on-Modules** and **Verdin carrier boards**. The adapter acts as a bridge between the **Lino board-to-board connectors** and the **Verdin X1 SODIMM connector**, ensuring that compatible interfaces are routed correctly while integrating additional components required to support the Verdin carrier board ecosystem.

Because the **Lino SoM connector architecture differs from the Verdin SODIMM interface**, certain peripherals and supporting circuitry must be implemented on the adapter itself. These include components such as the **Ethernet PHY, Wi-Fi/Bluetooth module, clock sources, and power management circuitry**, which allow the Lino module to provide functionality expected by Verdin carrier boards.

2.1 Block Diagram

The adapter architecture is organized into several functional subsystems including **power management, networking connectivity, high-speed interface routing, peripheral expansion, and system control logic**. Some interfaces are routed directly between the connectors, while others pass through dedicated functional blocks that provide protocol support, signal conditioning, or additional control logic.

The **Lino-Verdin Adapter** therefore integrates multiple hardware blocks that complement the Lino SoM functionality and enable compatibility with Verdin carrier boards. These blocks include components responsible for **power regulation and monitoring, Ethernet connectivity, wireless communication, clock generation, and system control**.

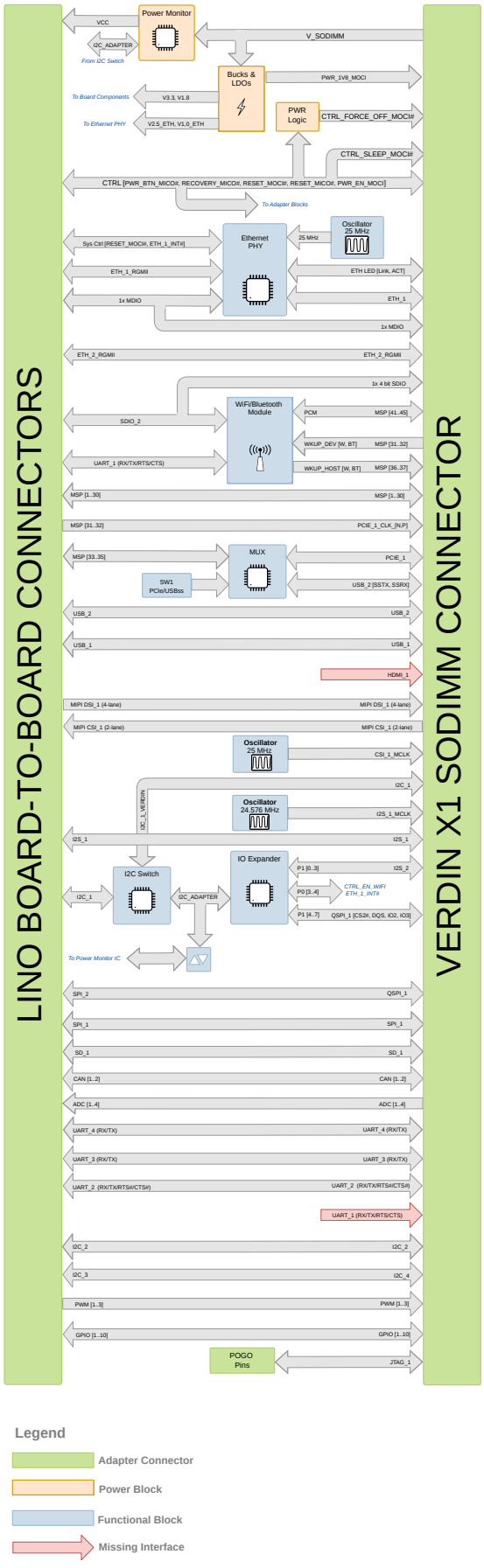
The following block diagram (Figure 1) illustrates the main architectural elements of the **Lino-Verdin Adapter**, highlighting the relationship between the **Lino module connectors**, the **Verdin carrier board connector**, and the intermediate functional blocks used to provide interface adaptation and additional system functionality.

The architecture can be divided into several functional domains including:

- **Power management and monitoring**
- **Ethernet connectivity**
- **Wireless connectivity**
- **High-speed interface routing and multiplexing**
- **Low-speed peripheral expansion**
- **Clock generation**
- **System control and debugging**

The block diagram also shows how signals from the **Lino SoM connectors** are routed either directly to the **Verdin SODIMM connector** or through intermediary functional blocks that provide protocol support, clocking resources, or additional control capabilities required by the adapter.

Figure 1: Lino-Verdin Adapter Block Diagram



Legend

- Adapter Connector
- Power Block
- Functional Block
- Missing Interface

2.2 Power Architecture

The adapter derives its main input supply from the **Verdin carrier board through the SODIMM connector**. This input voltage (**V_SODIMM**) is distributed to the power subsystem where **buck converters and LDO regulators** generate the required voltage rails used by the adapter components.

The power subsystem generates the rails required for:

- **Ethernet PHY supply domains**
- **Wireless module power**
- **logic and control circuitry**
- **adapter peripheral devices**

A **power monitor IC** connected to the adapter I^2C bus provides voltage and current monitoring for the adapter supply rails. This allows system software to supervise power conditions during operation.

In addition to voltage regulation, the adapter includes **power control logic** responsible for coordinating system signals such as power enable, reset, and sleep control between the Lino module and the Verdin carrier board.

2.3 System Control and Debug

The adapter routes several **system control signals** between the Lino SoM and the Verdin connector, including:

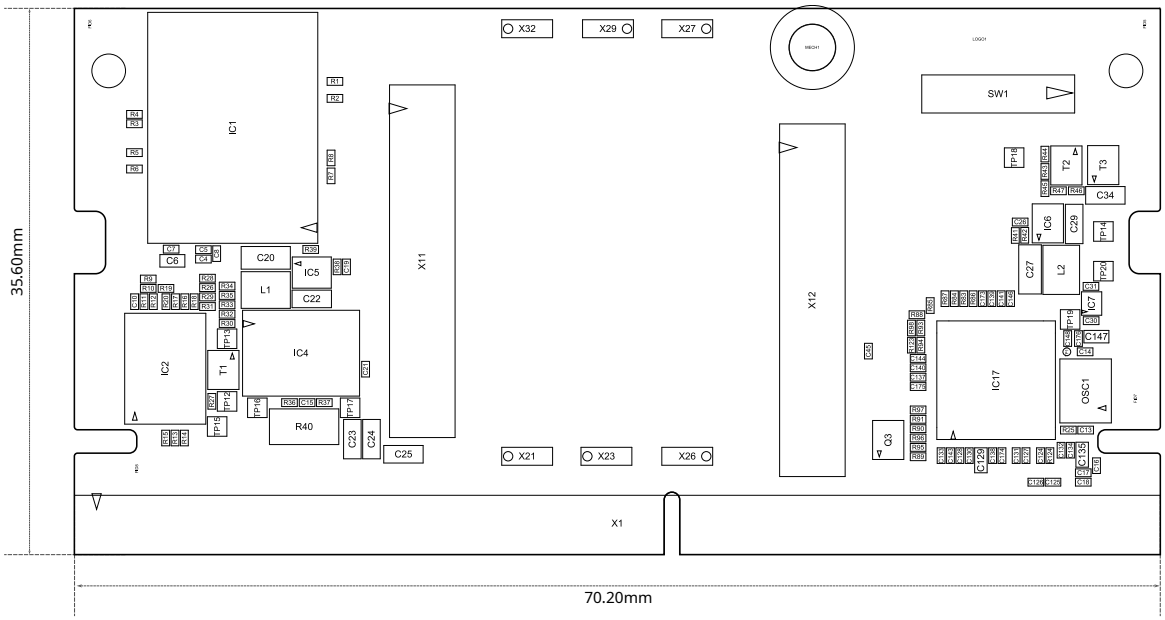
- **power button control**
- **system reset**
- **recovery mode control**
- **sleep and force-off signals**

Additionally, **debug access** is provided through dedicated **POGO pins**, allowing access to interfaces such as **JTAG** for development and debugging purposes.

2.4 Physical Drawing

2.4.1 Top Side Connectors

Figure 2: Lino-Verdin Adapter top side connectors (top view)



3 Connectors

The **Lino-Verdin Adapter** provides the mechanical and electrical interface between the **Lino System-on-Module** and **Verdin carrier boards** through a combination of **board-to-board connectors** and a **SODIMM edge connector**.

On the Lino side, the adapter connects to the module using **two Amphenol BergStak® board-to-board connectors** (refer to part number `10164228-1001A1RLF`). These connectors provide the mechanical and electrical interface between the **Lino SoM** and the adapter board. Together, they expose the full set of interfaces available on the Lino module, including **high-speed interfaces, low-speed peripheral signals, control lines, and multiple power domains**.

Each board-to-board connector provides **100 signal positions with a 0.40 mm pitch**, resulting in a **total of 200 interconnect pins** between the Lino module and the adapter. The fine-pitch BergStak® connector family is designed for **compact layouts and controlled-impedance routing**, enabling reliable implementation of high-speed interfaces. The connector system is optimized for **repeatable mating cycles and mechanical robustness**, making it suitable for both development and production environments.

On the carrier board side, the adapter exposes a **Verdin-compatible edge connector** that mates with the **Verdin X1 SODIMM connector** present on Verdin carrier boards. Through this connector, the adapter routes compatible signals from the Lino SoM and integrates additional hardware blocks required to provide functionality expected by Verdin carrier boards.

3.1 Mating Connector (Adapter Board)

Mating connectors for the carrier board are available with two stacking height options, the Lino-Verdin Adapter is equiped with the **1.5 mm version of the mating connector** to the connectors on the Lino SoM.

3.2 Pin Assignment

The pin assignment of the **Verdin edge connector** used by the adapter is described in Table 1. The table lists the signals routed between the **Lino SoM connectors** and the **Verdin carrier board interface**, together with their corresponding functions.

Additional details regarding signal compatibility and interface classification are described in the **Interfaces Description** section of this document.

Naming Convention
On the Lino iMX93 system-on-module, signals routed to connector **X1** are identified by pin names starting with **P** (for example, `P10` or `P12`), while signals routed to connector **X2** are identified by pin names starting with **S** (for example, `S28` or `S30`).

Table 1: Edge connector pin assignment (X1)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
Odd pins					
1	JTAG_1_TDI	–	–	POGO connector X21	JTAG test data input
3	JTAG_1_TRST#	–	–	POGO connector X27	JTAG test reset, active-low
5	JTAG_1_TDO	–	–	POGO connector X23	JTAG test data output
7	JTAG_1_VREF	–	–	POGO connector X26	JTAG reference voltage
9	JTAG_1_TCK	–	–	POGO connector X29	JTAG test clock
11	GND	GND	–	–	Ground reference
13	JTAG_1_TMS	–	–	POGO connector X32	JTAG test mode select
15	PWM_1	PWM_1	P1	–	Pulse-width modulation output
17	GPIO_9_DSI	GPIO_9	P46	–	General-purpose input/output
19	PWM_3_DSI	PWM_3	P5	–	Pulse-width modulation output
21	GPIO_10_DSI	GPIO_10	P48	–	General-purpose input/output
23	DSI_1_D3_N	DSI_1_D3_N	S34	–	MIPI DSI differential data lane 3 negative
25	DSI_1_D3_P	DSI_1_D3_P	S36	–	MIPI DSI differential data lane 3 positive
27	GND	GND	–	–	Ground reference
29	DSI_1_D2_N	DSI_1_D2_N	S40	–	MIPI DSI differential data lane 2 negative
31	DSI_1_D2_P	DSI_1_D2_P	S42	–	MIPI DSI differential data lane 2 positive
33	GND	GND	–	–	Ground reference
35	DSI_1_CLK_N	DSI_1_CLK_N	S46	–	MIPI DSI differential clock negative
37	DSI_1_CLK_P	DSI_1_CLK_P	S48	–	MIPI DSI differential clock positive

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
39	GND	GND	–	–	Ground reference
41	DSI_1_D1_N	DSI_1_D1_N	S52	–	MIPI DSI differential data lane 1 negative
43	DSI_1_D1_P	DSI_1_D1_P	S54	–	MIPI DSI differential data lane 1 positive
45	GND	GND	–	–	Ground reference
47	DSI_1_D0_N	DSI_1_D0_N	S58	–	MIPI DSI differential data lane 0 negative
49	DSI_1_D0_P	DSI_1_D0_P	S60	–	MIPI DSI differential data lane 0 positive
51	GND	GND	–	–	Ground reference
53	I2C_2_DSI_SDA	I2C_2_SDA	P20	–	I^2C bus data signal
55	I2C_2_DSI_SCL	I2C_2_SCL	P22	–	I^2C bus clock signal
57	–	I2C_3_HDMI_SDA	–	–	Not connected
59	–	I2C_3_HDMI_SCL	–	–	Not connected
61	–	HDMI_1_HPD	–	–	Not connected
63	–	HDMI_1_CEC	–	–	Not connected
65	GND	GND	–	–	Ground reference
67	–	–	–	–	Not connected
69	–	–	–	–	Not connected
71	GND	GND	–	–	Ground reference
73	–	–	–	–	Not connected
75	–	–	–	–	Not connected
77	GND	GND	–	–	Ground reference
79	–	–	–	–	Not connected
81	–	–	–	–	Not connected
83	GND	GND	–	–	Ground reference

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
85	–	–	–	–	Not connected
87	–	–	–	–	Not connected
89	GND	GND	–	–	Ground reference
91	CSI_1_MCLK	CSI_1_MCLK	–	25 MHz oscillator low power LVCMOS output oscillator	Camera module master clock
93	I2C_4_CSI_SDA	I2C_3_SDA	P24	–	I2C bus data signal
95	I2C_4_CSI_SCL	I2C_3_SCL	P26	–	I2C bus clock signal
97	GND	GND	–	–	Ground reference
99	–	–	–	–	Not connected
101	–	–	–	–	Not connected
103	GND	GND	–	–	Ground reference
105	–	–	–	–	Not connected
107	–	–	–	–	Not connected
109	GND	GND	–	–	Ground reference
111	CSI_1_CLK_P	CSI_1_CLK_P	S76	–	MIPI CSI differential clock positive
113	CSI_1_CLK_N	CSI_1_CLK_N	S78	–	MIPI CSI differential clock negative
115	GND	GND	–	–	Ground reference
117	CSI_1_D1_P	CSI_1_D1_P	S82	–	MIPI CSI differential data lane 1 positive
119	CSI_1_D1_N	CSI_1_D1_N	S84	–	MIPI CSI differential data lane 1 negative
121	GND	GND	–	–	Ground reference
123	CSI_1_D0_P	CSI_1_D0_P	S88	–	MIPI CSI differential data lane 0 positive
125	CSI_1_D0_N	CSI_1_D0_N	S90	–	MIPI CSI differential data lane 0 negative
127	GND	GND	–	–	Ground reference
129	UART_1_RXD	–	–	–	Not connected

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
131	UART_1_TXD	–	–	–	Not connected
133	UART_1_RTS	–	–	–	Not connected
135	UART_1_CTS	–	–	–	Not connected
137	UART_2_RXD	UART_2_RXD	P13	–	UART receive data
139	UART_2_TXD	UART_2_TXD	P15	–	UART transmit data
141	UART_2_RTS	UART_2_RTS	S5	–	UART request to send
143	UART_2_CTS	UART_2_CTS	S7	–	UART clear to send
145	GND	GND	–	–	Ground reference
147	UART_3_RXD	UART_3_RXD	P17	–	UART receive data
149	UART_3_TXD	UART_3_TXD	P19	–	UART transmit data
151	UART_4_RXD	UART_4_RXD	P23	–	UART receive data
153	UART_4_TXD	UART_4_TXD	P25	–	UART transmit data
155	USB_1_EN	USB_1_EN	P27	–	USB power enable
157	USB_1_OC#	USB_1_OC#	P29	–	USB overcurrent indication, active-low
159	USB_1_VBUS	USB_1_VBUS	P31	–	USB VBUS power sense
161	USB_1_ID	–	–	GPIO Expander PCAL6416AHF, pin P0_1 (2)	USB OTG identification signal
163	USB_1_D_N	USB_1_D_N	P33	–	USB 2.0 differential data negative
165	USB_1_D_P	USB_1_D_P	P35	–	USB 2.0 differential data positive
167	GND	GND	–	–	Ground reference
169	USB_2_SSTX_N[1]	MSP_35	–	Differential multiplexer TMUXHS4212, pin 17	USB SuperSpeed transmit differential negative
171	USB_2_SSTX_P[1]	MSP_36	–	Differential multiplexer TMUXHS4212, pin 16	USB SuperSpeed transmit differential positive
173	GND	GND	–	–	Ground reference

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
175	USB_2_SSRX_N[1]	MSP_33	–	Differential multiplexer TMUXHS4212, pin 19	USB SuperSpeed receive differential negative
177	USB_2_SSRX_P[1]	MSP_34	–	Differential multiplexer TMUXHS4212, pin 18	USB SuperSpeed receive differential positive
179	GND	GND	–	–	Ground reference
181	USB_2_D_N	USB_2_D_N	P57	–	USB 2.0 differential data negative
183	USB_2_D_P	USB_2_D_P	P59	–	USB 2.0 differential data positive
185	USB_2_EN	USB_2_EN	P61	–	USB power enable
187	USB_2_OC#	USB_2_OC#	P63	–	USB overcurrent indication, active-low
189	–	ETH_2_RGMII_INT#	–	–	Not connected
191	ETH_2_RGMII_MDIO	ETH_MDIO	P67	Gigabit ethernet transceiver DP83867IRRGZR, MDIO (17)	Ethernet management data I/O with 1 kΩ pull-up to +V1.8
193	ETH_2_RGMII_MDC	ETH_MDC	P69	Gigabit ethernet transceiver DP83867IRRGZR, MDC (16)	Ethernet management data clock
195	GND	GND	–	–	Ground reference
197	ETH_2_RGMII_RXC	ETH_2_RGMII_RXC	S71	–	RGMII receive clock
199	ETH_2_RGMII_RX_CTL	ETH_2_RGMII_RX_CTL	S73	–	RGMII receive control
201	ETH_2_RGMII_RXD_0	ETH_2_RGMII_RXD0	S77	–	RGMII receive data 0
203	ETH_2_RGMII_RXD_1	ETH_2_RGMII_RXD1	S79	–	RGMII receive data 1
205	ETH_2_RGMII_RXD_2	ETH_2_RGMII_RXD2	S81	–	RGMII receive data 2
207	ETH_2_RGMII_RXD_3	ETH_2_RGMII_RXD3	S83	–	RGMII receive data 3
209	GND	GND	–	–	Ground reference
211	ETH_2_RGMII_TX_CTL	ETH_2_RGMII_TX_CTL	S89	–	RGMII transmit control
213	ETH_2_RGMII_TXC	ETH_2_RGMII_TXC	S87	–	RGMII transmit clock
215	ETH_2_RGMII_TXD_3	ETH_2_RGMII_TXD3	S91	–	RGMII transmit data 3

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
217	ETH_2_RGMII_TXD_2	ETH_2_RGMII_TXD2	S93	–	RGMII transmit data 2
219	ETH_2_RGMII_TXD_1	ETH_2_RGMII_TXD1	S97	–	RGMII transmit data 1
221	ETH_2_RGMII_TXD_0	ETH_2_RGMII_TXD0	S99	–	RGMII transmit data 0
223	GND	GND	–	–	Ground reference
225	ETH_1_MDI0_P	ETH_1_MDIO_P	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_P_A (1)	Ethernet MDI pair 0 positive
227	ETH_1_MDI0_N	ETH_1_MDIO_N	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_M_A (2)	Ethernet MDI pair 0 negative
229	GND	GND	–	–	Ground reference
231	ETH_1_MDI1_N	ETH_1_MDI1_N	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_M_B (5)	Ethernet MDI pair 1 negative
233	ETH_1_MDI1_P	ETH_1_MDI1_P	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_P_B (4)	Ethernet MDI pair 1 positive
235	ETH_1_LED_1	ETH_1_ACT	–	Gigabit ethernet transceiver DP83867IRRGZR, LED_2 (45)	Ethernet LED output with 7 Ω pull-down
237	ETH_1_LED_2	ETH_1_LINK	–	Gigabit ethernet transceiver DP83867IRRGZR, LED_0 (47)	Ethernet LED output with 7 Ω pull-down
239	ETH_1_MDI2_P	ETH_1_MDI2_P	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_P_C (7)	Ethernet MDI pair 2 positive
241	ETH_1_MDI2_N	ETH_1_MDI2_N	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_M_C (8)	Ethernet MDI pair 2 negative
243	GND	GND	–	–	Ground reference
245	ETH_1_MDI3_N	ETH_1_MDI3_N	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_M_D (11)	Ethernet MDI pair 3 negative
247	ETH_1_MDI3_P	ETH_1_MDI3_P	–	Gigabit ethernet transceiver DP83867IRRGZR, TD_P_D (10)	Ethernet MDI pair 3 positive
249	–	–	–	–	Not connected
251	+V_SODIMM	VCC	–	–	Main supply input

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
253	+V_SODIMM	VCC	–	–	Main supply input
255	+V_SODIMM	VCC	–	–	Main supply input
257	+V_SODIMM	VCC	–	–	Main supply input
259	+V_SODIMM	VCC	–	–	Main supply input
Even pins					
2	ADC_1	ADC_1	P2	–	Analog-to-digital converter input
4	ADC_2	ADC_2	P4	–	Analog-to-digital converter input
6	ADC_3	ADC_3	S1	–	Analog-to-digital converter input
8	ADC_4	ADC_4	S3	–	Analog-to-digital converter input
10	GND	GND	–	–	Ground reference
12	I2C_1_SDA	I2C_1_VERDIN_SDA	–	I^2C Switch SDA (13)	I^2C bus data signal with 2.2 kΩ pull-up to +V1.8
14	I2C_1_SCL	I2C_1_VERDIN_SCL	–	I^2C Switch SCI (10)	I^2C bus clock signal with 2.2 kΩ pull-up to +V1.8
16	PWM_2	PWM_2	P3	–	Pulse-width modulation output
18	GND	GND	–	–	Ground reference
20	CAN_1_TX	CAN_1_TX	P10	–	CAN transmit signal
22	CAN_1_RX	CAN_1_RX	P12	–	CAN receive signal
24	CAN_2_TX	CAN_2_TX	S28	–	CAN transmit signal
26	CAN_2_RX	CAN_2_RX	S30	–	CAN receive signal
28	GND	GND	–	–	Ground reference
30	I2S_1_BCLK	I2S_1_BCLK	S94	–	I2S bit clock
32	I2S_1_SYNC	I2S_1_SYNC	S96	–	I2S frame sync
34	I2S_1_D_OUT	I2S_1_D_OUT	S98	–	I2S serial data output

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
36	I2S_1_D_IN	I2S_1_D_IN	S100	–	I2S serial data input
38	I2S_1_MCLK	–	–	25 MHz oscillator low power LVCMOS output oscillator	I2S master clock
40	GND	GND	–	–	Ground reference
42	I2S_2_BCLK	I2S_2_BCLK	–	GPIO Expander PCAL6416AHF, pin P1_0 (10)	I2S bit clock
44	I2S_2_SYNC	I2S_2_SYNC	–	GPIO Expander PCAL6416AHF, pin P1_3 (13)	I2S frame sync
46	I2S_2_D_OUT	I2S_2_D_OUT	–	GPIO Expander PCAL6416AHF, pin P1_2 (12)	I2S serial data output
48	I2S_2_D_IN	I2S_2_D_IN	–	GPIO Expander PCAL6416AHF, pin P1_1 (11)	I2S serial data input
50	GND	GND	–	–	Ground reference
52	QSPI_1_CLK	SPI_2_CLK	S20	–	QuadSPI clock
54	QSPI_1_CS#	SPI_2_CS	S18	–	QuadSPI chip select, active-low
56	QSPI_1_IO0	SPI_2_MOSI	S22	–	QuadSPI data I/O 0
58	QSPI_1_IO1	SPI_2_MISO	S24	–	QuadSPI data I/O 1
60	QSPI_1_IO2	QSPI_1_IO2	–	GPIO Expander PCAL6416AHF, pin P1_6 (16)	QuadSPI data I/O 2
62	QSPI_1_IO3	QSPI_1_IO3	–	GPIO Expander PCAL6416AHF, pin P1_7 (17)	QuadSPI data I/O 3
64	QSPI_1_CS2#	QSPI_1_CS2#	–	GPIO Expander PCAL6416AHF, pin P1_4 (14)	QuadSPI second chip select, active-low
66	QSPI_1_DQS	QSPI_1_DQS	–	GPIO Expander PCAL6416AHF, pin P1_5 (15)	QuadSPI data strobe
68	GND	GND	–	–	Ground reference
70	SD_1_D2	SD_1_D2	P60	–	SD card data D2
72	SD_1_D3	SD_1_D3	P64	–	SD card data D3

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
74	SD_1_CMD	SD_1_CMD	P66	–	SD card command signal
76	SD_1_PWR_EN	SD_1_PWR_EN	P72	–	SD card power enable
78	SD_1_CLK	SD_1_CLK	P68	–	SD card clock
80	SD_1_D0	SD_1_D0	P74	–	SD card data D0
82	SD_1_D1	SD_1_D1	P76	–	SD card data D1
84	SD_1_CD#	SD_1_CD#	P78	–	SD card card detect, active-low
86	GND	GND	–	–	Ground reference
88	MSP_1/2_N	MSP_1	S11	–	Module-specific signal
90	MSP_1/2_P	MSP_2	S13	–	Module-specific signal
92	MSP_3	MSP_3	S15	–	Module-specific signal
94	MSP_4/5_N	MSP_4	S17	–	Module-specific signal
96	MSP_4/5_P	MSP_5	S19	–	Module-specific signal
98	GND	GND	–	–	Ground reference
100	MSP_6/7_N	MSP_6	S23	–	Module-specific signal
102	MSP_6/7_P	MSP_7	S25	–	Module-specific signal
104	MSP_8	MSP_8	S27	–	Module-specific signal
106	MSP_9/10_N	MSP_9	S29	–	Module-specific signal
108	MSP_1/10_P	MSP_10	S31	–	Module-specific signal
110	GND	GND	–	–	Ground reference
112	MSP_11/12_N	MSP_11	S35	–	Module-specific signal
114	MSP_11/12_P	MSP_12	S37	–	Module-specific signal
116	MSP_13	MSP_13	S39	–	Module-specific signal
118	MSP_14/15_N	MSP_14	S41	–	Module-specific signal

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
120	MSP_14/15_P	MSP_15	S43	–	Module-specific signal
122	GND	GND	–	–	Ground reference
124	MSP_16/17_N	MSP_16	S47	–	Module-specific signal
126	MSP_16/17_P	MSP_17	S49	–	Module-specific signal
128	MSP_18	MSP_18	S51	–	Module-specific signal
130	MSP_19/20_N	MSP_19	S53	–	Module-specific signal
132	MSP_19/20_P	MSP_20	S55	–	Module-specific signal
134	GND	GND	–	–	Ground reference
136	MSP_21/22_N	MSP_21	S59	–	Module-specific signal
138	MSP_21/22_P	MSP_22	S61	–	Module-specific signal
140	MSP_23	MSP_23	S63	–	Module-specific signal
142	MSP_24/25_N	MSP_24	S65	–	Module-specific signal
144	MSP_24/25_P	MSP_25	S67	–	Module-specific signal
146	GND	GND	–	–	Ground reference
148	MSP_26/27_N	MSP_26	S64	–	Module-specific signal
150	MSP_26/27_P	MSP_27	S66	–	Module-specific signal
152	MSP_28	MSP_28	S68	–	Module-specific signal
154	MSP_29/30_N	MSP_29	S70	–	Module-specific signal
156	MSP_29/30_P	MSP_30	S72	–	Module-specific signal
158	GND	GND	–	–	Ground reference
160	WiFi_BT_WKUP_DEV	MSP_31	–	IC1 – BT_DEV_WAKE (J9)	Module-specific signal with 100 kΩ pull-up to +V1.8
162	WiFi_W_WKUP_DEV	MSP_32	–	IC1 – WLAN_DEV_WAKE (J8)	Module-specific signal with 100 kΩ pull-up to +V1.8

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
164	MSP_33	MSP_33	–	–	Not connected
166	MSP_34	MSP_34	–	–	Not connected
168	MSP_35	MSP_35	–	–	Not connected
170	GND	GND	–	–	Ground reference
172	WiFi_BT_WKUP_HOST	MSP_36	–	IC1 – BT_WAKE_HOST (E7)	Module-specific signal with 100 kΩ pull-up to +V1.8
174	WiFi_W_WKUP_HOST	MSP_37	–	IC1 – WLAN_WAKE_HOST (F7)	Module-specific signal with 100 kΩ pull-up to +V1.8
176	MSP_38	MSP_38	–	–	Not connected
178	WiFi_LTE_COEX_IN	MSP_39	–	IC1 – WCI_SIN (C6)	Module-specific signal
180	WiFi_LTE_COEX_OUT	MSP_40	–	IC1 – WCI_SOUT (B6)	Module-specific signal
182	GND	GND	–	–	Ground reference
184	PCM_CLK	MSP_41	–	IC1 – PCM_CLK (D8)	Module-specific signal
186	PCM_DIN	MSP_42	–	IC1 – PCM_DIN (E9)	Module-specific signal
188	PCM_DOUT	MSP_43	–	IC1 – PCM_DOUT (F9)	Module-specific signal
190	PCM_SYNC	MSP_44	–	IC1 – PCM_SYNC (F8)	Module-specific signal
192	PCM_MCLK	MSP_45	–	IC1 – PCM_MCLK (E8)	Module-specific signal
194	GND	GND	–	–	Ground reference
196	SPI_1_CLK	SPI_1_CLK	P52	–	SPI clock
198	SPI_1_MISO	SPI_1_MISO	P54	–	SPI controller input, peripheral output
200	SPI_1_MOSI	SPI_1_MOSI	P56	–	SPI controller output, peripheral input
202	SPI_1_CS	SPI_1_CS	P58	–	SPI chip select
204	GND	GND	–	–	Ground reference
206	GPIO_1	GPIO_1	P30	–	General-purpose input/output

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
208	GPIO_2	GPIO_2	P32	–	General-purpose input/output
210	GPIO_3	GPIO_3	P34	–	General-purpose input/output
212	GPIO_4	GPIO_4	P36	–	General-purpose input/output
214	+V1.8	PWR_1V8_MOCI	–	–	1.8 V control and interface supply
216	GPIO_5_CSI	GPIO_5	P38	–	General-purpose input/output
218	GPIO_6_CSI	GPIO_6	P40	–	General-purpose input/output
220	GPIO_7_CSI	GPIO_7	P42	–	General-purpose input/output
222	GPIO_8_CSI	GPIO_8	P44	–	General-purpose input/output
224	GND	GND	–	–	Ground reference
226	PCIE_1_CLK_N	MSP_31	P39	–	PCIe reference clock negative
228	PCIE_1_CLK_P	MSP_32	P41	–	PCIe reference clock positive
230	GND	GND	–	–	Ground reference
232	PCIE_1_L0_RX_N[1]	MSP_33	–	Differential multiplexer TMUXHS4212, pin 15 (15)	PCIe lane 0 receive negative
234	PCIE_1_L0_RX_P[1]	MSP_34	–	Differential multiplexer TMUXHS4212, pin 14 (14)	PCIe lane 0 receive positive
236	GND	GND	–	–	Ground reference
238	PCIE_1_L0_TX_N[1]	MSP_35	–	Differential multiplexer TMUXHS4212, pin 13 (13)	PCIe lane 0 transmit negative
240	PCIE_1_L0_TX_P[1]	MSP_36	–	Differential multiplexer TMUXHS4212, pin 12 (12)	PCIe lane 0 transmit positive
242	GND	GND	–	–	Ground reference
244	PCIE_1_RESET#	–	–	GPIO Expander PCAL6416AHF, pin P0_0 (1)	PCIe reset, active-low
246	CTRL_RECOVERY_MICO#	CTRL_RECOVERY_MICO	P80	–	Recovery mode control, active-low
248	CTRL_PWR_BTN_MICO#	CTRL_PWR_BTN_MICO	P82	–	Power button control, active-low

Continued on next page

Table 1: Edge connector pin assignment (X1) (Continued)

X1 pin	Module specification signal name	B2B function name	B2B pin number	Non-SoC function name (pin number)	Description/Remarks
250	CTRL_FORCE_OFF_MOCI#	–	–	–	Force-off control, active-low
252	CTRL_WAKE1_MICO#	–	–	GPIO Expander PCAL6416AHF, pin P0_2 (3)	Wake input, active-low with 100 kΩ pull-up to +V1.8
254	CTRL_PWR_EN_MOCI	–	–	IC5 EN (4)	Power enable control
256	CTRL_SLEEP_MOCI#	–	–	IC5 EN (4)	Sleep control, active-low
258	CTRL_RESET_MOCI#	–	–	IC1 WLAN_RESET (H7)	Module reset, active-low with 100 kΩ pull-up to +V1.8
260	CTRL_RESET_MICO#	–	–	T2 G (5)	Carrier/control reset, active-low

[1] Multiplexed interface between USB_2 SuperSpeed differential pairs and PCIe lane 0 differential pairs.

4 Interfaces Description

The **Lino-Verdin Adapter** integrates the physical layer devices required to provide networking functionality compatible with **Verdin carrier boards**. These components implement the hardware interface between the **MAC interfaces available on the Lino SoM** and the external network interfaces exposed through the **Verdin edge connector (X1)**.

The adapter includes dedicated PHY implementations for the following interfaces:

- **Ethernet PHY**
- **Wi-Fi/Bluetooth PHY**

These devices are implemented directly on the adapter and connect to the **Lino board-to-board connectors (X11 and X12)** on one side and to the **Verdin edge connector (X1)** on the other side.

Signal assignments for the connectors involved in these interfaces are described in the following tables:

- Signals from the **Lino board-to-board connector X11**
- Signals from the **Lino board-to-board connector X12**
- Signals exposed through the **Verdin edge connector X1**

4.1 Ethernet PHY

The adapter integrates an **Ethernet PHY** implementing the physical layer of the Ethernet interface.

The PHY connects to the **RGMII interface of the Lino SoM** through the **X11/X12 board-to-board connectors** and exposes the Ethernet interface through the **Verdin edge connector (X1)**. This allows the Lino SoM to provide standard Ethernet connectivity when used with Verdin carrier boards.

The Ethernet subsystem includes the following signals:

- **RGMII transmit and receive data paths**
- **MDIO management interface**
- **Ethernet interrupt signal**
- **Ethernet link and activity LED signals**
- **25 MHz reference clock**

The signal assignments are listed in:

- Table 2: ethernet signals exposed through the **board-to-board connectors X11 and X12**
- Table 3: ethernet signals exposed through the **Verdin edge connector X1**

Table 2: Ethernet transceiver to Lino

X11 pin	Adapter signal name	Ethernet transceiver signal name (pin)	I/O	Description/Remarks
Managemente Signals				
P67	ETH_MDIO	MDIO (17)	I/O	Ethernet management data input/output signal with 1 kΩ pull-up to +V1.8
P69	ETH_MDC	MDC (16)	O	Ethernet management data clock signal

Continued on next page

Table 2: Ethernet transceiver to Lino (Continued)

X11 pin	Adapter signal name	Ethernet transceiver signal name (pin)	I/O	Description/Remarks
Data Signals				
P73	ETH_1_RGMII_RXC	RX_CLK (32)	O	RGMII receive clock signal
P75	ETH_1_RGMII_RX_CTL	RX_CTRL (38)	O	RGMII receive control signal with 5.76 kΩ and 2.49 kΩ +V1.8 voltage divider
P77	ETH_1_RGMII_RXD_0	RX_D0 (33)	O	RGMII receive data bit 0 with 10 kΩ and 2.49 kΩ +V1.8 voltage divider
P79	ETH_1_RGMII_RXD_1	RX_D1 (34)	O	RGMII receive data bit 1
P81	ETH_1_RGMII_RXD_2	RX_D2 (35)	O	RGMII receive data bit 2
P83	ETH_1_RGMII_RXD_3	RX_D3 (36)	O	RGMII receive data bit 3
P85	ETH_1_RGMII_TX_CTL	TX_CTRL (37)	I	RGMII transmit control signal
P89	ETH_1_RGMII_TXC	GTX_CLK (29)	I	RGMII transmit clock signal
P97	ETH_1_RGMII_TXD_0	TX_D0 (28)	I	RGMII transmit data bit 0
P95	ETH_1_RGMII_TXD_1	TX_D1 (27)	I	RGMII transmit data bit 1
P93	ETH_1_RGMII_TXD_2	TX_D2 (26)	I	RGMII transmit data bit 2
P91	ETH_1_RGMII_TXD_3	TX_D3 (25)	I	RGMII transmit data bit 3

Table 3: Ethernet transceiver to edge connector

X1 pin	Adapter signal name	Ethernet transceiver signal name (pin)	I/O	Description/Remarks
Control Signals				
191	ENET_MDIO	MDIO (17)	I/O	Ethernet MDIO management data signal with 1 kΩ pull-up to +V1.8
193	ENET_MDC	MDC (16)	I	Ethernet MDIO management clock signal
Data Signals				
225	ETH_1_MDI0_P	TD_P_A (1)	I/O	Ethernet MDI pair A positive signal
227	ETH_1_MDI0_N	TD_M_A (2)	I/O	Ethernet MDI pair A negative signal
231	ETH_1_MDI1_N	TD_M_B (5)	I/O	Ethernet MDI pair B negative signal
233	ETH_1_MDI1_P	TD_P_B (4)	I/O	Ethernet MDI pair B positive signal
239	ETH_1_MDI2_P	TD_P_C (7)	I/O	Ethernet MDI pair C positive signal
241	ETH_1_MDI2_N	TD_M_C (8)	I/O	Ethernet MDI pair C negative signal
245	ETH_1_MDI3_N	TD_M_D (11)	I/O	Ethernet MDI pair D negative signal
247	ETH_1_MDI3_P	TD_P_D (10)	I/O	Ethernet MDI pair D positive signal
LED Signals				
235	ETH_1_LED_2	LED_0 (47)	O	Ethernet LED signal, indicates that link is established with 1 kΩ pull-up to +V1.8
237	ETH_1_LED_1	LED_2 (45)	O	Ethernet LED signal, indicates receive or transmit activity with 1 kΩ pull-up to +V1.8
Reset Signal				
258	CTRL_RESET_MOCI#	RESET (43)	I	Ethernet PHY reset signal with 100 kΩ pull-up to +V1.8

4.2 PCIe / USB SuperSpeed Switching Circuit

This design implements a high-speed signal multiplexing stage that allows the shared differential lanes to operate either as **PCIe Gen1** or **USB 2.0 SuperSpeed (USB 3.x)**, depending on system configuration. The switching function is realized using the **TMUXHS4212IRKS (IC9)**, a high-speed differential signal multiplexer. This device routes two pairs of differential signals between the SoC (MSP interface) and the external connector (X1), enabling dynamic selection between PCIe and USB SuperSpeed modes.

4.2.1 Signal Mapping

The MSP high-speed differential pairs are connected to the A-side of the multiplexer, while the switched outputs are routed either to the USB SuperSpeed interface or to the PCIe interface on connector X1. The detailed signal assignment between the connector pins and the multiplexer pins is given in Table 4.

A manual configuration switch is provided to select the interface mode. The switch is pulled up to **1.8 V** through a **10 kΩ** resistor, selecting **PCI Express (PCIe)** by default when left open. Closing the switch overrides the pull-up and selects **USB SuperSpeed (USB SS)** operation. The interface mode is determined during system initialization.

Table 4: PCIe USB switch

X1 pin	Verdin function name	Multiplexer function name (pin)	I/O	Description/Remarks
PCIe Signals				
175	USB_2_SSRX_N	B0_P (19)	I/O	USB SuperSpeed RX negative
177	USB_2_SSRX_P	B0_N (18)	I/O	USB SuperSpeed RX positive
169	USB_2_SSTX_N	B1_P (17)	I/O	USB SuperSpeed TX negative
171	USB_2_SSTX_P	B1_N (16)	I/O	USB SuperSpeed TX positive
USB Signals				
232	PCIE_1_L0_RX_N	C0_P (15)	I/O	PCIe Lane 0 RX negative
234	PCIE_1_L0_RX_P	C0_N (14)	I/O	PCIe Lane 0 RX positive
238	PCIE_1_L0_TX_N	C1_P (13)	I/O	PCIe Lane 0 TX negative
240	PCIE_1_L0_TX_P	C1_N (12)	I/O	PCIe Lane 0 TX positive

4.2.2 Power and Decoupling

The multiplexer is powered from the 1.8 V rail. Local decoupling is provided by 100 nF capacitors, placed close to the supply pins of the device.

4.2.3 Design Considerations

Because the circuit switches high-speed differential pairs, PCB layout must preserve signal integrity. In particular, the USB SuperSpeed and PCIe lanes are routed as controlled-impedance differential pairs with tight intra-pair length matching and minimal discontinuities. Stub lengths should be kept as short as possible, and the placement of the multiplexer should minimize the total path length on both switched interfaces.

4.3 Wi-Fi and Bluetooth PHY

Wireless connectivity is provided through an integrated **Wi-Fi/Bluetooth module** on the adapter. This module implements the **radio and physical layer functionality** required for wireless networking and Bluetooth communication.

The wireless PHY connects to the Lino SoM through the **X11/X12 board-to-board connectors** using multiple control and data interfaces and exposes the wireless functionality through the Verdin interface.

The corresponding signal assignments are listed in:

- Table 5: ethernet signals exposed through the **board-to-board connectors X11 and X12**
- Table 6: ethernet signals exposed through the **Verdin edge connector X1**

Table 5: Wi-Fi/Bluetooth transceiver to Lino

X11/X12 pin	Adapter signal name	Wi-Fi transceiver signal name (pin)	I/O	Description/Remarks
X11 Signals				
P11	UART_1_TXD	UART_RX (G8)	I	UART transmit data signal
P6	UART_1_RTS	UART_CTSn (H8)	I	UART request-to-send control signal
P8	UART_1_CTS	UART_RTSn (H9)	O	UART clear-to-send control signal
P9	UART_1_RXD	UART_TX (G9)	O	UART receive data signal
X12 Signals				
S8	SD_2_CMD	SD_CMD (B4)	I	SDIO command signal
S10	SD_2_CLK	SD_CLK (A4)	I	SDIO clock signal
S12	SD_2_D0	SD_DAT0 (B3)	I/O	SDIO data bit 0
S16	SD_2_D1	SD_DAT1 (A3)	I/O	SDIO data bit 1
S2	SD_2_D2	SD_DAT2 (B5)	I/O	SDIO data bit 2
S4	SD_2_D3	SD_DAT3 (A5)	I/O	SDIO data bit 3

Table 6: Wi-Fi/Bluetooth transceiver to edge connector

X1 pin	Adapter signal name	Wi-Fi transceiver signal name (pin)	I/O	Description/Remarks
Wake Signals				
160	MSP_31	BT_DEV_WAKE (J9)	I	Bluetooth device wake signal with 100 kΩ pull-up to +V1.8
162	MSP_32	WLAN_DEV_WAKE (J8)	I	Wi-Fi device wake signal with 100 kΩ pull-up to +V1.8
172	MSP_36	BT_WAKE_HOST (E7)	O	Bluetooth host wake signal with 100 kΩ pull-up to +V1.8
174	MSP_37	WLAN_WAKE_HOST (F7)	O	Wi-Fi host wake signal with 100 kΩ pull-up to +V1.8
Coexistence Interface Signals				
178	MSP_39	WCI_SIN (C6)	I	Wireless coexistence interface input signal
180	MSP_40	WCI_SOUT (B6)	O	Wireless coexistence interface output signal

Continued on next page

Table 6: Wi-Fi/Bluetooth transceiver to edge connector (Continued)

X1 pin	Adapter signal name	Wi-Fi transceiver signal name (pin)	I/O	Description/Remarks
Pulse Code Modulation Signals				
184	MSP_41	PCM_CLK (D8)	O	PCM clock signal used by the Bluetooth audio interface
186	MSP_42	PCM_DIN (E9)	I	PCM data input signal used by the Bluetooth audio interface
188	MSP_43	PCM_DOUT (F9)	O	PCM data output signal used by the Bluetooth audio interface
190	MSP_44	PCM_SYNC (F8)	O	PCM frame synchronization signal used by the Bluetooth audio interface
192	MSP_45	PCM_MCLK (E8)	O	Master clock signal for the PCM audio interface used by the Bluetooth sub-system
Control Signals				
–	CTRL_EN_WIFI		–	Enable signal from GPIO Expander P0_4
258	CTRL_RESET_MOCI#	WLAN_RESET (H7)	O	Active-low reset signal used to reset the Wi-Fi/Bluetooth PHY module with 100 kΩ pull-up to +V1.8

5 Test Points

The **Lino-Verdin Adapter** includes a set of **test points (TPs)** that support debugging, signal observation, and hardware validation during development, manufacturing, and system bring-up. These test points provide convenient electrical access to selected signals on the adapter without interfering with normal operation, allowing engineers to monitor signals, verify power rails, and troubleshoot system behavior during integration with both the **Lino System-on-Module** and **Verdin carrier boards**.

Each test point is identified by a unique reference designator (for example, `TP01`, `TP02`) and is connected to specific signals available on the adapter. These signals may include **power supply rails, reset and control signals, communication interfaces, and selected status or debug signals** associated with the adapter circuitry. The test points are intended primarily for **measurement, validation, and debugging purposes** and should not be used as permanent system interfaces.

Where applicable, the electrical characteristics of the monitored signals (such as the presence of **pull-up or pull-down resistors** or connections to internal adapter circuitry) should be considered when performing measurements to ensure correct interpretation of signal levels.

Table 7 lists the test points available on the **Lino-Verdin Adapter**, providing access to selected debug, power, and control signals used for system validation and troubleshooting.

Table 7: Test points

Test Point	Signal name	Description/Remarks
TP1	I2C_1_SCL IC switch TCA9543APWR pin 9	I^2C serial clock line for the adapter components with 2.2 kΩ pull-up to +V1.8
TP2	I2C_1_SDA IC switch TCA9543APWR pin 10	I^2C serial data line for the adapter components with 2.2 kΩ pull-up to +V1.8
TP3	–	Not connected
TP4	–	Not connected
TP5	+V3.3 3.3V for the adapter components	Output of the buck regulator TPS62A02DRLR (IC5)
TP6	VIN+ connected to a POGO pad	Positive input of the current/power monitor INA219BIDR (IC4)
TP7	VIN- connected to a POGO pad	Negative input of the current/power monitor INA219BIDR (IC4)
TP8	+V1.8 1.8V for the adapter components	Output of the buck regulator TPS62A02DRLR (IC6)
TP9	OUT 1.0V for Ethernet transceiver	Output of the buck regulator TLV75510PDQNR (IC7)
TP10	OUT 2.5V for Ethernet transceiver	Output of the LDO/ linear voltage regulator TLV75525PDQNR (IC8)
TP11	CLK_OUT	Ethernet transceiver clock output
TP12	I2C_1_SCL current/power monitor (IC4)	I^2C SCL signal for the current/power monitor level-shifted to +V3.3
TP13	I2C_1_SDA current/power monitor (IC4)	I^2C SDA signal for the current/power monitor level-shifted to +V3.3
TP14	VCC input voltage	VCC input of the adapter
TP15	SW 3.3V for the adapter components	Output of the buck regulator TPS62A02DRLR (IC5)
TP16	VIN+ near the current/power monitor	Positive input of the current/power monitor INA219BIDR (IC4)

Continued on next page

Table 7: Test points (Continued)

Test Point	Signal name	Description/Remarks
TP17	VIN- near the current/power monitor	Negative input of the current/power monitor INA219BIDR (IC4)
TP18	SW 1.8V for the adapter components	Output of the buck regulator TPS62A02DRLR (IC6)
TP19	OUT 1.0V for Ethernet transceiver	Output of the buck regulator TLV75510PDQNR (IC7)
TP20	OUT 2.5V for Ethernet transceiver	Output of the LDO/ linear voltage regulator TLV75525PDQNR (IC8)

6 Operating Conditions

The **Lino-Verdin Adapter** is designed to operate together with the **Lino System-on-Module** and **Verdin carrier boards** within the environmental and electrical limits defined by the module and the components integrated on the adapter.

The **Lino SoM family** is designed for **industrial operating environments**, supporting an ambient operating temperature range of **-40 °C to +85 °C**. The adapter is intended to operate within the same temperature range when used with compatible components and carrier boards.

During operation, the following conditions should be observed to ensure reliable system performance:

- The **supply voltages** provided by the carrier board must remain within the limits defined for the Lino SoM and the PHY devices on the adapter.
- The **ambient temperature** must remain within the supported operating temperature range of the Lino SoM and the integrated PHY components.
- Proper **thermal management and airflow** should be ensured when operating in high-temperature environments.
- Signal integrity requirements for **high-speed interfaces**, including Ethernet, SDIO, and PCIe, should be respected according to the design guidelines.

Operating the adapter outside of these limits may result in reduced reliability or malfunction of the **Lino SoM**, the **network PHY devices**, or other components present on the adapter.

Table 8 lists the absolute maximum ratings for selected signals relevant to the system. Exceeding these limits may cause permanent damage to the device.

Table 8: Absolute maximum ratings

Signal	Description	Minimum	Maximum	Unit
V_IN	Main input supply to PMIC (carrier board input)	-0.3	6.0	V
NVCC_BBSM_1P8	Battery-backed secure domain supply	-0.3	2.15	V
GPIO supply voltage	SoC I/O pins with 3.3 V logic level	-0.3	3.8	V
ADC_IN	ADC analog input (referenced to VDD_ANA_1P8)	-0.3	2.1	V
USB VBUS input detect USB1_VBUS, USB2_VBUS	USB VBUS sense input (via external resistor divider)	-0.3	3.95	V

Operating Conditions
The maximum operating conditions of the **Lino-Verdin Adapter** are defined by the specifications of the **Lino System-on-Module**, the **Ethernet transceiver**, the **Wi-Fi+Bluetooth module**, and the **Verdin carrier board** used in the system.

7 Product Compliance

Up-to-date information about product compliance, such as RoHS, CE, UL 94, Conflict Minerals, REACH, and others, can be found on our website[2].

[2] https://www.toradex.com/support/product-compliance

8 Device and Documentation Support

8.1 Trademarks

MIPI® is a registered trademark of MIPI Alliance.

The Bluetooth® word mark is a registered trademark owned by Bluetooth SIG, Inc.

Secure Digital® and SD® are registered trademarks of SD Card Association.

DISCLAIMER