

Product Change Notification (PCN): 01821101 SMARC Development Board V1.1B

Date of publication: 26 Jun 2026

Table of Contents

- 1. Affected Products
- 2. Product Phase-in / Phase-out Schedule
- 3. Description of Changes
- 4. Customer Impact
- 5. Contact

Hardware Revision — SMARC Development Board V1.2A (01821200)

The SMARC Development Board V1.1B (01821101) is being replaced by V1.2A (01821200). This revision consolidates hardware bug fixes and design improvements identified during V1.0/V1.1 field use and design review. The most impactful fix is the correction of the CSI0 interface wiring, which was non-functional on V1.1B.

Compatibility: The SMARC edge-connector pinout is unchanged. V1.2A remains fully compatible with existing SMARC SoMs. No software changes are required.

1. Affected Products

End of Life Product		Replacement Product	
Part Number	Product Name	Part Number	Product Name
01821101	SMARC Development Board V1.1B	01821200	SMARC Development Board V1.2A

2. Product Phase-in / Phase-out Schedule

End of Life Product		Replacement Product	
Part Number	Estimated Schedule	Part Number	Estimated Schedule
01821101	No LTB/LTS	01821200	Samples: 1 Jul 2026

3. Description of Changes

Change #1: CSI0 Interface Wiring Corrected BUG FIX

- The CSI0_D0 and CSI0_D1 lanes were swapped in the harness on V1.1B, preventing the CSI camera interface from functioning. The harness wiring has been corrected in V1.2A so the CSI interface now operates at the hardware level.

Change #2: USB / SD / HDMI Power-Switch ICs Replaced BUG FIX

- The USB, SD and HDMI power-switch ICs (AP22615AWU-7) have been replaced with AOZ1353DI-01 across all affected rails (USB1 OTG, USB3, SD card and HDMI). On the previous part, the OC#/EN tie caused output flickering under over-current conditions. The replacement eliminates this flickering and also reduces the BOM.

Change #3: Dedicated 5V/6A Buck Converter Added (U39) ADDITION

- A new 5V/6A buck converter (U39) has been added to handle the current demand when both backlights draw 2A simultaneously. This offloads the main 5V buck converter and prevents it from exceeding its current budget in dual-backlight configurations.

Change #4: Power-Control Extension Connector (J81) Standardized IMPROVEMENT

- The J81 pinout has been updated per Toradex requirements. UART debug routing is now selectable between J81 and the FTDI debug interface via new jumpers J79 and J83.

Change #5: LCD0_VDD_EN Signal Added to Jumper Area ADDITION

- The LCD0_VDD_EN control signal has been added to the jumper section (J89/J90/J91 expanded to 6-pin), giving users direct control over LCD power enable in the jumper area.

Change #6: Display Adapter Stacking Height Increased BUG FIX

- On V1.1B, connecting both a DP and an HDMI cable simultaneously with the DSI-to-HDMI adapter caused a mechanical conflict. The adapter stacking height has been increased from 8mm to 10mm (ME1-ME4; J44 changed from LSS-130-03 to LSS-130-02), allowing standard HDMI and non-latching DP cables to be connected at the same time.

Change #7: Signal Integrity and Layout Improvements IMPROVEMENT

- Multiple signal-integrity, layout and documentation improvements across the board, including:
 - SDIO_RST# corrected from 3.3V to 1.8V translation on the M.2 Key E connector (translating FETs removed)
 - Corrected Ethernet LED1/LED2 assignment; MDI signals updated with differential-pair markers
 - JTAG signals spaced out to reduce crosstalk; additional GND stitching vias added for SDIO signals and for signals routed under the SoM
 - I2S signals spread out; HP_FB trace reworked (rotated 90°, thickness increased) to reduce resistive coupling
 - L1/L2 ferrites consolidated to a single 6A ferrite bead (L2, PN 2260) to meet the SMARC SoM current specification
 - FTDI OE delay added to prevent GPIO output flickering on USB connect; floating MOSFET gates stabilized with pull-ups
 - SD card LED D29 back-feed eliminated (3V3 removed from U46; D45 added)
 - INT4_POWER net renamed to INT4_GND; silkscreen, jumper alignment and overlay corrections applied to match the SMARC specification naming
 - Jumper note clarifications for the M.2 Key B dual-lane (KeyB/KeyE) configuration and the 3-wire PWM fan option

Note on J3/J5 pogo pins: These connectors are not conformant with the SMARC specification. This was an existing condition in V1.1B and is now explicitly documented on the schematic in V1.2A. There is no functional change.

4. Customer Impact

Hardware

- Customers upgrading from V1.1B to V1.2A gain:
 - A functional CSI camera interface — the CSIO_D0/D1 wiring defect is resolved
 - Stable USB, SD and HDMI power switching — no more flickering under over-current
 - Sufficient power headroom for dual 2A backlight configurations
 - DP and HDMI cables can now be connected simultaneously with the DSI adapter
 - Standardized J81 connector with selectable UART debug routing
 - LCDO_VDD_EN control signal available in the jumper area
 - Corrected Ethernet LED1/LED2 assignment
 - Improved signal integrity on SDIO, PCIe, JTAG, I2S and Ethernet

The SMARC edge-connector pinout is **unchanged**. V1.2A is fully compatible with existing SMARC SoMs and carrier board designs.

Software

- No software impact. V1.2A is a carrier-board hardware revision only; the BSP, Toradex Easy Installer and Torizon all run on the SoM and are unaffected.
- Note: the CSI interface is now functional at the hardware level. Enabling it in software still requires the relevant SoM device-tree or overlay configuration, as before.

5. Contact

- Please contact Toradex if you have any questions.
- For commercial and sales questions, please contact shop@toradex.com
- For technical questions, please contact support@toradex.com