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Lino Family Specification

Family Specification

Preliminary – Subject to Change

Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
02-Jun-2026	Rev. 0.1	V1.0	Initial documentation

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Abbreviations

Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
BTB	Board To Board
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.

Continued on next page

Abbreviations (Continued)

Abbreviation	Explanation
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1 Introduction

1.1 Overview

This document is a specification that defines the Lino Computer-on-Module family (referred to hereafter as “module”). It defines the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also defines the mechanical form factor, including key dimensions and possible thermal solutions.

1.2 Motivations

The following motivations are central to the definition of the Lino family specification, built around ARM-based system-on-chips.

1. **Scalable AI and Control Platform**
   The Lino family enables scalable embedded solutions ranging from real-time industrial control to edge AI and machine-learning applications (SoCs with integrated NPU). This allows designers to target diverse verticals such as industrial automation, robotics, smart gateways, HMI systems, and intelligent edge devices within a unified product family.

2. **Optimized for Performance and Efficiency**
   The family is designed for energy-efficient, application-focused performance. Depending on the selected processor, configurations may include application cores, real-time cores, and optional hardware acceleration. This enables the right balance between compute capability and system-level power consumption.

3. **Cost-Effective Alternative to Other Architectures**
   Compared to industrial computing platforms, the Lino family provides a lower power footprint, reduced system complexity, and competitive performance per watt. Integrated hardware acceleration options reduce the need for external hardware accelerators.

4. **Common Architecture Across Multiple SoCs**
   The Lino family is architected to host multiple processor variants within a common mechanical and electrical framework. This enables long-term scalability, simplified migration between performance tiers, and reduced carrier board redesign effort.

5. **Heterogeneous Processing Capability**
   The architecture supports heterogeneous processing concepts, allowing the combination of application-class cores with real-time cores and optional acceleration engines. This enables deterministic control alongside high-level operating systems within the same system.

6. **Industrial Connectivity**
   The family supports a wide set of industrial and embedded interfaces including Gigabit Ethernet, USB, CAN FD, SD/SDIO, I^{2}C, SPI, UART, PWM, ADC, and display interfaces where available. This makes the platform suitable for next-generation connected systems and industrial IoT deployments.

7. **Robust Board-to-Board Connector Solution**
   The Lino family is based on a high-density board-to-board connector architecture, enabling reliable signal integrity for high-speed interfaces while maintaining mechanical robustness suitable for industrial applications.

8. **1.8 V Logic I/O Architecture**
   In alignment with market design trends, the primary I/O voltage domain is 1.8 V. This reduces overall power consumption and improves signal integrity, while still supporting level translation where required for higher-voltage peripherals.

9. **Direct Breakout™ Carrier Design Philosophy**

The Direct Breakout™ approach reduces design complexity by routing key high-speed and critical signals directly to the module connectors. This simplifies carrier board development, reduces PCB layer count requirements, and accelerates time-to-market.

10. **Flexible Thermal Strategy**
The Lino family offers modular thermal solutions customized for various performance levels. This enables deployment across fanless industrial systems, enclosed embedded platforms, and performance-oriented edge computing devices.

2 Module Overview

2.1 Interface Compatibility Classes

The interfaces of the Lino modules are split into three distinct groups: "Always Compatible", "Reserved", and "Module-specific".

"Always Compatible" interfaces are features that shall be present on each SoM in the Lino Family. Customers can expect upgradeability and maximum scalability.

"Reserved" interfaces are features that are defined and reserved but possibly missing on some SoMs. The reason for that could be that certain SoCs do not feature an interface, or there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means that any Lino SoM can be inserted into any Lino carrier board without risking damage caused by incompatible reserved pins.

A "Module-specific" interface is a feature that is not guaranteed to be functionally or electrically compatible between modules. Different Lino modules may provide various functionalities on the same sets of "Module-specific" pins. If a carrier board design relies on such features, the selection of Lino modules suitable for being used with that particular carrier board design may be limited. An incompatible SoM/carrier board combination may disable all functionalities or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

2.1.1 "Always Compatible" Interfaces

The table in Figure 1 shows the interfaces that are provided by every Lino module. The "GPIO Capable" column indicates whether the assigned pins can be used as GPIOs. The "Instances" column indicates the number of interfaces that the Lino specification guarantees to be present for the "Always Compatible" interfaces. Customers should consult the datasheet for specific Lino module variants to check for special features or restrictions on interfaces.

Table 1: Always compatible interfaces

Description	Instance(s)	Name	Note(s)	GPIO Capable
Gigabit Ethernet (RGMII)	1	ETH_1	Media-dependent interface, backward compatible with Fast Ethernet with MDIO interface	No
GPIO	10	GPIO_[1..10]	General-Purpose Input/Output[1]	Yes
I^2C	3	I2C_[1..3]	General-Purpose	Yes[2]
PWM	3	PWM_[1..3]	General-Purpose Pulse Width Modulation	Yes
SD	1	SD_1	4-bit interface, I/O voltage might be switchable between 1.8V and 3.3V for UHS-I support	Yes[2]
SPI	1	SPI_1	Single Chip-Select pin	Yes
System Control	1	CTRL_PWR_EN_MOCI CTRL_PWR_BTN_MICO# CTRL_RECOVERY_MICO# CTRL_RESET_MOCI# CTRL_RESET_MICO#	Power control and reset signals connected to the SoC BBSM domain	No
UART (Rx, Tx)	2	UART_1..2	General-Purpose debug interface	Yes
UART (Rx, Tx)	1	UART_3	Primary operating system debug port (console)	Yes
USB 2.0 Device-only	2	USB_[1..2]	High-Speed USB 2.0 interface (480 Mbps), backward compatible with Full- and Low-Speed USB[3]	No

[1] GPIO functions may be limited on some modules. Please check the datasheet of the respective module or the Pinout Designer tool.
[2] GPIO capable via ALT function.
[3] Configured for Device operation by default (USB_ID biased to 1.8 V). OTG role swapping is not supported.

2.1.2 “Reserved” Interfaces

Some of the “Reserved” interfaces are extending the functionality of an “Always Compatible” interface. For example, the additional USB 3.x SuperSpeed signals in the “Reserved” class must be used in conjunction with the USB 2.0 Host interface signals. There are additional RTS/CTS hardware flow control signals that need to be used in conjunction with the respective general-purpose UART that is in the “Always Compatible” class. Since the “Reserved” interfaces are possibly missing on some SoCs, it is mandatory to consult the module datasheet for further information. A useful tool is the Toradex Pinout Designer, which can help to compare the available features of different Lino modules.

Table 2: Reserved interfaces

Description	Instance(s)	Name(s)	Note(s)	GPIO Capable
ADC	4	ADC_[1..4]	Analog-to-Digital converter 12 bit resolution	No
CAN FD	2	CAN_[1..2]	CAN or CAN FD compatible	Yes[1]
Gigabit Ethernet (RGMII)	1	ETH_2	Media-dependent interface (PHY on module), backward compatible with Fast Ethernet	No
I^2C	1	PMIC_I2C	Reserved for on-board I^2C components shall not be used as general purpose I^2C	No[2]
I^2S	1	I2S_1	Digital audio interface (I^2S/SAI) full-duplex, master or slave operation, DMA supported	Yes[1]
MIPI CSI	1	CSI_1	Camera Serial Interface	No
MIPI DSI	1	DSI_1	Display Serial Interface, up to 4 data lanes	No
SDIO	1	SD_2	4-bit interface, suitable for SD cards or SDIO peripherals	Yes[3]
SPI	1	SPI_2	Single chip-select pin	Yes[1]
UART (CTS, RTS)	2	UART_[1..2]	Complementary hardware flow control signals for the fully compatible general purpose UART interfaces	Yes
UART (Rx, Tx)	1	UART_4	Secondary operating system (real-time OS) debug port it might be usable as general purpose UART	Yes

[1] GPIO capable via ALT function, but the GPIO functions may be limited on some modules. Please check the datasheet of the respective module or the Pinout Designer tool.

[2] Electrically GPIO capable, but reserved for mandatory on-module I^2C communication (e.g., PMIC, GPIO expander, RTC). Reassigning as GPIO will prevent proper SoM operation.

[3] Electrically GPIO capable, but reserved for external SD card.

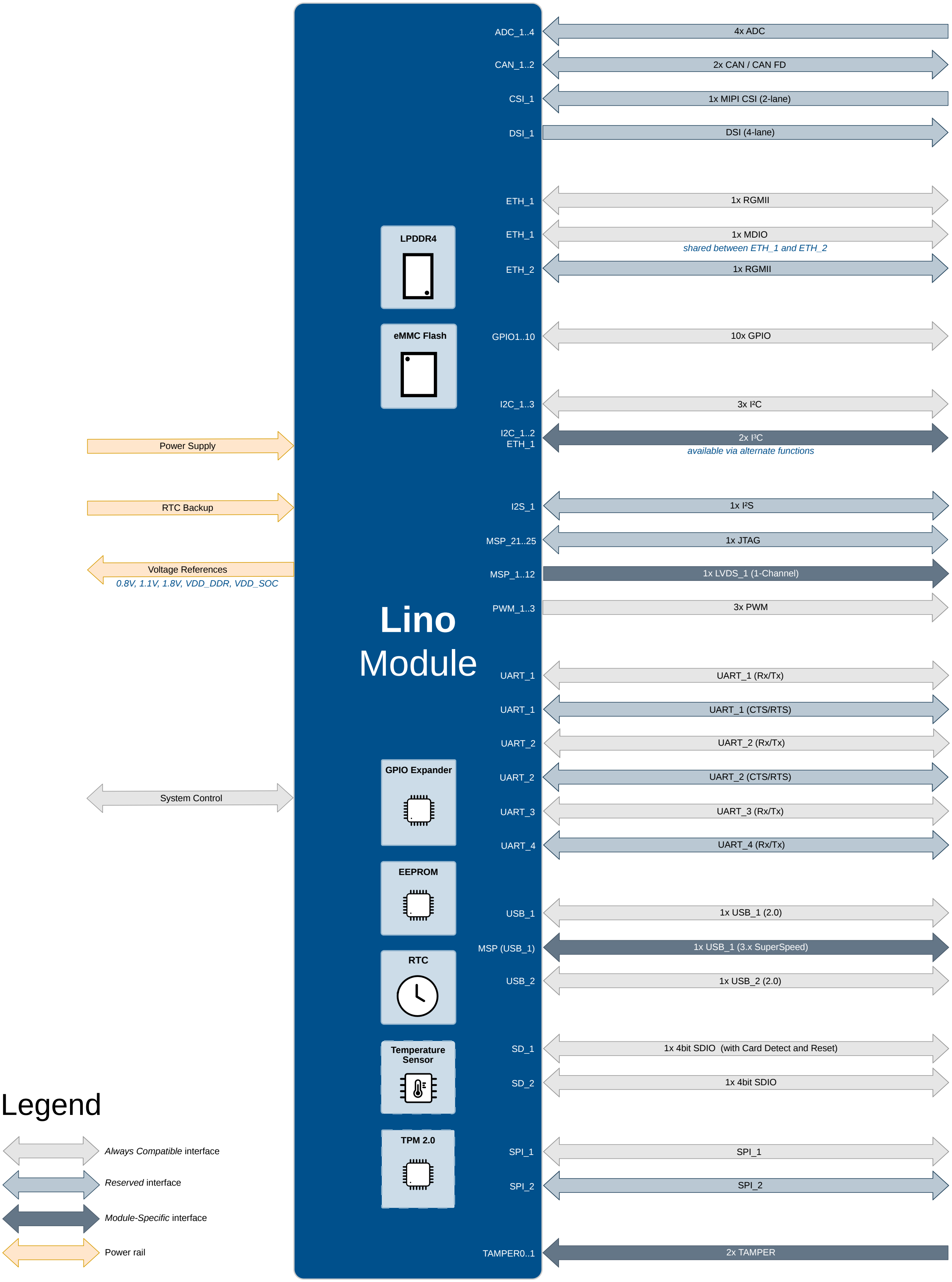
2.1.3 “Module-specific” Interfaces

”Module-specific” interfaces allow for the possibility of including interfaces that may not be widely adopted (yet) or interfaces that may be specific to a particular device or groups of devices. The concept provides a mechanism for extending features that are present on ”Always Compatible” or “Reserved” pins, e.g., providing additional PCI-Express lanes. It should be noted that Toradex does its best to keep “Module-specific” interfaces standard across modules that share such interfaces. For example, suppose both module A and module B have an LVDS interface available in the same configuration as a “Module-specific” interface. In that case, it is a priority to assign them to the same pins in the “Module-specific” area of the connector. Hence, both module A and module B would ideally share compatibility between this part of the “Module-specific” interface.

2.2 Architecture

The block diagram in Figure 1 shows the basic architecture of the Lino module, depicting the “Always Compatible” interfaces, “Reserved” interfaces, and some examples of “Module-specific” interfaces.

Figure 1: Block Diagram



2.3 Module and Carrier Board Compatibility

To ensure that any carrier board design is compatible with all Lino modules, only the standard functions of the “Always Compatible” and “Reserved” interfaces should be used. Alternate functions are not guaranteed to be compatible. Special care must be taken with the “Module-specific” signals. The “Module-specific” signals might be electrically incompatible between different Lino modules. This means that the system might not work, and this may result in damage done to the module or the carrier board.

The Toradex Pinout Designer tool can be used for comparing available features and interfaces of different Lino modules. Make sure to enable the note fields in the viewing options to get additional information. Even though the Pinout Designer is a very powerful tool, it is still recommended to read the datasheets of the different Lino modules to check the functional and electrical compatibility of the interfaces/pins.

> ⚠ **Check interface specifications when using "Module specific" interfaces**
> If a custom carrier board implements any “Module-specific” interfaces, it may not be 100% compatible with all Lino modules. Where “Module-specific” interfaces are common between different Lino modules, they shall be provided on the same pins where possible. Therefore, designs that make use of the “Module-specific” interfaces of a specific Lino module may be compatible with other Lino modules. Please check the interface specifications of individual Lino modules carefully.

3 Interface Specifications

3.1 Signal Naming Convention

Identical signals of different interfaces are distinguished by adding the interface index as a suffix (e.g., `PWM_1`, `PWM_2`, etc.). Interface indexing usually starts at one. Signals named after a standard or following a widely acknowledged common naming convention (such as the Ethernet or LVDS interfaces) may use a zero-based index. Differential pair signal components are suffixed with either a `P` (for positive) or `N` (for negative). Active low signals are suffixed with a `#`. The underscore ("_") is used as a separator to delimit fragments of the signal name (such as signal group, channel, and signal descriptor components) to make the signal name easy to read and interpret.

3.2 Standard Interfaces

Lino standard interfaces are the common name for the "Always Compatible" and "Reserved" interfaces. Toradex Pinout Designer eases the configuration of standard interfaces to facilitate the development process.

3.2.1 ADC

Up to four ADC inputs may be available in the Reserved class.

- Resolution and performance depend on module implementation.
- Typical input voltage range is 0 V to the analog supply voltage.
- These pins are dedicated analog inputs and cannot be used as GPIOs.

3.2.2 CAN

Up to two CAN interfaces may be available in the Reserved class. Depending on the module, support for CAN FD (Flexible Data Rate) may be included. External CAN transceivers are required on the carrier board.

3.2.3 Gigabit Ethernet (RGMII)

The primary Ethernet interface is a media-independent interface supporting 10/100/1000 Mbit operation via RGMII.

The PHY may be located either on the module or on the carrier board depending on the specific module variant. Designers should refer to the module documentation to determine whether only magnetics or a full external PHY is required.

MDIO and MDC are provided for PHY management.

3.2.4 I^{2}C

Three general-purpose I^{2}C interfaces are part of the Always Compatible class.

Additional I^{2}C interfaces may exist in the Reserved class and may be associated with display or camera subsystems.

Reserved I^{2}C interfaces may or may not be available for general-purpose use depending on the module configuration. Designers should verify availability in the respective module datasheet.

3.2.5 I2S (Digital Audio)

The `I2S_1` interface is located in the Reserved class.

When implemented, it provides:

- Bit clock (BCLK)
- Frame sync (LRCLK)
- Serial data in
- Serial data out

Availability and lane configuration depend on the module.

3.2.6 JTAG

The JTAG interface may be available for debugging and boundary-scan testing depending on the module.

The nominal I/O voltage is typically 1.8 V and the JTAG adapter reference voltage should be derived from the JTAG reference pin provided on the module to ensure compatibility across variants.

3.2.7 MIPI CSI

A MIPI CSI camera interface may be available in the Reserved class.

Supported lane configuration, resolution, and data rate depend on the module.

3.2.8 MIPI DSI

A MIPI DSI display interface may be available in the Reserved class.

Lane count and maximum supported data rate depend on the module variant.

3.2.9 PWM

Three PWM signals are part of the Always Compatible class.

The PWM interfaces provide hardware-generated pulse-width modulation outputs with programmable:

- Frequency
- Duty cycle
- Polarity
- Output enable state

The signals operate in the module’s primary I/O voltage domain and are driven as digital outputs from the processor. Timing generation is handled by dedicated timer/PWM hardware blocks, allowing stable waveform generation without continuous CPU intervention.

PWM parameters are configured via memory-mapped registers, and the interfaces can operate independently of the main processor load once configured. Resolution and maximum frequency depend on the selected clock source and prescaler configuration within the module.

Additional PWM-capable pads may exist in the Reserved class depending on module implementation and pin multiplexing configuration.

3.2.10 SDIO

The primary SDIO interface (`SD_1`) is intended for connection to removable SD memory cards.
It supports up to 4 data lines (`DAT0`-`DAT3`) in addition to `CMD` and `CLK`.

The I/O voltage may operate at 3.3 V or 1.8 V depending on module configuration and supported speed modes. Some modules may support voltage switching during card initialization to enable higher-speed operation.

Required pull-up resistors for CMD and DATA lines are typically implemented on the module. Carrier board designers should not add external pull-ups unless explicitly specified in the module documentation.

A secondary SDIO interface (`SD_2`) is located in the Reserved class. When available on a given module, it is intended for connection to SDIO-based peripherals such as wireless communication modules or other embedded devices rather than removable memory cards. Availability and electrical characteristics depend on the specific module variant.

3.2.11 SPI

One SPI interface is part of the Always Compatible class and supports a single chip-select signal. An additional SPI interface may be available in the Reserved class depending on module implementation. Availability and multiplexing constraints depend on the selected module.

3.2.12 UART

Three UART interfaces (`Rx/Tx`) are part of the Always Compatible class.

- `UART_1` and `UART_2` are general-purpose.
- `UART_3` is typically intended for primary system debug output.

`RTS/CTS` hardware flow-control signals for `UART_1` and `UART_2` are located in the Reserved class.

The `UART_4` interface is in the Reserved class and may be available depending on module configuration.

Use of the primary debug UART for general-purpose communication is possible but not recommended, as maintaining access to system logs simplifies development and field diagnostics.

3.2.13 USB 2.0

The Lino family provides two USB 2.0 High-Speed interfaces as part of the Always Compatible class.

- Compliant with USB 2.0 High-Speed (480 Mbps)
- Backward compatible with Full- and Low-Speed USB
- Role (Host or Device) depends on module implementation and carrier design
- OTG capability depends on ID pin routing and module configuration

Some modules may implement fixed-role operation, while others may allow configurable host/device mode. Refer to the specific module documentation for supported configurations.

3.3 “Module-specific” Interfaces

The “Module-specific” pins on the Lino module may be used for allocating any types of interfaces not fitting in any of the ”Always Compatible” and “Reserved” interfaces categories.

> **Do not use the module with an incompatible carrier board**
> Even the interface voltage depends on the module and could lead to malfunction if a Lino module is used in an incompatible carrier board!

The “Module-specific” pins are allocated on the module edge connector in groups of lanes with one Rx and one Tx pair. However, the "Module-specific" pins might be used in different directions, and also for single-ended signals.

3.4 Physical Pin Definition and Location

The Lino Family modules provide a total of **200 connector pins** across their dual board-to-board connectors. Of these, **36 pins (18%) are dedicated to ground**, ensuring low-impedance return paths and supporting signal integrity for high-speed and high-frequency interfaces. The primary supply rail (VCC) is provided through **six dedicated power pins**, enabling stable and reliable power delivery to the module.

Tables 3 and 4 describe the complete pinout of the board-to-board connectors. These tables list the assigned function of each pin and indicate its compatibility classification according to the Lino Family Specification. A detailed explanation of the compatibility groups is provided in Section 2.1.

> **Naming Convention**
> On the Lino Family system-on-modules, signals routed to the primary connector are identified by pin names starting with **P** (for example, `P10` or `P12`), while signals routed to the secondary connector are identified by pin names starting with **S** (for example, `S28` or `S30`).

Table 3: Primary connector pinout

Signal Group Power Group	Lino Signal Module Outside	CONN DF40 pin		Lino Signal Module Inside	Signal Group Power Group
PWM NVCC_GPIO	PWM_1	P1	P2	ADC_1	ADC AVDD_1P8_ADC
	PWM_2	P3	P4	ADC_2	
	PWM_3	P5	P6	UART_1_RTS	UART NVCC_GPIO
Ground	GND	P7	P8	UART_1_CTS	
UART NVCC_GPIO	UART_1_RXD	P9	P10	CAN_1_TX	CAN NVCC_AON
	UART_1_TXD	P11	P12	CAN_1_RX	
	UART_2_RXD	P13	P14	GND	Ground
	UART_2_TXD	P15	P16	I2C_1_SDA	I2C NVCC_AON/NVCC_GPIO
DEBUG UART NVCC_AON	UART_3_RXD	P17	P18	I2C_1_SCL	
	UART_3_TXD	P19	P20	I2C_2_SDA	
Ground	GND	P21	P22	I2C_2_SCL	
DEBUG UART NVCC_AON	UART_4_RXD	P23	P24	I2C_3_SDA	
	UART_4_TXD	P25	P26	I2C_3_SCL	
USB_1 USB1_VDD33	USB_1_EN	P27	P28	GND	Ground
	USB_1_OC#	P29	P30	GPIO_1	GPIO NVCC_GPIO
	USB_1_VBUS	P31	P32	GPIO_2	
	USB_1_D_N	P33	P34	GPIO_3	
	USB_1_D_P	P35	P36	GPIO_4	
Ground	GND	P37	P38	GPIO_5	

Continued on next page

Table 3: Primary connector pinout (Continued)

Signal Group Power Group	Lino Signal Module Outside	CONN DF40 pin		Lino Signal Module Inside	Signal Group Power Group
Module-Specific Pins (MSP)	MSP_31	P39	P40	GPIO_6	GPIO NVCC_GPIO
	MSP_32	P41	P42	GPIO_7	
Ground	GND	P43	P44	GPIO_8	
Module-Specific Pins (MSP)	MSP_33	P45	P46	GPIO_9	
	MSP_34	P47	P48	GPIO_10	
Ground	GND	P49	P50	GND	Ground
Module-Specific Pins (MSP)	MSP_35	P51	P52	SPI_1_CLK	SPI NVCC_GPIO
	MSP_36	P53	P54	SPI_1_MISO	
Ground	GND	P55	P56	SPI_1_MOSI	
USB_2 USB1_VDD33	USB_2_D_N	P57	P58	SPI_1_CS	
	USB_2_D_P	P59	P60	SD_1_D2	SDIO NVCC_SD2
	USB_2_EN	P61	P62	GND	Ground
	USB_2_OC#	P63	P64	SD_1_D3	SDIO NVCC_SD2
RGMII NVCC_WAKEUP/NVCC_GPIO	GPIO_11	P65	P66	SD_1_CMD	
	ETH_MDIO	P67	P68	SD_1_CLK	
	ETH_MDC	P69	P70	GND	Ground
Ground	GND	P71	P72	SD_1_PWR_EN	SDIO NVCC_SD2
RGMII NVCC_WAKEUP	ETH_1_RGMII_RXC	P73	P74	SD_1_D0	
	ETH_1_RGMII_RX_CTL	P75	P76	SD_1_D1	
	ETH_1_RGMII_RXD_0	P77	P78	SD_1_CD#	
	ETH_1_RGMII_RXD_1	P79	P80	CTRL_RECOVERY_MICO#	System Control
	ETH_1_RGMII_RXD_2	P81	P82	CTRL_PWR_BTN_MICO#	
	ETH_1_RGMII_RXD_3	P83	P84	CTRL_PWR_EN_MOCI	
	ETH_1_RGMII_TX_CTL	P85	P86	CTRL_RESET_MOCI#	
Ground	GND	P87	P88	CTRL_RESET_MICO#	
RGMII NVCC_WAKEUP	ETH_1_RGMII_TXC	P89	P90	VCC	Power Supply
	ETH_1_RGMII_TXD_3	P91	P92	VCC	
	ETH_1_RGMII_TXD_2	P93	P94	VCC	
	ETH_1_RGMII_TXD_1	P95	P96	VCC	
	ETH_1_RGMII_TXD_0	P97	P98	VCC	
Ground	GND	P99	P100	VCC	

Cells in ⬜: Always compatible interface.
Cells in ▨: Reserved interface.
Cells in ⬛: Module-specific interface.
Cells in ▩: Pin connected to the ground.
Cells in 🟧: Pin connected to the power supply.

Table 4: Secondary connector pinout

Signal Group Power Group	Lino Signal Module Outside	CONN DF40 pin		Lino Signal Module Inside	Signal Group Power Group
ADC AVDD_1P8_ADC	ADC_3	S1	S2	SD_2_D2	SDIO NVCC_WAKEUP
	ADC_4	S3	S4	SD_2_D3	
UART NVCC_GPIO	UART_2_RTS	S5	S6	GND	Ground
	UART_2_CTS	S7	S8	SD_2_CMD	SDIO NVCC_WAKEUP
Ground	GND	S9	S10	SD_2_CLK	
Module-Specific Pins (MSP)	MSP_1	S11	S12	SD_2_D0	
	MSP_2	S13	S14	GND	Ground
	MSP_3	S15	S16	SD_2_D1	SDIO NVCC_WAKEUP
	MSP_4	S17	S18	SPI_2_CS	SPI NVCC_GPIO
	MSP_5	S19	S20	SPI_2_CLK	
Ground	GND	S21	S22	SPI_2_MOSI	
Module-Specific Pins (MSP)	MSP_6	S23	S24	SPI_2_MISO	
	MSP_7	S25	S26	GND	Ground
	MSP_8	S27	S28	CAN_2_TX	CAN NVCC_GPIO
	MSP_9	S29	S30	CAN_2_RX	
	MSP_10	S31	S32	GND	Ground
Ground	GND	S33	S34	DSI_1_D3_N	DSI
Module-Specific Pins (MSP)	MSP_11	S35	S36	DSI_1_D3_P	
	MSP_12	S37	S38	GND	Ground
	MSP_13	S39	S40	DSI_1_D2_N	DSI
	MSP_14	S41	S42	DSI_1_D2_P	
	MSP_15	S43	S44	GND	Ground
Ground	GND	S45	S46	DSI_1_CLK_N	DSI
Module-Specific Pins (MSP)	MSP_16	S47	S48	DSI_1_CLK_P	
	MSP_17	S49	S50	GND	Ground
	MSP_18	S51	S52	DSI_1_D1_N	DSI
	MSP_19	S53	S54	DSI_1_D1_P	
	MSP_20	S55	S56	GND	Ground
Ground	GND	S57	S58	DSI_1_D0_N	DSI
Module-Specific Pins (MSP)	MSP_21	S59	S60	DSI_1_D0_P	
	MSP_22	S61	S62	GND	Ground
Module-Specific Pins (MSP)	MSP_23	S63	S64	MSP_26	Module-Specific Pins (MSP)
	MSP_24	S65	S66	MSP_27	
	MSP_25	S67	S68	MSP_28	
Ground	GND	S69	S70	MSP_29	
RGMII NVCC_WAKEUP	ETH_2_RGMII_RXC	S71	S72	MSP_30	
	ETH_2_RGMII_RX_CTL	S73	S74	GND	Ground

Continued on next page

Table 4: Secondary connector pinout (Continued)

Signal Group Power Group	**Lino Signal** Module Outside	**CONN DF40 pin**		**Lino Signal** Module Inside	**Signal Group** Power Group
Ground	GND	S75	S76	CSI_1_CLK_P	CSI
RGMII NVCC_WAKEUP	ETH_2_RGMII_RXD_0	S77	S78	CSI_1_CLK_N	
	ETH_2_RGMII_RXD_1	S79	S80	GND	Ground
	ETH_2_RGMII_RXD_2	S81	S82	CSI_1_D1_P	CSI
	ETH_2_RGMII_RXD_3	S83	S84	CSI_1_D1_N	
Ground	GND	S85	S86	GND	Ground
RGMII NVCC_WAKEUP	ETH_2_RGMII_TXC	S87	S88	CSI_1_D0_P	CSI
	ETH_2_RGMII_TX_CTL	S89	S90	CSI_1_D0_N	
	ETH_2_RGMII_TXD_3	S91	S92	GND	Ground
	ETH_2_RGMII_TXD_2	S93	S94	I2S_1_BCLK	I2S NVCC_GPIO
Ground	GND	S95	S96	I2S_1_SYNC	
RGMII NVCC_WAKEUP	ETH_2_RGMII_TXD_1	S97	S98	I2S_1_D_OUT	
	ETH_2_RGMII_TXD_0	S99	S100	I2S_1_D_IN	

Cells in ⬜: Always compatible interface.
Cells in 🟦: Reserved interface.
Cells in ⬛: Module-specific interface.
Cells in ◼: Pin connected to the ground.
Cells in 🟧: Pin connected to the power supply.

4 Mechanical Specifications

4.1 Overview

The Lino module form factor mechanical dimensions have been specified based on careful analysis of required board space for typical device packages (SoC, memory ICs, power ICs, Wi-Fi module, and peripheral ICs) and certain key features. This has been balanced with the requirement to keep the form factor as small as reasonably possible.

4.2 Module Dimensions

Units of measurement
All dimensions, if not otherwise noted, are in mm.

Figure 2: Module dimensions top side (mm)

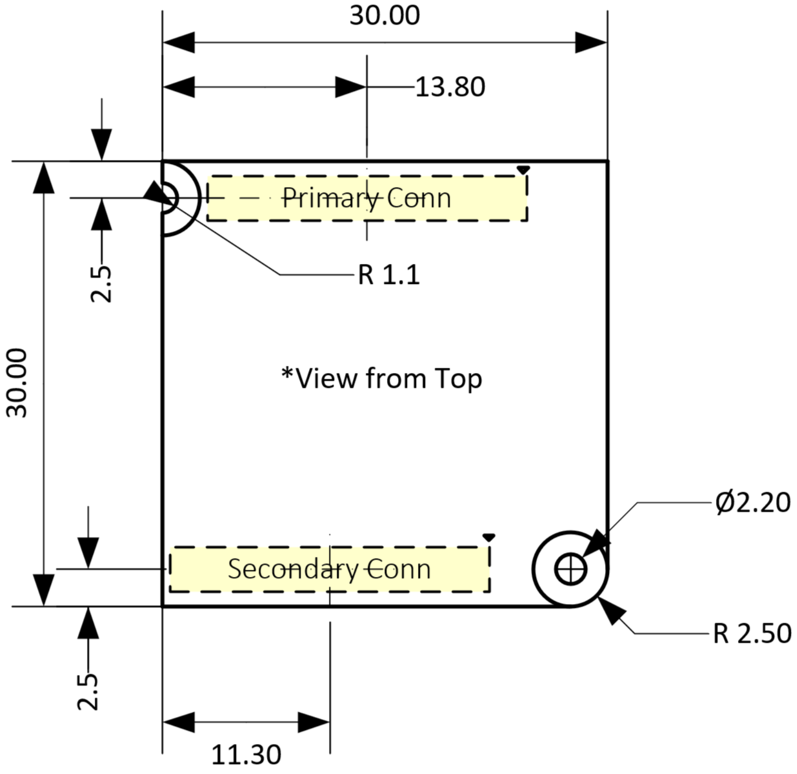
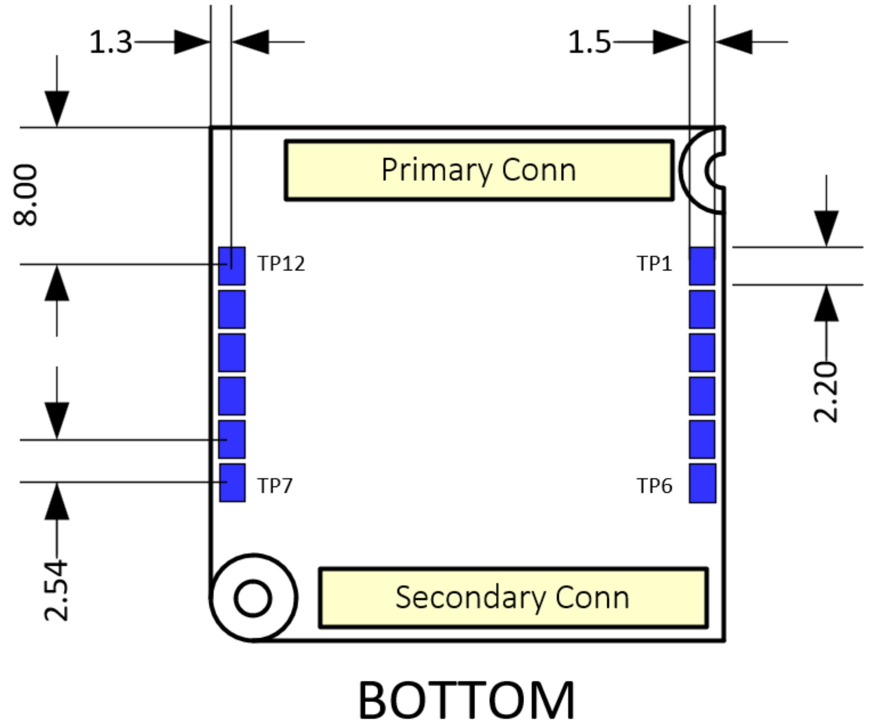


Figure 3: Module dimensions bottom side (mm)



4.3 Module Connector and Stacking Height

The Lino uses two Amphenol® BergStack® Board-to-Board connectors, providing high mechanical robustness and reliable electrical performance for demanding embedded applications. Each connector provides 100 signal positions with a 0.40 mm pitch, resulting in a total of **200 pins** with a **0.8 mm pitch**, arranged in high-density arrays optimized for compact board-to-board stacking. The dual-connector architecture distributes signals and mechanical load across both connectors, ensuring stable mating and long-term reliability.

The board-to-board connectors are available to customers for custom carrier board designs, both during development and production. For detailed ordering information, please refer to the applicable product documentation or contact your sales representative.

4.3.1 Mating Parts (Carrier Side)

Mating parts for the carrier board are available with multiple stacking height options:

- 1.5mm stacking height
- 4.0 mm stacking height

Table 5: Mating parts for the Carrier Side

PN (Carrier Side)	Stacking Height	Remarks
Amphenol 10164227-1001A1RLF	1.5 mm	With alignment bosses
Amphenol 10164227-1001A2RLF	1.5 mm	Without alignment bosses
Amphenol 10164227-1004A1RLF	4.0 mm	With alignment bosses

Continued on next page

Table 5: Mating parts for the Carrier Side (Continued)

PN (Carrier Side)	Stacking Height	Remarks
Amphenol 10164227-1004A2RLF	4.0 mm	Without alignment bosses

Unless otherwise specified, part numbers refer to versions with 10 µm gold plating on contacts. For 30 µm gold plating options, refer to the respective ordering code variant in the manufacturer's documentation.

4.3.2 Connector Stacking Height and Component Clearance

The following table compares the different mating part options.

- **Connector Height**: The stacking height defined by the connector combination.
- **Board-to-Board Distance**: The nominal space between the carrier board and the module PCB.
- **Component Height (Carrier Board)**: The recommended maximum height of components underneath the module.

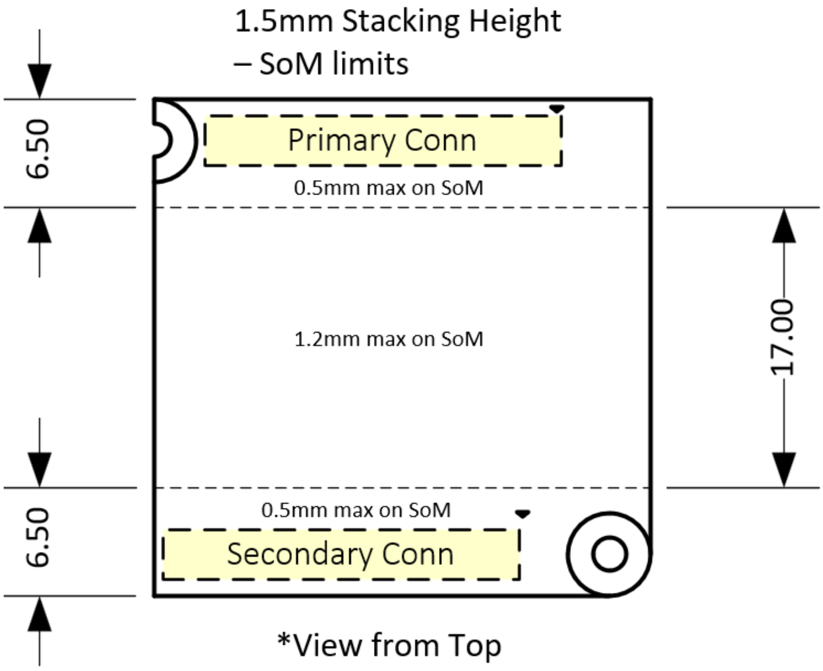
Table 6: Amphenol 10164228-1001A1RLF Connector Stacking Height

Stacking height	Board-to-board distance	Max. component height on carrier board	Remarks
1.5 mm	1.5 mm	$\leq$ 0.5 mm	Ultra-low profile option; minimal clearance under module
4.0 mm	4.0 mm	$\leq$ 3.0 mm	Recommended stacking height for standard Lino carrier designs

Even if a module does not fully utilize the available component height allowance, it is advisable not to place additional components in the unused space between the module and the carrier board. Reserving the complete component height ensures mechanical compatibility with existing and future module versions.

If components taller than 2 mm need to be placed underneath the module, a connector variant with a larger stacking height is recommended.

Figure 4: Stacking Height



4.4 Fixation of the Module

The Lino Family modules can be connected to the Carrier Boards through the 200 pin Board-to-Board connectors. The connectors are designed to accommodate small angular offsets during mating. It allows a limited degree of initial angular misalignment to ease connector engagement, while final seated alignment must be nearly straight with only minimal angular tolerance. This ensures smooth mating, protects contacts from damage, and guarantees reliable long-term electrical performance.

For many applications, the fixation through the connector is enough. However, for harsh environment applications where higher vibration and shock tolerance/resistance is required, the module can be screwed down to the carrier board. This is also recommended if heavier heatsinks are mounted directly to the module. There are four mounting holes at the edge of the module designed to be used with M3 screws.

4.5 Thermal Solution

The thermal solution is fixed to the SoM and Carrier Board using four M3 screws, and its design should allow the same screws to be used while ensuring that it can be applied to a SoM even when the SoM is mounted to a carrier board and fully inserted into the board-to-board connector. The solution must rely on all four standard stand-offs assembled to Lino carrier boards and four matching screws to guarantee an industrial, robust, vibration-proof installation, and the thermal solution should cover the entire area of the module's PCB with the same radius on the corners.

4.6 Carrier Board Space Requirements

The required PCB area for the module depends on the module fixing method and cooling solution.

4.7 Pin Numbering

The pin number one is marked on the primary and secondary connectors on Figure 2.

4.7.1 Generic Test Point Interfaces

Every Lino module provides 11 and 12 test points on the module PCB's top and bottom sides respectively, as shown in the Figure 3. The bottom side test points are split into groups of 6 pads. Each set is symmetrical about the centered Y-axis (the Y plane is orthogonal to the connector edge).

Top Side Test Points
The top-side test points are distributed across the PCB rather than grouped.

The test points are "Module-specific" pins. The signals connected to these test points are defined for each Lino module for factory testing purposes. Customer carrier boards shall leave these pads unconnected.

5 Electrical Specifications

This section defines the **family-level electrical architecture** of the Lino modules, including power supply, system control signals, voltage domains, and test interfaces. Electrical characteristics that are module-specific (e.g., maximum current consumption, timing constraints, pin multiplexing options, or rail sequencing details) are defined in the respective Lino module datasheets.

5.1 Power Supply

5.1.1 Main Supply – VCC

The Lino family defines a single main input rail:

- **VCC**: Module main supply input
- **Voltage range:** 3.135 V to 5.5 V (3.3 V / 5 V nominal)
- **Connector pins (Primary connector):** `P90`, `P92`, `P94`, `P96`, `P98`, `P100`
- **Signal group:** Power
- **Compatibility classification:** *Always Compatible*

The carrier board shall provide a stable and properly decoupled VCC rail within the specified operating range.

Maximum input current, inrush current, and total power dissipation depend on the specific module variant and are specified in the respective Lino module datasheet.

5.2 System Control and Reset Signals

The following system control and reset signals are defined at family level and are available on the Primary connector. These signals ensure consistent system integration across all Lino modules.

Unless otherwise specified, control signals operate in the **1.8 V domain**.

5.2.1 CTRL_RECOVERY_MICO# (P80)

- **Type:** Open-drain input
- **Voltage domain:** 1.8 V
- **Compatibility classification:** Always Compatible

Function:
Forces the module into recovery mode when asserted during power-up.

- Assertion method: Short to GND during power-up
- Internal pull-up: 10 kΩ to 1.8 V (on module)

If unused, the carrier board may leave this signal unconnected.

5.2.2 CTRL_PWR_BTN_MICO# (P82)

- **Type:** Open-drain input
- **Voltage domain:** 1.8 V
- **Compatibility classification:** Always Compatible

Function:
Implements the module power-button behavior.

- Short press: Turns the module ON from the OFF state
- Long press (> 5 s, module-dependent): Requests controlled power-off
- Internal pull-up: 100 kΩ to 1.8 V (on module)

If unused, the carrier board may leave this signal unconnected.

5.2.3 CTRL_PWR_EN_MOCI (P84)

- **Type:** Output
- **Voltage domain:** 1.8 V
- **Compatibility classification:** Always Compatible

Function:
Indicates that the module is powered and enables carrier-board peripheral power rails.

This signal can be used by the carrier board to control external regulators or load switches supplying peripherals.

5.2.4 CTRL_RESET_MOCI# (P86)

- **Type:** Open-drain output (active low)
- **Voltage tolerance:** 3.3 V tolerant
- **Compatibility classification:** Always Compatible

Function:
Reset output for carrier-board peripherals.

- No pull-up resistor is provided on the module
- The carrier board shall provide an external pull-up resistor
  - Recommended pull-up voltage: 1.8 V or 3.3 V

5.2.5 CTRL_RESET_MICO# (P88)

- **Type:** Open-drain input
- **Voltage domain:** 1.8 V
- **Compatibility classification:** Always Compatible

Function:
External reset input for the module.

- Assertion method: Short to `GND`
- Internal pull-up: 100 kΩ to 1.8 V (on module)

If unused, the carrier board may leave this signal unconnected.

5.3 Power Management States (Family Concept)

The Lino family defines common high-level power states to ensure consistent system behavior across all module variants.

The detailed rail sequencing and internal behavior are module-specific and described in the respective module datasheet.

5.3.1 Module OFF

- VCC present
- Module not running
- `CTRL_PWR_EN_MOCI` deasserted

5.3.2 Running

- SoC powered and executing
- `CTRL_PWR_EN_MOCI` asserted
- Reset signals deasserted

5.3.3 Reset

- SoC reset active
- `CTRL_RESET_MOCI#` asserted

5.3.4 Low-power / Sleep

- SoC in low-power mode
- Detailed behavior is module-specific

The exact mapping of these states to power rails and control-signal behavior may vary per module and is defined in the respective module datasheets.

5.4 Signal Voltage Domains

This section defines the signal voltage domains at family level. The detailed voltage specification for each individual pin is provided in:

- The **Voltage** column of the Lino Family Pinout Specification
- The respective module datasheet

5.4.1 1.8 V Domain

Most digital I/O operate in the 1.8 V domain, including: - GPIO - UART - SPI - I^{2}C - CAN - Ethernet (RGMII) - System control signals

Carrier-board circuitry interfacing to these signals shall be compatible with 1.8 V logic levels unless otherwise specified.

5.4.2 3.3 V / 1.8 V Domain

- `SD_1` signals support a selectable voltage domain (1.8 V or 3.3 V), depending on the module variant and configuration.

Refer to the respective module documentation for domain selection details.

5.4.3 5 V Tolerant Inputs

5 V tolerant inputs are not defined at family level. Any signal that supports 5 V tolerance (e.g., `USB_1_VBUS`) shall be explicitly specified in the respective Lino module documentation (e.g., module datasheet and pinout specification).

5 V Signals
Designers shall not assume 5 V tolerance unless explicitly stated.

5.5 Test Points

To support manufacturing, validation, and debugging, the Lino family defines a set of dedicated test points on the module. These pads allow access to debug, programming, and internal voltage rails that are not available on the family connector.

Test Points are intended for factory use and development purposes. Unless explicitly required, customer carrier boards shall not connect to these pads.

5.5.1 JTAG Test Points

The Lino family does not provide JTAG signals on the family connector, so the allocation of JTAG-related test points is defined at family level to ensure consistent debug access across all Lino modules.

Allocated signals:

- `TDI` (Test Data In): serial data input to the JTAG interface, used to shift instructions and data into the device.
- `TDO` (Test Data Out): serial data output from the JTAG interface, used to shift instructions and data out of the device.
- `TMS` (Test Mode Select): control signal that defines JTAG state machine transitions.
- `TCLK` / `TCK` (Test Clock): clock signal that synchronizes JTAG data shifting and state transitions.
- `RST`: hardware reset signal used to reset the device or the JTAG logic. Available on the SoM connector.
- `VREF`: reference voltage that defines the logic level for the JTAG interface signals. Available on the SoM connector.

Since the Lino family does not route JTAG signals to the family connector, these signals must be exposed through dedicated test points.

The location and description of the JTAG test points are shown in Figure 5 and Table 7, respectively.

Figure 5: JTAG test points

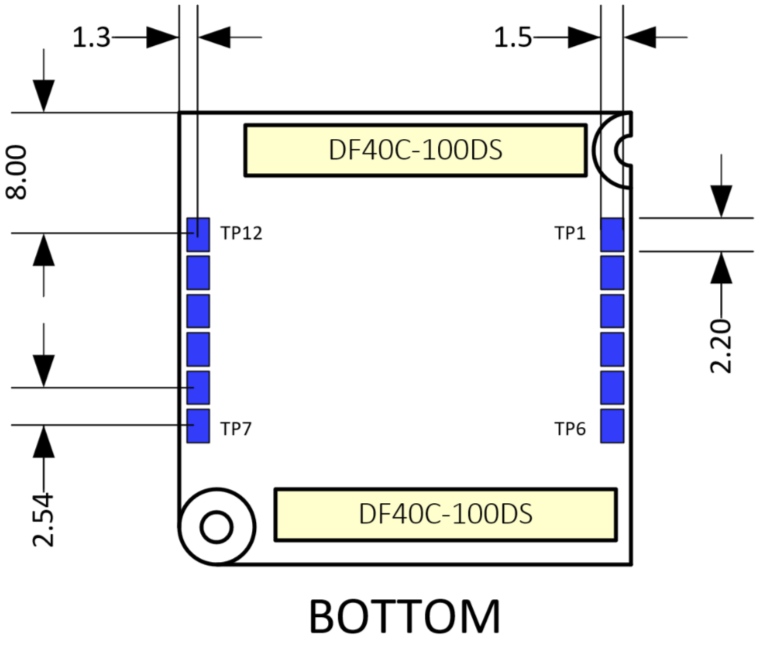


Table 7: JTAG test points

TP	Signal	Description/Remarks
TP1	TDI	Test Data In: Serial data input to the SoC JTAG interface. External pull-up as required by the SoC
TP3	TDO	Test Data Out: Serial data output from the SoC JTAG interface
TP6	JTAG_VREF	JTAG reference voltage (1.8 V) used by the external debugger to match I/O logic levels
TP7	TRST#	Test Reset (active low): Optional JTAG reset input. Biasing (pull-up or pull-down) per SoC requirements
TP9	TCK	Test Clock: JTAG clock input. External pull-up as required by the SoC
TP12	TMS	Test Mode Select: JTAG state machine control input. External pull-up as required by the SoC

Pull resistors
Signal direction and pull resistor requirements depend on the specific SoC used in the module.

5.5.2 PMIC / Programming Test Points

These test points are **module-specific**. The exact signals connected to these pads are defined in the respective Lino module documentation.

They are primarily intended for:

- Factory programming
- PMIC configuration
- Low-level recovery
- Production testing

Signal allocation:

- `PMIC_I2C_SDA`

- `PMIC_I2C_SCL`
- `PMIC_VIO` (+1.8 V) or `+VDD_SOC`

These signals are used during factory programming and power-management configuration. Customer carrier boards shall leave these pads unconnected.

5.5.3 Voltage Test Points

Voltage test points are also **module-specific**. They access to internal power rails for:

- Electrical validation
- Failure analysis
- Manufacturing verification analysis.

Internal rails shall be exposed through test points to allow electrical verification during manufacturing and debugging. Typical rails include internal core, memory, and auxiliary supplies.

Typical voltage test points include:

- `+V3.3`
- `+VDD_DDR`
- `+VDD_CORE`
- `+VDD_ARM`
- `PMIC_RST_OUT`

The exact set of rails available may vary per module. These pads are intended for testing and diagnostic purposes only and shall not be used to power external circuitry.

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