Toradex
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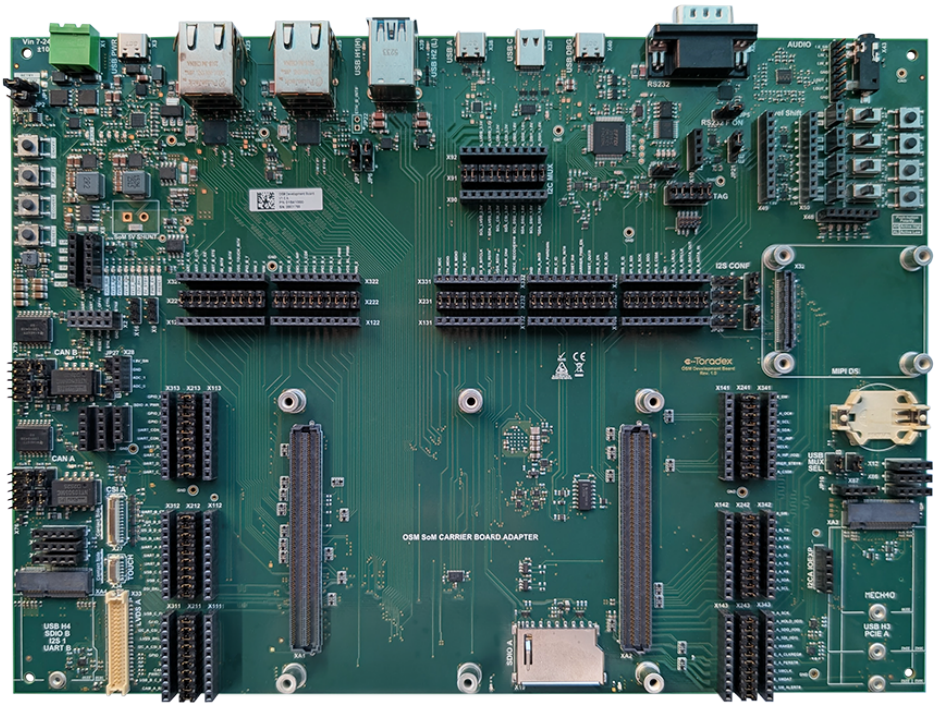
OSM Development Board

Datasheet

Preliminary – Subject to Change



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Abbreviations

Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
BTB	Board To Board
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.

Continued on next page

Abbreviations (Continued)

Abbreviation	Explanation
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1 Introduction

The **OSM Development Board** is a flexible and feature-rich evaluation platform designed to explore and assess the functionality and performance of the OSM (Open Standard Module) product family.

Complementing the OSM System on Module, the OSM Development Board provides access to a wide range of industry-standard interfaces, including high-speed connectivity, multimedia, and expansion capabilities. These interfaces are made available through robust connectors and standard pitch headers, enabling straightforward evaluation, prototyping, and system development.

The board is based on the **OSM standard form factor**, supporting **any OSM size modules** through a mezzanine adapter concept. This architecture allows compatibility across different module sizes while maintaining full adherence to the OSM specification and design guidelines.

The OSM Development Board is intended for:

- Hardware development and system bring-up
- Software and BSP development
- Validation and verification of OSM modules
- Customer evaluation and prototyping

The platform integrates a comprehensive set of interfaces, including:

- Multiple Ethernet ports (including Gigabit and high-speed connectivity)
- USB interfaces (Type-A and Type-C, including debug access)
- PCIe and M.2 expansion (Key B and Key E)
- Display interfaces (MIPI DSI, LVDS)
- Camera interfaces (MIPI CSI)
- Audio, CAN, UART, SPI, I^2C, and GPIO

In addition, the board provides extensive **debugging, measurement, and configuration capabilities**, including:

- JTAG and UART debug interfaces
- Dedicated test points for key signals and power rails
- Configurable jumpers for signal routing and interface selection

The OSM Development Board is designed as a **reference platform**, following semiconductor vendor reference designs and OSM design guidelines to minimize development risk and ensure optimal signal integrity and performance.

Complete CAE design data, including schematics and layout files, is available from the Toradex developer website, enabling users to accelerate their own carrier board designs. To ensure optimal compatibility and user experience with the OSM Development Board, the carrier board is compatible with the DSI to HDMI Adapter[1]. This adapter uses a MIPI DSI interface to provide an HDMI output that seamlessly integrates with all OSM System on Modules, guaranteeing an enhanced and comprehensive user experience.

1.1 Reference Documents

For detailed technical information, please refer to the documents listed below.

[1] https://developer.toradex.com/hardware/accessories/add-ons/dsi-hdmi-adapter

1.1.1 OSM Family Specification

https://sget.org/standards/osm/

1.1.2 OSM Carrier Board Design Guide

TBA
More information about the carrier board design guide will be available on the next releases of the datasheet.

1.1.3 OSM Computer on Module family overview

https://www.toradex.com/de/computer-on-modules/osm-arm-family

1.1.4 Toradex Developer Website – OSM Computer on Module documents

https://developer.toradex.com/hardware/osm-som-family/modules/

1.1.5 Carrier Board Layout Guide

https://docs.toradex.com/102492-layout-design-guide.pdf

1.1.6 Toradex Developer Website – OSM Development Board Design Files

https://developer.toradex.com/hardware/osm-som-family/carrier-boards/osm-development-board

1.1.7 Audio Codec datasheet

https://www.nuvoton.com/export/resource-files/DS_NAU88C22_DataSheet_EN_Rev1.1.pdf

1.1.8 CAN Transceiver datasheet

https://www.ti.com/lit/gpn/ISO1042

1.1.9 EEPROM datasheet

https://www.st.com/resource/en/datasheet/m24c02-w.pdf

1.1.10 Gigabit Ethernet Transceiver datasheet

https://ww1.microchip.com/downloads/en/DeviceDoc/00002841B.pdf

1.1.11 GPIO expander datasheet

https://www.nxp.com/docs/en/data-sheet/PCAL6416A.pdf

1.1.12 Pushbutton On/Off controller datasheet

https://www.analog.com/media/en/technical-documentation/data-sheets/2954fb.pdf

1.1.13 RS232 Transceiver datasheet

https://www.ti.com/lit/ds/symlink/trs3122e.pdf

1.1.14 Temperature sensor datasheet

https://www.ti.com/lit/ds/symlink/tmp1075.pdf

1.1.15 USB HUB datasheet

https://ww1.microchip.com/downloads/en/DeviceDoc/USB5744-Data-Sheet-DS00001855J.pdf

1.1.16 USB Type-C Configuration Channel Logic IC datasheet

https://www.ti.com/lit/ds/symlink/tusb321ai.pdf

1.1.17 UV/OV and Reverse Protection Controller datasheet

https://www.analog.com/media/en/technical-documentation/data-sheets/LTC4368.pdf

1.1.18 Toradex Developer Website – Toradex DSI to HDMI Adapter

https://developer.toradex.com/hardware/accessories/add-ons/dsi-hdmi-adapter/

1.2 Main Features

The OSM Development Board provides a comprehensive set of interfaces and peripherals to enable rapid prototyping, evaluation, and development. The main features are grouped as follows:

1.2.1 USB Interfaces

- 1x USB Type-C connector supporting Dual-Role-Port (DRP) functionality (host/device) with USB 2.0/3.x
- 1x stacked USB Type-A connector providing multiple USB ports via an on-board USB hub
- 1x USB Type-C debug connector supporting UART and JTAG through a USB-to-serial interface
- Integrated USB hub with signal multiplexing and port control

1.2.2 Networking Interfaces

- 2x RJ45 connectors supporting 10/100/1000 Mbps Ethernet with on-board Ethernet PHYs

1.2.3 Wireless and Expansion Interfaces

- 1x M.2 Key-B socket for cellular modules with Nano SIM card support
- 1x M.2 Key-E socket for Wi-Fi/Bluetooth modules

1.2.4 Display and Camera Interfaces

- 1x MIPI® CSI camera interface connector
- 1x MIPI® DSI display interface connector supporting external display adapters (e.g., HDMI, LVDS, RGB)
- 1x LVDS display and touch interface connector

1.2.5 Storage Interfaces

- 1x 4-bit SD card interface
- 1x I^2C EEPROM (2 Kbit) for non-volatile storage

1.2.6 Audio Interfaces

Audio codec with support for:

- 3.5 mm audio jack (headphone/microphone)
- Line-in/line-out via headers
- Additional audio interfaces via expansion connectors

1.2.7 Serial and Communication Interfaces

- 1x RS232 serial interface via DB9 connector
- 2x CAN interfaces (header-based), supporting Classical CAN and CAN FD
- Multiple UART interfaces (including debug access)

1.2.8 Low-Speed and Control Interfaces

- Multiple I^2C buses with multiplexing and level shifting (1.8 V / 3.3 V domains)
- SPI interfaces with jumper-configurable routing
- Multiple PWM outputs
- Multiple ADC inputs with header breakout
- GPIO access via:
  - Direct headers
  - I^2C GPIO expander

1.2.9 Debug and Test Interfaces

- 1x JTAG connector for system debugging
- Test points and header access for signal probing and measurement
- Flexible jumper matrix for signal routing and configuration

1.2.10 Power Management

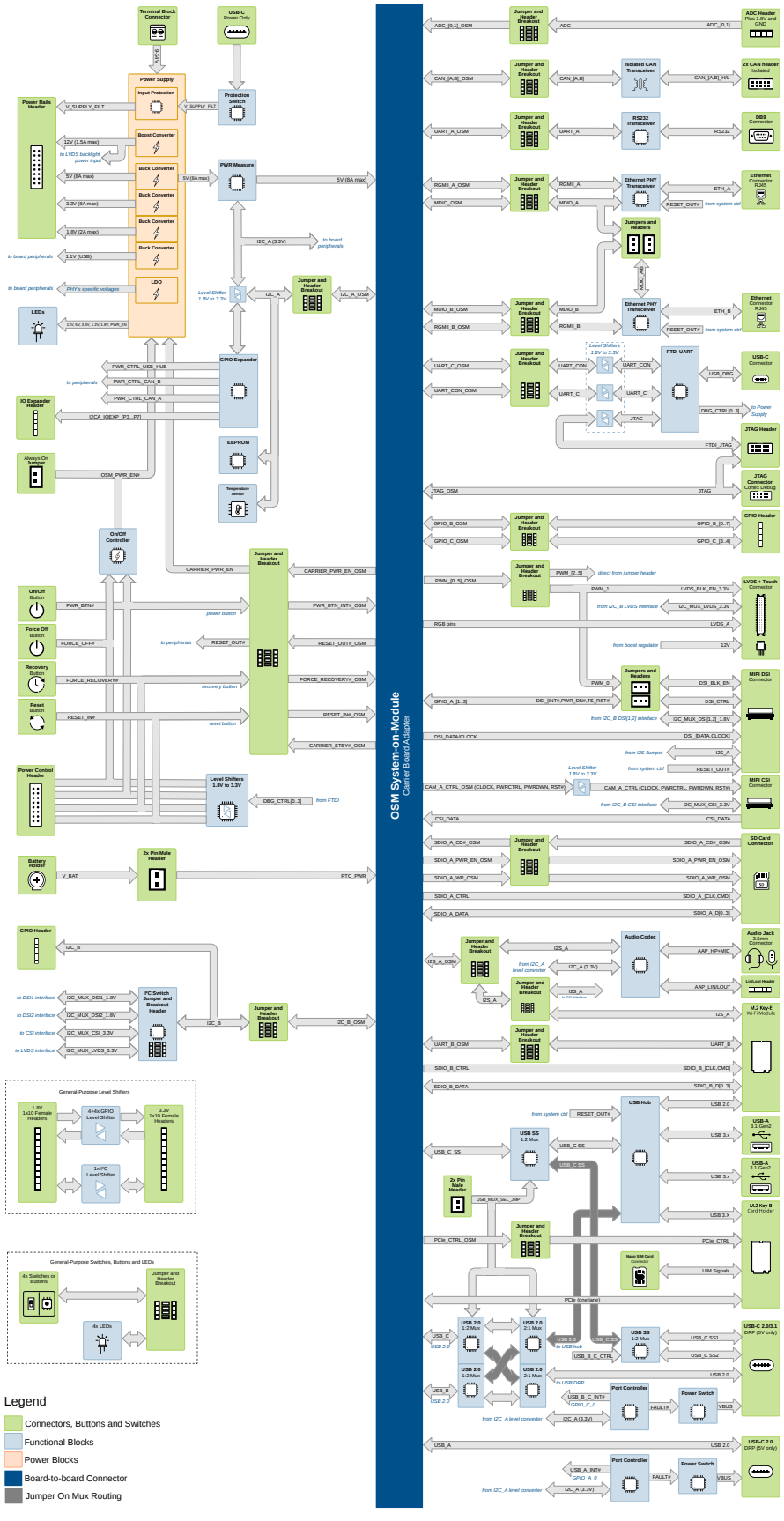
- Wide input voltage range with protection against:
  - Undervoltage
  - Overvoltage
  - Overcurrent
  - Reverse polarity
- Integrated power tree with multiple DC-DC converters (e.g., 5 V, 3.3 V, 1.8 V, 1.2 V rails)
- Power sequencing and control circuitry
- Power measurement and monitoring circuitry
- Real-time clock (RTC) backup battery holder

1.2.11 User Interface and Miscellaneous

- General-purpose push buttons (power, reset, recovery)
- General-purpose switches and LEDs
- Level shifters enabling mixed-voltage I/O (1.8 V or 3.3 V)
- OSM System-on-Module board-to-board connector
- Flexible signal breakout area for rapid prototyping and debugging

1.3 Hardware Architecture Block Diagram

Figure 1: OSM Development Board Hardware Architecture



1.4 Physical Drawing

1.4.1 Top Side Connectors

Figure 2 highlights the connectors and expanders on the top side of the OSM Development Board, and Table 1 adds the description of the signals exposed on each connector.

Figure 2: OSM Development Board connectors and controls

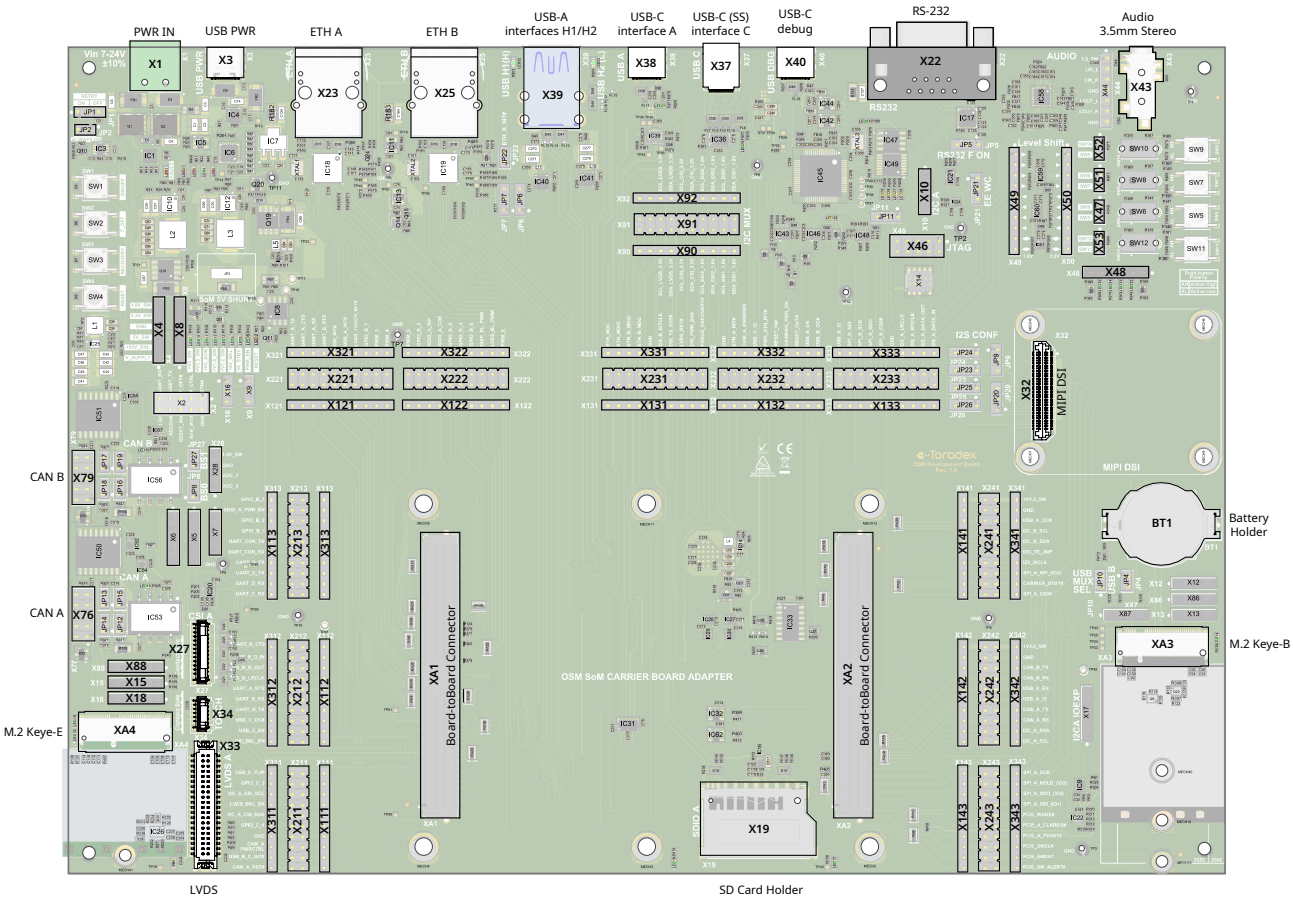


Table 1: Top side connectors

Designator	Description	Remarks
BT1	C2032 battery holder	Backup power for RTC
X1	Power connector	Power input
X2	Power control connector	
X3	USB-C PD connector	Power input
X4	Power Out pin header A	V_SUPPLY, 12V, 5V, 3.3V, 1.8V and GND
X5	Vcc test pin socket	Connected to SOM
X6	Vendor defined pin header	Vendor Defined
X7	Reserved pin header	Reserverd
X8	Power Out pin header B	V_SUPPLY, 12V, 5V, 3.3V, 1.8V and GND
X9	UART_CON RX pin header	
X10	I^2C A pin header	3.3V level
X12	M.2 Key B GPIO pin Socket	
X13	M.2 Key B ANTCTL pins	
X14	JTAG Debug Connector	
X15	M.2 Key E I^2C pin socket	
X16	UART_CON TX pin header	
X17	I^2C A pin socket	Connected through I/O expander
X18	Vendor defined M.2 Key E pin header	
X19	SD Card Holder	
X22	D-Sub Connector	RS485 interface
X23	Gigabit Ethernet RJ45 Connector	Ethernet_A (RGMII via PHY)
X25	Gigabit Ethernet RJ45 Connector	Ethernet_B (RGMII via PHY)
X27	MIPI CSI Connector	High-speed camera interface
X28	ADC pin header	Analog Measurement
X32	MIPI DSI Connector	High-speed display interface
X33	LVDS Connector	High-speed display interface
X34	Capacitive Touchscreen Connector	
X37	USB TYPE-C USB 3.2 Gen 2	Dual-Role-Port SuperSpeed USB
X38	USB Type C 2.0	Dual-Role-Port
X39	USB Type A 3.0 double row	SuperSpeed USB
X40	USB type C 2.0 Connector	USB Debug
X43	3.5mm Stereo Jack With Detect Contact	
X44	Audio Line-in and Line-out pin header	
X46	JTAG pin header	
X47	Switch 5/6 pin header	Switch output
X48	LED control socket	
X49	1.8V GPIO/I^2C pin socket	Connected to level shifter
X50	3.3V GPIO/I^2C pin socket	Connected to level shifter
X51	Switch 9/10 pin header	Switch output

Continued on next page

Table 1: Top side connectors (Continued)

Designator	Description	Remarks
X52	Switch 7/8 pin header	Switch output
X53	Switch 11/12 pin header	Switch output
X76	CAN A pin header	Isolated interface
X79	CAN B pin header	Isolated interface
X86	M.2 Key B GPIO pin socket	
X87	M.2 Key B control pin socket	
X88	M.2 Key E control pin socket	
X90	LVDS/CSI/DSI1/DSI2 I^2C pin socket	Connected to bus switch
X91	3.3V peripheral I^2C jumper header	
X92	LVDS/CSI/DSI1/DSI2 I^2C pin socket	3.3V level
X111	GPIO pin socket	
X112	UART/USB/I^2S pin socket	
X113	GPIO/UART pin socket	
X121	GPIO/UART/PWM pin socket	
X122	GPIO/PWM/SDIO pin socket	
X131	Ethernet A/Ethernet B/GPIO/I^2S pin socket	
X132	GPIO/USB/control pin socket	
X133	I^2C/I^2S/USB pin socket	
X141	DSI/GPIO/USB/I^2C/Power Control pin socket	
X142	CAN/GPIO/USB/I^2C pin socket	
X143	PCIe/SPI pin socket	
X211	USB/GPIO/Camera control jumper header	
X212	UART/GPIO/USB/I^2S pin socket	
X213	GPIO/UART/SDIO jumper header	
X221	GPIO/UART/PWM jumper header	
X222	GPIO/PWM/SDIO jumper header	
X231	Ethernet_A/Ethernet_B/GPIO/I^2S jumper header	
X232	GPIO/USB/Power control jumper header	
X233	SPI/GPIO/USB/I^2S jumper header	
X241	DSI/GPIO/USB/I^2C/Power Control jumper header	
X242	CAN/GPIO/USB/I^2C pin socket	
X243	PCIe/SPI jumper header	
X311	USB/GPIO/Camera control pin socket	
X312	USB/GPIO/Power control pin socket	
X313	GPIO/UART/SDIO pin socket	
X321	GPIO/UART/PWM pin socket	
X322	GPIO/PWM/SDIO pin socket	
X331	Ethernet_A/Ethernet_B/GPIO/I^2S pin socket	
X332	GPIO/USB/Power control pin socket	

Continued on next page

Table 1: Top side connectors (Continued)

Designator	Description	Remarks
X333	SPI/GPIO/USB/I^{2}S pin socket	
X341	DSI/GPIO/USB/I^{2}C/Power Control pin socket	
X342	CAN/GPIO/USB/I^{2}C pin socket	
X343	PCIe/SPI/Audio pin socket	
XA1	Board-to-board connector	OSM Adapter Connector X1
XA2	Board-to-board connector	OSM Adapter Connector X2
XA3	M.2 Card Holder Key B	
XA4	M.2 Card Holder Key E	

1.4.2 Bottom Side Connectors

Figure 3 highlights the connectors and expanders on the bottom side of the OSM Development Board, and Table 2 adds the description of the signals exposed on each connector.

Figure 3: OSM Development Board connectors and controls

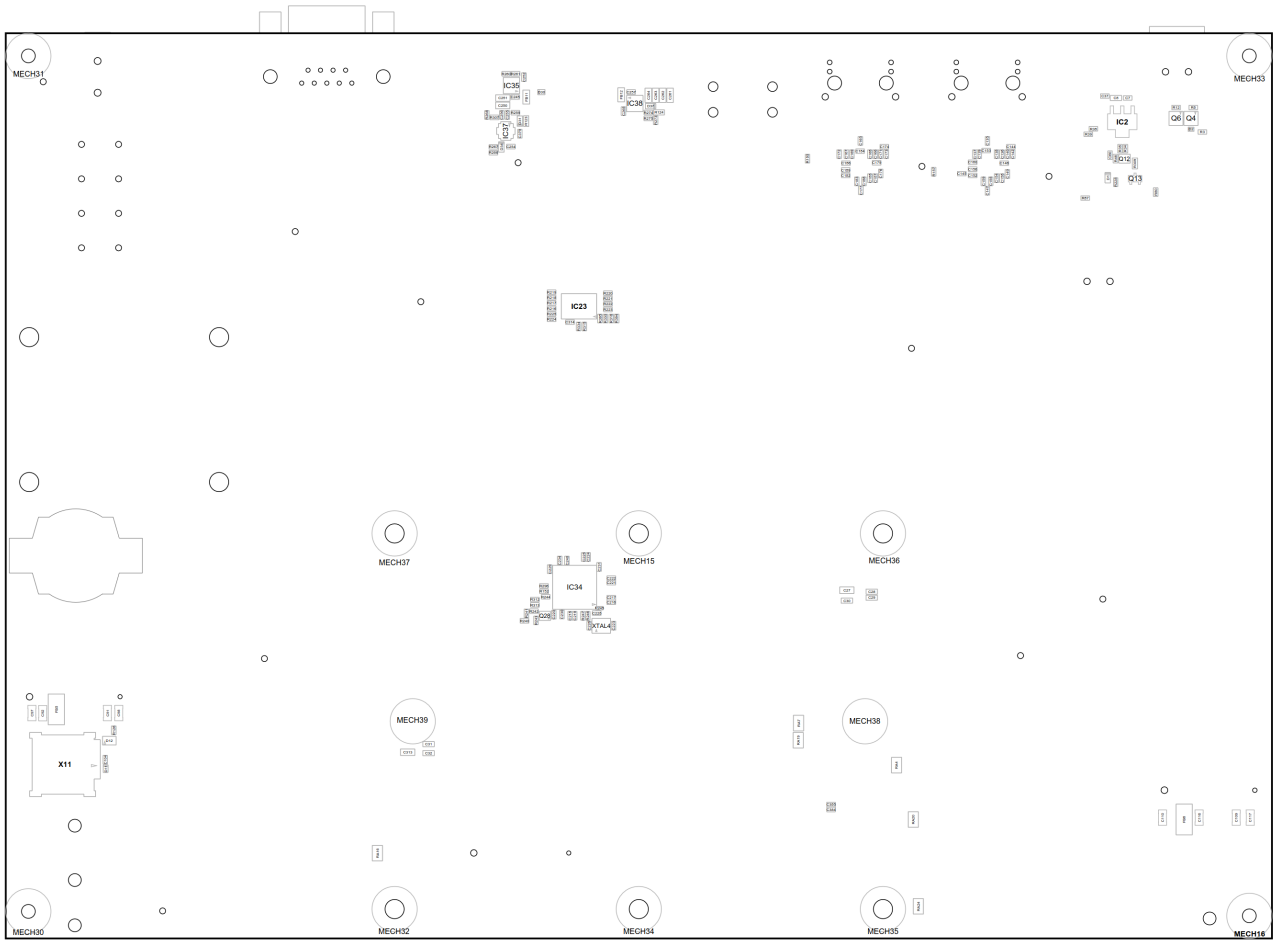


Table 2: Bottom side connectors

Designator	Description	Remarks
X11	Nano SIM Card Holder	Connected to M.2 Key B interface

2 Interfaces Description

2.1 OSM System-on-Module

Connector Type: Direct solder-down (Land Grid Array - LGA) [2]

For the pinout of the OSM module, please refer to the applicable OSM module datasheet or to the OSM Family Specification or the OSM Carrier Board Design guide for the abstract pinout.

2.2 Power Supply

The OSM Development Board can be powered through two input connectors: **X1 (Terminal Block)** and **X3 (USB-C power only)**. Both connectors are electrically tied to the same input rail `+V_SUPPLY_FILT`, providing a wide input voltage range suitable for development and evaluation purposes.

The Terminal Block power connector X1 and the USB-C power connector X3 are independent input sources and are not directly interconnected on the board. Only one of these connectors should be used to supply power at any given time. Simultaneous connection of multiple power sources is not supported and may lead to undefined behavior or potential damage to the board and/or the connected power supplies.

Input Voltage Range and Power Considerations
The supported input voltage range is 7 V to 24 V (±10%). For applications with higher power consumption (e.g., above 35 W), operation at higher input voltages is recommended to reduce input current and improve efficiency.

The input supply is routed through a multi-stage protection and conditioning circuit before reaching the internal system rails. This stage is based on the **LTC4368IDD-2#PBF** input protection controller and provides comprehensive protection against abnormal operating conditions, including:

- Overvoltage (OV) and undervoltage (UV)
- Reverse polarity
- Inrush current during hot-plug events
- Surge and transient events

The protected and filtered output rail is available as `+V_SUPPLY_FILT`, which serves as the main input to the downstream power tree.

The input stage includes:

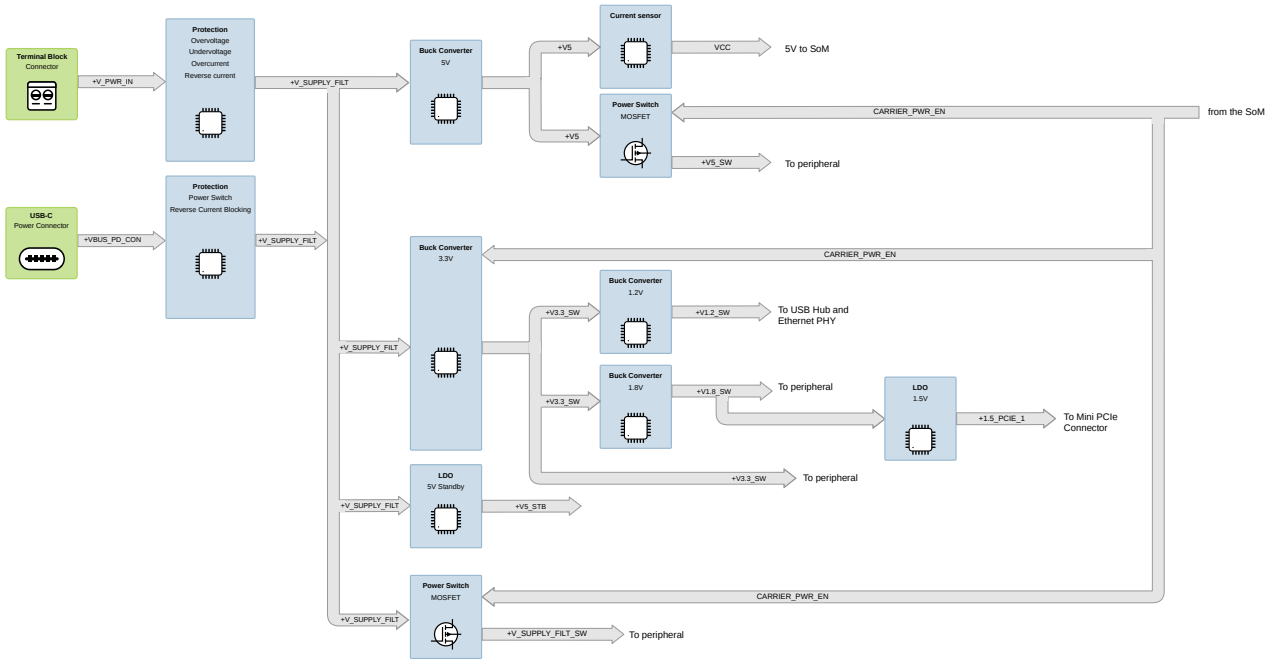
- A TVS diode for surge suppression
- A ferrite bead for EMI filtering
- Bulk and high-frequency decoupling capacitors
- Back-to-back MOSFETs providing ideal diode behavior and reverse polarity protection

Inrush current is actively controlled by the **LTC4368** and limited to approximately **1.5 A**, ensuring safe hot-plug operation and reducing stress on upstream supplies. The device continuously monitors the input voltage using precision resistor dividers and disconnects the load if voltage thresholds are violated. Fault conditions are indicated via an on-board LED, and an automatic retry mechanism (default of approximately 550 ms) can be configured via a jumper.

Other regulated voltage domains are generated on the Development Board from the protected input rail. The board's power supply architecture is illustrated in Figure 4.

[2] The OSM module has flat pads (lands) on the bottom and It is soldered directly onto the carrier board (like a BGA, but with lands instead of balls)

Figure 4: Power supply architecture



The on-board regulators generate multiple supply rails required for system operation, including standby, core, and peripheral voltages. The nominal voltages and available current for each rail are summarized in Table 3.

Table 3: On-Board Power Supplies

Nominal voltage	Maximum current	Maximum power
12V	2.34A	28.08W
5V	8.00A	40W
3.3V	8.00A	26.4W
2.5V	0.50A	1.25W
1.8V	2.00A	3.6W
1.0V	0.50A	0.5W
1.1V	2.00A	2.2W

2.2.1 Terminal Block Power Supply Connector (X1)

Connector Type: Phoenix 1923759

Table 4: Terminal Block Power Supply Connector (X1)

Pin	Description	Voltage / Range
1	GND	Ground reference
2	+V_PWR_IN	7-24V ± 10%

2.2.2 USB-C Power Supply Connector (X3)

Connector Type: GCT USB4105-GF-A-120

Table 5: USB-C Power Supply Connector (X3)

Pin	Description	Voltage / Range
1	+V_PWR_IN_1	7-24V ±10%
2	GND	Ground reference

2.2.3 Power Out Header (X4, X8)

Two female pin headers X4 and X8 provide access to the main system power rails and can be used to power external circuits and evaluation hardware. The pinout of both connectors is the same and is shown in Table 6.

Connector Type: 1x6 Pin Header Female, 2.54 mm pitch.

Table 6: Power Out Header (X4 and X8)

Pin	Power Signal	Description/Remarks
1	+V_SUPPLY_FILT_SW	Protected and switched input rail (7-24V), derived from +V_PWR_IN via LTC4368 unregulated voltage
2	+V12_BL	Boosted 12V rail for display backlight supply
3	+V5_SW	Switched 5V rail generated by main buck regulator up to 8A
4	GND	System ground reference
5	+V3.3_SW	Switched 3.3V rail for peripherals and I/O up to 8A
6	+V1.8_SW	Switched 1.8V rail for logic and low-power domains up to 2A

2.2.4 Power Control

The OSM Development Board power control is implemented using the **LTC2954 Pushbutton On/Off Controller**, which manages system power sequencing and user interaction. The signal CARRIER_PWR_EN is used to enable the main and peripheral power rails, while the signal PMIC_5V_EN is used to enable the 5V buck converter.

For detailed information on the LTC2954 functionality, refer to its datasheet. The controller provides debounced pushbutton handling, controlled power-up sequencing, and system reset generation.

The board includes the following user-accessible switches:

- SW1 - Power button
- SW2 - Hard Reset button
- SW3 - Recovery button
- SW4 - Reset button

The installed OSM module can also control board power via the open-drain signal CARRIER_PWR_EN, allowing a controlled and safe system shutdown.

Power Control Header (X2)

The **Power CTRL connector (X2)** provides external access to power control and reset signals. Table 7 shows the pinout of the respective connector.

Connector Type: 2x3 Pin Header Female, 2.54 mm pitch.

Table 7: Power Control Header (X2)

Pin	Signal Name	IO Type	Voltage	Pull-up/Pull-down	Description/Remarks
1	PWR_BTN#	I/O (OD)	+1.9V	100kΩ to +1.9V	Connected to the POWER ON/OFF button SW1. Pulled-up to 1.9V inside pushbutton controller IC. - Short pulling down turning on Development Board power and Computer Module. - Long pulling down forcing Development Board power off.
2	GND	PWR	–	–	System ground reference.
3	PWR_CTRL	I	+3.3V max	100kΩ to GND	Behaviour is similar to the *Always ON* jumper JP2. HIGH level on the PWR_CTRL input forcing on the OSM Development Board power.
4	PWR_BTN_INT#	I/O (OD)	+1.8V	on SoM	Pulling down for a longer period of time is shutting down the module. Short pulling down is turning on module from off state. Open-drain input with pull-up resistor on the module. The signal can be left floating on carrier boards.
5	FORCE_OFF#	I/O (OD)	+5V	100kΩ to +V5_STB	Forcing the turning-off of the main power rail. This signal is ignored for the first 512ms during the power-up sequence. The signal is 5V tolerant.
6	RESET_IN#	I/O (OD)	+1.8V	on SoM	Open-drain input, which resets the module if shorted to ground. There is an on-module pull-up. This means it can be left floating on the carrier board.
7	UART_CON_PCC_TX	O	+1.8V	–	UART console transmit signal from the module to the external connector. Used for debug output and system console.
8	FORCE_RECOVERY#	I	+1.8V	Pull-up on SoM	Forces the module into recovery/bootloader mode when asserted low during reset or power-up.
9	UART_CON_PCC_RX	I	+1.8V	–	UART console receive signal to the module from external host. Used for debug input and command interface.
10	+V1.8_SW	PWR	+1.8V	–	1.8V switched supply rail available for external use.

Pin 3 of connector X2 can be used to override the pushbutton controller behavior. Table 8 describes the board behavior depending on the level of the PWR_CTRL signal.

Table 8: Power Control Behavior

PWR_CTRL	Description
0V	The Pushbutton controller is working normally
3.3V	The OSM Development Board is Always On when power is applied

Always-ON Jumper (JP2)

Jumper JP2 is used to configure the *Always On* behavior of the board.

Connector Type: 1x2 Pin Header Male, 2.54 mm pitch.

Table 9: Always-ON Jumper (JP2)

Jumper Position	Description
OPEN	The board power supply is controlled with Power On/Off buttons.
CLOSED	The board power supply will be in the "Always On" state. OSM Development Board will be powered up as soon as external power is applied to the connector X57 or X58.

By default, jumper JP2 is open, and the board power is controlled via the pushbutton controller.

2.2.5 Power Supply Input Protection

The input supply is protected against ESD events, reverse polarity, overvoltage, undervoltage, and overcurrent conditions. The protection circuit is based on the LTC4368 from Analog Devices.

This circuit also provides inrush current limiting and controlled startup behavior, ensuring reliable operation during hot-plug events.

For detailed information, refer to the LTC4368 datasheet.

Table 10: Power Supply Input Ratings

Parameter Name	Min	Typ	Max	Unit
Recommended input voltage	**7.0**	**7–24**	**24.0**	**V**
Input voltage (Absolute maximum, limited with TVS diode)	–	–	±30	V
Undervoltage threshold	6.6	7.0	7.4	V
Overvoltage threshold	25.5	27.0	28.5	V
Overcurrent / inrush current limit	1.2	1.5	1.8	A
Reverse current protection	0	300	500	mA

Jumper JP1 configures the retry behavior of the input protection circuit.

Connector Type: 1x3 Pin Header Male, 2.54 mm pitch

Table 11: Jumper Position (JP1)

Jumper Position	Description/Remarks
1-2	Power supply input will restart automatically after a forward overcurrent fault. The restart delay time is defined by capacitor C300 (5.5ms/nF). The typical value for the Development Board is 550ms.
2-3	Power supply input stays OFF after a forward overcurrent fault. The external power supply should be switched OFF and ON to restore the board power.

By default, jumper JP1 is in position 1-2, enabling automatic retry after a fault condition.

2.2.6 Power Monitoring

The board includes a high-side current and voltage monitoring IC **INA219 (IC8)**, allowing measurement of the system power consumption.

The device is connected to the I^2C_A bus and is accessible at address 0x40. It measures the input rail voltage and the voltage drop across a precision shunt resistor, enabling calculation of:

- Input voltage
- Input current
- Power consumption

This feature is useful during system bring-up, validation, and power optimization of the OSM module and connected peripherals.

2.3 ADC – Analog-to-Digital Interface

The Development Board exposes **two ADC input channels** from the SoM, labeled `ADC[0..1]`, which are routed directly to the external header `X28` for easy access and integration. These ADC inputs operate within the `+V1.8_SW` voltage domain, meaning that any external analog source must remain within the valid input range of the SoM ADC and be referenced to the board ground. Since no additional buffering or protection circuitry is implemented on these lines, proper signal conditioning must be ensured by the user. This may include external voltage dividers, filtering, or protection components to prevent overvoltage and ensure reliable and safe operation.

Table 12 shows the typical characteristics of the ADC interface.

Table 12: ADC typical characteristics

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input voltage range	0	–	VREF	V	Defined by SoM ADC reference
Resolution	–	10 to 12	–	bits	SoM dependent
Input impedance	–	High	–	Ω	Avoid heavy loading
Sampling rate	–	–	1	MS/s	Depends on SoM

Design Notes

- Inputs must remain within the SoM voltage domain (**1.8 V domain**)
- External filtering (RC) is recommended for noisy signals
- Overvoltage must be avoided (no internal protection)

Table 13 shows the pinout for the ADC interface.

Table 13: ADC interface

OSM pin	Signal name	Description / Remarks
D45	ADC_0	ADC input channel 0 from the SoM; exposed on the PWM/ADC interface area for external analog measurement.
D43	ADC_1	ADC input channel 1 from the SoM; exposed on the PWM/ADC interface area for external analog measurement.

2.4 Audio Subsystem

The OSM Development Board integrates a high-performance **audio subsystem** based on the **WM8904CGEFL/RV** low-power stereo audio codec. This device provides high-quality digital-to-analog (DAC) and analog-to-digital (ADC) conversion, supporting both playback and recording paths.

The codec interfaces with the SoM via **I^2S (digital audio)** and **I^2C (control interface)** and supports:

- Stereo headphone output

- Line-level input and output
- Microphone input with integrated bias generation
- Flexible analog routing and filtering

2.4.1 Audio Codec

The OSM Development Board integrates the WM8904CGEFL/RV audio codec to provide a complete analog and digital audio interface solution. This device enables high-quality audio playback and recording by interfacing directly with the SoM through standard digital audio interfaces such as I^2S, while handling all necessary analog signal conditioning on the carrier board.

The codec is designed to support a wide range of audio applications, including line-in/line-out, microphone input, and headphone output. By integrating key analog functions such as amplification, bias generation, and filtering, the WM8904 simplifies system design and reduces the need for external audio components, while maintaining high audio performance and low power consumption.

The WM8904 is a **low-power, high-performance stereo codec** featuring:

- 24-bit DAC and ADC paths
- Integrated headphone driver
- Programmable gain amplifiers (PGA)
- Microphone bias generator (MICBIAS)
- Low-noise analog front-end

Key Features

- Sampling rates up to 96 kHz
- High SNR and low THD audio performance
- Capless headphone output support
- Integrated digital audio processing
- I^2S / PCM digital audio interface
- I^2C control interface

2.4.2 Signal Conditioning and Protection

The audio subsystem on the OSM Development Board incorporates signal conditioning and protection mechanisms to ensure reliable operation and high audio quality when interfacing with external devices.

All external audio lines are protected against electrostatic discharge (ESD) using dedicated protection diodes, safeguarding the codec and surrounding circuitry from transient voltage events. In addition, RC filtering networks are implemented on sensitive analog paths to suppress high-frequency noise and improve signal integrity.

Ferrite beads are used on selected audio lines to reduce electromagnetic interference (EMI), preventing unwanted coupling between digital and analog domains. Furthermore, AC coupling capacitors are included in the signal path to eliminate DC offsets between the codec and external devices, ensuring proper biasing and optimal audio performance.

2.4.3 Digital Audio Interface

I^2S Interfae

The codec is connecetd to the SoM through the I2S_A interface, providing full-duplex digital audio

streaming. Table 14 shows the connection between the audio and control signals from the SoM to the codec.

Table 14: Audio interface

XA2 pin	SoM signal	Codec pin	Codec signal	I/O	Description
I²S interface					
C8	I2S_MCLK	28	MCLK	I	Master clock input to codec
A95	I2S_A_BITCLK	29	BCLK / GPIO4	I	Bit clock
A94	I2S_A_LRCLK	30	LRCLK	I	Left/right word clock
B100	I2S_A_DATA_IN	31	ADCDAT	O	Audio data from SoM (DAC input)
A96	I2S_A_DATA_OUT	32	DACDAT	I	Audio data to SoM (ADC output)
I²C interface[1]					
D18	I2C_A_SCL	2	SCLK	I	Serial clock
D19	I2C_A_SDA	3	SDA	I/O	Serial data

[1] The control signals are responsible for power management, audio routing, gain control, and sampling configuration.

Codec Mode
- The codec operates as an I²S slave
- The codec configuration is handled via the I2C_A bus.
- Clocking is driven by the SoM

2.4.4 Analog Audio Paths

Stereo Jack Output (X43)

The WM8904 provides a stereo output via the signals

- AAP_HP_L: left output
- AAP_HP_R: right output

Which are routed to a **3.5 mm audio jack** (X43). The implementation includes ferrite beads (FB17, FB18) for EMI filtering, along with AC coupling and additional filtering to ensure signal integrity. The output path is protected by ESD diodes and leverages the codec's integrated output stage, allowing it to directly drive audio devices while minimizing the need for external components.

Stereo Jack Input (X43)

The design supports an analog microphone input on the same stereo audio jack (X43), using the signals

- AAP_MICIN: microphone input
- AAP_MICBIAS: microphone bias voltage

The WM8904 internally generates the bias voltage, which is decoupled using 4.7 µF capacitor. The input path is AC-coupled and includes EMI filtering via ferrite bead (FB21) as well as ESD protection. This implementation supports electret microphones, provides a low-noise signal path, and allows programmable gain control through the codec.

Line Input

A stereo line-level input is provided through connector X44, using the signals

- AAP_LIN_L: left line input
- AAP_LIN_R: right line input

The input path includes AC coupling 10 µF capacitors and RC filtering networks to ensure proper signal conditioning before reaching the codec.

Line Output

A stereo line-level output is provided through connector X44, using the signals

- AAP_LOUT_L: left line output
- AAP_LOUT_R: right line output

The output path includes filtering via ferrite beads (FB19, FB20), as well as AC coupling and EMI suppression to ensure clean signal transmission to the external interface.

2.4.5 Audio Connectors

Headphone Jack (X43)

- Standard 3.5 mm stereo jack with microphone support
- Connections:
  - Left audio
  - Right audio
  - Microphone input
  - Ground

Line Audio Connector (X44)

Provides access to

- Line input (L/R)
- Line output (L/R)
- Ground reference
- Optional supply rail (+1.8V switchable)

2.4.6 Power and Filtering

The audio subsystem includes dedicated filtering for optimal signal quality:

- Ferrite beads for analog/digital isolation
- Local decoupling capacitors on:
  - MICBIAS
  - Audio inputs/outputs
- Separation of analog and digital grounds (where applicable)

2.5 CAN – Controller Area Network

The OSM Development Board provides two independent **Controller Area Network (CAN)** interfaces:

- CAN_A
- CAN_B

Both interfaces are implemented using **isolated CAN transceivers**, enabling robust and reliable communication in electrically noisy environments while providing galvanic isolation between the system and the CAN bus. Each CAN interface uses the Texas Instruments ISO1042BDWR, which integrates high-speed CAN transceiver (ISO 11898-2 compliant) and galvanic isolation.

Key features of the isolated CAN transceivers are the following

- Bus interface: differential (CANH/CANL)
- CAN standard: ISO 11898-2 (high-speed CAN)
- Common-mode range: ±30 V (bus fault tolerance)
- Data rate: up to 5 Mbps
- Integrated protection: ESD, thermal shutdown, bus fault protection
- Isolation voltage: 5 kVRMS (galvanic isolation)
- Supply domain: separate logic-side and bus-side supplies

The CAN signals are exposed via the X2B board-to-board connector, allowing direct access to both CAN channels, and the pinout of these interfaces is shown in Table 15.

Table 15: CAN interfaces

XA2B Pin	Signal Name	Direction	Description
CAN A			
D21	CAN_A_RX	Input	CAN_A receive data
A24	CAN_A_TX	Output	CAN_A transmit data
CAN B			
A22	CAN_B_RX	Input	CAN_B receive data
A23	CAN_B_TX	Output	CAN_B transmit data

2.6 CSI – Camera Serial Interface

The OSM Development Board provides a **MIPI CSI-2 camera interface** through connector XA1, enabling direct connection of CMOS image sensors or camera modules.

This interface supports high-speed differential signaling compliant with the **MIPI CSI-2 specification**, allowing efficient transfer of image data to the System-on-Module (SoM).

Key features include:

- Up to 4 data lanes + 1 clock lane
- High-speed differential signaling (100 Ω impedance)
- Integrated I^2C control interface for camera configuration
- Dedicated camera master clock (MCLK) output
- On-board ESD and EMI protection for robust operation

2.6.1 MIPI CSI-A High-Speed Interface

The CSI interface uses **low-voltage differential signaling** for high-speed data transmission between the image sensor and the SoM.

Table 16 shows the MIPI CSI pinout.

Table 16: MIPI CSI interface

SoC Ball	Signal Name	Direction	Description
Data Signals			
A22	CSI_A_CLOCK_P	Input	Differential clock positive
A21	CSI_A_CLOCK_N	Input	Differential clock negative
A19	CSI_A_DATA0_P	Input	Data lane 0 positive
A18	CSI_A_DATA0_N	Input	Data lane 0 negative
B20	CSI_A_DATA1_P	Input	Data lane 1 positive
B19	CSI_A_DATA1_N	Input	Data lane 1 negative
B23	CSI_A_DATA2_P	Input	Data lane 2 positive
B22	CSI_A_DATA2_N	Input	Data lane 2 negative
A25	CSI_A_DATA3_P	Input	Data lane 3 positive
A24	CSI_A_DATA3_N	Input	Data lane 3 negative
Camera Clock Output			
B17	CAM_MCK	Output	Camera clock output
Control Signals[1]			
D22	CAM_A_SCL or CSI_A_TX_P	Output	I^2C clock (multiplexed)
D20	CAM_A_SDA or CSI_A_TX_N	Bidirectional	I^2C data (multiplexed)

[1] The control signals are used for camera configuration and status monitoring via I^2C, e.g. register monitoring and parameter tuning.

Electrical Characteristics

- Differential impedance: **100 Ω (controlled)**
- Signaling standard: **MIPI D-PHY (CSI-2)**
- **MIPI CSI Connector (X27)**
  - **Connector Type:** 24-position FFC/FPC, 0.5 mm pitch, vertical
  - **Recommended Part:** Hirose `FH12-24S-0.5SH(55)` or equivalent
- High-speed serial transmission with embedded clocking
- Lane utilization depends on SoM configuration

2.6.2 ESD and EMI Protection

The MIPI CSI interface includes **dedicated protection circuitry** to ensure signal integrity and robustness. High-speed CSI differential pairs are protected using low-capacitance ESD diodes placed close to the connector to minimize exposure to external discharges while preserving signal integrity and performance.

2.7 DSI – Display Serial Interface

The OSM Development Board provides a **MIPI DSI (Display Serial Interface)** through connector XA2, enabling direct connection of display modules. This interface supports high-speed differential signaling compliant with the **MIPI DSI specification**, allowing efficient transmission of pixel data from the System-on-Module (SoM) to the display.

Key features include:

- Up to 4 data lanes + 1 clock lane

- High-speed differential signaling (100 Ω impedance)
- Optional Display Tearing Effect (TE) signal for synchronization
- Dual-use capability with LVDS_A interface signals
- On-board ESD and EMI protection for robust operation

2.7.1 MIPI DSI High-Speed Interface

The DSI interface uses low-voltage differential signaling (MIPI D-PHY) for high-speed transmission of display data.

Table 17 shows the pinout of the MIPI DSI interface, which pins may also be used as an LVDS interface. The selection of which interface to use is carried out in software.

Table 17: MIPI DSI interface

SoC Ball	Signal Name	Direction	Description
Clock Signals			
D9	DSI_CLOCK_P / LVDS_A_CLK_P	Output	Differential clock positive
D10	DSI_CLOCK_N / LVDS_A_CLK_N	Output	Differential clock negative
Data Signals			
D15	DSI_DATA0_P / LVDS_A_LANE0_P	Output	Data lane 0 positive
D16	DSI_DATA0_N / LVDS_A_LANE0_N	Output	Data lane 0 negative
D12	DSI_DATA1_P / LVDS_A_LANE1_P	Output	Data lane 1 positive
D13	DSI_DATA1_N / LVDS_A_LANE1_N	Output	Data lane 1 negative
B20	DSI_DATA2_P / LVDS_A_LANE2_P	Output	Data lane 2 positive
B21	DSI_DATA2_N / LVDS_A_LANE2_N	Output	Data lane 2 negative
D6	DSI_DATA3_P / LVDS_A_LANE3_P	Output	Data lane 3 positive
D7	DSI_DATA3_N / LVDS_A_LANE3_N	Output	Data lane 3 negative
Synchronization Signal			
B13	DSI_TE_OSM	Input	Tearing Effect signal from display

Electrical Characteristics

- Differential impedance: **100 Ω (controlled)**
- Signaling standard: **MIPI D-PHY (DSI)**
- **MIPI DSI Connector (X32)**
  - **Connector Type:** 60-position board-to-board (mezzanine) connector, 0.5 mm pitch, vertical, dual-row
  - **Recommended Part:** Samtec `LSS-130-03-L-DV-A-K-TR`
- High-speed serial transmission
- Lane configuration depends on SoM and display requirements

The syncronization signal in Table 17 is used for **frame synchronization** between display and SoM. It helps prevent screen tearing and frame misalignment.

2.7.2 ESD and EMI Protection

The MIPI CSI interface includes **dedicated protection circuitry** to ensure signal integrity and robustness. High-speed CSI differential pairs are protected using low-capacitance ESD diodes placed close to the connector to minimize exposure to external discharges while preserving signal integrity and performance.

2.7.3 Functional Description and Integration Guidelines

The SoM generates pixel data and serializes it into the MIPI DSI format, which is then transmitted over differential pairs to the display module. The display receives this high-speed data stream and reconstructs the image frames for rendering. In addition to the data path, a synchronization mechanism may be used in which the display asserts the DSI_TE (Tearing Effect) signal. The SoM uses this signal to align frame updates, ensuring smooth and tear-free display operation.

2.8 Ethernet

The OSM Development Board provides two independent **Gigabit Ethernet interfaces**, ETH_A and ETH_B, each implemented using a dedicated **DP83867 Ethernet PHY**. These PHYs interface the SoM MAC through an **RGMII interface** and support **10 / 100 / 1000 Mbps (10/100/1000BASE-T)** operation.

In the transmit path, data from the SoM is passed to the PHY via RGMII, where it is encoded and driven through the integrated magnetics of the RJ45 connector, ensuring proper isolation and signal conditioning before being transmitted over the Ethernet cable. In the receive path, incoming Ethernet signals are first filtered and isolated by the magnetics, then decoded by the PHY and forwarded back to the SoM.

Both PHYs are controlled via a shared **MDIO/MDC management interface**, which is used for configuration, link negotiation, and status monitoring. Proper operation of the Ethernet interfaces relies on correct PHY configuration and timing alignment, particularly RGMII clock delays, as well as controlled impedance routing, robust grounding and shielding.

Each interface is routed to an **RJ45 connector with integrated magnetics**, providing a complete, standards-compliant Ethernet solution suitable for high-reliability and high-throughput applications.

Key features include

- Two independent Gigabit Ethernet channels (ETH_A, ETH_B)
- **DP83867 PHY** per interface with RGMII connection to the SoM
- Support for **10 / 100 / 1000 Mbps** Ethernet
- Integrated PHY features such as:
  - Internal delay support for RGMII timing
  - Auto-negotiation and auto MDI/MDIX
- Standard **RJ45 connectors with integrated magnetics**
- On-board **ESD protection and EMI filtering**
- Dedicated **link and activity LED outputs**

Ethernet Connectors

- ETH_A: connector X23 (RJ45 with magnetics)
- ETH_B: connector X25 (RJ45 with magnetics)

Both interfaces include:

- Meeting **IEC61000-4-2** standards
- Integrated transformer isolation

- Common-mode filtering
- LED indicators (link/activity)

2.8.1 ETH_A Interface Signals

Table 18 shows the connections of the ETH_A.

Table 18: Ethernet A interface

SoC Ball	Signal Name	Direction	Description
Control Signals			
C40	ETH_MDC	Output	Management Data Clock
D36	ETH_MDIO	Bidirectional	Management Data I/O
Data Signals			
D41	ETH_A_(S)(R)GMII_TXD0	Output	Transmit data bit 0
D40	ETH_A_(S)(R)GMII_TXD1	Output	Transmit data bit 1
B31	ETH_A_(S)(R)GMII_TXD2	Output	Transmit data bit 2
B30	ETH_A_(S)(R)GMII_TXD3	Output	Transmit data bit 3
D25	ETH_A_(R)(G)MII_TX_CLK	Input	Transmit clock
D29	ETH_A_(R)(G)MII_TX_EN(ER)	Output	Transmit enable
A27	ETH_A_(S)(R)GMII_RXD0	Input	Receive data bit 0
A28	ETH_A_(S)(R)GMII_RXD1	Input	Receive data bit 1
D32	ETH_A_(R)(G)MII_RXD2	Input	Receive data bit 2
B33	ETH_A_(R)(G)MII_RXD3	Input	Receive data bit 3
D33	ETH_A_(R)(G)MII_RX_CLK	Input	Receive clock
C38	ETH_A_(R)(G)MII_RX_DV(ER)	Input	Receive data valid
D37	ETH_A_SDP	Input/Output	PHY signal detect / status

2.8.2 ETH_B Interface Signals

Table 19 shows the connections of the ETH_B.

Table 19: Ethernet B interface

SoC Ball	Signal Name	Direction	Description
Control Signals			
D27	ETH_B_MDC	Output	Management Data Clock
D30	ETH_B_MDIO	Bidirectional	Management Data I/O
Data Signals			
D13	ETH_B_(S)(R)GMII_TXD0	Output	Transmit data bit 0
D14	ETH_B_(S)(R)GMII_TXD1	Output	Transmit data bit 1
D16	ETH_B_(S)(R)GMII_TXD2	Output	Transmit data bit 2
D17	ETH_B_(S)(R)GMII_TXD3	Output	Transmit data bit 3
C12	ETH_B_(R)(G)MII_TX_CLK	Input	Transmit clock

Continued on next page

Table 19: Ethernet B interface (Continued)

SoC Ball	Signal Name	Direction	Description
C14	ETH_B_(R)(G)MII_TX_EN(ER)	Output	Transmit enable
D11	ETH_B_(S)(R)GMII_RXD0	Input	Receive data bit 0
D10	ETH_B_(S)(R)GMII_RXD1	Input	Receive data bit 1
D5	ETH_B_(R)(G)MII_RXD2	Input	Receive data bit 2
D3	ETH_B_(R)(G)MII_RXD3	Input	Receive data bit 3
D2	ETH_B_(R)(G)MII_RX_CLK	Input	Receive clock
D8	ETH_B_(R)(G)MII_RX_DV(ER)	Input	Receive data valid
D7	ETH_B_SDP	Input/Output	PHY signal detect / status

2.8.3 LED Status Indicators

Each Ethernet connector includes LED outputs controlled by the PHY, as shown in Table 20.

Table 20: Ethernet status indicators

Pin	Signal	Interface	Description/Remarks
Ethernet A			
P14 (X23)	ETH_A_ACT	ETH_A	Activity indicator
P12 (X23)	ETH_A_LINK	ETH_A	Link status indicator
Ethernet B			
P14 (X25)	ETH_B_ACT	ETH_B	Activity indicator
P12 (X25)	ETH_B_LINK	ETH_B	Link status indicator

2.9 GPIO – General-Purpose Input/Output

The GPIO implementation closely follows the development-board pattern used by Toradex: the carrier brings a bank of SoM GPIOs into a configurable jumper field, allowing the same SoM-capable pins to be used either as generic GPIOs or as alternate board-control functions. The GPIO sheet explicitly labels the bank as `GPIO_OSM[0..23]` and ties the interface to `+V1.8_SW`, indicating a **1.8 V logic domain**.

A number of these pins are reused for board-level functions such as:

- display power enable,
- display backlight enable,
- camera power and reset,
- SPI chip-select alternatives.

This is a common carrier-board design choice: the pins remain software-configurable, but the default wiring gives them a meaningful development-board purpose.

Table 21: GPIO Interface

OSM Pin	Signal Name	Description/Remarks
Bank A		

Continued on next page

Table 21: GPIO Interface (Continued)

OSM Pin	Signal Name	Description/Remarks
A51	GPIO_A_0	USB_A_INT#: active-low interrupt signal indicating events from the USB_A interface routed through jumper matrix as GPIO_A_0_JMP[1]
A50	GPIO_A_1	DSI_INT#: active-low interrupt signal from the DSI display or associated touch/display controller routed through jumper matrix as GPIO_A_1_JMP[1]
D47	GPIO_A_2	DSI_TS_RST#: active-low reset signal for the DSI touch controller routed through jumper matrix as GPIO_A_2_JMP[2]
C44	GPIO_A_3	DSI_PWR_DN#: active-low power-down control signal for the DSI display subsystem routed through jumper matrix as GPIO_A_3_JMP[2]
C43	GPIO_A_4	LVDS_RST#: active-low reset signal for the LVDS display or associated circuitry routed through jumper matrix as GPIO_A_4_JMP[2]
A54	GPIO_A_5	LVDS_TOUCH_INT#: active-low interrupt signal from the LVDS touch controller routed through jumper matrix as GPIO_A_5_JMP[1]
C37	SPI_A_CS1# / GPIO_A_6	CAM_A_PWRDWN#: active-low power-down control signal for Camera A module routed through jumper matrix as GPIO_A_6_JMP[3]
B40	SPI_B_CS1# / GPIO_A_7	ETH_A_INT#: active-low interrupt signal from the Ethernet PHY routed through jumper matrix as GPIO_A_7_JMP[3]
Bank B		
B69	GPIO_B_0	GPIO_B_0: general-purpose input/output signal routed through jumper matrix as GPIO_B_0_JMP[4]
B73	GPIO_B_1	GPIO_B_1: general-purpose input/output signal routed through jumper matrix as GPIO_B_1_JMP[5]
B74	GPIO_B_2	GPIO_B_2: general-purpose input/output signal routed through jumper matrix as GPIO_B_2_JMP[5]
B75	GPIO_B_3	GPIO_B_3: general-purpose input/output signal routed through jumper matrix as GPIO_B_3_JMP[5]
B68	GPIO_B_4	GPIO_B_4: general-purpose input/output signal routed through jumper matrix as GPIO_B_4_JMP[4]
B66	GPIO_B_5	GPIO_B_5: general-purpose input/output signal routed through jumper matrix as GPIO_B_5_JMP[4]
C62	GPIO_B_6	GPIO_B_6: general-purpose input/output signal routed through jumper matrix as GPIO_B_6_JMP[4]
C61	GPIO_B_7	GPIO_B_7: general-purpose input/output signal routed through jumper matrix as GPIO_B_7_JMP[1]
Bank C		
C20	GPIO_C_0	USB_B_C_INT#: active-low interrupt signal from USB multiplexer routed through jumper matrix as GPIO_C_0_JMP[6]
D24	GPIO_C_1	USB_C_FLIP: signal indicating USB Type-C cable orientation (CC polarity detection) routed through jumper matrix as GPIO_C_1_JMP[6]
D21	GPIO_C_2	LVDS_BKL_EN: enable signal for LVDS display backlight control routed through jumper matrix as GPIO_C_2_JMP[6]
C21	GPIO_C_3	GPIO_C_3: general-purpose input/output signal routed through jumper matrix as GPIO_C_3_JMP[6]

Continued on next page

Table 21: GPIO Interface (Continued)

OSM Pin	Signal Name	Description/Remarks
D19	DISP_VDD_EN / GPIO_C_4	GPIO_C_4: general-purpose input/output signal routed through jumper matrix as GPIO_C_4_JMP[6]
D26	DISP_BL_EN / GPIO_C_5	DSI_BKL_EN: enable signal for DSI display backlight control routed through jumper matrix as GPIO_C_5_JMP[7]
B16	CAM_A_PWR / GPIO_C_6	CAM_A_PWRCTRL: power control signal enabling the Camera A power rail routed through jumper matrix as GPIO_C_6_JMP[6]
C19	CAM_A_RST# / GPIO_C_7	CAM_A_RST#: active-low reset signal for Camera A module routed through jumper matrix as GPIO_C_7_JMP[6]

[1] The signal pass through jumper X221 and is only available at their respective destination when the corresponding jumper pins are closed.
[2] The signal pass through jumper X231 and is only available at their respective destination when the corresponding jumper pins are closed.
[3] The signal pass through jumper X232 and is only available at their respective destination when the corresponding jumper pins are closed.
[4] The signal pass through jumper X222 and is only available at their respective destination when the corresponding jumper pins are closed.
[5] The signal pass through jumper X213 and is only available at their respective destination when the corresponding jumper pins are closed.
[6] The signal pass through jumper X211 and is only available at their respective destination when the corresponding jumper pins are closed.
[7] The signal pass through jumper X212 and is only available at their respective destination when the corresponding jumper pins are closed.

2.10 I²C – Inter-Integrated Circuit

The OSM Development Board provides I²C buses used for on-board system management, monitoring, and identification devices. A shared low-speed I²C bus with multiple peripherals connected in parallel, using pull-ups to the main logic rail.

Key Characteristics

- I²C buses: `I2C_[A..B]`
- Voltage domain: mixed 1.8 V / 3.3 V, with level shifting (IC26) between domains
- Pull-ups: implemented on the board for both voltage domains
- Address conflicts: avoided by configuring I²C components' addresses

2.10.1 I²C SoM Pin Mapping

Table 22 shows the mapping between the I²C interfaces of the OSM Development Board and the corresponding I²C signals of the OSM System-on-Module.

Table 22: I²C interfaces

Board-toBoard pin	OSM Dev Board signal	SoM signal name	SoM pad	Description
I²C A				
D18	I2C_A_SCL	I2C_A_SCL SoC: I2C3_SCL alternate function of GPIO29	AA15	I²C clock line (shared bus)
D19	I2C_A_SDA	I2C_A_SDAL SoC: I2C3_SCL alternate function of GPIO28	AA16	I²C data line (shared bus)
I²C B				
B17	I2C_B_SCL	I2C_B_SCL SoC: I2C1_SCL signal	AA20	I²C clock line (shared bus)
B18	I2C_B_SDA	I2C_B_SDA SoC: I2C1_SDA signal	AA21	I²C data line (shared bus)

2.10.2 I²C Components

The OSM Development Board integrates several peripheral devices connected to the primary I²C bus (`I2C_A`). This bus is routed from the SoM through dedicated pins and distributed to on-board compo-

nents such as the EEPROM, temperature sensor, and power monitor. All devices share the same I²C lines and are differentiated by their unique slave addresses, which are either fixed or configurable via hardware pins. The bus operates across mixed voltage domains, with level shifting implemented on-board to ensure compatibility between the SoM and peripheral devices.

Table 23 shows the addresses of the on-board I²C components.

Table 23: I2C components and address mapping

SoM Pin	Signal Name	Part Number	Address	Description / Remarks
EEPROM				
14	I2C_A_SCL	M24C02	0x57	EEPROM clock line, address set via E0/E1/E2 pins
12	I2C_A_SDA		0x57	EEPROM data line, shared I²C bus
Temperature Sensor				
14	I2C_A_SCL	TMP1075DSGR	0x4F	Temperature sensor clock line, address configurable via A0/A1/A2
12	I2C_A_SDA		0x4F	Temperature sensor data line
Power Monitor				
14	I2C_A_SCL	INA219BIDR	0x40	Power monitor clock line, measures voltage/current
12	I2C_A_SDA		0x40	Power monitor data line

2.11 I²S – Inter-IC Sound

The OSM Development Board exposes **Inter-IC Sound (I²S)** signals from the SoM to the carrier, providing two independent digital audio interfaces for external audio connectivity and evaluation:

- I2S_A
- I2S_B

These interfaces are routed directly from the SoM to the carrier board and are exposed for development use through external headers and on-board routing options. The design enables flexible connection to external audio devices such as codecs, amplifiers, or digital microphones.

Both interfaces follow a development-board philosophy:

- Direct signal exposure with minimal conditioning
- Configurable routing via jumpers
- Support for external or on-board audio devices

In addition to external access, the I2S_A interface is **connected to an on-board audio codec** (the **WM8904CGEFL/RV** from Cirrus), which is selected by default through jumper configuration.

External Interface (Headers)

Both I²S interfaces are exposed on dedicated dual-row pin headers:

- **TSW-110-07-G-D (Samtec)**

These headers provide direct access to the associated clock and data lines, enabling connection to the SoM I²S interfaces and simplifying integration with external audio codecs, DACs, ADCs, and other digital audio peripherals.

2.11.1 I²S Signal Mapping

Table 24 shows the I²S signal mapping.

Table 24: I²S interfaces

XA2 Pin	Signal Name	OSM signal name	OSM pad	I/O	Description / Remarks
Shared Signal					
C8	I2S_MCLK_OSM	I2S_MCLK	V18	O	Master clock for audio system this signal is shared between both I²S interfaces and can be used by either interface
I²S A					
A95	I2S_A_BITCLK_OSM	I2S_A_BITCLK	W20	O	Bit clock
A94	I2S_A_LRCLK_OSM	I2S_A_LRCLK	W18	O	Left/Right channel select
A96	I2S_A_DATA_OUT_OSM	I2S_A_DATA_OUT	W21	O	Audio data output from SoM
B100	I2S_A_DATA_IN_OSM	I2S_A_DATA_IN	V21	I	Audio data input to SoM
I²S B					
D52	I2S_B_BITCLK_OSM	I2S_B_BITCLK	T19	O	Bit clock
A45	I2S_B_LRCLK_OSM	I2S_B_LRCLK	T18	O	Left/Right channel select
A46	I2S_B_DATA_OUT_OSM	I2S_B_DATA_OUT	W19	O	Audio data output
A47	I2S_B_DATA_IN_OSM	I2S_B_DATA_IN	V19	I	Audio data input

2.12 JTAG – Joint Test Action Group

The OSM Development Board provides a JTAG / SWD debug interface for system development, debugging, and programming of the SoM.

The interface supports both **JTAG (IEEE 1149.1)** and **SWD (Serial Wire Debug)** protocols, enabling flexible use with a wide range of external debug tools. It is routed to a standard **Cortex debug connector**, allowing direct connection to industry-standard debuggers, and also provides optional access through an auxiliary header for external adapters (e.g., FTDI-based solutions).

This interface enables:

- Low-level hardware and software debugging
- Firmware programming and device bring-up
- Boundary scan testing
- Real-time system analysis and tracing

Table 25 shows the detailed signal mapping between the SoM and the debug connectors.

Table 25: JTAG interface

X14 pin	Signal name	SoM Signal Name	SoM Pin	Description / Remarks
1	VREF	–	–	Target reference voltage (+1.8V_SW)
2	JTAG_TMS	JTAG_TMS	C54	Test Mode Select / SWD data
3	GND	–	–	Ground
4	JTAG_TCK	JTAG_TCK	C46	Test Clock / SWD clock

Continued on next page

Table 25: JTAG interface (Continued)

X14 pin	Signal name	SoM Signal Name	SoM Pin	Description / Remarks
5	GND	–	–	Ground
6	JTAG_TDO	JTAG_TDO	B38	Test Data Out / trace output
7	Key	–	–	Not connected
8	JTAG_TDI	JTAG_TDI	C49	Test Data In
9	GND_DET	–	–	Ground detect
10	JTAG_TRST#	JTAG_nRESET	C51	System reset

2.12.1 FTDI JTAG Interface

In addition to the standard Cortex debug connector, the OSM Development Board provides an auxiliary **FTDI-based JTAG interface** accessible through connector X46. This interface is implemented using an **FTDI FT4232HL USB-to-multiprotocol bridge**, which enables JTAG, UART, and other debug functions over a single USB connection.

The FTDI device acts as a **USB PHY and protocol bridge**, converting USB signals from the debug USB connector into JTAG signals (TCK, TDI, TDO, TMS, TRST#) as well as UART signals. The USB interface is connected to a **USB Type-C debug connector**, allowing direct connection to a host PC for development and debugging.

Signal level compatibility between the FTDI device and the SoM is ensured through **level shifters**, which translate between the FTDI I/O voltage domain (typically **3.3 V**) and the SoM domain (typically **1.8 V**). This guarantees safe operation and proper logic-level matching across all debug interfaces.

The FTDI circuitry includes:

- Dedicated **3.3 V and 1.8 V LDO regulators** for the debug domain
- **ESD protection** on USB and external interface lines
- **EEPROM (I^2C)** for FTDI configuration and USB descriptor storage
- Optional routing of FTDI channels to JTAG and UART interfaces

The X46 header exposes the JTAG signals after level shifting, using a **2×5, 2.54 mm pin header**, ensuring compatibility with external adapters if required.

Table 26 shows the detailed signal mapping of the FTDI JTAG header.

Table 26: FTDI JTAG interface

X46 pin	Signal Name	I/O	Voltage	Description / Remarks
1	FTDI_JTAG_TCK	O	1.8V via level shifter	JTAG test clock generated by FTDI
2	JTAG_TCK	I	1.8V	JTAG test clock to SoM
3	FTDI_JTAG_TDI	O	1.8V via level shifter	JTAG test data input (to SoM)
4	JTAG_TDI	I	1.8V	JTAG data input to SoM
5	FTDI_JTAG_TDO	I	1.8V via level shifter	JTAG test data output from SoM
6	JTAG_TDO	O	1.8V	JTAG data output from SoM

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Table 26: FTDI JTAG interface (Continued)

X46 pin	Signal Name	I/O	Voltage	Description / Remarks
7	FTDI_JTAG_TMS	O	1.8V via level shifter	JTAG test mode select
8	JTAG_TMS	I	1.8V	JTAG mode select to SoM
9	FTDI_JTAG_TRST#	O	1.8V via level shifter	JTAG test reset (active low)
10	JTAG_TRST#	I	1.8V	JTAG reset to SoM

Direction: relative to the SoM.

Notes

- Signals on the left side (`FTDI_*`) originate from the **FT4232HL FTDI bridge**
- Signals on the right side (`JTAG_*`) connect to the SoM **JTAG interface**
- All signals pass through **level shifters** (3.3V to/from 1.8V)
- The FTDI operates from the **debug USB interface** and provides JTAG over USB

2.13 LVDS – Low-Voltage Differential Signaling

The OSM Development Board provides an **Low-Voltage Differential Signaling (LVDS) display interface** through connector XA1, enabling direct connection of LVDS-compatible display panels.

This interface supports high-speed differential signaling for transmission of pixel data from the System-on-Module (SoM) to external displays.

Key features include:

- Up to 4 LVDS data lanes + 1 clock lane
- Differential signaling with 100 Ω controlled impedance
- Support for standard LVDS display panels
- On-board ESD and EMI protection

2.13.1 LVDS High-Speed Interface

The LVDS interface uses differential signaling for robust, low-noise transmission of display data. Table 27 shows the pinout of the LVDS signals from the board-to-board connector.

Table 27: LVDS interface

XA1 pin	Signal name	Direction	Description
A2	LVDS_A_CLK_P	Output	Differential clock positive
A3	LVDS_A_CLK_N	Output	Differential clock negative
B14	LVDS_A_LANE0_P	Output	Data lane 0 positive
B13	LVDS_A_LANE0_N	Output	Data lane 0 negative
B9	LVDS_A_LANE1_P	Output	Data lane 1 positive
B8	LVDS_A_LANE1_N	Output	Data lane 1 negative
B6	LVDS_A_LANE2_P	Output	Data lane 2 positive
B5	LVDS_A_LANE2_N	Output	Data lane 2 negative

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Table 27: LVDS interface (Continued)

XA1 pin	Signal name	Direction	Description
B3	LVDS_A_LANE3_P	Output	Data lane 3 positive
B2	LVDS_A_LANE3_N	Output	Data lane 3 negative

2.13.2 Electrical Characteristics

LVDS interface characteristics

- Differential impedance: **100 Ω (LVDS pairs)**
- Signaling standard: **LVDS**
- Low voltage swing for reduced EMI
- High data throughput suitable for display applications

2.13.3 ESD and EMI Protection

The LVDS interface incorporates protection mechanisms to ensure both signal integrity and overall system robustness. ESD protection is implemented using low-capacitance diodes on the LVDS differential pairs. These devices are selected to preserve high-speed signal performance while providing effective protection against electrostatic discharge events. For optimal effectiveness, the protection components are placed as close as possible to connector XA1.

2.14 PCI Express

The OSM Development Board exposes high-speed expansion interfaces through two M.2 sockets: XA3 (Key B) and XA4 (Key E). These connectors provide standardized interfaces for integrating wireless, cellular, and storage peripherals, while mapping directly to the available interfaces on the OSM SoM.

The XA3 (Key B) socket supports a **PCIe Gen2 x1 interface**, a **USB 3.0 / USB 2.0 interface**, and a **UIM (SIM card) interface**, enabling full LTE/5G modem functionality. Additional signals such as SMBus, control lines (`PERST#`, `CLKREQ#`, `W_DISABLE#`), and status LEDs are also provided to ensure compatibility with standard M.2 Key B modules.

The XA4 (Key E) socket is optimized for wireless connectivity modules such as Wi-Fi and Bluetooth devices. The Key E interface uses an **SDIO interface as the primary host bus**, complemented by **USB 2.0**, **UART**, **I²S**, and **I²C** signals. This allows integration of combo wireless modules requiring multiple auxiliary interfaces for control, audio, and coexistence signaling.

Both connectors provide additional system integration features, including:

- Control signals for module enable, reset, and wake-up
- Status indication outputs (e.g., WLAN, WWAN, WPAN LEDs)
- Auxiliary interfaces such as SMBus/I²C for device management
- RF coexistence (COEX) and antenna control signals (Key E)
- SIM/UIM interface for cellular modules (Key B)

2.14.1 Mini PCIe Key B Connector (XA3)

Connector Type: Mini PCIe Card Connector TE 2199230-5

Table 28: Mini PCIe key B connector (XA3)

Pin	Signal name	I/O	Voltage	Pull-up / Pull-down	Description / Remarks
1	CONFIG_3	I	–	–	Configuration strap test point (TP43)
2	+V3.3_M2B	PWR	+3.3V	–	Main 3.3V supply (filtered via FB5)
3	GND	PWR	0V	–	Ground
4	+V3.3_M2B	PWR	+3.3V	–	Main 3.3V supply
5	GND	PWR	0V	–	Ground
6	M.2B_FULL_CARD_POWER_OFF#	I	+3.3V	–	Card power off
7	USBH3_D_P	I/O	–	–	USB 3 D+ AC couple
8	M.2B_W_DISABLE1#	I	3.3V	47kΩ pull-up	Wireless disable
9	USBH3_D_N	I/O	–	–	USB 3 D- AC couple
10	M.2B_LED#	O	3.3V	–	LED control 1kΩ series
11	GND	PWR	0V	–	Ground
20	GPIO_5	I/O	1.8V	–	General purpose
21	CONFIG_0	I	–	–	Configuration strap test point (TP23)
22	GPIO_6	I/O	1.8V	–	General purpose
23	GPIO_11	I/O	1.8V	–	General purpose
24	GPIO_7	I/O	1.8V	–	General purpose
25	DPR	–	–	–	Not connected
26	GPIO_10	I/O	1.8V	–	General purpose
27	GND	PWR	0V	–	Ground
28	GPIO_8	I/O	1.8V	–	General purpose
29	USBH3_SSRX_N	I/O	–	–	USB 3 RX- AC couple
30	UIM_RESET	O	–	–	SIM reset
31	USBH3_SSRX_P	I/O	–	–	USB 3 RX+ AC couple
32	UIM_CLK	O	–	–	SIM clock
33	GND	PWR	0V	–	Ground
34	UIM_DATA	I/O	–	–	SIM data
35	USBH3_SSTX_N	I/O	–	–	USB 3 TX- AC couple
36	UIM_PWR	PWR	–	–	SIM power
37	USBH3_SSTX_P	I/O	–	–	USB 3 TX+ AC couple
38	DEVSLP	–	–	–	Not connected
39	GND	PWR	0V	–	Ground
40	SMB_CLK/GPIO_0	I	1.8V	–	SMBus clock
41	PCIE_A_HS0_N	I/O	–	–	PCIe RX-
42	SMB_DATA/GPIO_1	I/O	1.8V	–	SMBus data

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Table 28: Mini PCIe key B connector (XA3) (Continued)

Pin	Signal name	I/O	Voltage	Pull-up / Pull-down	Description / Remarks
43	PCIE_A_HS0_P	I/O	–	–	PCIe RX+
44	ALERT#/GPIO_2	I/O	1.8V	–	Alert / GPIO
45	GND	PWR	0V	–	Ground
46	GPIO_3	I/O	1.8V	–	General purpose
47	PCIE_A_HS00_N	I/O	–	–	PCIe TX- AC couple
48	GPIO_4	I/O	1.8V	–	General purpose
49	PCIE_A_HS00_P	I/O	–	–	PCIe TX+ AC couple
50	PERST#	I	3.3V	–	PCIe reset
51	GND	PWR	0V	–	Ground
52	CLKREQ#	I/O	3.3V	–	PCIe clock request pull-up network
54	PEWAKE#	I/O	3.3V	–	Wake signal pull-up network
55	REFCLK+	I	–	–	PCIe refclk+
55	REFCLK-	I	–	–	PCIe refclk-
56	NC	–	–	–	Not connected
57	GND	PWR	0V	–	Ground
58	NC	–	–	–	Not connected
59	ANTCTL0	O	1.8V	–	Antenna control
60	COEX3	–	–	–	Not connected
61	ANTCTL1	O	1.8V	–	Antenna control
62	COEX2	–	–	–	Not connected
63	ANTCTL2	O	1.8V	–	Antenna control
64	COEX1	–	–	–	Not connected
65	ANTCTL3	O	1.8V	–	Antenna control
66	UIM_CD	I	–	–	SIM detect
67	M.2B_RESET#	I	3.3V	–	Module reset
68	SUSCLK	–	–	–	Not connected
69	CONFIG_1	I	–	–	Configuration strap test point (TP24)
70	+V3.3_M2B	PWR	+3.3V	–	Power
71	GND	PWR	0V	–	Ground
72	+V3.3_M2B	PWR	+3.3V	–	Power
73	GND	PWR	0V	–	Ground
74	+V3.3_M2B	PWR	+3.3V	–	Power
75	CONFIG_2	I	–	–	Configuration strap test point (TP25)

2.14.2 Mini PCIe Key E Connector (XA4)

Connector Type: Mini PCIe Card Connector TE 2199230-4

Table 29: Mini PCIe key E connector (XA4)

Pin	Signal name	I/O	Voltage	Pull-up / Pull-down	Description / Remarks
1	GND	PWR	0V	–	Ground
2	+V3.3_M2E	PWR	+3.3V	–	Main supply
3	USBH4_D_P	I/O	–	–	USB 2.0 D+
4	+V3.3_M2E	PWR	+3.3V	–	Power
5	USBH4_D_N	I/O	–	–	USB 2.0 D-
6	LED_1#	O	3.3V	–	LED output 1kΩ series
7	GND	PWR	0V	–	Ground
8	M.2E_I2S_BCLK	O	1.8V	–	I^2S bit clock
9	SDIO_CLK	O	1.8V	–	SDIO clock
10	M.2E_I2S_LRCLK	O	1.8V	–	I^2S LR clock
11	SDIO_CMD	I/O	1.8V	–	SDIO command
12	M.2E_I2S_DATA_IN	I	1.8V	–	I^2S data input
13	SDIO_DATA0	I/O	1.8V	–	SDIO data
14	M.2E_I2S_DATA_OUT	O	1.8V	–	I^2S data output
15	SDIO_DATA1	I/O	1.8V	–	SDIO data
16	LED_2#	O	3.3V	–	LED output 1kΩ series
17	SDIO_DATA2	I/O	1.8V	–	SDIO data
18	GND	PWR	0V	–	Ground
19	SDIO_DATA3	I/O	1.8V	–	SDIO data
20	UART_WAKE#	I/O	1.8V	–	UART wake
21	SDIO_WAKE#	I/O	1.8V	–	SDIO wake
22	UART_RXD	I	1.8V	–	UART RX
23	SDIO_RESET#	O	1.8V	–	SDIO reset
32	UART_TXD	O	1.8V	–	UART TX
33	GND	PWR	0V	–	Ground
34	UART_CTS	I	1.8V	–	UART CTS
36	UART_RTS	O	1.8V	–	UART RTS
39	GND	PWR	0V	–	Ground
44	COEX3	–	–	–	Not connected
45	GND	PWR	0V	–	Ground
46	M.2E_COEX_RXD	I	1.8V	–	RF coexistence
48	M.2E_COEX_TXD	O	1.8V	–	RF coexistence
51	GND	PWR	0V	–	Ground
54	M.2E_W_DISABLE2#	I	3.3V	–	Wireless disable
56	M.2E_W_DISABLE1#	I	3.3V	–	Wireless disable
57	GND	PWR	0V	–	Ground
58	M.2E_I2C_DATA	I/O	1.8V	2.2k pull-up	I^2C data
60	M.2E_I2C_CLK	I/O	1.8V	2.2k pull-up	I^2C clock

Continued on next page

Table 29: Mini PCIe key E connector (XA4) (Continued)

Pin	Signal name	I/O	Voltage	Pull-up / Pull-down	Description / Remarks
62	M.2E_ALERT#	I/O	1.8V	–	Alert
64	GND	PWR	0V	–	Ground
69	GND	PWR	0V	–	Ground
71	GND	PWR	0V	–	Ground
72	+V3.3_M2E	PWR	+3.3V	–	Power
73	GND	PWR	0V	–	Ground
74	+V3.3_M2E	PWR	+3.3V	–	Power
75	GND	PWR	0V	–	Ground

2.14.3 SIM Card Holder (X11)

The nano SIM holder (X11) is routed to the UIM interface of the XA3 M.2 Key B socket, providing SIM connectivity.

Connector Type: NANO SIM, GCT SIM8066-6-1-14-01-A

Table 30: SIM card holder (X11)

Pin	Signal name	I/O Type	Voltage	Description/Remarks
1	VCC	PWR	1.8V / 3.0V	SIM card supply voltage (UIM_PWR from M.2 Key B)
2	RESET	O	1.8V	SIM reset signal (UIM_RESET)
3	CLOCK	O	1.8V	SIM clock signal (UIM_CLK)
4	I/O	I/O	1.8V	Bidirectional SIM data line (UIM_DATA)
5	GND	PWR	0V	Ground reference
6	CD	I	–	Card detect signal (UIM_CD)
7	VPP	–	–	Not connected (legacy SIM programming voltage, unused)
G1-G4	Shield	PWR	0V	Connector shielding, tied to ground for EMI protection

Notes

- All SIM interface signals originate from the UIM interface of the M.2 Key B connector (XA3)
- Signal lines are protected by ESD diode array
- Supply decoupling is provided by 100 nF near the connector
- The interface operates in the 1.8 V domain, with VCC switched from the module
- CD (Card Detect) allows software to detect SIM insertion/removal

2.15 PWM – Pulse Width Modulation Interface

The board provides **six PWM-capable SoM signals**, grouped as `PWM[0..5]`. These signals are routed through a configurable jumper array `PWM_JMP[0..5]`, enabling flexible signal routing. This architecture follows the development board approach: it allows direct access to the raw PWM outputs from the SoM for external use, while also enabling selective connection to on-board subsystems, such as display backlight control.

The PWM interface is associated with +V1.8_SW, so the raw PWM outputs operate in the **1.8 V domain**. One important board-level example is LVDS_BL_PWM: on the LVDS sheet, this PWM signal is translated to LVDS_BKL_PWM_3.3V for the panel connector, demonstrating how the board adapts a 1.8 V SoM PWM signal to a 3.3 V display-facing control signal.

Table 31: PWM signal mapping

OSM pin	Signal name	Jumper	Description / Remarks
B61	DISP_BL_PWM	X222	General-purpose PWM output channel 0 used for DSI display backlight PWM control
B59	LVDS_BL_PWM	X222	General-purpose PWM output channel 1 used for LVDS display backlight PWM control
B58	PWM_2	X222	General-purpose PWM output channel 2
B62	PWM_3	X221	General-purpose PWM output channel 3
B63	PWM_4	X221	General-purpose PWM output channel 4
B65	PWM_5	X222	General-purpose PWM output channel 5

Jumper: The PWM signals are routed through jumpers on the table and are only available at their respective destination when the corresponding jumper pins are closed.

2.16 SD Card Interface

The OSM Development Board provides an **SD Card interface** routed from the SoM to a standard SD card connector, enabling removable storage for applications such as data logging, firmware updates, and multimedia storage.

The interface is based on the **SDIO_A controller** and supports **SD/SDHC/SDXC cards** using a **4-bit data bus**, ensuring compatibility with standard SD card specifications. In addition to the core data, command, and clock signals, the design includes **card detect** and **write-protect** functionality for proper card management.

The SD card supply is controlled via an **on-board power switch**, allowing software-controlled power sequencing and improved reliability. All external signal lines are protected using **ESD protection devices**, ensuring robustness against electrostatic discharge events.

The SD card interface is routed to connector X19, which provides:

- 4-bit SD data interface (DAT0–DAT3)
- Command (CMD) and clock (CLK) signals
- Card detect (CD) and write-protect (WP) signals
- Controlled power supply

Table 32 shows the detailed signal mapping between the SoM and the SD card connector.

Table 32: SD Card interface

B2B pin	SoM signal name	SD card pin	SD signal name	Description / Remarks
Command and Control Signals				
C78	SDIO_A_CMD	2	CMD	Command line 10kΩ pull-up
D82	SDIO_A_CLK	5	CLK	SD clock signal

Continued on next page

Table 32: SD Card interface (Continued)

B2B pin	SoM signal name	SD card pin	SD signal name	Description / Remarks
D71	SDIO_A_CD#	10	CD	Card detect (active low) 22Ω series resistor
C76	SDIO_A_WP	11	WP	Write protect status 22Ω series resistor and 100kΩ pull-down
Data Signals				
C79	SDIO_A_D0	7	DAT0	Data line 0 10kΩ pull-up
D83	SDIO_A_D1	8	DAT1	Data line 1 10kΩ pull-up
C68	SDIO_A_D2	1	DAT2	Data line 2 10kΩ pull-up
C82	SDIO_A_D3	9	DAT3	Data line 3 10kΩ pull-up

2.16.1 eMMC vs SD Card (SDIO) Comparison

The OSM platform supports both on-module eMMC storage and external SD card storage via SDIO_A. The following comparison highlights their typical roles and characteristics.

Table 33: eMMC SD Card comparison

Feature	eMMC (on SoM)	SD Card (SDIO_A)
Location	On-module	External (removable)
Interface	Dedicated eMMC controller	SDIO interface
Bus Width	8-bit	1-bit / 4-bit
Performance	High (HS200/HS400 possible)	Moderate (UHS depending on card)
Reliability	High (soldered device)	Lower (removable media)
Boot Capability	Primary boot device	Secondary / alternative boot
Hot-Plug	No	Yes (with software support)
Use Case	OS, root filesystem	Data logging, updates, removable storage

2.17 SPI – Serial Peripheral Interface

The OSM Development Board provides **Serial Peripheral Interface (SPI)** connectivity through signals routed from the SoM and exposed on the carrier.

- Direct breakout of SoM SPI signals
- Flexible chip-select routing using GPIO-capable pins
- Shared usage with other peripheral functions where applicable

The SPI interface is intended for:

- External peripheral expansion (ADC, DAC, sensors, displays)
- On-board device control (via chip-select GPIO reuse)
- Development and prototyping

All SPI signals are routed in the **low-voltage I/O domain (1.8 V)** and may require level shifting for com-

patibility with external devices.

2.17.1 SPI Bus Signals

The SPI interface consists of the standard signals:

- Clock (SCLK)
- Master Out Slave In (MOSI)
- Master In Slave Out (MISO)
- Chip Select (CS#)

These signals are routed from the SoM through dedicated pins and may be shared with GPIO functionality.

2.17.2 SPI Signal Mapping

OSM Development Board exposes two SPI interfaces, `SPI_A` and `SPI_B`, which are accessible through two dual-row pin headers

- `X243` and `X241` for `SPI_A`
- `X233` for `SPI_B`
- `X232` for the chip select of both `SPI_A` and `SPI_B`

Each interface is routed to a dedicated **TSW-110-07-G-D** (Samtec) header, allowing connection to external SPI peripherals for development and prototyping. These headers expose all relevant SPI signals, including clock, data, and chip-select lines, and in the case of SPI_A, also provide the additional I/O lines required for Quad-SPI operation. This layout enables flexible use of both SPI buses without requiring direct access to the high-density board-to-board connectors.

Table 34 shows the SPI signal mapping.

Table 34: SPI interfaces

XA2 pin	Dev Board signal name	OSM signal name	OSM pad	Direction	Description / Remarks
SPI_A Interface					
C4	SPI_A_SDO (IO0)	SPI_A_SDO	V15	Output	SPI_A Master Out (MOSI / IO0 in Quad SPI mode)
C3	SPI_A_SDI (IO1)	SPI_A_SDI	U15	Input	SPI_A Master In (MISO / IO1 in Quad SPI mode)
C6	SPI_A_SCK	SPI_A_SCK	U16	Output	SPI_A serial clock
C13	SPI_A_WP (IO2)	SPI_A_WP	W16	Output	SPI_A write-protect
C5	SPI_A_HOLD (IO3)	SPI_A_HOLD	W15	Output	SPI_A hold#
SPI_B Interface					
A93	SPI_B_SDO	SPI_B_SDO	Y23	Output	SPI_B Master Out (MOSI)
A92	SPI_B_SDI	SPI_B_SDI	Y22	Input	SPI_B Master In (MISO)
A90	SPI_B_SCK	SPI_B_SCK	Y21	Output	SPI_B serial clock

Continued on next page

Table 34: SPI interfaces (Continued)

XA2 pin	Dev Board signal name	OSM signal name	OSM pad	Direction	Description / Remarks
Chip Select					
C12	SPI_A_CS0#	SPI_A_CS0#	Y15	Input	Chip-select for SPI_A device
C37	SPI_A_CS1# / GPIO_A_6	GPIO_A_6	K17	Input	Chip-select for SPI_A device or general-purpose GPIO configured as GPIO
A89	SPI_B_CS0#	SPI_B_CS0#	AA23	Input	Chip-select for SPI_B device
B40	SPI_B_CS1# / GPIO_A_7	GPIO_A_7	L17	Input	Chip-select for SPI_B device or general-purpose GPIO configured as GPIO

2.18 UART – Universal Asynchronous Receiver-Transmitter

The system provides multiple **Universal Asynchronous Receiver-Transmitter (UART)** interfaces for asynchronous serial communication. These interfaces support standard logic-level UART signaling from the SoM and, where required, can be interfaced to RS-232 levels using the external transceiver **TRS3122ERGER**.

The TRS3122E is a dual-driver/dual-receiver RS-232 transceiver that:

- Converts **logic-level UART signals (TTL/CMOS)** to **RS-232 voltage levels**
- Includes an **internal charge pump** to generate RS-232 voltages from a single supply
- Supports data rates up to **~1 Mbps**
- Provides ±**15 kV ESD protection** (Human Body Model - HBM) on RS-232 pins

The following UART interfaces are available on connector **XA1**:

- UART_A – Full interface control (RX, TX, RTS, CTS)
- UART_B – Full interface control (RX, TX, RTS, CTS)
- UART_C – Basic UART (RX, TX)
- UART_D – Basic UART (RX, TX)
- UART_CON – Console/debug UART (RX, TX)

Logic Levels
All UART signals operate at 1.8V logic levels (SoM I/O domain) and must be level-shifted when interfacing with RS-232 equipment.

2.18.1 UART Signal Mapping

Table 35 summarizes all UART signals available on connector **XA1**, including their pin assignment, interface grouping, and functional description.

Table 35: UART interfaces

XA1 Pin	Signal Name	I/O	Description/Remarks
UART_A Interface			
A43	UART_A_RX	O	Receive data input to the SoM from external device
A39	UART_A_TX	I	Transmit data output from the SoM to external device
A37	UART_A_RTS	I	Hardware flow control output for transmit request (Request to Send - RTS)
A40	UART_A_CTS	O	Hardware flow control input for transmit permission (Clear to Send - CTS)

Continued on next page

Table 35: UART interfaces (Continued)

XA1 Pin	Signal Name	I/O	Description/Remarks
UART_B Interface			
A36	UART_B_RX	O	Receive data input to the SoM from external device
B34	UART_B_TX	I	Transmit data output from the SoM to external device
C45	UART_B_RTS	I	Hardware flow control output for transmit request (RTS)
A49	UART_B_CTS	O	Hardware flow control input for transmit permission (CTS)
UART_C Interface			
A68	UART_C_RX	O	Receive data input to the SoM from external device
A71	UART_C_TX	I	Transmit data output from the SoM to external device
UART_D Interface			
A69	UART_D_RX	O	Receive data input to the SoM from external device
A72	UART_D_TX	I	Transmit data output from the SoM to external device
UART Console Interface (UART_CON)			
A74	UART_CON_RX	O	Receive data input to the SoM from external device (console)
A75	UART_CON_TX	I	Transmit data output from the SoM to external device (console)

2.19 USB – Universal Serial Bus

The OSM Development Board provides a flexible USB subsystem designed to support a wide range of use cases, from basic USB 2.0 connectivity to high-speed USB 3.x applications and USB Type-C integration. The design is organized into three primary USB interface groups, each serving a distinct role within the system architecture.

The first interface group, USB_A, is a direct USB 2.0 connection from the SoM. This interface provides straightforward access to standard USB functionality and is typically used for simple host or device connections without additional routing or switching logic.

The second group, USB_B, is also a USB 2.0 interface originating from the SoM, but routed through an on-board USB multiplexer. This allows the signal path to be dynamically switched between different destinations, enabling more complex configurations such as shared access between connectors or integration with other subsystems like USB hubs or Type-C routing paths.

The third group, USB_C, implements a full USB Type-C interface. In addition to USB 2.0 signaling, this interface includes SuperSpeed differential pairs, Configuration Channel (CC) pins for cable orientation and role detection, VBUS power control, and dedicated Type-C controller logic. This enables support for modern USB-C features such as dual-role operation and high-speed data transfer.

Beyond these primary interfaces, the board integrates several supporting USB-related features:

- A dedicated **USB Type-C Power Delivery (PD) input interface** on connector X3, allowing the board to be powered via USB-C with negotiated voltage and current levels
- A **dual-role USB Type-C connector** on X37, supporting both host and device operation depending on system configuration and connected peripherals
- A **USB switch / mux stage** that routes USB_B and hub traffic toward the Type-C interface, enabling flexible signal sharing and system-level USB topology control
- A separate **debug USB Type-C connector** on X40, intended for development, debugging, or auxiliary USB connectivity

All USB-related control and data signals originate from the OSM module and are routed through the SoM connectors (XA1 and XA2) to the carrier board. From there, they interface with power switches, Type-C controllers, and multiplexing logic, forming a complete USB subsystem that supports both standard and advanced USB use cases.

From an electrical perspective, the USB interfaces are designed to meet USB 2.0 and USB 3.x specifications. High-speed differential pairs are routed with controlled impedance and minimal skew to ensure signal integrity across the board, including through multiplexing stages:

- **USB 2.0 signals** are routed with **90 Ω differential impedance**
- **USB 3.x SuperSpeed signals** are routed with **90 Ω differential impedance**
- Differential signaling integrity is preserved across switching and muxing elements

2.19.1 USB A

The USB_A interface provides a direct USB 2.0 connection from the OSM module to the connector X38 (USB type C connector), supporting standard host or device functionality depending on system configuration. It includes the differential data pair, power control, and status signals required for reliable USB operation, as well as optional identification and protection mechanisms. This interface is typically used for straightforward USB connectivity, offering access to the raw USB signals along with board-level power switching and overcurrent monitoring.

The signal mapping and detailed description of the USB_A interface are provided in Table 36.

Table 36: USB A interface (connector X38)

Signal name	XA2 pin	Description / Remarks
Control Signals		
USB_A_OC#	A27	Input signal indicating an overcurrent condition on the USB power line to use this signal, X241 must be closed
USB_A_ID	D22	Identification signal used to determine host/device role (typically for OTG applications) to use this signal, X242 must be closed
USB_A_VBUS	D23	USB power supply line provides 5 V to connected devices
USB_A_EN	D24	Control signal used to enable or disable the USB power switch for the VBUS line to use this signal, X242 must be closed
Data Signals		
USB_A_D_N	A5	USB 2.0 differential data line (negative), used for bidirectional data transmission
USB_A_D_P	A6	USB 2.0 differential data line (positive), paired with D- for signaling

2.19.2 USB_B

The USB_B interface provides a USB 2.0 connection from the OSM module to the switches IC27 to IC30. This architecture enables flexible signal routing, allowing the interface to be dynamically shared between different paths such as the Type-C connector and internal USB hub or switching logic.

Similar to USB_A, the interface includes the differential data pair, power control, and status signals required for the USB operation. In addition, the presence of the mux stage allows the system to adapt the USB topology based on configuration or operational mode, making it suitable for more advanced use cases involving multiple USB endpoints.

The signal mapping and detailed description of the USB_B interface are provided in Table 37.

Table 37: USB B interface

Signal name	OSM pin	Description / Remarks
Control Signals		
USB_A_EN	A78	Control signal used to enable or disable the USB power switch for the VBUS line to use this signal, X242 must be closed
USB_A_OC#	A79	Input signal indicating an overcurrent condition on the USB power line to use this signal, X241 must be closed
USB_A_VBUS	A80	USB power supply line provides 5 V to connected devices
USB_A_ID	A81	Identification signal used to determine host/device role (typically for OTG applications) to use this signal, X242 must be closed
Data Signals		
USB_A_D_P	B77	USB 2.0 differential data line (positive), paired with D- for signaling
USB_A_D_N	B78	USB 2.0 differential data line (negative), used for bidirectional data transmission

2.19.3 USB_C

The USB_C interface provides a full USB 2.0 and USB 3.x connection from the OSM module to the USB Type-C subsystem. This interface includes both the USB 2.0 differential pair (D+, D-) and the SuperSpeed differential pairs (SSTX, SSRX), enabling high-speed data communication through the Type-C connector.

In addition to the data paths, the interface integrates several control and configuration signals required for Type-C operation. These include VBUS control (USB_C_VBUS), power enable (USB_C_EN), configuration channel signaling (USB_C_CC#), and cable orientation / role detection (USB_C_ID). The SuperSpeed lanes are AC-coupled on the carrier board, ensuring compliance with USB 3.x electrical requirements and proper signal integrity toward the external connector.

The presence of these signals allows the board to support advanced USB Type-C features such as dual-role operation, cable orientation handling, and controlled power delivery through the VBUS path. The interface is designed to integrate seamlessly with the on-board switching and Type-C control logic, enabling flexible system-level USB configurations.

The signal mapping and detailed description of the USB_C interface are provided in Table 38.

Table 38: USB C interface

Signal Name	OSM Pin	Description / Remarks
Control Signals		
USB_C_EN	B28	Enables USB-C VBUS
USB_C_ID	B36	Role detection
USB_C_OC#	C33	Overcurrent indication
USB_C_VBUS	C34	VBUS sensing
Data Signals		
USB_C_D_P	A33	USB 2.0 differential data (positive)
USB_C_D_N	A34	USB 2.0 differential data (negative)
USB_C_SSRX_P	A30	SuperSpeed RX positive
USB_C_SSRX_N	A31	SuperSpeed RX negative
USB_C_SSTX_P	B25	SuperSpeed TX positive

Continued on next page

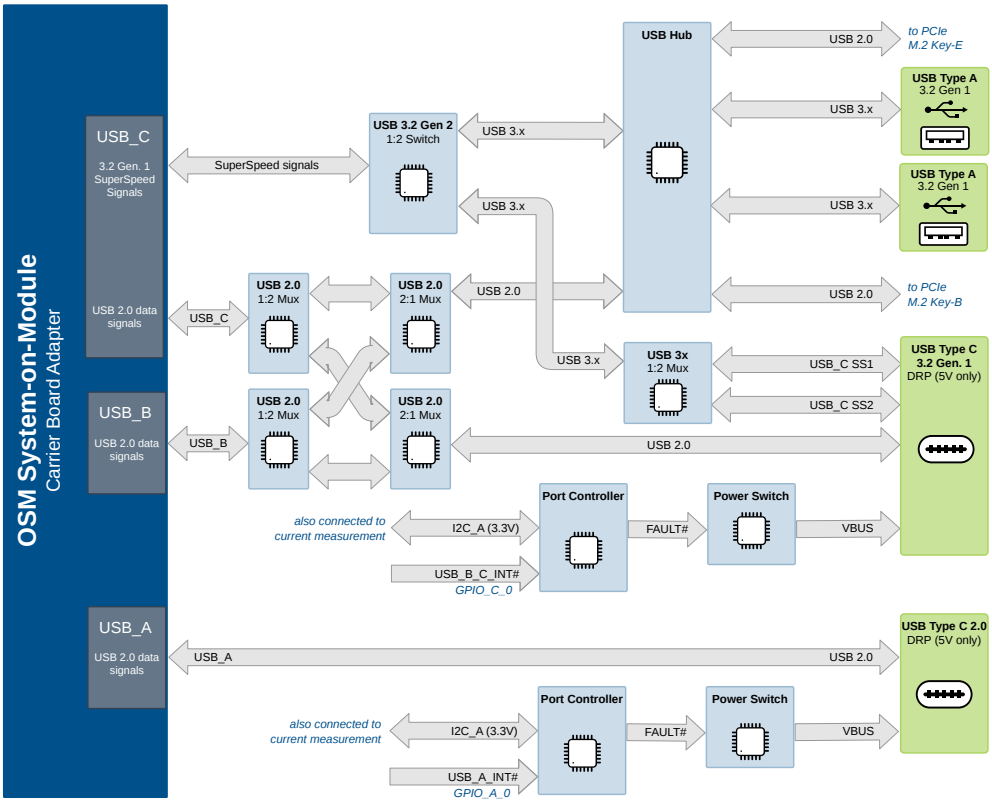
Table 38: USB C interface (Continued)

Signal Name	OSM Pin	Description / Remarks
USB_C_SSTX_N	B26	SuperSpeed TX negative

2.19.4 USB Switching and Muxing Architecture

The USB signal routing is illustrated in the system block diagram Figure 5, which shows how the USB_A, USB_B, and USB_C interfaces from the SoM are interconnected through a combination of **USB 2.0 muxes, USB 3.x switches, and a central USB hub**.

Figure 5: USB block diagram



At a high level, the architecture allows the USB interfaces to be dynamically routed between: - the **USB Type-C connectors** - the **on-board USB hub** - and external interfaces such as **PCIe M.2 sockets**

For the **USB 2.0 paths**, multiple mux stages (1:2 and 2:1) are used to selectively route the USB_B and USB_C data lines. As shown in the diagram, these muxes enable:

- routing USB 2.0 signals either **directly to the Type-C interface** or
- **toward the USB hub** for multi-port expansion

For the **USB 3.x SuperSpeed paths**, a dedicated high-speed switch connects the SoM SuperSpeed lanes (USB_C SS1/SS2) either to:

- the **USB Type-C connector**, or
- the **USB hub SuperSpeed input**

This switching stage preserves signal integrity while enabling flexible high-speed routing, as indicated by the “USB 3.x 1:2 switch” block in the diagram.

Control of the routing is performed through:

- **Type-C port controllers** (handling CC logic, orientation, and role)
- **GPIO-based control signals** (e.g., `USB_B_C_INT#`, `USB_A_INT#`)
- **I²C control interface** for configuration and monitoring

In addition, each USB path integrates **power switches and VBUS control**, allowing proper power delivery and fault handling, as shown by the “Power Switch” and “Port Controller” blocks.

Overall, the switching and muxing architecture enables:

- dynamic selection between **direct Type-C connectivity and hub-based expansion**
- sharing of USB resources across multiple connectors
- support for both **USB 2.0 and USB 3.x topologies**
- proper electrical isolation and signal integrity across all routing paths

2.19.5 USB Hub

The block diagram shows a central **USB hub (USB 3.2 Gen 1)** that expands a single upstream USB connection into multiple downstream interfaces. The hub receives its upstream connection through the muxing stage, allowing either `USB_B` or `USB_C` to feed the hub depending on system configuration.

From the hub, multiple downstream ports are distributed:

- to external USB connectors
- to internal interfaces **PCIe M.2 Key-B and Key-E**
- and to additional USB endpoints on the board

Both **USB 2.0 and USB 3.x signals** are distributed by the hub, with SuperSpeed lanes routed separately from USB 2.0 data paths, as indicated in the diagram.

The hub is integrated with: - **power switching and VBUS control** for each port - **fault reporting (FAULT#)** - **current monitoring connections** - **I²C control interface** for configuration

3 Test Points

Table 39: Test points

TP pin	Signal name	Description / Remarks
Primary power rails and distribution monitoring		
TP1	+V_SUPPLY_FILT	Protected input supply rail after LTC4368
TP2	GND	Ground reference
TP3	GND	Ground reference
TP4	GND	Ground reference
TP5	GND	Ground reference
TP6	GND	Ground reference
TP7	GND	Ground reference
TP8	GND	Ground reference
TP9	GND	Ground reference
TP10	GND	Ground reference
TP11	GND	Ground reference
TP12	GND	Ground reference
TP13	+VBUS_PD	USB-C power delivery voltage
TP14	VBUS_FET_EN	USB PD successfull negotiation signal
TP15	+5_VCC_IN	Before current sensing shunt resistor
TP16	+5_VCC_IN	After current sensing shunt resistor
TP17	+5_VCC_IN	5V module supply rail
TP18	+V12_BL	12V backlight rail
TP19	+V1.0_ETH	1.0V ethernet rail
TP20	+V2.5_SW	2.5V system rail
TP21	+V5_SW	2.5V system rail
TP22	+V_SUPPLY_FILT_SW	Switched main supply rail
M.2 Key B		
TP23	CONFIG_0	M.2 configuration pins
TP24	CONFIG_1	M.2 configuration pins
TP25	CONFIG_2	M.2 configuration pins
TP43	CONFIG_3	M.2 configuration pins
Access to key subsystem signals (SDIO, Ethernet, PCIe, Debug)		
TP26	SDIO_A_IOPWR	SDIO A I/O power rail monitoring
TP27	CLK_OUT	Clock output from Ethernet A PHY
TP28	CLK_OUT	Clock output from Ethernet B PHY
USB_A		
TP29	ILIM_5V_VBUS	USB current limit selector
TP30	EN_SNK1	VBUS sink power path control output
TP31	FRS_EN	FRS control of SRC load switch
TP32	DBG_ACC	Type-C debug accessory presence signal

Continued on next page

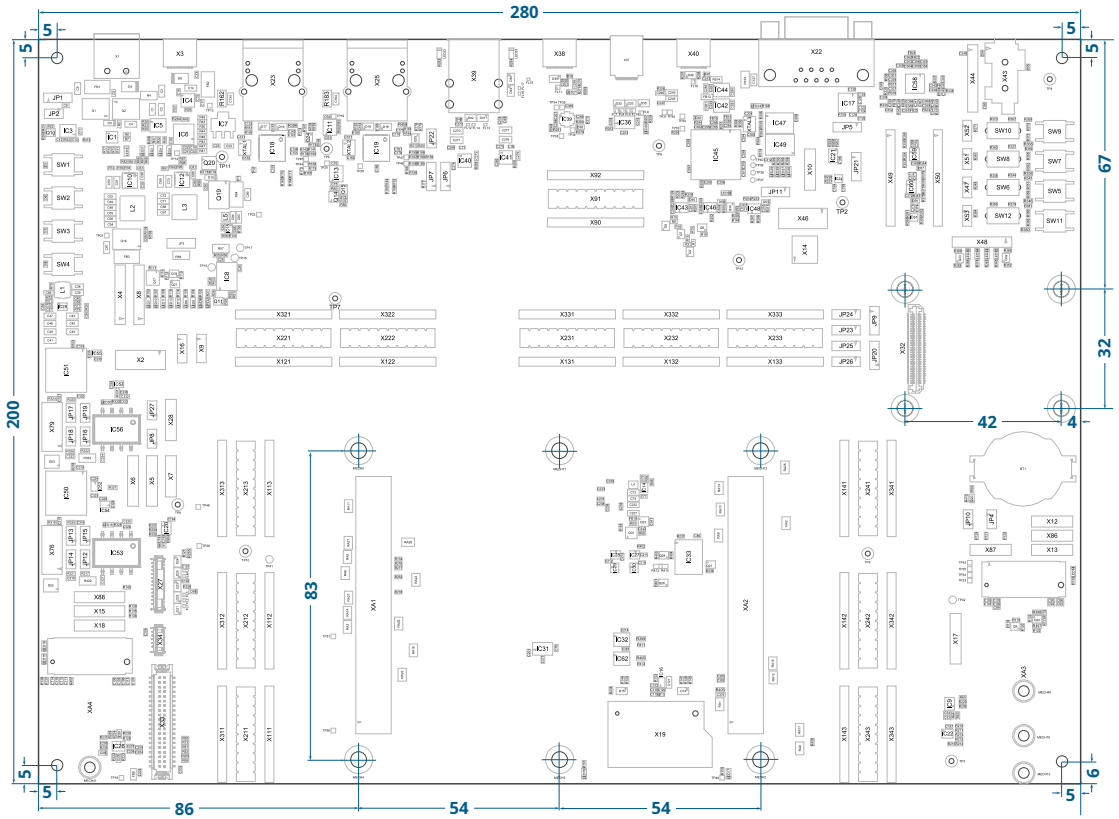
Table 39: Test points (Continued)

TP pin	Signal name	Description / Remarks
USB_B		
TP33	ILIM_5V_VBUS	USB current limit selector
TP34	EN_SNK1	VBUS sink power path control output
TP35	FRS_EN	FRS control of SRC load switch
TP36	DBG_ACC	Type-C debug accessory presence signal
FTDI UART		
TP37	FTDI_UARTC_3.3V_RTS	UART C Request to Send signal
TP38	FTDI_UARTC_3.3V_CTS	UART C Clear to Send signal
TP39	FTDI_UARTD_3.3V_RTS	UART D Request to Send signal
TP40	FTDI_UARTD_3.3V_CTS	UART D Clear to Send signal
JTAG		
TP41	TEST_GENERIC	General-purpose test signal
TP42	DEBUG_EN	Debug enable signal
Access to key subsystem signals (SDIO, Ethernet, PCIe, Debug - continued)		
TP44	ETH_A_GPIO0	Ethernet A GPIO
TP45	ETH_A_GPIO1	Ethernet A GPIO
TP46	ETH_B_GPIO0	Ethernet B GPIO
TP47	ETH_B_GPIO1	Ethernet B GPIO
TP48	VCC_OUT_IO	1.8V reference voltage for I/O
TP49	+V3.3_SD	SD card power rail
TP50	ETH_B_SDP	Ethernet B signal detect
TP51	ETH_A_SDP	Ethernet A signal detect

4 Mechanical Data

The dimensions on Figure 6 are in milimiters.

Figure 6: OSM Development Board dimensions



5 Design Data

The design data for Toradex Development Board is freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the Development Board design data, please use the link below:

http://developer.toradex.com/carrier-board-design

6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at http://www.toradex.com/support/product-compliance

7 Device and Documentation Support

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