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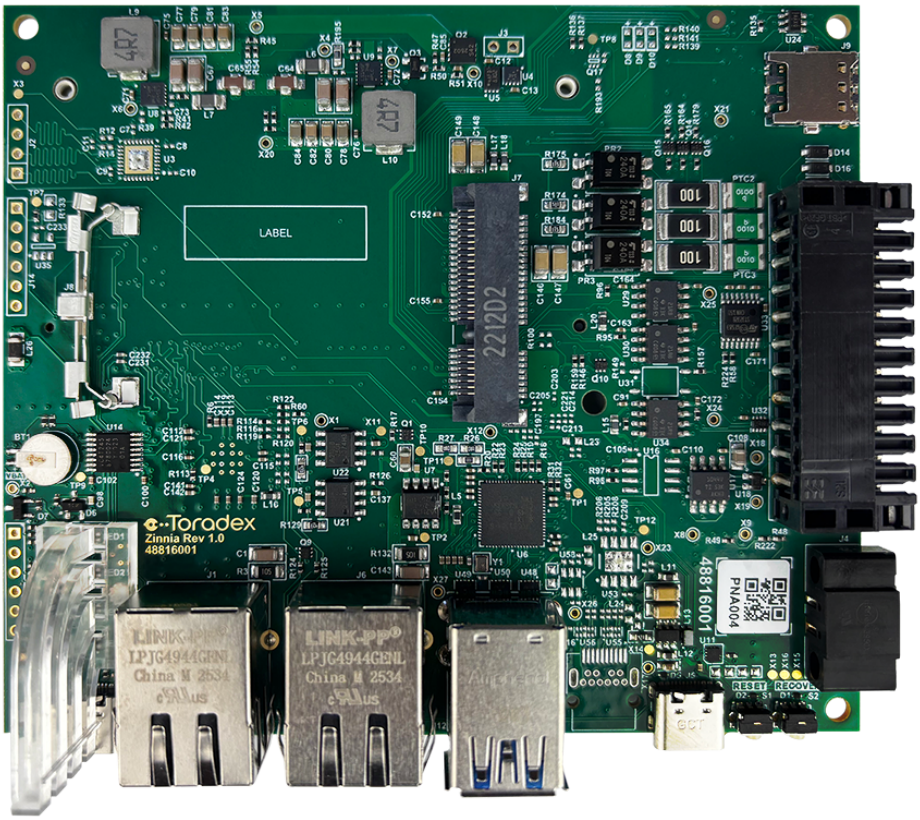
Zinnia Carrier Board

Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
17-Mar-2026	Rev. 0.1	V1.1	Initial documentation
10-Jun-2026	Rev. 0.2	V1.1	Section 4: add mechanical drawings

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Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
BTB	Board To Board
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.

Continued on next page

Abbreviations (Continued)

Abbreviation	Explanation
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1 Introduction

The Zinnia Carrier Board is compatible with the entire family of the Verdin system-on-modules. Designed with cost optimization in mind for small and medium production runs, it's perfectly suited for volume production. It complements the Verdin system-on-module by providing an array of industry-standard interfaces, and high-speed connectivity options, suited for diverse applications. Verdin interfaces are easily accessible via physical connectors and standard pitch headers.

The Zinnia Carrier Board is built on a 6-layer printed circuit board (PCB), and 4 layers are used for high-speed signal routing. CAE data for the board, including schematics, layout, and IPC-7351 compliant component libraries, are freely downloadable from the Toradex developer website.

1.1 Reference Documents

For detailed technical information, please refer to the documents listed below.

1.1.1 Verdin Family Specification

https://docs.toradex.com/109262-verdin-family-specification.pdf

1.1.2 Verdin Carrier Board Design Guide

https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

1.1.3 Verdin System-on-Module family overview

https://www.toradex.com/computer-on-modules/Verdin-arm-family

1.1.4 Toradex Developer Website – Verdin System-on-Module documents

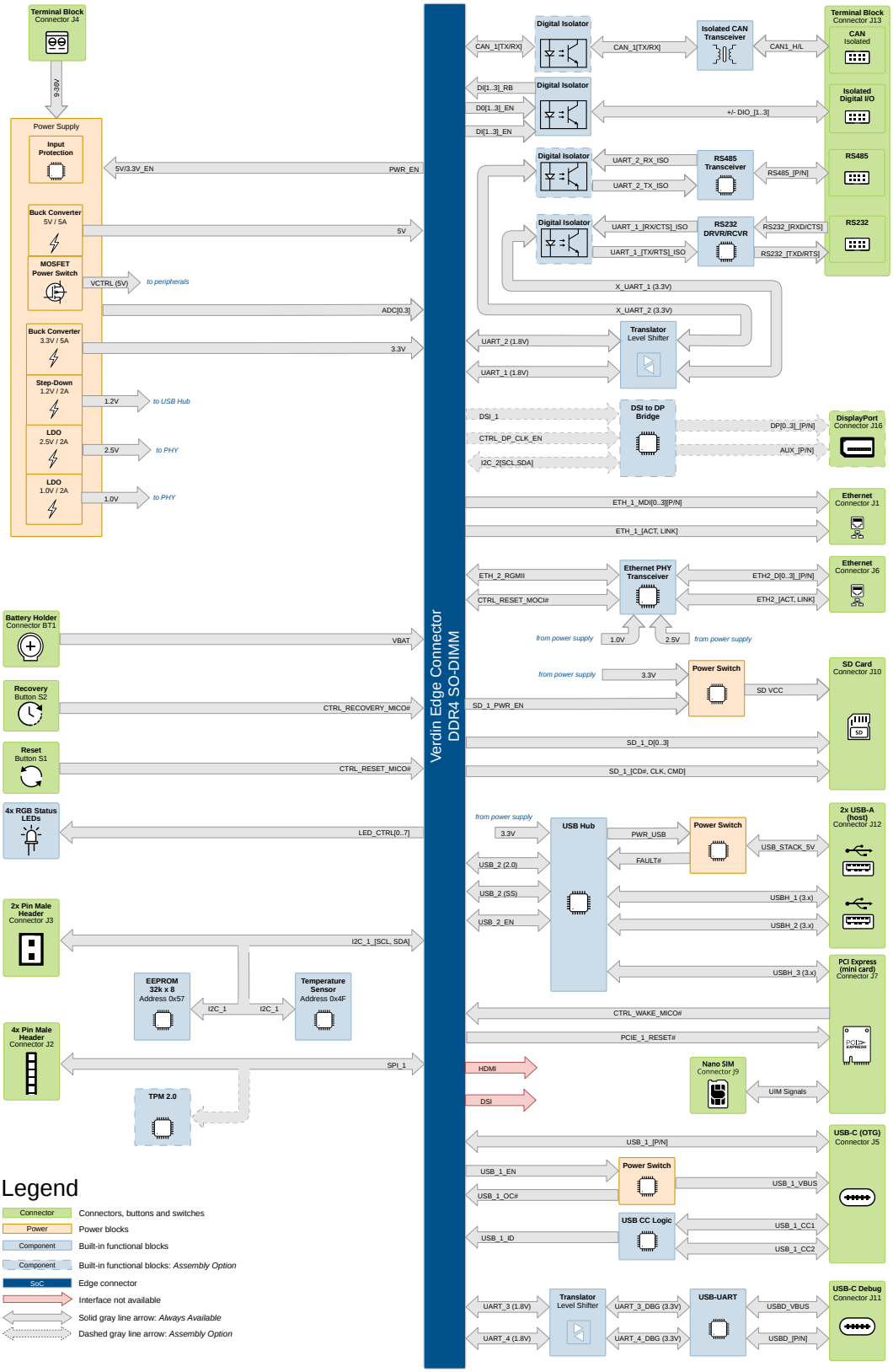
https://developer.toradex.com/products/verdin-som-family/modules

1.2 Main Features

- Power Input Requirements: DC 9 to 32V, 2A
- Operating temperature range: -40 to 85 °C
- 4x SoM ADC input to measure major power rails (Vin, 5V, 3V3, 1V8)
- 3x GPIO controlled tri-color status LEDs (green element from LED1 and LED2 are always on)
- 1x CAN-FD transceiver, with 120 ohm split termination
  - Zinnia Iso - Isolated CAN
  - Zinnia (other variants) - Non-Isolated CAN
- 1x 32 kB I^2C EEPROM
- 1x Gigabit Ethernet connector from SoM's onboard PHY
- 1x Gigabit Ethernet RGMII (DP83867)
- 3x GPIO controlled +/-32V photorelays
- Micro SD card connector
- MiniPCIe connector (can be used for LTE modem, Ethernet card or other MiniPCIe cards)
  - USB 3.2
  - Nano SIM card connector
- 1x RS-232 Interface, with flow control
  - Zinnia Iso - Isolated RS-232
  - Zinnia (other variants) - Non-Isolated RS-232
- 1x RS-485 Interface, with 120 ohm termination
  - Zinnia Iso - Isolated RS-485
  - Zinnia (other variants) - Non-Isolated RS-485
- 1.8V UART connection for Linux console connection (J14)
- 3.3V UART connection for Linux console connection (J15)
- 2x USB 3.0 Type A connector
- 1x USB 2.0 OTG on USB-C connector, typically used for Linux image reflash
- 1x Zinnia Iso only: TPM 2.0 IC on SPI bus
- 1x I^2C temperature sensor
- 3x Digital inputs, 5 to 32V input voltage
- RTC backup battery holder for batteries size 6.8 mm diameter × 2.1 mm height
- Reset and Recovery mode buttons
- Extension connector with the following
  - 1x SPI interface
  - 1x I^2C interface
- Power Rails:
  - 5V/5A
  - 3.3V/5A
  - 1.8V/100mA (sourced from the SoM's `PWR_1V8_MOCI` rail)

1.3 Block Diagram

Figure 1: Zinnia Carrier Board Hardware Architecture



1.4 Physical Drawing and Connectors

1.4.1 Physical Drawing

- Size of the board 115mm x 95mm

1.4.2 Connectors

Table 1: List of connectors

Connector(s)	Manufacturer	Part Number	Side	Description/Remarks
Top				
J1/J6	Link-PP	LPJG4944GENL	Top	RJ45 MagJack, Gigabit Ethernet with integrated magnetics
J2	–	–	Top	SPI header, 4-pin
J3	–	–	Top	I^2C header, 1.8V, 2-pin, 1.87kΩ pull-up to 1.8V
J4	Molex	39506-1002	Top	Terminal block header, 2-pin, 3.5 mm pitch, horizontal, with retention
J5	GCT	USB4105-GF-A	Top	USB 2.0 OTG, Type-C typically used for linux image reflash
J7	TE Connectivity	1775862-2	Top	MiniPCIe connector, 52-pin, surface-mount (SMD)
J8	TE Connectivity	1717832-2	Top	MiniPCIe latch connector
J9	Global Connector Technology	SIM8055-6-1-14-00-A	Top	Nano-SIM connector, 6-pin, push-pull type, 1.35 mm height
J11	Global Connector Technology	USB4105-GF-A-120	Top	USB Type-C receptacle (debug), 24-pin (16+8 dummy)
J12	AMPHENOL	GSB4112312HR	Top	2x USB 3.0 Type A connectors
J13	Weidmuller	1728700000	Top	Terminal block header, 20-pin, 3.5 mm pitch right-angle (90°)
J14	–	–	Top	6 pin header 1.8V UART connection for Linux console
J15	–	–	Top	6 pin header 3.3V UART connection for Linux console
J16	Pulse	E9320-001-01	Top	DisplayPort connector assembled only on DP_TPM variant
Bottom				
J10	Global Connector Technology	MEM2052-00-195-00-A	Bottom	Micro SD Card connector push-push type
M1	TE Connectivity	2309409-2	Bottom	DDR4 SODIMM connector, 260-pin, 5.2 mm height

2 Interfaces Description

This section provides an overview of the interfaces available on the Zinnia Carrier Board and their connection to the Verdin System-on-Module (SoM). It describes the characteristics of each interface, including signal routing, connector types, and intended functionality. The goal is to clarify how the carrier board enables access to the SoM's capabilities and how external peripherals and systems can be integrated.

- **Connector Type**: DDR4 SO-DIMM 260 pin Socket
- **Manufacturer**: TE-2309409-2

For the pinout of the Verdin SoM, please refer to the respective Verdin SoM datasheet. Standoffs are available on the Zinnia Carrier Board for fixing the Verdin SoM to the carrier board.

2.1 ADC – Analog to Digital Converter

The design implements four analog measurement channels, identified as `ADC_1` to `ADC_4`, routed to the Verdin SoM (`M1`). Each ADC input is conditioned through a combination of passive components to ensure signal stability, filtering, and protection. Table 2 summarizes the mapping of each ADC channel to the corresponding Verdin connector pin, along with the expected input voltage levels derived from the monitored power rails.

Table 2: Analog to digital converter

Verdin connector (M1)	Verdin function name	Range	Description/Remarks
2	ADC_1	9 to 32 V	Input voltage: 0.551V at 24 V from the main input
4	ADC_2	0 to 5 V	Input voltage: 1.538V at 5 V from the U8 buck regulator output
6	ADC_3	0 to 3.3 V	Input voltage: 1.65V at 3.3 V from the U9 buck regulator output
8	ADC_4	0 to 1.8 V	Input voltage: 1.246V at 1.8 V from the PMIC output of the SoM

The measured voltages are scaled through resistor divider networks:

- 200 kΩ (2x 100 kΩ) / 4.7 kΩ for `ADC_1` to measure the 9 to 32 V input,
- 27 kΩ/12 kΩ for `ADC_2` to measure the 5V buck regulator output,
- 27 kΩ/27 kΩ for `ADC_3` to measure the 3.3V buck regulator output,
- 12 kΩ/27 kΩ for `ADC_4` to measure the 1.8V output from the SoM.

These dividers ensure that all monitored voltages are reduced to a level compatible with the ADC input range of the SoM while preserving measurement resolution.

Each divider output is filtered by an RC low-pass network formed with 100 nF capacitors, together with the effective series resistance of the divider. This filtering stage reduces high-frequency noise prior to ADC sampling.

Each conditioned signal is routed directly to the corresponding ADC pin on the Verdin SoM (pins 2, 4, 6, and 8 of connector `M1`), maintaining a symmetrical topology across all channels for consistent measurement behavior. The resulting voltages at the ADC inputs, as listed in Table 2, represent the nominal operating conditions of the respective power domains.

All ADC inputs are designed to remain within the valid input range (typically 0 V to the reference voltage of each channel). The RC filters are dimensioned to balance noise suppression and ADC sampling bandwidth, while the uniform channel design ensures predictable performance across all inputs. Test points are provided to allow probing and validation of each ADC signal during development and production testing.

ADC Connector
The analog to digital connector inputs of the SoM are **not exposed** on any connector of the Zinnia carrier board. The purpose of the ADC nets is to measure the main power rails.

2.2 Buttons – Recovery Mode and Reset

Buttons `S1` and `S2` provide a means to reset the SoM module, and put the SoM into recovery mode.

- `S1`: reset button. Pressing `S1` will issue a reset to the SoM module.
- `S2`: recovery button. It is used to enter recovery mode for Linux image reflash.

2.3 CAN Transceivers

The Zinnia Carrier Board provides a single CAN interface implemented using a dedicated CAN transceiver (`U17`). This interface is routed to connector `J13`, which exposes the differential CAN signals and ground references required for robust field communication.

On the **Zinnia Carrier Board Iso** variant, the CAN interface is **galvanically isolated**. In this configuration, the digital side (Verdin SoM) is isolated from the bus side, improving noise immunity and protecting against ground potential differences. In non-isolated variants, the transceiver is directly connected to the SoM.

The CAN controller signals from the Verdin SoM operate at 1.8 V logic levels. A level-shifting stage is implemented between the SoM and the CAN transceiver to translate these signals to the required voltage domain of the transceiver, ensuring proper signal integrity and reliable operation.

2.3.1 Termination Network

The CAN bus includes an onboard **split termination network**, designed to improve electromagnetic compatibility (EMC) and stabilize the common-mode voltage of the differential pair.

The termination consists of:

- Two resistors:
  - 60.4 Ω (connected to `CAN1_H`)
  - 60.4 Ω (connected to `CAN1_L`)
- A center-tap capacitor:
  - 4.7 nF to `GND_CAN1`

This configuration forms a **split termination** (2 × 60.4 Ω, or approximately 120 Ω differential) with a capacitive midpoint to ground, reducing common-mode noise emissions. In addition, ESD protection is provided on the CAN lines by device `U18` (`ESDCAN06-2BWY`), ensuring robustness against electrostatic discharge events on the external connector.

Table 3 shows the CAN connector pinout.

Table 3: CAN connector signals.

Pin	Signal	Bus	Voltage	Description/Remarks
CAN Interface Signals				
2	CAN1_H	CAN	5 V	CAN high differential signal connected via split termination (R108 = 60.4Ω)
4	CAN1_L	CAN	5 V	CAN low differential signal connected via split termination (R107 = 60.4Ω)

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Table 3: CAN connector signals. (Continued)

Pin	Signal	Bus	Voltage	Description/Remarks
CAN Ground Signals				
1	GND_CAN1	CAN	–	Ground reference for CAN interface
3	GND_CAN1	CAN	–	

2.4 Digital I/O / Relays

The Zinnia Carrier Board provides three isolated digital I/O channels on field connector `J13`. Each channel is implemented as a bidirectional, opto-isolated interface capable of operating with external industrial voltage levels while maintaining galvanic isolation from the Verdin SoM.

In this section, the notation `+DIO_x` and `-DIO_x` refers to the field terminals of each digital I/O channel, where `x = 1, 2, 3` corresponds to channels `DIO1`, `DIO2`, and `DIO3`, respectively.

2.4.1 Digital I/O Channel Architecture

Each digital I/O channel (`DIO1`, `DIO2`, `DIO3`) consists of the following functional blocks:

- **Input isolation stage** Implemented using optocouplers (`TLP185GR`). External voltages applied between `+DIO_x` and `-DIO_x` drive the internal LED of the optocoupler, allowing the signal to be transferred across the isolation barrier.

  The input stage is designed to support typical industrial voltage ranges:

  - **Nominal input range**: 5 V to 24 V DC
  - **Recommended operating range**: 5 V to 32 V DC
  - **Absolute tolerance (protected)**: up to ~36 V (limited by protection components)

- **Current regulation and protection** Devices such as `PSSI2021` (e.g., `U38`, `U39`, `U43`) implement a **constant current source** that drives the optocoupler LED.

  This stage is critical for reliable operation across a wide input voltage range. Instead of directly driving the LED with a resistor (which would result in current varying significantly with input voltage), the current source ensures that the LED current remains approximately constant over the full operating range.

  This provides the following advantages:

  - **Stable switching threshold** independent of input voltage (5 V vs 24 V)
  - **Consistent optocoupler performance**, improving detection accuracy
  - **Reduced power dissipation variation** across the input range
  - **Improved noise immunity**, especially for long industrial cables

  In practice, once the input voltage exceeds the minimum threshold required by the current source, the LED current is regulated to a fixed value (typically a few milliamperes), ensuring that the optocoupler operates in a well-defined region. This results in a clear distinction between OFF and ON states, even when the input voltage varies.

  Additional protection includes:

  - Resettable fuses (`PTC1`, `PTC2`, `PTC3`) for overcurrent protection

  - Clamp diodes (`D11-D16`) for reverse polarity protection and transient voltage suppression

- **Output isolation stage** The output stage is implemented using solid-state relays (`TLP240A`), which provide an isolated switching function between `+DIO_x` and `-DIO_x`.

2.4.2 Relay Outputs

The design integrates three solid-state relay outputs: `PR1`, `PR2`, and `PR3`, implemented using `TLP240A`. Each relay provides an **isolated contact function** between the field terminals: `+DIO_x` to `-DIO_x`, where `x` is the digital I/O channel 1 to 3.

This means:

- **Output ON**: relay closed, connecting `+DIO_x` and `-DIO_x`
- **Output OFF**: relay open, terminals isolated

Output Mode Behavior
The output does NOT connect `-DIO_x` to system ground. It behaves as a floating, isolated contact (dry contact equivalent).

2.4.3 Functional Summary

The digital I/O subsystem provides:

- Three fully isolated digital channels
- Configurable as input or output
- Output behaves as an isolated contact between field terminals

Table 4 shows the digital I/O connector pinout.

Table 4: Digital IO relays

J13 Pin	Signal	I/O	Typical Voltage	Description / Remarks
Digital I/O Channel 1				
9	+DIO_1	I/O	5 V to 24 V	Field-side positive terminal for `DIO_1`. In input mode, voltage between `+DIO_1` and `-DIO_1` is sensed through the protected and isolated input path. In output mode, `PR2` closes an isolated contact between `+DIO_1` and `-DIO_1.`
10	-DIO_1	I/O	5 V to 24 V	Field-side negative terminal for `DIO_1`. In output mode, this pin is not switched to board `GND`; instead, the relay provides a floating isolated contact between `+DIO_1` and `-DIO_1`.
Digital I/O Channel 2				
11	+DIO_2	I/O	5 V to 24 V	Field-side positive terminal for `DIO_2`. In input mode, voltage between `+DIO_2` and `-DIO_2` is sensed through the protected and isolated input path. In output mode, `PR1` closes an isolated contact between `+DIO_2` and `-DIO_2.`
12	-DIO_2	I/O	5 V to 24 V	Field-side negative terminal for `DIO_2`. In output mode, this pin is not switched to board `GND`; instead, the relay provides a floating isolated contact between `+DIO_2` and `-DIO_2`.

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Table 4: Digital IO relays (Continued)

J13 Pin	Signal	I/O	Typical Voltage	Description / Remarks
Digital I/O Channel 3				
13	+DIO_3	I/O	5 V to 24 V	Field-side positive terminal for `DIO_3`. In input mode, voltage between `+DIO_3` and `-DIO_3` is sensed through the protected and isolated input path. In output mode, `PR3` closes an isolated contact between `+DIO_3` and `-DIO_3.`
14	-DIO_3	I/O	5 V to 24 V	Field-side negative terminal for `DIO_3`. In output mode, this pin is not switched to board `GND`; instead, the relay provides a floating isolated contact between `+DIO_3` and `-DIO_3`.

2.5 Ethernet

The Zinnia Carrier Board implements two independent Ethernet interfaces, both supporting **10/100/1000BASE-T Gigabit Ethernet** operation.

2.5.1 Native SoM Ethernet Interface

The first Ethernet interface is routed directly from the Verdin SoM to RJ45 MagJack connector `J1`. The interface utilizes the SoM-integrated Ethernet PHY, with the four MDI differential pairs routed directly to the connector through integrated magnetics.

Signal integrity and robustness are ensured by ESD protection arrays (`U1`, `U2`) placed close to the connector, controlled impedance routing of the differential pairs, and proper magnetics integration within the RJ45 connector.

Link and activity LEDs are driven directly from the SoM Ethernet signals through resistor networks, interfacing with the LED indicators integrated in the MagJack.

2.5.2 External Ethernet Interface (RGMII + PHY)

The second Ethernet interface is implemented using an external Gigabit Ethernet PHY, `U19` (**DP83867IRRGZR**), connected to the Verdin SoM via an **RGMII (Reduced Gigabit Media Independent Interface)**.

The RGMII interface provides a high-speed parallel connection between the SoM MAC and the PHY, including:

- Transmit signals: `TXD[3:0]`, `TX_CTL`, `TX_CLK`
- Receive signals: `RXD[3:0]`, `RX_CTL`, `RX_CLK`
- Management interface: `MDC`, `MDIO`
- Interrupt signal: `INT#`

The interface operates at **125 MHz DDR signaling** in Gigabit mode and requires controlled trace length matching. The DP83867 supports internal clock delay insertion, reducing the need for external delay lines and simplifying PCB routing.

2.5.3 On-board Ethernet PHY

The Zinnia Carrier Board integrates the `DP83867IRRGZR`, a high-performance Gigabit Ethernet PHY supporting:

- **10BASE-T / 100BASE-TX / 1000BASE-T**
- **RGMII v2.0** with configurable internal delays

- **Auto-negotiation and auto-MDI/MDIX**
- **Energy Efficient Ethernet (IEEE 802.3az)**
- Integrated cable diagnostics and loopback modes

Key design aspects

- **Clocking** The PHY requires a stable reference clock (typically 25 MHz) for internal timing generation.
- **Power domains** The PHY is powered from multiple dedicated supply rails:
  - `1V0_ETH` for the core (`VDD1P0`)
  - `1V8` for I/O (`VDDIO`)
  - `2V5` for analog circuitry (`VDDA2P5`)
  - `VDDA1P8` for sensitive analog blocks

  Each rail is locally decoupled with a combination of bulk (µF) and high-frequency (100 nF) capacitors to ensure low noise and stable operation.
- **Strapping configuration** Bootstrap resistors define PHY configuration at power-up, including RGMII timing mode, PHY address, and LED behavior.
- **LED outputs** Dedicated PHY LED pins drive link and activity indicators on the RJ45 connector through external resistor networks.

2.5.4 PHY to Connector Interface

On the line side, the PHY MDI pairs are routed to RJ45 MagJack connector `J6` through integrated magnetics.

Protection and robustness are ensured by ESD protection arrays (`U20`, `U23`), controlled impedance routing, and proper separation between analog (MDI) and digital (RGMII) domains. The interface supports full Gigabit Ethernet operation over standard twisted-pair cabling.

2.5.5 Design Considerations

- **Signal integrity** is ensured through controlled impedance routing and tight length matching of RGMII signals
- **Isolation** is provided by Ethernet magnetics between PHY and external network
- **Protection** is implemented using ESD devices on both Ethernet ports
- **Flexibility** is achieved through the external PHY, enabling independent interface configuration and diagnostics

2.5.6 Functional Summary

The Ethernet subsystem provides:

- Two independent Gigabit Ethernet interfaces
- Direct SoM Ethernet connection (integrated PHY)
- External PHY-based Ethernet (`DP83867IRRGZR`) via RGMII
- Full support for **10/100/1000BASE-T**
- Integrated ESD protection and magnetics
- LED-based link and activity indication

Table 5, Table 6, and Table 7 summarize the implemented Ethernet connections.

Table 5: Ethernet 1 connector (from SoM on-board PHY)

J1 pin	Connector signal	Verdin function name	M1 pin	I/O	Description / Remarks
Ethernet 1 MDI Signals					
9	D0+	ETH_1_MDI0_P	225	I/O	MDI pair 0 positive routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
8	D0-	ETH_1_MDI0_N	227	I/O	MDI pair 0 negative routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
7	D1+	ETH_1_MDI1_P	233	I/O	MDI pair 1 positive routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
6	D1-	ETH_1_MDI1_N	231	I/O	MDI pair 1 negative routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
5	D2+	ETH_1_MDI2_P	239	I/O	MDI pair 2 positive routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
4	D2-	ETH_1_MDI2_N	241	I/O	MDI pair 2 negative routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
3	D3+	ETH_1_MDI3_P	247	I/O	MDI pair 3 positive routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
2	D3-	ETH_1_MDI3_N	245	I/O	MDI pair 3 negative routed from Verdin SoM to RJ45 MagJack through integrated magnetics, ESD protected by TVS diode DT1240-04LP-7
LED Indication Signals					
11	G+	3.3V	–	PWR	Green LED anode, driven by the Verdin LINK LED output through resistor network R1
12	G-	ETH_1_LED2(LINK)	237	O	Green LED cathode return inside the MagJack LED circuit
13	Y+	3.3V	–	PWR	Yellow LED anode, driven by the Verdin ACT LED output through resistor network R2
14	Y-	ETH_1_LED1(ACT)	235	O	Yellow LED cathode return inside the MagJack LED circuit
Ground and Shield					
1	GND	–	–	PWR	Connector ground reference
10	GND	–	–	PWR	Connector ground reference
S	SHIELD	–	–	PWR	Connector shield AC-coupled to GND through 1 nF and 1 MΩ for EMI control

Table 6: Ethernet 2 connector

J6 pin	Connector signal name	PHY signal name (pin)	I/O	Description / Remarks
Ethernet 2 MDI Signals				
2	D3-	TD_M_D (11)	I/O	MDI pair D negative bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
3	D3+	TD_P_D (10)	I/O	MDI pair D positive bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
4	D2-	TD_M_C (8)	I/O	MDI pair C negative bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
5	D2+	TD_P_C (7)	I/O	MDI pair C positive bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
6	D1-	TD_M_B (5)	I/O	MDI pair B negative bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
7	D1+	TD_P_B (4)	I/O	MDI pair B positive bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
8	D0-	TD_M_A (2)	I/O	MDI pair A negative bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
9	D0+	TD_P_A (1)	I/O	MDI pair A positive bi-directional between PHY and connector, ESD protected by TVS diode DT1240-04LP-7
LED Indication Signals				
11	G+	3.3 V	PWR	Green LED anode, driven by PHY LED output (link indication)
12	G-	LED_0 (47)	O	Green LED cathode return inside MagJack
13	Y+	3.3 V	PWR	Yellow LED anode, driven by PHY LED output (activity indication)
14	Y-	LED_2 (45)	O	Yellow LED cathode return inside MagJack
Ground and Shield				
1	GND	–	PWR	Connector ground reference
10	GND	–	PWR	Connector ground reference
S	SHIELD	–	PWR	Connector shield AC-coupled to GND through 1 nF and 1 MΩ for EMI control

Table 7: Ethernet 2 RGMII

M1 pin	Verdin signal	PHY signal name	PHY pin	I/O	Description / Remarks
Ethernet Management					
193	ETH_2_RGMII_MDC	MDC	16	I	Management clock from the Verdin SoM to the DP83867 PHY
191	ETH_2_RGMII_MDIO	MDIO	17	I/O	Management data line between the Verdin SoM and the PHY 1.87 kΩ pull-up to 1.8V
189	ETH_2_RGMII_INT#	INT#/LED_0	44	O	PHY interrupt line to the Verdin SoM 10 kΩ pull-up to 1.8V
Ethernet Data Signals					
197	ETH_2_RGMII_RXC	RGMII_RXC	32	O	RGMII receive clock from the PHY to the Verdin SoM
199	ETH_2_RGMII_RX_CTL	RGMII_RX_CTL	38	O	RGMII receive control from the PHY to the Verdin SoM 2.49 kΩ/5.76 kΩ strap network

Continued on next page

Table 7: Ethernet 2 RGMII (Continued)

M1 pin	Verdin signal	PHY signal name	PHY pin	I/O	Description / Remarks
201	ETH_2_RGMII_RXD_0	RGMII_RXD0	33	O	RGMII receive data bit 0 from the PHY to the Verdin SoM 2.49 kΩ/5.76 kΩ strap network
203	ETH_2_RGMII_RXD_1	RGMII_RXD1	34	O	RGMII receive data bit 1 from the PHY to the Verdin SoM
205	ETH_2_RGMII_RXD_2	RGMII_RXD2	35	O	RGMII receive data bit 2 from the PHY to the Verdin SoM 2.49 kΩ/5.76 kΩ strap network (DNP)
207	ETH_2_RGMII_RXD_3	RGMII_RXD3	36	O	RGMII receive data bit 3 from the PHY to the Verdin SoM
213	ETH_2_RGMII_TXC	RGMII_TXC	29	I	RGMII transmit clock from the Verdin SoM to the PHY
211	ETH_2_RGMII_TX_CTL	RGMII_TX_CTL	37	I	RGMII transmit control from the Verdin SoM to the PHY
221	ETH_2_RGMII_TXD_0	RGMII_TXD0	28	I	RGMII transmit data bit 0 from the Verdin SoM to the PHY
219	ETH_2_RGMII_TXD_1	RGMII_TXD1	27	I	RGMII transmit data bit 1 from the Verdin SoM to the PHY
217	ETH_2_RGMII_TXD_2	RGMII_TXD2	26	I	RGMII transmit data bit 2 from the Verdin SoM to the PHY
215	ETH_2_RGMII_TXD_3	RGMII_TXD3	25	I	RGMII transmit data bit 3 from the Verdin SoM to the PHY

2.6 LED Status Indicators

The Zinnia Carrier Board provides a set of LED indicators to offer immediate visual feedback on system power, operational status, and peripheral activity. These indicators are distributed across both sides of the board and are used to monitor key supply rails, relay outputs, and interface signals.

Table 8: RGB status LED GPIO mapping.

LED	Colour	Verdin Signal Name	GPIO Signal (active high)	SODIMM pin # (M1)
LED1	Blue	I2S_2_D_OUT	LED.GPIO7	46
	Green	– always on	–	–
	Red	I2S_2_D_IN	LED.GPIO8	48
LED2	Blue	Not connected	–	46
	Green	– always on	–	–
	Red	Not connected	–	48
LED3	Blue	I2S_1_D_IN	LED.GPIO4	36
	Green	QSPI_1_CS#	LED.GPIO5	54
	Red	I2S_2_SYNC	LED.GPIO6	44
LED4	Blue	I2S_1_BCLK	LED.GPIO1	30
	Green	I2S_1_SYNC	LED.GPIO2	32
	Red	I2S_1_D_OUT	LED.GPIO3	34

In addition to the fixed-function LEDs, the board features three tri-colour (RGB) status LEDs that are directly controlled by GPIO signals from the Verdin SoM. These LEDs allow flexible indication of system states through programmable color combinations. Each color channel (red, green, and blue) can be driven independently via dedicated GPIOs, as detailed in Table 8.

Green LED Always On
The green elements on `LED1` and `LED3` are always on and cannot be controlled.

2.7 MicroSD

The Zinnia Carrier Board provides a MicroSD card socket on connector `J10`. The interface is connected to the Verdin SoM `SD_1` signals and supports standard **SD / SDIO 4-bit operation**.

The socket is supplied by a switched **3.3 V rail**, generated through power switch `U25` (`AP22653AW6-7`). This device provides controlled power-up of the card, including current limiting and protection against short-circuit conditions. Local decoupling capacitors ensure stable supply operation during card insertion and high-speed data transfers.

2.7.1 Signal Protection

All high-speed signal lines connected to the MicroSD card are protected using dedicated ESD protection arrays `DT1240-04LP-7` (`U26`, `U27`). These devices are low-capacitance transient voltage suppressors specifically designed for high-speed interfaces. They are placed close to the connector to protect the following signals:

- SD data lines (`SD_1_DAT[0:3]`)
- Command line (`SD_1_CMD`)
- Clock line (`SD_1_CLK`)
- Card detect (`SD_1_CD#`)

The protection devices provide:

- **Electrostatic discharge (ESD) protection** Protects the SoM and surrounding circuitry against high-voltage discharges caused by user interaction during card insertion and removal.
- **Transient voltage suppression (TVS)** Clamps fast voltage spikes, e.g., Electrical Fast Transient (EFT) or cable-induced transients, to safe levels before they reach sensitive SoC pins.
- **Low capacitance** Ensures minimal impact on signal integrity, which is critical for high-speed SDIO operation.

2.7.2 Card Detection

The `SD_1_CD#` signal is routed to the SoM to detect card insertion and removal events. This signal is also protected by the ESD arrays, ensuring reliable operation in environments subject to electrical noise and user interaction.

2.7.3 Design Considerations

- **Hot-plug robustness** The combination of power switching `AP22653AW6-7` and ESD protection `DT1240-04LP-7` components enables safe insertion and removal of MicroSD cards during operation.
- **Signal integrity** The use of low-capacitance protection devices ensures that high-speed SD signals remain within specification.
- **System protection** The design prevents damage to the SoM caused by:
  - ESD events during handling
  - Voltage transients on external interfaces
  - Fault conditions on the card supply rail

Table 9 summarizes the MicroSD interface.

Table 9: MicroSD card interface

J10 pin	Signal Name	Verdin function (M1 pin)	I/O	Voltage	Description/Remarks
Command and Control Pins					
9	SD_1_CD#	SD_1_CD# (84)	I	3.3V	Card detect[1]
5	SD_1_CLK	SD_1_CLK (78)	O	1.8V / 3.3V	Clock[1]
3	SD_1_CMD	SD_1_CMD (74)	I/O	1.8V / 3.3V	Command[1]
Data Pins					
7	SD_1_D0	SD_1_D0 (80)	I/O	1.8V / 3.3V	Data line 0[1]
8	SD_1_D1	SD_1_D1 (82)	I/O	1.8V / 3.3V	Data line 1[1]
1	SD_1_D2	SD_1_D2 (70)	I/O	1.8V / 3.3V	Data line 2[1]
2	SD_1_D3	SD_1_D3 (72)	I/O	1.8V / 3.3V	Data line 3[1]

[1] Using dedicated ESD protection arrays `DT1240-04LP-7`.

2.8 MiniPCIe

The Zinnia Carrier Board provides a MiniPCIe socket (`J7`) intended primarily for WWAN and modem modules. While the connector follows the MiniPCIe mechanical and pinout convention, the implemented electrical interfaces are centered on USB, SIM/UIM, reset, LED, and control signals rather than a native PCIe connection from the Verdin SoM.

Although the MiniPCIe socket (`J7`) includes routing on the standard MiniPCIe high-speed lane pins (`PERn0`, `PERp0`, `PETn0`, `PETp0`), these differential provides USB SuperSpeed signals from USB hub `U6`, with AC-coupling capacitors implemented on the transmit path. No functional Verdin PCIe reference clock is routed to the slot.

As a result, the current Zinnia implementation provides flexible peripheral options via USB connectivity on the MiniPCIe connector. The slot is primarily intended for WWAN/modem applications using USB, SIM, reset, LED, and control signals, rather than a native PCIe link.

Table 10 summarizes the PCIe-related routing implemented in the design.

Table 10: MiniPCIe signals

J7 pin	MiniPCIe signal	Signal destination / mapping	I/O	Description / Remarks
Control Signals				
1	WAKE#	CTRL_WAKE1_MICO#	I	Wake signal 27 kΩ pull-up to 1.8V
20	W_DISABLE#	3.3V	I	Wireless disable via 27 kΩ pull-up (interface always on)
Power Signals				
2, 24, 39, 41, 52	3.3V	MPCI1_3V3	PWR	Main supply
Multiple pins[1]	GND	GND	GND	Ground reference

Continued on next page

Table 10: MiniPCIe signals (Continued)

J7 pin	MiniPCIe signal	Signal destination / mapping	I/O	Description / Remarks
SIM Signals				
8	UIM_PWR	VCC of Nano SIM (J9) pin C1	O	SIM power
10	UIM_DATA	IO of Nano SIM (J9) pin C7	I/O	SIM data
12	UIM_CLK	CLK of Nano SIM (J9) pin C3	O	SIM clock
14	UIM_RESET	RST of Nano SIM (J9) pin C2	O	SIM reset
16	UIM_VPP	VPP of Nano SIM (J9) pin C6		
High-speed Signals				
22	PERST#	PCIE_1_RESET#	O	Reset
23	PERn0	USB Hub DS3_RXM, pin 36	I	USB SS RX negative
25	PERp0	USB Hub DS3_RXP, pin 35	I	USB SS RX positive
31	PETn0	USB Hub DS3_TXM, pin 39	O	USB SS TX negative via 100 nF AC-coupling capacitor
33	PETp0	USB Hub DS3_TXP, pin 38	O	USB SS TX positive via 100 nF AC-coupling capacitor
36	USB_D-	USB Hub DS3_DP, pin 65	I/O	USB 2.0 data -
38	USB_D+	USB Hub DS3_DM, pin 64	I/O	USB 2.0 data +
LED Indicators				
42	LED_WWAN#	LED not connected	O	WWAN LED
44	LED_WLAN#	LED not connected	O	WLAN LED
46	LED_WPAN#	LED not connected	O	WPAN LED

[1] Ground pins: 4, 9, 15, 18, 21, 26, 27, 29, 34, 35, 37, 40, 43, 50.

2.8.1 SIM Interface (J9)

The board includes a Nano SIM socket (`J9`) connected to the MiniPCIe UIM signals. Table 11 summarizes the MiniPCIe and SIM connections.

Table 11: MiniPCIe to Nano SIM

J9 pin	Nano SIM signal (J9)	MiniPCIe signal	I/O	Description / Remarks
C1	VCC	UIM_PWR	O	SIM supply (1.8 V / 3 V)
C2	RST	UIM_RESET	O	Reset
C3	CLK	UIM_CLK	O	Clock
C5	GND	GND	PWR	Ground
C6	VPP	UIM_VPP	O	Programming voltage pin[1]
C7	IO	UIM_DATA	I/O	SIM data

Continued on next page

Table 11: MiniPCIe to Nano SIM (Continued)

J9 pin	Nano SIM signal (J9)	MiniPCIe signal	I/O	Description / Remarks
C8	CD	–	–	Card detect not connected

[1] Legacy SIM programming voltage output. This signal is not used in modern SIM interfaces and is left unconnected in the Zinnia design

ESD protection is implemented using `TPD4E001`, and the SIM lines include localized 30 pF capacitive filtering.

2.8.2 Design Considerations

- The MiniPCIe slot is intended primarily for **USB-based extension cards**
- The slot includes **SIM/UIM support** for cellular modem use
- `PERST#` is implemented, but a complete Verdin-native PCIe link is not
- High-speed differential pairs are present on the standard MiniPCIe lane pins, but they are not sourced from a native SoM PCIe interface
- The 3.3 V rail (`MPCI1_3V3`) powers the installed module and must support the module peak current demand

Functional Summary
- USB 3.2 connectivity for modem modules
- SIM / UIM interface support
- Reset and control signals
- LED status routing
- High-speed differential routing on standard MiniPCIe lane pins
- No complete native PCIe interface from the Verdin SoM

2.9 Power Supply

The Zinnia Carrier Board is powered via the input connector `J4`, which provides the main supply rail to the system. The connector accepts a wide input voltage range, with support for 9 V to 32 V DC. The input is protected by a fuse (`F1`) rated at 5 A (part number `0680L5000-05`), located close to the connector to safeguard the board against overcurrent conditions.

The supplied voltage is distributed to the onboard power management circuitry, which generates the required regulated rails for the Verdin SoM and peripheral interfaces. Overall power consumption depends on the selected SoM and connected peripherals, particularly USB devices. Under typical conditions with no external loads, the combined carrier board and SoM power consumption ranges between approximately 4 W and 6 W.

Power Input Polarity and Voltage
Care must be taken to ensure correct polarity when connecting the power supply, as indicated in the table, and to operate within the specified voltage range to guarantee reliable system operation.

2.10 Serial Interfaces – RS-232 / RS-485

The Zinnia Carrier Board provides serial communication interfaces supporting both **RS-232** and **RS-485** standards. These interfaces enable robust communication with industrial and legacy equipment. The serial interfaces are implemented using external transceivers, which convert the Verdin SoM UART signals to 3.3 V voltage level.

2.10.1 RS-232 Interface

The RS-232 interface provides a **single-ended, full-duplex communication channel**. It is implemented using an RS-232 transceiver that converts the SoM UART signals (logic-level) to 3.3 V.

Key characteristics:

- **Signal type**: Single-ended
- **Voltage levels**: Typically 3.3 V
- **Communication mode**: Full-duplex (TX and RX independent)
- **Use case**: Legacy serial devices, debugging, configuration interfaces

The interface includes:

- TX and RX signals
- Optional hardware flow control (depending on routing)
- Protection and level shifting via the RS-232 transceiver

2.10.2 RS-485 Interface

The RS-485 interface provides a **differential, half-duplex communication channel**, suitable for long-distance and noise-immune communication in industrial environments.

Key characteristics:

- **Signal type**: Differential
- **Voltage levels**: Typically 3.3 V differential
- **Communication mode**: Half-duplex
- **Use case**: Industrial networks, Modbus, multi-drop communication

The interface includes: - Differential pair - Direction control (driver enable / receiver enable) - Termination and biasing resistors (as implemented in the design) - Protection components for robust field operation

2.10.3 Design Considerations

- **Level translation** Both interfaces use dedicated transceivers to convert between SoM logic levels and field-level signaling.
- **Noise immunity** RS-485 provides improved noise immunity due to differential signaling and is suitable for longer cable runs.
- **Interface selection** RS-232 is preferred for point-to-point communication, while RS-485 is suited for multi-node industrial networks.
- **Protection** ESD and transient protection are implemented on external connector signals to ensure reliability.

Table 12 summarizes the key components used to implement the isolated RS-232 and RS-485 interfaces.

Table 12: Serial components

Designator	Part	Function	Description / Remarks
U28	MIE05W0505BGYE-3R-P	Isolated DC/DC converter	Generates isolated 5 V field-side supply for the serial interface domain.

Continued on next page

Table 12: Serial components (Continued)

Designator	Part	Function	Description / Remarks
U29	ISO6721RBDR	Digital isolator	Isolation device used in the RS-232 data path.
U30	ISO6721RBDR	Digital isolator	Isolation device used in the RS-232 handshake path.
U33	ST3232BTR	RS-232 transceiver	Converts logic-level UART signals to RS-232 voltage levels.
U34	ISO6721RBDR	Digital isolator	Isolation device used in the RS-485 signal path.
U32	THVD1420DRLR	RS-485 transceiver	Implements the isolated half-duplex RS-485 differential interface.
J13	1728700000	Field connector	Weidmuller 2x10 right-angle terminal block used for serial, CAN, and digital I/O field signals.

2.10.4 Serial Interface Summary

Table 13 summarizes the available serial interfaces and their corresponding connectors.

Table 13: RS-232 and RS-485 serial communication

J13 pin	Signal	Connected to	I/O	Description / Remarks
RS-232 Interface				
6	RS232_RXD	UART_1_RXD	I	RS-232 receive data from the connector into the transceiver level-shfted to 3.3 V, isolated through ISO6721RBDR
8	RS232_TXD	UART_1_TXD	O	RS-232 transmit data driven from the transceiver to the connector level-shfted to 3.3 V, isolated through ISO6721RBDR
10	RS232_RTS	UART_1_RTS	O	Request-to-send output driven from the board to the connector level-shfted to 3.3 V, isolated through ISO6721RBDR
12	RS232_CTS	UART_1_CTS	I	Clear-to-send input from the connector into the transceiver level-shfted to 3.3 V, isolated through ISO6721RBDR
RS-485 Interface				
7	RS485_P	UART_2_RXD	I/O	Differential RS-485 positive line on the connector level-shfted to 3.3 V, protected via TVS diode; bi-directional half-duplex signal
9	RS485_N	UART_2_TXD	I/O	Differential RS-485 negative line on the connector level-shfted to 3.3 V, protected via TVS diode; bi-directional half-duplex signal
Isolated Ground Reference				
5	GND_RS	Isolated field ground	PWR	Ground reference for the isolated RS-232 / RS-485 field side.
11	GND_RS	Isolated field ground	PWR	Additional ground reference for the isolated field side.

Isolation Note
The serial interface pins are **not isolated by default**. Isolation is only present on variants whose part number explicitly contains **ISO**. Always verify the specific variant before relying on isolation.

2.11 USB Interfaces

The Zinnia Carrier Board implements three distinct USB interface groups, supporting a combination of **USB 2.0 (480 Mbps)** and **USB 3.2 Gen 1 (5 Gbps)** operation depending on the interface and routing.

2.11.1 USB Type-C OTG Interface (J5)

Connector `J5` is a USB Type-C port connected to the Verdin SoM `USB_1` interface. In the current design, this port supports **USB 2.0 (480 Mbps)** operation only. No SuperSpeed (USB 3.x) differential pairs are routed to this connector, therefore the interface operates exclusively in USB 2.0 mode.

The Type-C interface is implemented using:

- **Type-C controller** `TUSB320LIRWBR` (`U11`) for CC configuration and cable orientation detection
- **ESD protection** `TPD4E001` (`U12`) on the USB data lines
- **Common-mode choke** `L13` for EMI suppression
- **Load switch** `AP22653AW6-7` (`U10`) for controlled VBUS delivery and over-current protection

Table 14 summarizes the USB OTG interface.

Table 14: USB OTG interface

J5 pin	USB connector signal (J5)	Signal destination and mapping	I/O	Description / Remarks
Configuration Channel Signals				
A5	CC1	USB_1_ID CC1 (TUSB320LIRWBR)	I/O	Configuration channel for cable attach/orientation and role detection
B5	CC2	USB_1_ID CC2 (TUSB320LIRWBR)	I/O	Configuration channel for cable attach/orientation and role detection
Data Signals				
A6, B6	D+	USB_1_P via inductor, ESD protected	I/O	USB 2.0 positive data line ESD protected and filtered through the common-mode choke
A7, B7	D-	USB_1_N via inductor, ESD protected	I/O	USB 2.0 negative data line ESD protected and filtered through the common-mode choke
Sideband Use Signals				
A8	SBU1	Not connected	–	Sideband use pins are not implemented in the current design
B8	SBU2	Not connected	–	Sideband use pins are not implemented in the current design
Power and Ground Signals				
A1, A12, B1, B12	GND	System GND	PWR	Ground reference and shield return for the USB Type-C receptacle
A4, A9, B4, B9	VBUS	USB_1_VBUS via ferrite bead	PWR	Switched VBUS path with load switch control and over-current monitoring

USB OTG (J5) supports USB 2.0 only: No SuperSpeed TX/RX pairs are routed to this connector.

2.11.2 USB Debug Interface (J11)

Connector `J11` is a dedicated USB Type-C debug port and does not expose a general-purpose USB interface from the SoM. Instead, it is connected to a USB-to-UART bridge:

- **Device** `CP2105-F01-GMR` (`U45`)

This interface supports **USB 2.0 (480 Mbps)** on the USB side and provides **UART channels for debug** and console access. Additional circuitry includes:

- **ESD protection** `TPD4E001` (`U46`) on USB lines
- **Common-mode choke** common mode inductor (`L21`) for EMI filtering
- **Filtered VBUS input** through `L22`

This port, summarized by Table 15, is intended exclusively for debug access and not for USB host/device expansion.

Table 15: USB debug interface

J11 pin	USB connector signal	Signal destination and mapping	I/O	Description / Remarks
USB-UART Bridge (U45)				
–	–	TXD_ECI UART_3_RXD_DBG (pin 13)	O	Data received from USB is converted to UART RX (towards SoM)
–	–	RXD_ECI UART_3_TXD_DBG (pin 12)	I	UART TX data from SoM is converted to USB and transmitted over D+/D-
Data Signals				
A6, B6	D+	USB_D_P via inductor to USB-UART	I/O	USB positive data line for the debug USB-to-UART bridge
A7, B7	D-	USB_D_N via inductor to USB-UART	I/O	USB negative data line for the debug USB-to-UART bridge
Configuration Channel Signals				
A5	CC1	System GND 5.1 kΩ pull-down	I/O	Configuration channel for the debug USB-C receptacle
B5	CC2	System GND 5.1 kΩ pull-down	I/O	Configuration channel for the debug USB-C receptacle
Sideband Use Signals				
A8	SBU1	Not connected	–	Sideband use pin is not implemented in the current design
B8	SBU2	Not connected	–	Sideband use pin is not implemented in the current design
Power and Ground Signals				
A1, A12, B1, B12	GND	System GND	PWR	Ground reference and shield return for the debug USB Type-C
A4, A9, B4, B9	VBUS	USB_D_VBUS via ferrite bead USB-UART	PWR	VBUS input for the USB-to-UART bridge

2.11.3 USB Hub and Type-A Interfaces (J12)

High-speed USB host expansion is implemented using hub `U6` (`CYUSB3304-68LTXI`), which provides:

- **Upstream interface** to the Verdin SoM `USB_2`:
  - **USB 3.2 Gen 1 (5 Gbps)**
  - Backward compatible with **USB 2.0 (480 Mbps)**
- **Downstream ports**:
  - Two ports routed to stacked dual Type-A connector `J12`
  - One port routed to the MiniPCIe connector `J7` (USB 2.0 only)

Each Type-A port on `J12` supports:

- **USB 3.2 Gen 1 (5 Gbps)** via SuperSpeed differential pairs
- **USB 2.0 (480 Mbps)** via D+/D- lines

The interface includes:

- **Power switching** using `AP22653AW6-7` (`U47`) for controlled 5 V VBUS supply and over-current protection
- **ESD protection**:
  - `DT1240-04LP-7` TVS diodes, component `U50`, for USB 2.0 lines, and components `U48`, `U49` for the SuperSpeed pairs
- **Common-mode filtering and impedance control** on high-speed lines

- **AC-coupling capacitors** on SuperSpeed transmit pairs

Table 16 summarizes the USB interfaces using the USB 3.2 hub.

Table 16: USB hub interface

Port	Signal name	Signal destination and mapping	I/O	Description / Remarks
Upstream port				
9	US_RXP	USB_2_SSTX_P from Verdin connector	O	SuperSpeed transmit positive line without AC coupling
8	US_RXM	USB_2_SSTX_N from Verdin connector	O	SuperSpeed transmit negative line without AC coupling
6	US_TXP	USB_2_SSRX_P from Verdin connector	I	SuperSpeed receive positive line without AC coupling
5	US_TXM	USB_2_SSRX_N from Verdin connector	I	SuperSpeed receive negative line without AC coupling
57	US_D+	USB_2_P from Verdin connector	I/O	USB positive data line
58	US_D-	USB_2_N from Verdin connector	I/O	USB negative data line
Downstream 1 - J12 lower pin				
1	VBUS	USB_STACK_5V via U47 AP22653AW6-7	PWR	Switched VBUS supply for the lower Type-A port
2	D-	USBH1_N from USB hub pin 59, with ESD protection	I/O	USB negative data line for the lower port
3	D+	USBH1_P from USB hub pin 60, with ESD protection	I/O	USB positive data line for the lower port
4	GND	System GND	PWR	Ground reference
5	SSRX-	DS1_RX_N from USB hub pin 50, with ESD protection	I/O	SuperSpeed receive negative line
6	SSRX+	DS1_RX_P from USB hub pin 51, with ESD protection	I/O	SuperSpeed receive positive line
7	GND_DRAIN	System GND	PWR	SuperSpeed ground / drain reference
8	SSTX-	DS1_TX_N from USB hub pin 48, with ESD protection	I/O	SuperSpeed transmit negative line with AC coupling
9	SSTX+	DS1_TX_P from USB hub pin 47, with ESD protection	I/O	SuperSpeed transmit positive line with AC coupling
Shell	SHIELD	Connector shield	PWR	Connector shell tied to ground/shielding structure

Continued on next page

Table 16: USB hub interface (Continued)

Port	Signal name	Signal destination and mapping	I/O	Description / Remarks
Downstream 2 - J12 upper pin				
1	VBUS	USB_STACK_5V via U47 AP22653AW6-7	PWR	Switched VBUS supply for the upper Type-A port
2	D-	USBH2_N from USB hub pin 63, with ESD protection	I/O	USB negative data line for the upper port
3	D+	USBH2_P from USB hub pin 62, with ESD protection	I/O	USB positive data line for the upper port
4	GND	System GND	PWR	Ground reference
5	SSRX-	DS2_RX_N from USB hub pin 44, with ESD protection	I/O	SuperSpeed receive negative line
6	SSRX+	DS2_RX_P from USB hub pin 45, with ESD protection	I/O	SuperSpeed receive positive line
7	GND_DRAIN	System GND	PWR	SuperSpeed ground / drain reference
8	SSTX-	DS2_TX_N from USB hub pin 42, with ESD protection	I/O	SuperSpeed transmit negative line with AC coupling
9	SSTX+	DS2_TX_P from USB hub pin 41, with ESD protection	I/O	SuperSpeed transmit positive line with AC coupling
Shell	SHIELD	Connector shield	PWR	Connector shell tied to ground/shielding structure

Upstream 3 - MiniPCIe: Refer to the MiniPCIe interface section for details on the signals routed to the MiniPCIe slot.

MiniPCIe USB Connectivity
The MiniPCIe connector `J7` receives **USB 3.2** signals from the USB hub (`U6`), enabling support for USB-based WWAN modules.

2.11.4 Design Considerations

- **Mixed USB generations** The design combines USB 2.0-only interfaces (Type-C J5, debug J11, MiniPCIe) with USB 3.2 Gen 1 host expansion (Type-A J12 via hub).
- **Signal integrity** SuperSpeed routing follows controlled impedance design, with AC coupling and ESD protection placed close to the connectors.
- **Power management** All external USB ports include current-limited power switches with fault protection.
- **Interface roles**
  - `J5`: USB 2.0 OTG / device-capable interface
  - `J11`: Debug (USB-to-UART only)
  - `J12`: High-speed host expansion (USB 3.2 Gen 1)

3 Operating Conditions

3.1 Absolute Maximum Ratings

The absolute maximum ratings are listed in Table 17.

Table 17: Absolute maximum conditions

Parameter Description	Symbol / Net	Min	Max	Unit
Input voltage				
Input voltage (absolute maximum)	V_IN	-0.3	38	V
Input TVS Protection				
TVS breakdown voltage	V_BR	36.7	40.6	V
TVS clamping voltage	V_CLAMP	–	53.3	V
TVS peak pulse current	I_PP	–	7.5	A
5V Buck Converter				
Enable voltage EN to GND[1]	V_EN	-0.3	V_IN+0.3	V
Feedback voltage FB to GND[1]	V_FB	-0.3	5.5	V
RT voltage[2]	V_RT	-0.3	5.5	V
Bootstrap voltage BOOT to SW[3]	V_BOOT-SW	-0.3	5.5	V
Switch voltage	V_SW	-0.3	38	V
SW to GND transient voltage (<10 ns)	V_SW	-4	40	V
Open-drain power-good monitor output	V_PG	-0.3	20	V
Temperature				
Operating ambient temperature[4]	T_A	-40	85	°C
Junction temperature	T_J	-40	150	°C
Storage temperature	T_STG	-65	150	°C

[1] EN pin is not 5 V tolerant. Refer to the `LMR51450` datasheet for more information.
[2] Frequency setting pin used to set the switching frequency: short to ground defaults to 1 MHz.
[3] Bootstrap pin used to drive the high-side MOSFET.
[4] Depending on the variant of the System-on-Module.

Stress limits only
Operation beyond these limits may cause permanent damage.

3.2 Recommended Operating Conditions

The recommended operating conditions are summarized in Table 18.

Table 18: Recommended operating conditions

Parameter Description	Min	Typical	Max	Unit	Remarks
Input voltage (board input)	9	—	36	V	
TVS reverse stand-off voltage	—	33	—	V	Nominal selected TVS rating
Input fuse current rating	—	—	5	A	
Ambient temperature	-40	—	+85	°C	Depending on the variant

3.3 Operating Temperature Range

The Zinnia Carrier Board board is designed to operate within a temperature range of -40°C to 85°C, certain components have reduced operating temperature limits, as listed in Table 19.

Table 19: Temperature range for specific components

Component	Min. Temp. (°C)	Max. Temp. (°C)
MicroSD Card Holder	-25	85
HDMI / Display Connector	-20	80
USB Connectors	-20	85
Ethernet (RJ45)	-40	85
Board-to-Board Connector	-40	85
M.2 / LTE Connector	-40	85
Debug / Pin Headers	-40	85
General IO Connectors	-40	85

4 Mechanical Data

This section provides the mechanical specifications of the Zinnia Carrier Board, including overall dimensions, mounting hole locations, and connector placement. These parameters are essential for system integration, enclosure design, and thermal/mechanical validation.

Mechanical drawings included in this section define:

- Board outline and dimensions
- Mounting hole positions and recommended standoff usage
- Connector placement and keep-out areas

All dimensions are provided in millimeters unless otherwise specified.

4.1 Zinnia Carrier Board Dimensions

The Zinnia Carrier Board has the following overall size:

- 115.0 mm × 95.0 mm

Figure 2: Zinnia Carrier Board Top View

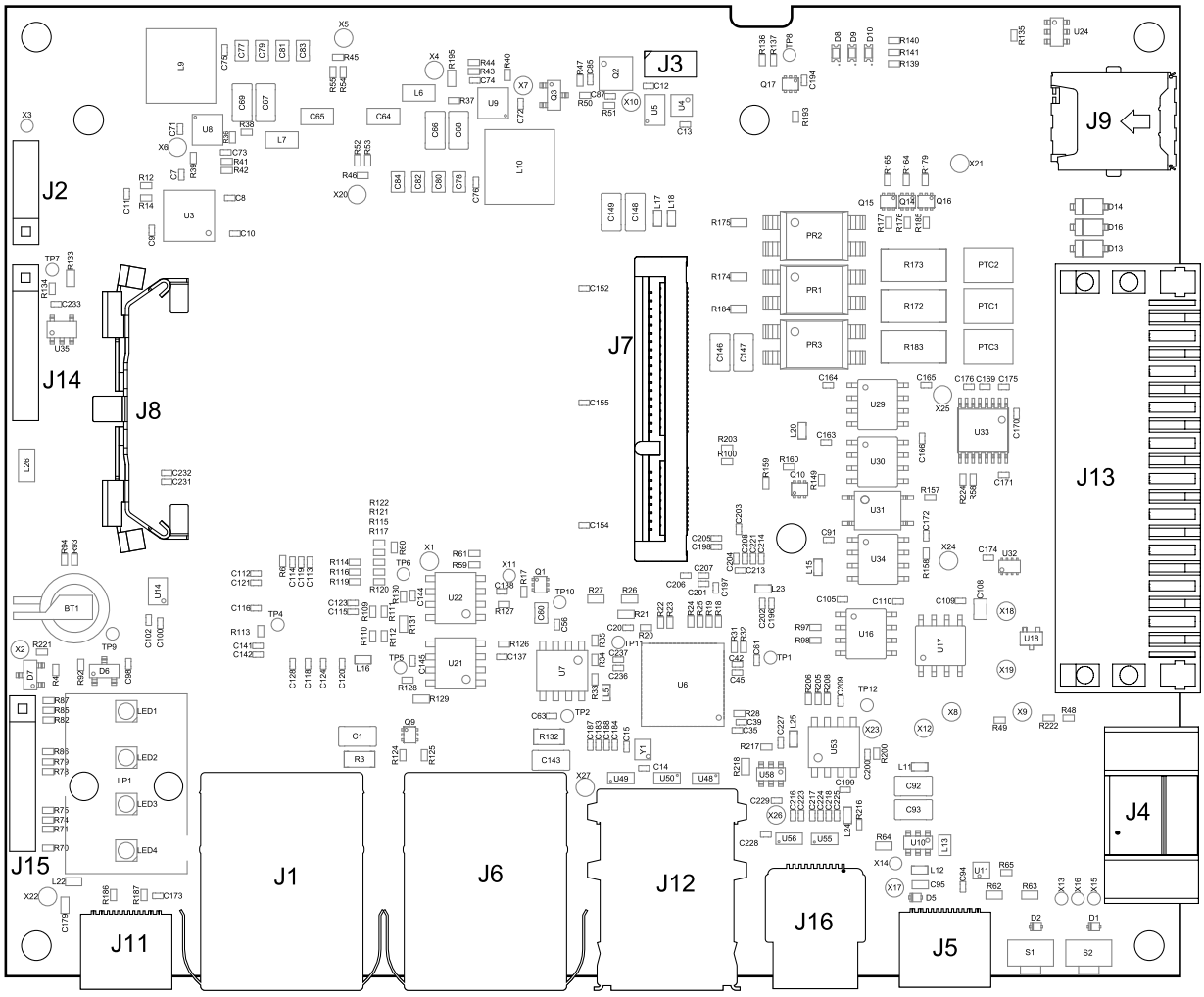

Table 20: Top side connectors

Connector	Manufacturer	Part Number	Description/Remarks
J1	Link-PP	LPJG4944GENL	Gigabit Ethernet
J2	Generic	–	SPI_1 4-pin header
J3	Generic	–	I2C_1 2-pin header
J4	Molex	0395061002	Main power connector
J5	GCT	USB4105-GF-A-120	USB2.0 DRP, Type-C connector
J6	Link-PP	LPJG4944GENL	Gigabit Ethernet
J7	TE Connectivity	1775862-2	Mini PCIe card connector
J8	TE Connectivity	1717832-2	Mini PCIe latch
J9	GCT	SIM8055-6-1-4-00-A	Nano SIM card holder
J11	GCT	USB4105-GF-A-120	Type-C USB2.0 DFP
J12	Amphenol	GSB4112312HR	Dual USB3.0, Type-A connector
J13	Weidmuller	1728700000	Field connector
J14	Generic	–	UART3, UART4 6-pin header
J15	Generic	–	UART3 DBG, UART4 DBG 6-pin header
J16	Pulse	E9320-001-01	Mini Display Port connector

Figure 3: Zinnia Carrier Board Bottom View

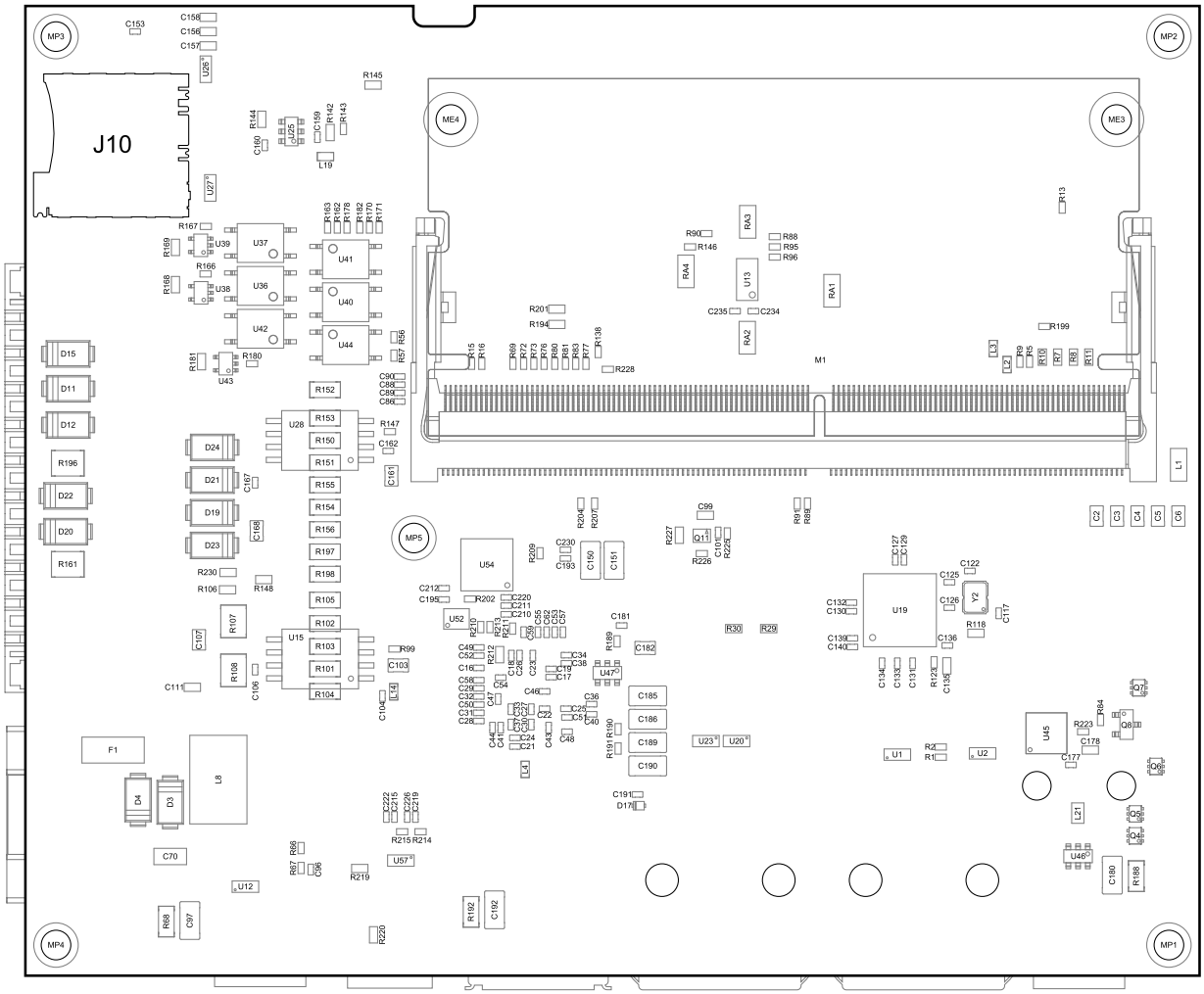

Table 21: Bottom side connectors

Connector	Manufacturer	Part Number	Description/Remarks
J10	Link-PP	LPJG4944GENL	MicroSD push-push holder

5 Design Data

The design data for Toradex carrier boards are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the carrier board design data, please use the web link below:

https://developer.toradex.com/carrier-board-design/reference-designs/#zinnia-carrier-board

6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website[1].

[1] https://www.toradex.com/support/product-compliance

7 Device and Documentation Support

7.1 Trademarks

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