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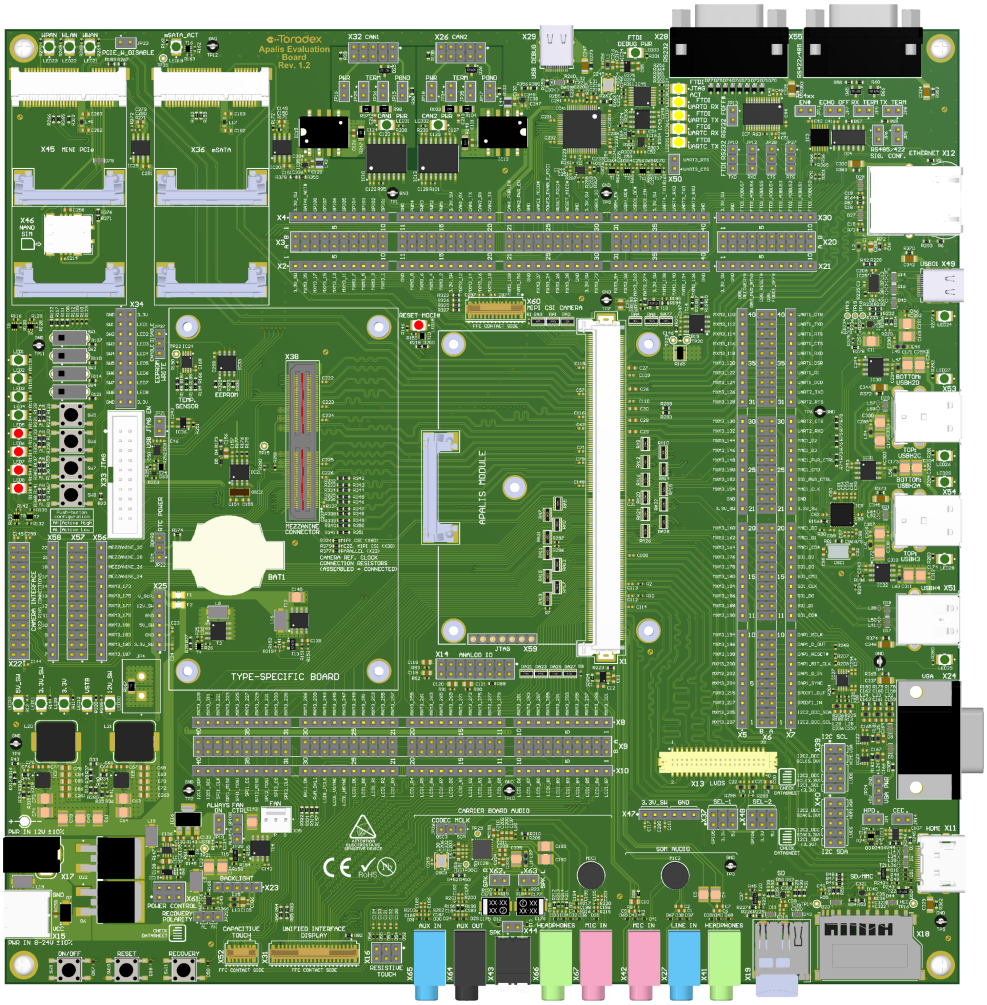
Apalis Evaluation Board V1.2

HW Datasheet



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
23-Nov-2023	Rev. 1.0	V1.2	Initial documentation for this product version. Changes from previous product version: - Added recovery mode button (SW11) and recovery polarity selection jumper (J29) - A MIPI-CSI camera connector (X60) was added - A Bridge-Tied-Load speaker output (X43 and X44) was added - Two onboard microphones were added - Many connectors and buttons were relocated - Major changes to the USB debugging circuit - The debug USB type B connector (X29) was replaced with a USB type C connector - The DB9 CAN connetors (X32) was replaced with two 10-pin IDC connectors (X26 and X32) - The 4-bit SD card connector (X19) was replaced with a MicroSD card connector - The 8-bit SD card connector (X18) was replaced with a 4-bit SD card connector - The DVI connector (X11) was replaced with an HDMI connector - The USB 3.0 micro-B connector (X49) was replaced wiht a USB type C connector - The SIM cardo connector (X46) was replaced with a Nano SIM card connector - The Generic RGB display interface (X20) was removed - The SATA connector (X37) was removed - The 4-pin fan connector (X48) was removed - The USB type B connector (X50) was removed - The Optical S/PDIF output (X21) was removed - The double serial DB9 connectors (X28) were replaced with a single DB9 connector. UART2 is no longer available in a DB9 connector - The PCIe x1 connectors (X43 and X44) were removed along with the associated PLX IC - The IrDA UART interface was removed - The audio IDC connectors (X41 and X42) were removed

Contents

1 Introduction

The Apalis Evaluation Board is a flexible development environment with which you can explore and evaluate the functionality and performance of the Apalis product family.

The Apalis family of Systems on Module supports a wide variety of industry-standard interfaces while providing advanced multimedia and high-speed connectivity, making it suitable for a variety of applications. Apalis SoM interfaces can be easily accessed using physical connectors and standard pitch headers. The GPIO usage allows easy probing of many interfaces and access to break and jumper signals.

The Apalis Evaluation Board PCB comprises four layers, of which only one is used for high-speed signal routing. This demonstrates how the Direct Breakout technology makes it easy to implement with minimal risk and effort. CAE data for the board, including schematics, layout, and IPC-7351-compliant component libraries, are freely downloadable from the Toradex developer website.

1.1 Reference Documents

Please refer to the documents listed below for detailed technical information about suitable systems on module and peripherals used on the Apalis Evaluation Board.

1.1.1 Apalis Systems on Module

https://www.toradex.com/computer-on-modules/apalis-arm-family

1.1.2 Pushbutton On/Off Controller datasheet

https://www.analog.com/media/en/technical-documentation/data-sheets/2954fb.pdf

1.1.3 USB Hub datasheet

https://ww1.microchip.com/downloads/aemDocuments/documents/OTH/ProductDocuments/DataSheets/00001692C.pdf

1.1.4 RS232 Transceiver datasheet

https://www.ti.com/lit/ds/symlink/max3243.pdf

1.1.5 RS485 Transceiver datasheet

https://www.analog.com/media/en/technical-documentation/data-sheets/adm3483_3485_3488_3490_3491.pdf

1.1.6 Audio Codec datasheet

https://www.nuvoton.com/export/resource-files/DS_NAU88C22_DataSheet_EN_Rev1.1.pdf

1.1.7 USB Type-C Configuration Channel Logic IC datasheet

https://www.ti.com/lit/ds/symlink/tusb321ai.pdf

1.1.8 Two-Channel Differential MUX/DeMUX datasheet

https://www.ti.com/lit/ds/symlink/tmuxhs4212.pdf

1.1.9 DC/DC Converters datasheets

http://www.aosmd.com/res/data_sheets/AOZ2261AQI-15.pdf

https://www.mornsun-power.com/public/uploads/pdf/B_XT-1WR2.pdf

1.1.10 EEPROM Datasheet

https://www.st.com/resource/en/datasheet/m24c02-w.pdf

1.1.11 Digital Temperature Sensor Datasheet

https://www.st.com/resource/en/datasheet/m24c02-w.pdf

1.1.12 Isolated CAN Transceiver datasheet

https://www.ti.com/lit/ds/symlink/iso1042.pdf

1.1.13 USB to Multipurpose UART/MPSSE datasheet

https://ftdichip.com/wp-content/uploads/2020/08/DS_FT4232H.pdf

1.1.14 RTC datasheet

https://www.st.com/resource/en/datasheet/m41t0.pdf

1.1.15 Bidirectional Current/Power Monitor datasheet

https://www.ti.com/lit/ds/symlink/ina219.pdf

1.1.16 Level Translating I^2C-bus Repeater datasheet

https://www.nxp.com/docs/en/data-sheet/PCA9617A.pdf

1.1.17 Apalis System on Module Carrier Board Design Guide

https://docs.toradex.com/101123-apalis-arm-carrier-board-design-guide.pdf

1.1.18 Toradex Developer Website - Carrier Board Design

https://developer.toradex.com/carrier-board-design

1.2 Abbreviations

Table 1: Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card

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Table 1: Abbreviations (Continued)

Abbreviation	Explanation
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

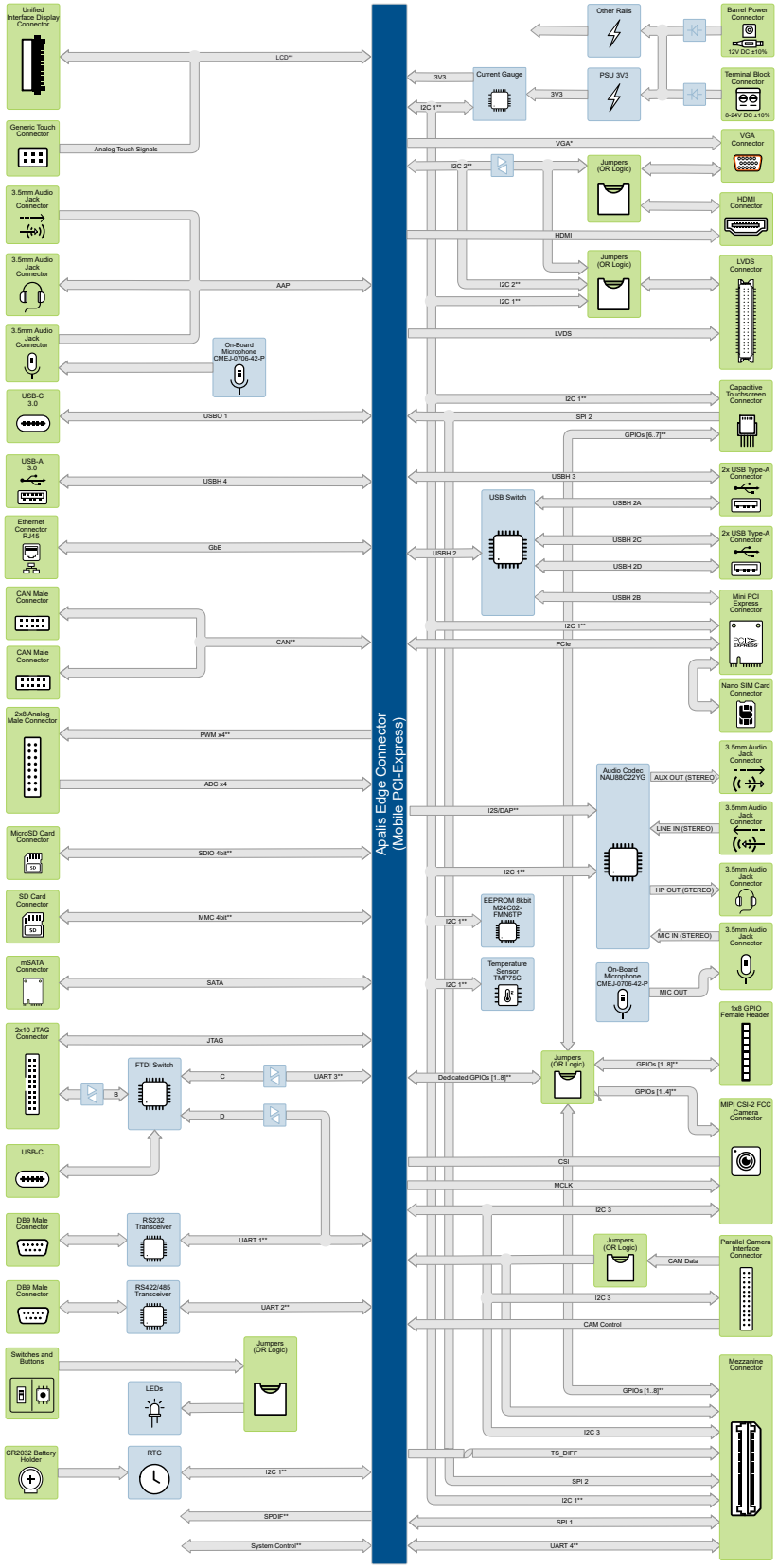
1.3 Main Features

The Apalis Evaluation Board provides the following features and communication interfaces:

- 4x USB Type-A connector providing USB 2.0 host functionality (3x through a USB Hub and 1x directly connected)
- 1x USB Type-A connector providing USB 3.0 host functionality
- 1x USB-C connector providing USB 3.x Dual-Role-Port (DRP) or host/client functionality
- 1x USB-C debug connector (optionally connected to UART3, UART1, and JTAG through the multi-purpose USB to serial converter based on the FT4232HL IC)
- 1x RJ45 connector featuring 10/100/1000 Mbps Ethernet interface
- 1x SD® Card connector featuring 4-Bit SD/MMC interface
- 1x MicroSD Card connector featuring 4-Bit SD interface
- 1x mSATA connector
- 1x Mini PCIe connector
- 1x "Type-Specific" Mezzanine Board Connector featuring module dependent interfaces
- 1x HDMI 2.0 connector featuring a digital (TDMS) interface
- 1x 15-pins D-Sub connector featuring Analog VGA interface
- 1x Dual-channel LVDS interface connector (up to 24-bit color)
- 1x Unified Display Connector featuring Digital RGB interface (up to 24-bit color) with built-in resistive touch input signals for direct LCD panel connection
- 1x Resistive touch screen 6-pin header (4/5-wire)
- 1x Capacitive Touchscreen interface connector
- 3x 3.5 mm stereo jacks to access the analog audio codec placed on the SoM (LINE IN, MIC IN, HEADPHONE OUT)
- 4x 3.5 mm stereo jacks to access the analog audio codec placed on the board (AUX IN, AUX OUT, MIC IN, HEADPHONES OUT)
- 1x 2-pin spring connector to access the SPEAKER OUT of the onboard's analog audio codec
- 1x S/PDIF In/Out digital audio interface exposed on a jumper array
- 1x 9-pin D-Sub connector featuring RS232 Serial Interface
- 1x 9-pin D-Sub connector featuring RS422/485 Serial Interface
- 3x I^2C, 2x SPI, 4x PWM, 4x Analog inputs, 4x PWM RC-filtered analog outputs
- 2x 10-pin CAN interface headers both supporting regular CAN (up to 1Mbps) and CAN FD (up to 5Mbps)
- 1x Real-time clock with battery backup
- 4x general-purpose switches and 4x general-purpose pushbuttons
- 8x general-purpose LEDs
- 3x Extremely Flexible and easy to use GPIO breakout and jumper arrays allowing easy signal re-routing, external connection, and measurement/probing
- 1x 20-pin JTAG connector
- 1x MIPI® CSI Camera Interface connector
- 1x Parallel Camera Interface connector
- 2x Electret microphones (1x connected to the SoM's audio codec, 1x-to the onboard audio)
- 1x SoM's Current/Power Monitor connected to the general-purpose I^2C bus.

1.4 Block Diagram

Figure 1: Apalis Evaluation Board Block Diagram



1.5 Physical Drawing

1.5.1 Top Side Connectors

Figure 2: Apalis Evaluation Board top side connectors and controls

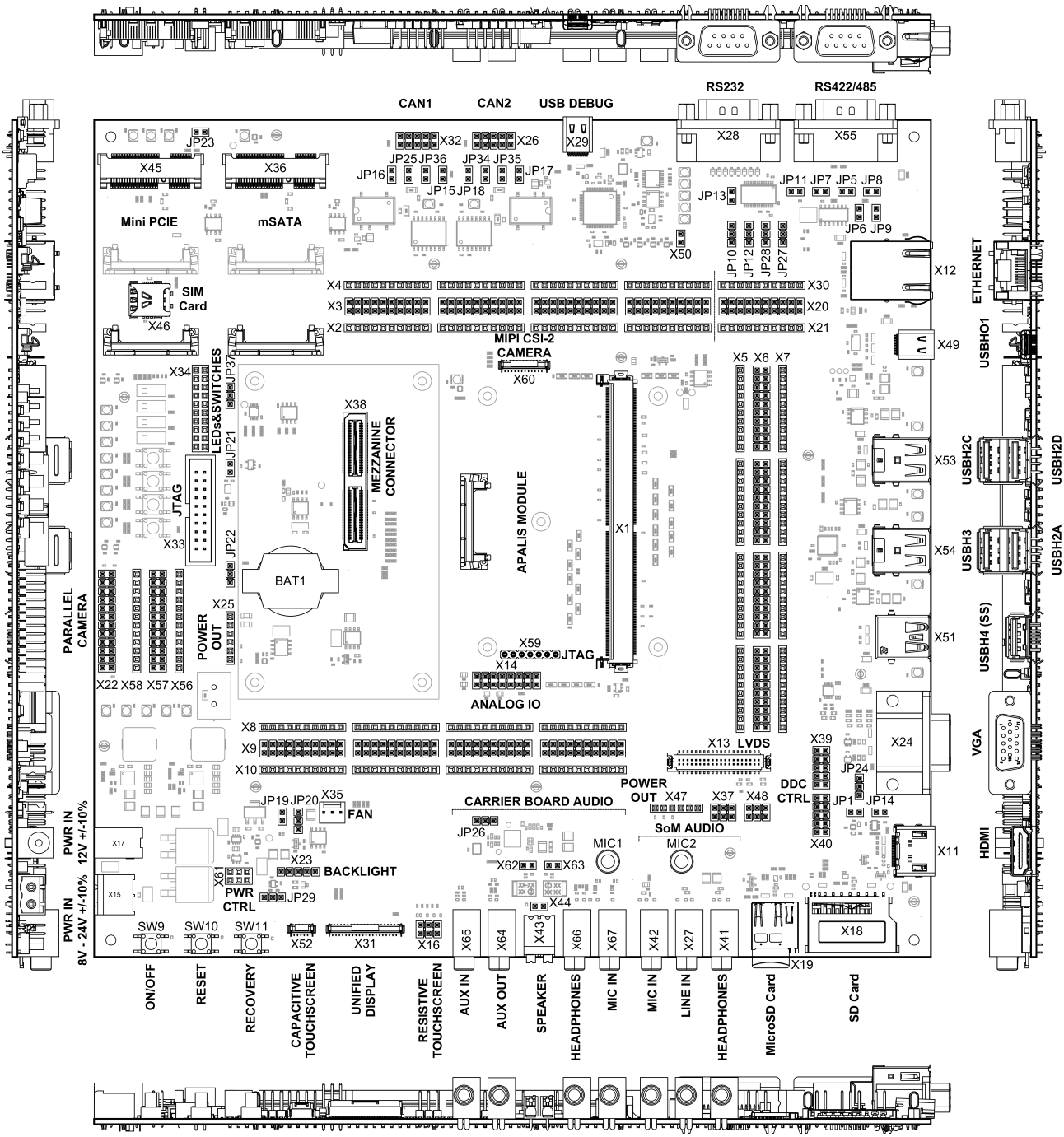


Table 2: Top Side Connectors

Designator	Description	Remarks
X1	Apalis MXM3 connector	
X2	MXM3 breakout area 1	
X3	Jumper Array 1	
X4	Function Tap 1	
X5	MXM3 breakout area 2	
X6	Jumper Array 2	
X7	Function Tap 2	
X8	MXM3 breakout area 3	
X9	Jumper Array 3	
X10	Function Tap 3	
X11	HDMI connector	
X12	Gigabit Ethernet connector	
X13	LVDS connector	
X14	Analog I/O connector	
X15	Power Supply connector	Power Input: 8 – 24V ±10%
X16	Resistive Touch-Screen connector	
X17	Power Supply connector	Power Input: 12V ±10%
X18	SD Card connector	
X19	MicroSD Card connector	
X20	FTDI Jumper Array	
X21	FTDI Function Tap	
X22	Parallel Camera connector	
X23	LCD Inverter connector	
X24	VGA connector	
X25	Power Out connector	
X26	CAN2 connector	
X27	LINE IN connector	SoM's Analog Audio Codec line input
X28	RS232 connector	
X29	USB Debugger connector	USB-C connector (USB 2.0 only)
X30	FTDI Function Tap	
X31	Unified Display connector	
X32	CAN1 connector	
X33	JTAG to Host connector	
X34	Switches/LEDs connector	
X35	FAN connector	
X36	mSATA connector	
X37	LVDS Display configuration jumper array	
X38	*"Type-specific" Mezzanine Board connector*	

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Table 2: Top Side Connectors (Continued)

Designator	Description	Remarks
X39	DDC SCL Interface Selection jumper array	
X40	DDC SDA Interface Selection jumper array	
X41	HEADPHONE OUT connector	SoM's Analog Audio Codec headphones' output
X42	MIC IN connector	SoM's Analog Audio Codec microphone's input
X43	SPEAKER OUT connector	Onboard Audio Codecs speaker output
X44	SPEAKER OUT connector	Onboard Audio Codecs speaker output
X45	Mini PCIe connector	
X46	SIM Card connector	Nano SIM
X47	Power supply output connector	
X48	LVDS Display configuration jumper array	
X49	USB DRP connector	USB-C with USB 3.x interface support
X50	UART3 CTS/RTS connector	
X51	USB HOST connector	Type-A. USBH4 with USB 3.x interface support
X52	Capacitive Touchscreen connector	
X53	2x USB HOST connector	Type-A. TOP: USBH2C – BOTTOM: USBH2D
X54	2x USB HOST connector	Type-A. TOP: USBH3 – BOTTOM: USBH2A
X55	RS422/485 connector	9-pin D-Sub
X56	Camera MXM3 Breakout Area	Some of these pins are routed through the Mezzanine Connector
X57	Camera Jumper Array	
X58	Camera Function Tap	Connected to X22
X59	JTAG to Apalis SoM connector	POGO pins
X60	MIPI CSI Camera connector	
X61	Power Control connector	
X62	SPEAKER OUT RIGHT connector	
X63	SPEAKER OUT LEFT connector	

2 Interface Description

2.1 Apalis System-On-Module

Connector Type: MXM3 321 pin Socket

Manufacturer: JAE, MM70-314B1-2

For the pin-out of the Apalis module, please refer to the applicable Apalis datasheet.

MXM3 Snap Lock and Spacers are available on Apalis Evaluation Board for securing the Apalis module to the carrier board. It is recommended to use M3-size screws to fasten the Apalis module to the spacers.

2.2 Power Supply

The Apalis Evaluation Board has two different power connectors that can be used to power the board:

- The connector X15 has a wide input voltage range of 8-24V ±10% DC.
- The connector X17 is a 12V ±10% input. It must be used when the 12V supply is required on the board (e.g., while using a cooling fan or it is needed on the LVDS connector). The 12V power supply is obtained directly from the connector X17, even though a 2A fuse protects this voltage, it is not regulated.

The on-board DC-DC converters provide the following supplies (maximum power):

- 5V / 8A (40W)
- 3.3V / 8A (26.4W)

The supply is protected against reverse input voltage polarity and short circuits, limiting the maximum current to about 8A. However, the protection diode in the input voltage path is thermally not designed to carry such a high current, especially at low input voltages. If your application requires more than 20W, please consider one of the following:

- Work with a high input voltage, close to the maximum of 24V
- Add a heat-sink to the polarity protection diode
- Short the polarity protection diode with a wire, **removing the reverse polarity protection**

Two power supply output connectors, X25 and X47, are available for powering some additional peripheral devices connected to the board.

2.2.1 Power Supply Input Connector (X15)

Connector type: Terminal Block, AUK TB5102PRB-H

Table 3: Power Supply Input Connector (X15)

Pin	Signal Name	Voltage / Range
1	GND_IN	
2	PWR_IN	8-24V ±10%

2.2.2 Power Supply Input Connector (X17)

Connector type: Barrel Jack, Switchcraft RAPC722X

Table 4: Power Supply Input Connector (X15)

Pin	Signal Name	Voltage / Range
1	12V_IN	12V ±10%
2	GND_IN	

2.2.3 Power Supply Output Connector (X25)

Connector type: 1×6Pin Header Female, 2.54mm

Table 5: Power Supply Output Connector (X25)

Pin	Signal Name	Remarks
1	3.3V_SW	
2	GND	
3	5V_SW	
4	GND	
5	12V_SW_UNREG_F	2A FUSE
6	V_SUPPLY_FILT_F	2A FUSE

Pins 5 and 6 are not regulated because they are directly connected to the power supply connectors X15 and X17.

2.2.4 Power Supply Output Connector (X47)

Connector type: 1×6Pin Header Female, 2.54mm

Table 6: Power Supply Output Connector (X47)

Pin	Signal Name	Remarks
1	3.3V_SW	
2	3.3V_SW	
3	3.3V_SW	
4	GND	
5	GND	
6	GND	

2.2.5 Current/Power Monitor

Current and power monitoring for the Apalis modules is available on the Evaluation Board. Current and voltage sensing is done by IC14 (INA219), which measures the voltage drop on the current-shunt resistor R165. IC14 is accessible on the I2C1 serial bus at address `0x40`. Please check the INA219 datasheet for details.

2.2.6 Power Control

Power control of the Apalis Evaluation Board is implemented using the Linear LTC2954 Pushbutton On/Off controller (IC17). The signal POWER_ENABLE_MOCI is used to enable the peripheral power supplies.

Please refer to the respective datasheet for further information about the signals provided by the push-button controller. Please refer to the document Apalis System on Module Carrier Board Design Guide for more information regarding the power-up sequence implemented on the board.

The Power CTRL Connector (X61) allows the Reset and Power Button control signals to be accessed externally.

2.2.6.1 Power Control Connector (X61)

Connector type: 2×3Pin Header Female, 2.54mm

Table 7: Power Control Connector (X61)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	PWR_BTN#	I/O (OD)	+1.9V	100k to +1.9V	It is connected to the POWER BUTTON SW9. Pulled up to 1.9V inside push-button controller IC17. Short pulling down turning on Development Board power and Computer Module. Long pulling down forcing the Evaluation Board power off.
2	GND	PWR			
3	PWR_CTRL	I	+3.3V	100k to GND	Behaviour is similar to the "Always-ON" Jumper JP19. HIGH level on the PWR_CTRL input forcing on the Apalis Evaluation Board power.
4	INT#	O (OD)	+1.8V	10k to 3.3V	Open-drain interrupt output from the push-button controller IC17. The signal can be left floating on carrier boards.
5	FORCE_OFF#	I/O (OD)	+3.3V	100k to 3.3V	Forcing the turning-off of the main power rail. This signal is ignored during the power-up sequence or when the Apalis module is in the RESET state.
6	RESET_MICO#	I/O (OD)	+3.3V	on SoM	Open-drain input, which resets the module if shorted to ground. There is an on-module pull-up. This means it can be left floating on the carrier board.

Pin 3 of the connector X61 can be used to override the pushbutton controller. The following table shows the behaviour of the board according to the level of the PWR_CTRL signal:

Connector type: 1×2 Pin Header Male, 2.54 mm

Table 8: PWR_CTRL Signal Levels

PWR_CTRL Level	Description
0V	The Pushbutton controller is working normally
3.3V	The Apalis Evaluation Board is Always On when power is applied

The jumper JP19 can also be used to obtain always-on behavior.
Connector type: 1×2 Pin Header Male, 2.54 mm

Table 9: Always-On Jumper (JP19)

Jumper Position	Description
OPEN	The board power supply is controlled via the power On/Off button.
CLOSED	Board power supply will be in the "Always On" state. Apalis Evaluation Board will be powered-up as soon as external power is applied.

2.2.7 Fan

The Apalis Evaluation Board has one FAN connector (X35). The fan connector is supplied with 12V by the 12V unregulated power supply. The fan supply is controlled using a transistor that can be connected to the GPIO8 signal for software control. Jumper JP20 determines this configuration:

Connector type: 1×3 Pin Header Male, 2.54 mm, shrouded

Table 10: Fan Mode Jumper (JP20)

Jumper Position	Description
1 - 2	Automatic ON
2 - 3	Enabled by GPIO8

2.2.7.1 Fan Connector (X35)

Connector type: 1×3 Pin Header Male with friction lock, 2.54 mm

Table 11: Fan Connector (X35)

Pin	Signal Name	I/O Type	Voltage
1	GND	PWR	
2	V_FAN_UNREG	PWR	+12V ±10%
3	NC		

V_FAN_UNREG is not a regulated power supply. It will be the same voltage that is provided on the X17 connector. Use only 12V ±10% power supplies with connector X17.

2.3 Indicators

Figure 3: Apalis Evaluation Board indicator LEDs

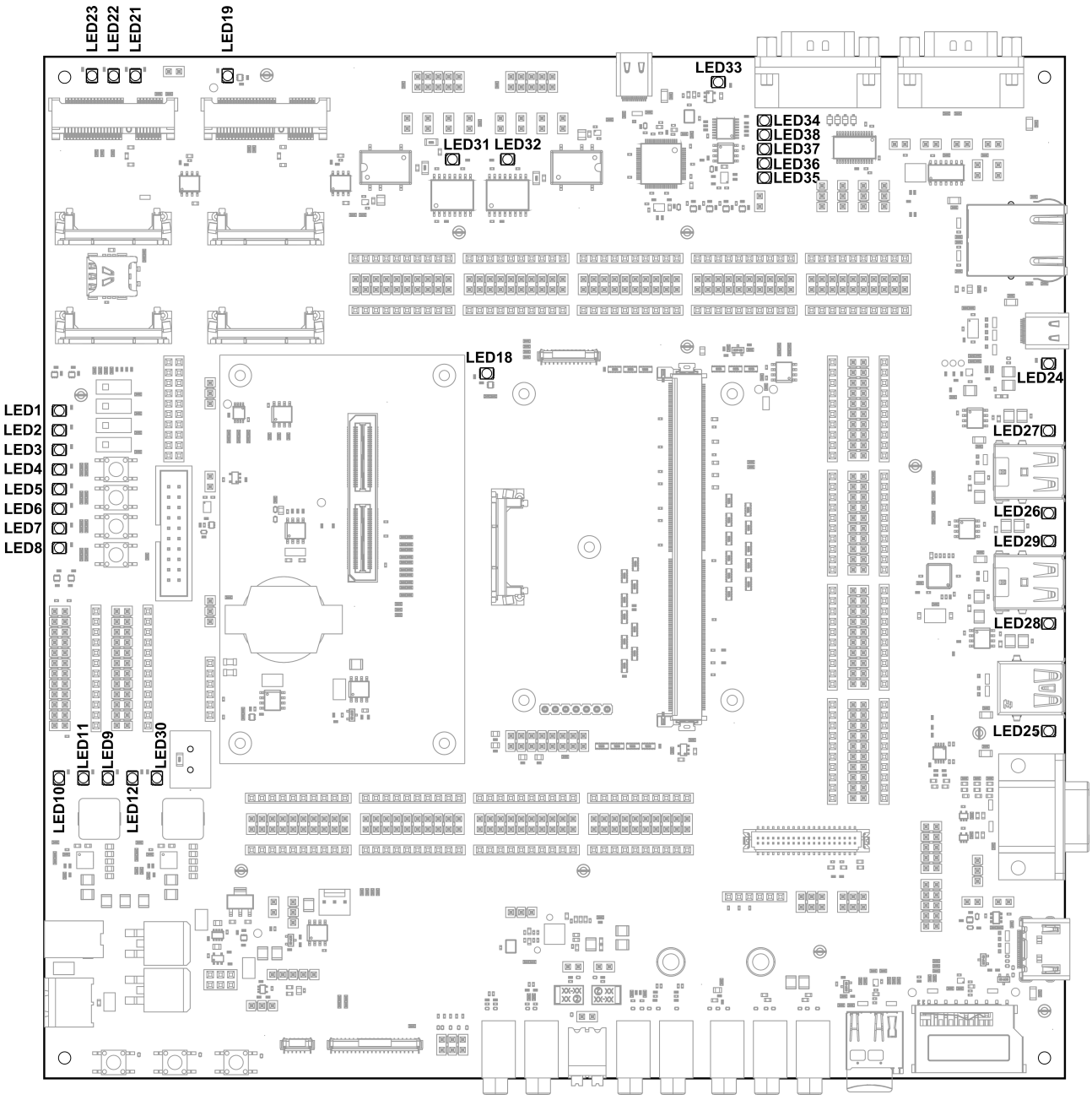

Table 12: Apalis Evaluation Board LED Indicators

Designator	Color	Description
LED1-8	Green	General-purpose LEDs. LED is on when a high logic level is applied to the respective X34 connector pin
LED9	Green	LED is on when 3.3V power is available
LED10	Green	LED is on when 5V_SW power is available
LED11	Green	LED is on when 3.3V_SW power is available

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Table 12: Apalis Evaluation Board LED Indicators (Continued)

Designator	Color	Description
LED12	Green	LED is on when VSTB (5V Development Board Standby) power is available
LED18	Red	LED is on when the Apalis Module and the board's peripherals are in reset state
LED19	Green	LED blinks when data is being transmitted on the SATA interface
LED21	Green	Mini PCIe status indicator: WWAN. (Indication depends on the installed card)
LED22	Green	Mini PCIe status indicator: WLAN. (Indication depends on the installed card)
LED23	Green	Mini PCIe status indicator: WPAN. (Indication depends on the installed card)
LED24	Green	LED is on when USBO1 DRP power is ON (Connector X49)
LED25	Green	LED is on when USBH4 Host power is ON (Connector X51)
LED26	Green	LED is on when USBH2C Host power is ON (Connector X53 UPPER)
LED27	Green	LED is on when USBH2D Host power is ON (Connector X53 LOWER)
LED28	Green	LED is on when USBH3 Host power is ON (Connector X54 UPPER)
LED29	Green	LED is on when USBH2A Host power is ON (Connector X54 LOWER)
LED30	Green	LED is on when 12V_SW_UNREG power is available
LED31	Green	LED is on when CAN1 transceiver power is ON
LED32	Green	LED is on when CAN2 transceiver power is ON
LED33	Green	LED is on when FTDI USB Debugger (IC41) power is available - USB Debugger connected to a PC
LED34	Yellow	LED when data is being transmitted on the FTDI USB Debugger interface
LED35	Yellow	LED when data is being transmitted on FTDI_UARTC_TX
LED36	Yellow	LED when data is being transmitted on FTDI_UARTC_RX
LED37	Yellow	LED when data is being transmitted on FTDI_UARTD_TX
LED38	Yellow	LED when data is being transmitted on FTDI_UARTD_RX

Refer to the Apalis Evaluation Board schematics for more details.

2.4 Ethernet

The Apalis Evaluation Board provides one RJ45 connector with integrated magnetics for 10/100/1000Mb Ethernet.

2.4.1 Ethernet Connector (X12)

Connector type: RJ45, LINK-PP LPJK7436A98NL

Table 13: Ethernet Connector (X11)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
1	ETH_1_CTREF_2				Integrated magnetics center tap 2
2	ETH_1_MDI2_N	34	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 2
3	ETH_1_MDI2_P	32	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 2
4	ETH_1_MDI1_P	56	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 1
5	ETH_1_MDI1_N	54	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 1

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Table 13: Ethernet Connector (X11) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
6	ETH_1_CTREF_1				Integrated magnetics center tap 1
7	ETH_1_CTREF_3				Integrated magnetics center tap 3
8	ETH_1_MDI3_P	38	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 3
9	ETH_1_MDI3_N	40	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 3
10	ETH_1_MDI0_N	48	I/O (Analog)		Negative differential Media Dependent Interface signal, lane 0
11	ETH_1_MDI0_P	50	I/O (Analog)		Positive differential Media Dependent Interface signal, lane 0
12	ETH_1_CTREF_0				Integrated magnetics center tap 0
13	ETH1_ACT_C	42 (via R5)	O (OD)		LED for indication of Ethernet activity
14	+V3.3_SW		PWR	+3.3V	Power supply for the indication LEDs
15	ETH1_LINK_GB	44 (via R293)	O (OD)		Not Connected
16	+V3.3_SW		PWR	+3.3V	Power supply for the indication LEDs
17	ETH1_LINK_C	44 (via R6)	O (OD)		LED for indication of established Ethernet link
S1/S2	GND_CHASSIS		PWR		

2.5 USB

2.5.1 USB Host/Client Interface

For the USB Host/Client interface, the Apalis Evaluation Board integrates a USB-C connector (X49). This connector is connected to the Apalis USBO1 port (USB2.0 + USB 3.x interface). This port is commonly used in recovery mode for loading new software to the module and can work as a dual-role-port (DRP).

The DRP behaviour is similar to the On-The-Go (OTG) functionality, but the term USB OTG is only used in conjunction with the USB Micro-AB or the obsolete USB Mini-AB receptacle. The ID pin is absent on the USB Type-C receptacle.

The determination of Host or Device functionality is handled differently in Type-C using the configuration channel (CC) pins. The CC pins perform the same functions that the ID pin previously served: indicate the role of equipment as host, device, or both. The CC pins are also used to detect if the connection is being made or was broken.

To handle all the operations required for the USB dual-role-port, the TUSB321AI IC has been used (IC26). It can function as an upstream-facing port (UFP), downstream-facing port (DFP), or a dual-role port (DRP) depending on pin configuration. The device handles all aspects of the USB Type-C connection process to determine the port role. When connected as a peripheral (UFP), the TUSB321AI indicates the VBUS current provided by the attached host through general-purpose input/output (GPIO) pins. When connected as a host (DFP), it advertises the VBUS current to the attached peripheral. For the details, please check the TUSB321AI datasheet.

A high-speed signal differential switch (IC25) is used to swap the USB SS signals on the USB-C connector according to USB-C cable orientation. The TUSB321AI IC controls this high-speed signal switch.

On the Evaluation Board, this port is configured as a dual-role port (DRP) by default, and its output current is limited to 1A.

Port configuration can be changed with the resistors R230 – R233. For the details please check the TUSB321AI datasheet.

The Apalis Evaluation Board cannot be powered through the USB-C connector X49.

2.5.1.1 USB DRP Connector (X49)

Connector type: USB-C, Stewart SS-52400-003

Table 14: USB DRP Connector (X49)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
A1	GND		PWR		
A2	USBO1_SSTX1_CON_P	68 (via IC25)	O		Positive differential USB 3.x transmit signal
A3	USBO1_SSTX1_CON_N	70 (via IC25)	O		Negative differential USB 3.x transmit signal
A4	VCC_USBO1		PWR	+5V	+5V USB power supply output
A5	USBO1_CC1_CON				Type-C configuration channel signal 1
A6	USBO1_D_CON_P	74	I/O		Positive differential USB 2.0 Signal
A7	USBO1_D_CON_N	76	I/O		Negative differential USB 2.0 Signal
A8	NC				Not Connected
A9	VCC_USBO1		PWR	+5V	+5V USB power supply output
A10	USBO1_SSRX2_CON_N	64 (via IC25)	I		Negative differential USB 3.x receive signal
A11	USBO1_SSRX2_CON_P	62 (via IC25)	I		Positive differential USB 3.x receive signal
A12	GND				
B1	GND		PWR		
B2	USBO1_SSTX2_CON_P	68 (via IC25)	O		Positive differential USB 3.x transmit signal
B3	USBO1_SSTX2_CON_N	70 (via IC25)	O		Negative differential USB 3.x transmit signal
B4	VCC_USBO1		PWR	+5V	+5V USB power supply output
B5	USBO1_CC2_CON				Type-C configuration channel signal 1
B6	USBO1_D_CON_P	74	I/O		Positive differential USB 2.0 Signal
B7	USBO1_D_CON_N	76	I/O		Negative differential USB 2.0 Signal
B8	NC				Not Connected
B9	VCC_USBO1		PWR	+5V	+5V USB power supply output
B10	USBO1_SSRX1_CON_N	64 (via IC25)	I		Negative differential USB 3.x receive signal
B11	USBO1_SSRX1_CON_P	62 (via IC25)	I		Positive differential USB 3.x receive signal
B12	GND		PWR		
MP1	GND		PWR		
MP2	GND		PWR		
S1/S2	GND_CHASSIS				
S3/S4	GND_CHASSIS				
S5/S6	GND_CHASSIS				

2.5.2 USB Host Interface

The Apalis Evaluation Board integrates a four-port USB Hub (SMSC USB2514B-AEZC) to provide four USB 2.0 host interfaces. For further information about the USB Hub, please refer to the datasheet.

In addition, the Apalis Evaluation Board features one USB 3.0 Type-A port (X51) which can be used with modules that support the USB Super Speed interface.

2.5.2.1 2x USB Host connector (X53)

Connector type: Stacked USB 2.0 Type-A, Stewart SS-52100-003

Table 15: 2x USB Host connector (X53)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
U1	VCC_USBH2C		PWR	+5V	+5V USB power supply output
U2	USBH2C_D_CON_N		I/O		Negative differential USB 2.0 signal
U3	USBH2C_D_CON_P		I/O		Positive differential USB 2.0 signal
U4	GND		PWR		
L1	VCC_USBH2D		PWR	+5V	+5V USB power supply output
L2	USBH2D_D_CON_N		I/O		Negative differential USB 2.0 signal
L3	USBH2D_D_CON_P		I/O		Positive differential USB 2.0 signal
L4	GND		PWR		
S1/S2	GND_CHASSIS		PWR		
S3/S4	GND_CHASSIS		PWR		

2.5.2.2 2x USB Host connector (X54)

Connector type: Stacked USB 2.0 Type-A, Stewart SS-52100-003

Table 16: 2x USB Host connector (X54)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
U1	VCC_USBH3		PWR	+5V	+5V USB power supply output
U2	USBH3_D_CON_N	88	I/O		Negative differential USB 2.0 signal
U3	USBH3_D_CON_P	86	I/O		Positive differential USB 2.0 signal
U4	GND		PWR		
L1	VCC_USBH2A		PWR	+5V	+5V USB power supply output
L2	USBH2A_D_CON_N		I/O		Negative differential USB 2.0 signal
L3	USBH2A_D_CON_P		I/O		Positive differential USB 2.0 signal
L4	GND		PWR		
S1/S2	GND_CHASSIS		PWR		
S3/S4	GND_CHASSIS		PWR		

2.5.2.3 2x USB Host connector (X51)

Connector type: USB 3.0 Type-A, Stewart SS-52000-001

Table 17: USB Host connector (X51)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
1	VCC_USBH4		PWR	+5V	+5V USB power supply output
2	USBH4_D_CON_N	100	I/O		Negative differential USB 2.0 signal
3	USBH4_D_CON_P	98	I/O		Positive differential USB 2.0 signal
4	GND		PWR		
5	USBH4_SSRX_CON_N	92	I		Negative differential USB 3.x receive signal
6	USBH4_SSRX_CON_P	94	I		Positive differential USB 3.x receive signal
7	GND		PWR		
8	USBH4_SSTX_CON_N	104	O		Negative differential USB 3.x transmit signal
9	USBH4_SSTX_CON_P	106	O		Positive differential USB 3.x transmit signal
S1/S2	GND_CHASSIS		PWR		

2.6 PCIe

The Apalis Evaluation Board makes the standard PCIe interface on the Apalis SoMs available through a Mini PCIe slot. Mini PCI Express edge connectors provide multiple connections and buses, such as listed below:

- PCI Express 1 lane (with SMBus)
- USB 2.0
- Indication LEDs for wireless network status
- SIM card for cellular applications (UIM signals)

2.6.1 Mini PCIe connector (X45)

Connector type: Mini PCIe Card, TE Connectivity 1775838-2 and Latch Molex 48099-5701

Table 18: Mini PCIe connector(X45)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	PCIE1_WAKE#	37 (via R267)	O (OD)	+3.3V	5.1k to 3.3V	Wake-up to SoM
3	NC					
5	NC					Not connected
7	NC					
9	GND		PWR			
11	PCIE1_CLK_N	53	O			Negative differential PCIe reference clock signal
13	PCIE1_CLK_P	55	O			Positive differential PCIe reference clock signal
15	GND		PWR			
17	NC					Not connected
19	NC					

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Table 18: Mini PCIe connector(X45) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
21	GND		PWR			
23	PCIE1_RX_N	41	I			Negative differential PCIe receive signal
25	PCIE1_RX_P	43	I			Positive differential PCIe receive signal
27	GND		PWR			
29	GND		PWR			
31	PCIE1_TX_N	47	O			Negative differential PCIe transmit signal
33	PCIE1_TX_P	49	O			Positive differential PCIe transmit signal
35	GND		PWR			
37	GND		PWR			
39	3.3V_PCIE1		PWR	+3.3V		+3.3V Power supply output
41	3.3V_PCIE1		PWR	+3.3V		
43	GND					
45	NC					Not connected
47	NC					
49	NC					
51	NC					
2	3.3V_PCIE1		PWR	+3.3V		+3.3V Power supply output
4	GND		PWR			
6	1.5V_PCIE1		PWR	+1.5V		+1.5V Power supply output
8	PCIE1_UIM_PWR		PWR			SIM Card Power
10	PCIE1_UIM_DATA		I/O			SIM Card Data
12	PCIE1_UIM_CLK		I			SIM Card Clock
14	PCIE1_UIM_RESET		I			SIM Card RESET
16	PCIE1_UIM_VPP		PWR			SIM Card Programming voltage
18	GND		PWR			
20	PCIE1_WDISABLE#	JP23	O (OD)	+3.3V	47k to 3.3V_PCIE1	PCIe Wireless interface disable
22	PCIE1_RESET#	26 (via R310)	O (OD)	+3.3V	10k to 3.3V_PCIE1	PCIe Power enable/RESET
24	3.3V_PCIE1		PWR	+3.3V		+3.3V Standby Power supply output
26	GND		PWR			
28	1.5V_PCIE1		PWR	+1.5V		+1.5V Power supply output
30	PCIE1_SMCLK	211 (via R265)	I/O	+3.3V	10k to 3.3V_PCIE1	PCIe SMBus Clock (**Not connected**)
32	PCIE1_SMDAT	209 (via R266)	I/O	+3.3V	10k to 3.3V_PCIE1	PCIe SMBus Data (**Not connected**)
34	GND		PWR			
36	USBH2B_D_N		I/O			Negative differential USB 2.0 data signal
38	USBH2B_D_P		I/O			Positive differential USB 2.0 data signal
40	GND		PWR			
42	PCIE1_WWAN#		I (OD)			WWAN LED
44	PCIE1_WLAN#		I (OD)			WLAN LED

Continued on next page

Table 18: Mini PCIe connector(X45) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
46	PCIE1_WPAN#		I (OD)			WPAN LED
48	1.5V_PCIE1		PWR	+1.5V		+1.5V Power supply output
50	GND		PWR			
52	3.3V_PCIE1		PWR	+3.3V		+3.3V Power supply output

2.6.2 Nano-SIM Connector (X46)

Connector type: Nano SIM, Molex 1042240820

Table 19: Nano-SIM Connector (X46)

Pin	Signal Name	I/O Type	Description
S1	PCIE_1_UIM_PWR	PWR	SIM Card Power
S2	PCIE_1_UIM_RESET	O	SIM Card RESET
S3	PCIE_1_UIM_CLK	O	SIM Card Clock
S4	GND	PWR	
S5	PCIE1_UIM_VPP	PWR	SIM Card Programming voltage
S6	PCIE_1_UIM_DATA	I/O	SIM Card Data
G1/G2	GND	PWR	
G3/G4	GND	PWR	

2.7 SATA

The Apalis Evaluation Board supports the Serial ATA (SATA) interface on the Apalis module and allows peripherals such as mSATA SSDs to be used.

For further information regarding the mSATA interface, please refer to Serial ATA Specification Rev. 3.1 Gold.

2.7.1 mSATA connector (X36)

Connector type: Mini PCIe Card, TE Connectivity 1775838-2 and Latch Molex 48099-5701

Table 20: mSATA connector (X36)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	NC					Not connected
3	NC					
5	NC					
7	NC					
9	GND		PWR			
11	NC					Not connected
13	NC					

Continued on next page

Table 20: mSATA connector (X36) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
15	GND		PWR			
17	NC					Not connected
19	NC					Not connected
21	GND		PWR			
23	SATA1_RX_P	25	I			Positiove differential SATA receive signal
25	SATA1_RX_N	27	I			Negative differential SATA receive signal
27	GND		PWR			
29	GND		PWR			
31	SATA1_TX_N	47	O			Negative differential SATA transmit signal
33	SATA1_TX_P	49	O			Positive differential SATA transmit signal
35	GND		PWR			
37	GND		PWR			
39	3.3V_mSATA1		PWR	+3.3V		+3.3V Power supply output
41	3.3V_mSATA1		PWR	+3.3V		
43	NC					Not connected
45	NC					
47	NC					
49	SATA1_mSATA_ACT#		O	+3.3V	100K to 3.3V_SW	Drive activity LED
51	SATA1_mSATA_PREDET#	(TP35)	O			mSATA drive presence detection
2	3.3V_mSATA1		PWR	+3.3V		+3.3V Power supply output
4	GND		PWR			
6	1.5V_mSATA1		PWR	+1.5V		+1.5V Power supply output
8	NC					Not connected
10	NC					
12	NC					
14	NC					
16	NC					
18	GND		PWR			
20	NC					Not connected
22	NC					
24	3.3V_mSATA1		PWR	+3.3V		+3.3V Power supply output
26	GND		PWR			
28	1.5V_mSATA1		PWR	+1.5V		+1.5V Power supply output
30	SATA1_mSATA_SCL	211 (via R159)	I/O	+3.3V	10k to 3.3V_PCIE1	SATA SMBus Clock (**Not connected**)
32	SATA1_mSATA_SDA	209 (via R160)	I/O	+3.3V	10k to 3.3V_PCIE1	SATA SMBus Data (**Not connected**)
34	GND		PWR			
36	NC					Not connected
38	NC					

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Table 20: mSATA connector (X36) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
40	GND		PWR			
42	NC					Not connected
44	NC					Not connected
46	NC					
48	1.5V_mSATA1		PWR	+1.5V		+1.5V Power supply output
50	GND		PWR			
52	3.3V_mSATA1		PWR	+3.3V		+3.3V Power supply output

2.8 SD Card

The Apalis Evaluation Board features one 4-bit MMC/SDIO and another 4-bit SDIO interface. The hardware-supported card detect function is implemented. It is possible to read the write-protect status by using a test point present on the PCB.

The Apalis family modules support SD Card Low Voltage Signalling mode. Therefore, if the SD card itself also supports this mode, communication will start at 3.3V and switch to 1.8V after the card has been initialized.

2.8.1 SD Card Connector (X18)

Connector type: SD/MMC Card Holder, Wurth 693063020911

Table 21: SD Card Connector (X18)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	MMC1_D3	146	I/O	+1.8V/+3.3V	Pull-up on SoM	Serial Data 3
2	MMC1_CMD	150	O	+1.8V/+3.3V	Pull-up on SoM	Command
3	GND		PWR			
4	3.3V_MMC		PWR	+3.3V		SD Card power input
5	MMC1_CLK	154	O	+1.8V/+3.3V		Serial Clock
6	GND		PWR			
7	MMC1_D0	160	I/O	+1.8V/+3.3V	Pull-up on SoM	Serial Data 0
8	MMC1_D1	162	I/O	+1.8V/+3.3V	Pull-up on SoM	Serial Data 1
9	MMC1_D2	144	I/O	+1.8V/+3.3V	Pull-up on SoM	Serial Data 2
10	MMC1_CD#	164	I	+3.3V	10k to 3.3V_SW	Card Detect
11	WP	(TP14)	I			Write Protection
S1/S2	GND		PWR			
S3/S4	GND		PWR			

The MMC1_PWR_CTRL (MXM3_148) signal allows powering ON and OFF the SD Card power supply (+3.3V_MMC).

2.8.2 MicroSD Card Connector (X19)

Connector type: MicroSD/MMC, Wurth 693071010811

Table 22: MicroSD Card connector (X19)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	SD1_D2	176	I/O	+1.8V/+3.3V		Serial Data 2
2	SD1_D3	178	I/O	+1.8V/+3.3V		Serial Data 3
3	SD1_CMD	180	O	+1.8V/+3.3V		Command
4	3.3V_SD		PWR	+3.3V		SD Card power input
5	SD1_CLK	184	O	+1.8V/+3.3V		Serial Clock
6	GND		PWR			
7	SD1_D0	186	I/O	+1.8V/+3.3V		Serial Data 0
8	SD1_D1	188	I/O	+1.8V/+3.3V		Serial Data 1
9	GND		PWR			
10A			I	+3.3V	10k to 3.3V_SW	Card Detect
10B			I	+3.3V		

The SD1_PWR_CTRL (MXM3_152) signal allows powering ON and OFF the MicroSD Card power supply (+3.3V_SD).

2.9 Display Interface

The Apalis Evaluation Board provides many options for connecting LCD displays and monitors, with the following four interfaces supported:

- 24-bit digital RGB
- Dual Channel LVDS
- HDMI
- VGA

2.9.1 HDMI Connector (X11)

Connector type: HDMI 2.0, Molex 2086581051

Table 23: HDMI connector (X11)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	HDMI1_TXD2_CON_P	222	O			Positive differential HDMI/DVI signal, lane 2
2	GND		PWR			
3	HDMI1_TXD2_CON_N	224	O			Negative differential HDMI/DVI signal, lane 2
4	HDMI1_TXD1_CON_P	228	O			Positive differential HDMI/DVI signal, lane 1
5	GND		PWR			
6	HDMI1_TXD1_CON_N	230	O			Negative differential HDMI/DVI signal, lane 1
7	HDMI1_TXD0_CON_P	234	O			Positive differential HDMI/DVI signal, lane 0

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Table 23: HDMI connector (X11) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
8	GND		PWR			
9	HDMI1_TXD0_CON_N	236	O			Negative differential HDMI/DVI signal, lane 0
10	HDMI1_TXC_CON_P	240	O			Positive differential HDMI/DVI clock signal
11	GND					
12	HDMI1_TXC_CON_N	242	O			Negative differential HDMI/DVI clock signal
13	HDMI1_CEC_CON	220	I/O	+3.3V	27k to 3.3V_SW	HDMI Consumer Electronic Control
14	HDMI1_HEC_CON	(TP16)				
15	I2C2_DDC_SCL_HDMI[1]		I/O	+5V	1.8k to V_DISP	DDC Interface Clock
16	I2C2_DDC_SDA_HDMI[1]		I/O	+5V	1.8k to V_DISP	DDC Interface Data
17	GND		PWR			
18	V_DISP		PWR	+5V		+5V DDC Power supply output
19	HDMI1_HPD_CON	232	I	+5V	100k to GND	Hot Plug Detect signal input
S1/S2	GND_CHASSIS		PWR			
S3/S4	GND_CHASSIS		PWR			

[1] For more information, see the Extended Display Identification Data (EDID) section.

2.9.2 LVDS Display Connector (X13)

The Apalis Evaluation Board LVDS interface can be used with the Toradex Capacitive Touch Display 10.1" LVDS.

Connector type: HDMI 2.0, Molex 2086581051

Table 24: LVDS Display Connector (X13)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
1	LVDS1_A_TX3_P	272	O		Positive differential LVDS signal, channel A, lane 3
3	LVDS1_A_TX3_N	270	O		Negative differential LVDS signal, channel A, lane 3
5	GND		PWR		
7	LVDS1_A_TX2_P	266	O		Positive differential LVDS signal, channel A, lane 2
9	LVDS1_A_TX2_N	264	O		Negative differential LVDS signal, channel A, lane 2
11	GND		PWR		
13	LVDS1_A_TX1_P	260	O		Positive differential LVDS signal, channel A, lane 1
15	LVDS1_A_TX1_N	258	O		Negative differential LVDS signal, channel A, lane 1
17	GND		PWR		
19	LVDS1_A_TX0_P	254	O		Positive differential LVDS signal, channel A, lane 0
21	LVDS1_A_TX0_N	252	O		Negative differential LVDS signal, channel A, lane 0
23	GND		PWR		
25	LVDS1_A_CLK_P	248	O		Positive differential LVDS clock signal, channel A
27	LVDS1_A_CLK_N	246	O		Negative differential LVDS clock signal, channel A

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Table 24: LVDS Display Connector (X13) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
29	GND		PWR		
31	LVDS1_SEL_1		O		Reserved LVDS display configuration pin
33	LVDS1_SEL_2		O		
35	PWM_BKL1	239	O		Display brightness control output
37	BKL1_ON	286	O		Display backlight ENABLE output
39	LVDS1_12V_SW_UNREG		PWR	+12V ±10%	Display backlight power supply output
2	GND		PWR		
4	LVDS1_B_CLK_N	276	O		Negative differential LVDS clock signal, channel B
6	LVDS1_B_CLK_P	278	O		Positive differential LVDS clock signal, channel B
8	GND		PWR		
10	LVDS1_B_TX0_N	282	O		Negative differential LVDS signal, channel B, lane 0
12	LVDS1_B_TX0_P	284	O		Positive differential LVDS signal, channel B, lane 0
14	GND		PWR		
16	LVDS1_B_TX1_N	288	O		Negative differential LVDS signal, channel B, lane 1
18	LVDS1_B_TX1_P	290	O		Positive differential LVDS signal, channel B, lane 1
20	GND		PWR		
22	LVDS1_B_TX2_N	294	O		Negative differential LVDS signal, channel B, lane 2
24	LVDS1_B_TX2_P	296	O		Positive differential LVDS signal, channel B, lane 2
26	GND		PWR		
28	LVDS1_B_TX3_N	300	O		Negative differential LVDS signal, channel B, lane 3
30	LVDS1_B_TX3_P	302	O		Positive differential LVDS signal, channel B, lane 3
32	LVDS1_3.3V_SW		PWR	+3.3V	LVDS display power supply output
34	LVDS1_5V_SW		PWR	+5V	LVDS display power supply output
36	I2C2_DDC_SDA_LVDS[1]		I/O	+3.3V/+5V	LVDS display configuration I^2C bus data signal
38	I2C2_DDC_SCL_LVDS[1]		I/O	+3.3V/+5V	LVDS display configuration I^2C bus clock signal
40	LVDS1_12V_SW_UNREG		PWR	+12V ±10%	Display backlight power supply output

[1] For more information, see the Extended Display Identification Data (EDID) section.

LVDS1_12V_SW_UNREG is not a regulated power supply. It will have the same voltage that is provided on the connector X17. Use only 12V ±10% power supply with connector X17.

2.9.2.1 LVDS Display Configuration Pins

The jumper arrays X37 and X48 can be used to configure the values of the pins 31 and 33 of the LVDS connector X13. The following table shows how these values can be changed.

Connector type: 2×3 Pin Header Male, 2.54 mm

Table 25: LVDS Display Configuration Signals

Jumper Position JP2, JP3	Description
1-2	LVDS1_SEL_1 / LVDS1_SEL_2 controlled by GPIO5 / GPIO6 respectively
3-4	LVDS1_SEL_1 / LVDS1_SEL_2 set to 3.3V_SW
5-6	LVDS1_SEL_1 / LVDS1_SEL_2 set to 5V_SW
OPEN	LVDS1_SEL_1 / LVDS1_SEL_2 set to GND

2.9.3 VGA Connector (X24)

Connector type: D-Sub 15-pin Female, AUK HDR15SN-H

Table 26: VGA connector (X24)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
1	VGA1_R_C	208	O (Analog)	+3.3V	Red color signal output
2	VGA1_G_C	210	O (Analog)	+3.3V	Green color signal output
3	VGA1_B_C	212	O (Analog)	+3.3V	Blue color signal output
4	NC				Not connected
5	GND		PWR		
6	GND		PWR		
7	GND		PWR		
8	GND		PWR		
9	VGA1_PIN9_R		PWR	JP24 selectable	+5V DC (powers EDID EEPROM chip on some monitors)
10	GND		PWR		
11	NC				Not connected
12	I2C2_DDC_SDA_VGA[1]		I/O		DDC Interface Data
13	VGA1_HSYNC_C		O	+5V	Horizontal synchronization output
14	VGA1_VSYNC_C		O	+5V	Vertical synchronization output
15	I2C2_DDC_SCL_VGA[1]		I/O		DDC Interface Clock

[1] For more information, see the Extended Display Identification Data (EDID) section.

2.9.3.1 VGA Display Configuration Pins

The jumper JP24 can be used to configure the value of pin 9 of the VGA connector X24. The following table shows how this value can be changed.

Connector type: 1×3 Pin Header Male, 2.54 mm

Table 27: VGA1_PIN9_R Configuration

Jumper Position	Description
1-2	VGA PIN9 set to GND

Continued on next page

Table 27: VGA1_PIN9_R Configuration (Continued)

Jumper Position	Description
2-3	VGA PIN9 set to V_DISP (5V_SW)

2.9.4 Unified Interface Display Connector (X31)

The Apalis Evaluation Board provides a digital RGB interface port (18-bpp) to interface with the LCD panels using a 40-way, Unified Interface Display connector (X31). It also includes a 4-wire resistive touch screen interface on the same FFC connector.

The Unified Interface Display connector (X31) is compatible with the Unified TFT Interface. A variety of LCD panels with integrated touch support are available for evaluation purposes at the Toradex Webshop.

- Resistive Touch Display 7" Parallel
- Capacitive Touch Display 7" Parallel

For more TFT display solutions, refer to the following developer webpage articles:

- Supported Displays
- Tianma RGB Display Adapter Board
- Generic RGB Display Adapter Board

Connector type: 40 Position FFC/FPC, vertical 0.5mm, Hirose FH12-40S-0.5SVA(54)

Table 28: Unified Interface Display Connector (X31)

Pin	Signal Name	Color Mapping 18bpp	MXM3 Pin	I/O Type	Voltage	Description
1	GND			PWR		
2	GND			PWR		
3	3.3V_SW			PWR	+3.3V	+3.3V power supply output
4	3.3V_SW			PWR	+3.3V	
5	BKL1_ON		286	O	+3.3V	Display backlight enable output
6	PWM_BKL1		239	O	+3.3V	Display brightness control output
7	RESET_MOCI_EDT#		26 (via R82)	O	+3.3V	Display RESET output
8	LCD1_B7	BLUE 5	301	O	+3.3V	Blue pixel color bit 5
9	LCD1_B6	BLUE 4	299	O	+3.3V	Blue pixel color bit 4
10	LCD1_B5	BLUE 3	297	O	+3.3V	Blue pixel color bit 3
11	LCD1_B4	BLUE 2	295	O	+3.3V	Blue pixel color bit 2
12	LCD1_B3	BLUE 1	293	O	+3.3V	Blue pixel color bit 1
13	LCD1_B2	BLUE 0	291	O	+3.3V	Blue pixel color bit 0
14	GND			PWR		
15	LCD1_G7	GREEN 5	283	O	+3.3V	Green pixel color bit 5
16	LCD1_G6	GREEN 4	281	O	+3.3V	Green pixel color bit 4
17	LCD1_G5	GREEN 3	279	O	+3.3V	Green pixel color bit 3
18	LCD1_G4	GREEN 2	277	O	+3.3V	Green pixel color bit 2

Continued on next page

Table 28: Unified Interface Display Connector (X31) (Continued)

Pin	Signal Name	Color Mapping 18bpp	MXM3 Pin	I/O Type	Voltage	Description
19	LCD1_G3	GREEN 1	275	O	+3.3V	Green pixel color bit 1
20	LCD1_G2	GREEN 0	273	O	+3.3V	Green pixel color bit 0
21	GND			PWR		
22	LCD1_R7	RED 5	265	O	+3.3V	Red pixel color bit 5
23	LCD1_R6	RED 4	263	O	+3.3V	Red pixel color bit 4
24	LCD1_R5	RED 3	261	O	+3.3V	Red pixel color bit 3
25	LCD1_R4	RED 2	259	O	+3.3V	Red pixel color bit 2
26	LCD1_R3	RED 1	257	O	+3.3V	Red pixel color bit 1
27	LCD1_R2	RED 0	255	O	+3.3V	Red pixel color bit 0
28	LCD1_PCLK		243	O	+3.3V	Pixel clock output
29	GND			PWR		
30	LCD1_HSYNC		247	O	+3.3V	Horizontal synchronization output
31	LCD1_VSYNC		245	O	+3.3V	Vertical synchronization output
32	LCD1_DE			O	+3.3V	Data enable signal control output
33	LCD1_CONF1[1]			O	+3.3V	Optional display configuration outputs (image rotation, image mirroring, etc.)
34	LCD1_CONF2[1]			O	+3.3V	
35	GND			PWR		
36	3.3V_SW			PWR		+3.3V power supply output
37	AN1_TSPY		319	I/O (Analog)	+3.3V	Vertical sensing plate positive connection
38	AN1_TSMX		317	I/O (Analog)	+3.3V	Horizontal sensing plate negative connection
39	AN1_TSMY		321	I/O (Analog)	+3.3V	Vertical sensing plate negative connection
40	AN1_TSPX		315	I/O (Analog)	+3.3V	Horizontal sensing plate positive connection

[1] Connected to 3.3V or GND via assembly option. The default assembly is GND.

The following table describes the assembly options available on the Apalis Evaluation Board concerning the Unified Interface Display:

Table 29: Unified Interface Display Connector Assembly Options

Solution Selected	Assembly Options	Assembled Components on Apalis Eval. Board V1.2	PCB Side
Unified Interface Display, rotate the display	Assemble appropriate 0R resistors R83, R84, R85, and R86. Refer to the LCD TFT datasheet for configuration details.	R85, R86	Top

2.9.5 Capacitive Touch Connector (X52)

Connector type: FPC/FFC, Hirose FH12-10S-0.5SVA(54)

Table 30: Capacitive Touch Connector (X52)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	I2C1_SDA	209	I/O	+3.3V	1.8k to 3.3V_SW	General-purpose I^2C bus data signal
2	I2C1_SCL	211	I/O	+3.3V		General-purpose I^2C bus clock signal
3	GND		PWR			
4	GPIO5	11	I	+3.3V		Touch controller interrupt input
5	GPIO6	13	O	+3.3V		Touch controller RESET output
6	3.3V_SW		PWR			Touch controller power supply output
7	CAP_TOUCH_SSP_CLK	235 (via R157)	O	+3.3V		SPI Touch controller clock output (Not Connected)
8	CAP_TOUCH_SSP_CS	233 (via R313)	O	+3.3V		SPI Touch controller chip select (Not Connected)
9	CAP_TOUCH_SSP_TX	231 (via R321)	O	+3.3V		SPI Touch controller data transmit (Not Connected)
10	CAP_TOUCH_SSP_RX	239 (via R322)	I	+3.3V		SPI Touch controller data receive (Not Connected)

2.9.6 Resistive Touchscreen Connector (X16)

Connector type: 2×3Pin Header Male, 2.54 mm

Table 31: Resistive Touchscreen Connector (X16)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
1	GND		PWR		
2	AN1_TSMY	321	I/O (Analog)	+3.3V	Vertical sensing plate negative connection
3	AN1_TSMX	317	I/O (Analog)	+3.3V	Horizontal sensing plate negative connection
4	AN1_TSPY	319	I/O (Analog)	+3.3V	Vertical sensing plate positive connection
5	AN1_TSPX	315	I/O (Analog)	+3.3V	Horizontal sensing plate positive connection
6	AN1_TSWIP	311 (via R89)	I (Analog)	+3.3V	Vertical/Horizontal sensing plate input in 5-wire touchscreens

2.9.7 LCD Backlight Inverter Connector (X23)

Connector type: 1×5Pin Header Male, 2.54 mm, **Not Assembled**

Table 32: LCD Backlight Inverter connector (X23) - **Not Assembled**

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	5V_DISPINV		PWR	+5V		+5V power supply output
2	GND_DISPINV		PWR			
3	BKL1_ON	286	O	+3.3V	100K to GND	Backlight enable signal output
4	GND_DISPINV		PWR			
5	NC					Not Connected

2.9.8 Extended Display Identification Data (EDID)

The I2C2 or I2C1 interface of the Apalis module can be used as the EDID interface to allow the module to query the video capabilities of the connected display.

It is possible to configure which display interface is connected to the EDID port of the Apalis module using the jumper arrays X39 and X40,

X39 and X40 are standard 2.54mm pitch headers, making it possible to use shunt jumpers to select one or more interfaces that will be connected to the EDID port of the module.

The following table describes how the jumper arrays X39 and X40 should be configured when using different display interfaces:

Connector type: 2x 2×5 Pin Header Male, 2.54 mm

Table 33: EDID Configurations

Jumper position X39, X40	I^2C Bus	Voltage	Description
1-2	I2C2	+5V	VGA (X24)
3-4	I2C2	+5V	HDMI (X11)
5-6	I2C2	+5V	LVDS (X13)
7-8	I2C2	+3.3V	LVDS (X13)
9-10	I2C1	+3.3V	LVDS (X13)

The LVDS display can be connected simultaneously with a HDMI or a VGA display. In this case, two jumpers should be used. One should be installed in positions 9–10, the other one in positions 1–2 or 3–4.

Shunt jumpers should not be installed in positions 5 - 6 simultaneously with those established in positions 7 – 8 or 9 – 10. Otherwise, it can cause damage to the Apalis module.

2.10 Audio

The Apalis Evaluation Board offers two audio interfaces (codecs). One is on the Apalis Module and the other is on the board.

2.10.1 Apalis Module Audio

The Apalis Module codec connections are available on the 3.5mm jack connectors X27, X41, X42.

2.10.1.1 LINE IN Connector (X27)

Connector type: 3.5mm Jack, CUI SJ1-3535NG-BE

Table 34: LINE IN Connector (X27)

Pin	Signal Name	MXM3 Pin	I/O Type	Description
1	AGND		PWR	
2	AAP1_LIN_L	310	I (Analog)	Line input Left
3	AAP1_LIN_R	312	I (Analog)	Line input Right

Continued on next page

Table 34: LINE IN Connector (X27) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Description
4	NC			Not connected
5	NC			

2.10.1.2 HEADPHONE OUT Connector (X41)

Connector type: 3.5mm Jack, CUI SJ1-3535NG-GR

Table 35: HEADPHONE OUT connector (X41)

Pin	Signal Name	MXM3 Pin	I/O Type	Description
1	AGND		PWR	
2	AAP1_HP_AC_L	316 (via C4)	O (Analog)	Headphones output Left
3	AAP1_HP_AC_R	318 (via C5)	O (Analog)	Headphones output Right
4	NC			Not connected
5	NC			

2.10.1.3 MIC IN Connector (X42)

Connector type: 3.5mm Jack, CUI SJ1-3535NG-PI

Table 36: MIC IN connector (X42)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Biasing	Description
1	AGND		PWR			
2	AAP1_MICIN	306	I (Analog)	+3.3V	2.2k to AVCC	Microphone input Left
3	AAP1_MIC_PWR_R		I (Analog)	+3.3V	2.2k to AVCC	Microphone input Right
4	AAP1_MIC2		I/O (Analog)			Onboard microphone output
5	NC					Not connected

Microphone MIC2, located on the board, can be used when the external microphone is disconnected.

2.10.2 Onboard Audio

The second analog audio interface is from the NAU88C22YG audio codec IC from Nuvoton. This codec is in the Apalis Evaluation Board. The connections for it are available on connectors X64, X65, X66, and X67, standard 3.5mm stereo connectors for AUX OUT, HEADPHONE OUT, AUX IN, and MIC IN, respectively.

The NAU88C22YG audio codec IC also contains a speaker driver, and its outputs are available on connectors X43, X44, X62, and X63.

A Master Clock signal is required for the audio codec IC NAU88C22YG properly. Some Apalis Systems on Module do not provide this signal (Check the datasheet for the specific Apalis SoM). By using the jumper JP26, it is possible to configure the clock signal source to be either from the SoM or the external oscillator OSC3.

Connector type: 1×3 Pin Header Male, 2.54 mm

Table 37: Onboard Codec Master Clock Configuration

Jumper position	Description
1-2	Master Clock signal sourced from the Apalis Module
2-3	Master Clock signal sourced from the external oscillator OSC3

2.10.2.1 AUX OUT Connector (X64)

Connector type: 3.5mm Jack, CUI SJ1-3535NG

Table 38: AUX OUT connector (X64)

Pin	Signal Name	I/O Type	Pull-up / Pull-down	Description
1	GND	PWR		
2	AAP2_AUXOUT2_CON	O (Analog)	4.7k to GND	Auxiliary output 2
3	AAP2_AUXOUT1_CON	O (Analog)	4.7k to GND	Auxiliary output 1
4	NC			Not connected
5	NC			

2.10.2.2 AUX IN Connector (X65)

Connector type: 3.5mm Jack, CUI SJ1-3535NG-BE

Table 39: AUX IN connector (X65)

Pin	Signal Name	I/O Type	Pull-up / Pull-down	Description
1	GND	PWR		
2	AAP2_AUXIN_CON_L	I (Analog)	47k to GND	Auxiliary input Left
3	AAP2_AUXIN_CON_R	I (Analog)	47k to GND	Auxiliary input Right
4	NC			Not connected
5	NC			

2.10.2.3 HEADPHONE OUT Connector (X66)

Connector type: 3.5mm Jack, CUI SJ1-3535NG-GR

Table 40: HEADPHONE OUT connector (X66)

Pin	Signal Name	I/O Type	Voltage	Pull-up / Pull-down	Description
1	GND	PWR			
2	AAP2_HP_CON_L	O (Analog)		10k to GND	Headphones output Left
3	AAP2_HP_CON_R	O (Analog)		10k to GND	Headphones output Right
4	NC				Not connected
5	AAP2_LLIN_CON_GPIO2		+3.3V	47k to +AAP2_VDDB	Headphones connect detection

2.10.2.4 MIC IN Connector (X67)

Connector type: 3.5mm Jack, CUI SJ1-3535NG-PI

Table 41: MIC IN connector (X67)

Pin	Signal Name	I/O Type	Biasing	Description
1	GND	PWR		
2	AAP2_LMIC_CON_P	I (Analog)	2.2k to AAP2_MICBIAS	Microphone input Left
3	AAP2_RMIC_CON_P	I (Analog)	2.2k to AAP2_MICBIAS	Microphone input Right
4	AAP2_MIC1	I/O (Analog)		Onboard microphone output
5	GND	PWR		

Microphone MIC1, located on the board, can be used when the external microphone is disconnected.

2.10.2.5 SPEAKER OUT RIGHT Connector (X62)

Connector type: 1×2Pin Header Male, 2.54 mm pitch

Table 42: SPEAKER OUT RIGHT Connector (X62)

Pin	Signal Name	I/O Type	Pull-up / Pull-down	Description
1	AAP_SPKOUT_AC_R	O (Analog)	47k to GND	Right speaker AC output
2	GND	PWR		

2.10.2.6 SPEAKER OUT LEFT Connector (X63)

Connector type: 1×2Pin Header Male, 2.54 mm pitch

Table 43: SPEAKER OUT LEFT Connector (X63)

Pin	Signal Name	I/O Type	Pull-up / Pull-down	Description
1	AAP_SPKOUT_AC_L	O (Analog)	47k to GND	Left speaker AC output
2	GND	PWR		

2.10.2.7 SPEAKER OUT Connector (X44)

Connector type: 1×2Pin Header Male, 2.54 mm pitch

Table 44: SPEAKER OUT Connector (X44)

Pin	Signal Name	I/O Type	Description
1	AAP2_SPKOUT_R	O (Analog)	BTL[1] Speaker Positive Output
2	AAP2_SPKOUT_L	O (Analog)	BTL[1] Speaker Negative Output

[1] BTL – Bridge-Tied-Load speaker output configuration. The two channels of a stereo amplifier are fed the same monaural audio signal, with one channel's electrical polarity reversed. A loudspeaker is connected between the two amplifier outputs, bridging the output terminals. This doubles the available voltage swing at the load compared with the same amplifier used without bridging.

2.10.2.8 SPEAKER OUT Terminal Block Connector (X43)

Connector type: 1×2Terminal block, CUI TBLH10-500-02BK

Table 45: SPEAKER OUT Terminal Block Connector (X43)

Pin	Signal Name	I/O Type	Description
1	AAP2_SPKOUT_R	O (Analog)	BTL[1] Speaker Positive Output
2	AAP2_SPKOUT_L	O (Analog)	BTL[1] Speaker Negative Output

[1] BTL – Bridge-Tied-Load speaker output configuration. The two channels of a stereo amplifier are fed the same monaural audio signal, with one channel's electrical polarity reversed. A loudspeaker is connected between the two amplifier outputs, bridging the output terminals. This doubles the available voltage swing at the load compared with the same amplifier used without bridging.

2.11 Type-Specific Interfaces

The type-specific (TS) mezzanine connector (X38) provides access to the type-specific interfaces on the Apalis module. These interfaces differ between Apalis modules. Various Type-specific Mezzanine Boards are available for each Apalis module and are connected to this interface to access the Type-specific features. Customers are free to develop their own Type-specific Mezzanine Boards for prototyping and development purposes. Please refer to the individual type-specific mezzanine board and relevant Apalis module datasheets.

2.11.1 Type-Specific Mezzanine Board Connector (X38)

Connector type: High-Speed Ground Plane Socket, Samtec QSH-060-01-L-D-A

Table 46: Type-Specific Mezzanine Board Connector (X38)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	GND		PWR			
3	TS_DIFF18_P	163 (via R341)	I/O			Positive differential TS Interface signal, pair 18
5	TS_DIFF18_N	161 (via R340)	I/O			Negative differential TS Interface, pair 18
7	TS6	159	I/O			Single-ended TS interface signal 6
9	TS_DIFF17_P	157 (via R339)	I/O			Positive differential TS Interface signal, pair 17
11	TS_DIFF17_N	155 (via R338)	I/O			Negative differential TS Interface, pair 17
13	GND		PWR			
15	TS_DIFF16_P	151 (via R337)	I/O			Positive differential TS Interface signal, pair 16
17	TS_DIFF16_N	149 (via R336)	I/O			Negative differential TS Interface, pair 16
19	GND		PWR			
21	TS_DIFF15_P	145 (via R335)	I/O			Positive differential TS Interface signal, pair 15
23	TS_DIFF15_N	143 (via R334)	I/O			Negative differential TS Interface, pair 15
25	GND		PWR			
27	TS_DIFF14_P	139 (via R333)	I/O			Positive differential TS Interface signal, pair 14
29	TS_DIFF14_N	137 (via R332)	I/O			Negative differential TS Interface, pair 14
31	GND		PWR			
33	TS5	135	I/O			Single-ended TS interface signal 5
35	TS_DIFF13_P	133	I/O			Positive differential TS Interface signal, pair 13
37	TS_DIFF13_N	131	I/O			Negative differential TS Interface, pair 13
39	GND		PWR			
41	TS_DIFF12_P	127	I/O			Positive differential TS Interface signal, pair 12
43	TS_DIFF12_N	125	I/O			Negative differential TS Interface, pair 12
45	GND		PWR			
47	TS4	123	I/O			Single-ended TS interface signal 4
49	TS_DIFF11_P	121	I/O			Positive differential TS Interface signal, pair 11
51	TS_DIFF11_N	119	I/O			Negative differential TS Interface, pair 11
53	GND		PWR			
55	TS_DIFF10_P	115	I/O			Positive differential TS Interface signal, pair 10
57	TS_DIFF10_N	113	I/O			Negative differential TS Interface, pair 10
59	GND		PWR			

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Table 46: Type-Specific Mezzanine Board Connector (X38) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
61	TS_DIFF9_P	109	I/O			Positive differential TS Interface signal, pair 9
63	TS_DIFF9_N	107	I/O			Negative differential TS Interface, pair 9
65	GND		PWR			
67	TS_DIFF8_P	103	I/O			Positive differential TS Interface signal, pair 8
69	TS_DIFF8_N	101	I/O			Negative differential TS Interface, pair 8
71	GND		PWR			
73	TS3	99	I/O			Single-ended TS interface signal 3
75	TS_DIFF7_P	97	I/O			Positive differential TS Interface signal, pair 7
77	TS_DIFF7_N	95	I/O			Negative differential TS Interface, pair 7
79	GND		PWR			
81	TS_DIFF6_P	91	I/O			Positive differential TS Interface signal, pair 6
83	TS_DIFF6_N	89	I/O			Negative differential TS Interface, pair 6
85	GND		PWR			
87	TS2	87	I/O			Single-ended TS interface signal 2
89	TS_DIFF5_P	85	I/O			Positive differential TS Interface signal, pair 5
91	TS_DIFF5_N	83	I/O			Negative differential TS Interface, pair 5
93	GND		PWR			
95	TS_DIFF4_P	79	I/O			Positive differential TS Interface signal, pair 4
97	TS_DIFF4_N	77	I/O			Negative differential TS Interface, pair 4
99	GND		PWR			
101	TS_DIFF3_P	73	I/O			Positive differential TS Interface signal, pair 3
103	TS_DIFF3_N	71	I/O			Negative differential TS Interface, pair 3
105	GND		PWR			
107	TS_DIFF2_P	67	I/O			Positive differential TS Interface signal, pair 2
109	TS_DIFF2_N	65	I/O			Negative differential TS Interface, pair 2
111	GND		PWR			
113	TS1	63	I/O			Single-ended TS interface signal 1 (Apalis module RECOVERY signal)
115	TS_DIFF1_P	61	I/O			Positive differential TS Interface signal, pair 1
117	TS_DIFF1_N	59	I/O			Negative differential TS Interface, pair 1
119	GND		PWR			
121	GND		PWR			
2	VSTB		PWR	+5V		5V Standby voltage
4	GND		PWR			
6	SPI2_CLK	235	O	+3.3V		SPI2 clock signal

Continued on next page

Table 46: Type-Specific Mezzanine Board Connector (X38) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
8	SPI2_CS	233	O	+3.3V		SPI2 chip select signal
10	SPI2_MOSI	231	O	+3.3V		SPI2 master output signal
12	SPI2_MISO	229	I	+3.3V		SPI2 master input signal
14	SPI1_CS	227	O	+3.3V		SPI1 chip select signal
16	SPI1_MOSI	225	O	+3.3V		SPI1 master output signal
18	SPI1_MISO	223	I	+3.3V		SPI1 master input signal
20	SPI1_CLK	221	O	+3.3V		SPI1 clock signal
22	GND		PWR			
24	CAM_MEZ_PIN24		I			Additional pin from SoM to camera connector, connected to X56, pin 9
26	CAM_MEZ_PIN26		I			Additional pin from SoM to camera connector, connected to X56, pin 10
28	CAM_MEZ_PIN28		I			Additional pin from SoM to camera connector, connected to X56, pin 11
30	CAM_MEZ_PIN30		I			Additional pin from SoM to camera connector, connected to X56, pin 12
32	GND		PWR			
34	MEZ_CAM1_MCLK	193 (via R379)	O			Mezzanine board camera master clock
36	GND		PWR			
38	I2C_CAM1_SCL	203	I/O	+3.3V	+1.8K to 3.3V_SW	Camera I^2C bus Clock
40	GND		PWR			
42	I2C_CAM1_SDA	201	I/O	+3.3V	+1.8K to 3.3V_SW	Camera I2 C bus Data
44	5V_SW		PWR	+5V		+5V switchable power supply output
46	5V_SW		PWR	+5V		
48	5V_SW		PWR	+5V		
50	5V_SW		PWR	+5V		
52	5V_SW		PWR	+5V		
54	NC					
56	V_SUPPLY_FILT_F		PWR	PWR_IN		Fused unregulated power supply output
58	V_SUPPLY_FILT_F		PWR	PWR_IN		
60	V_SUPPLY_FILT_F		PWR	PWR_IN		
62	3.3V		PWR	+3.3V		+3.3V power supply output
64	3.3V		PWR	+3.3V		
66	3.3V		PWR	+3.3V		
68	3.3V		PWR	+3.3V		
70	NC					
72	3.3V_SW		PWR	+3.3V		+3.3V switchable power supply output
74	3.3V_SW		PWR	+3.3V		
76	3.3V_SW		PWR	+3.3V		
78	3.3V_SW		PWR	+3.3V		

Continued on next page

Table 46: Type-Specific Mezzanine Board Connector (X38) (Continued)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
80	NC					
82	12V_SW_UNREG_F		PWR	+12V ±10%		+12V unregulated switchable power supply output
84	12V_SW_UNREG_F		PWR	+12V ±10%		
86	12V_SW_UNREG_F		PWR	+12V ±10%		
88	GND		PWR			
90	I2C1_SCL	211	I/O	+3.3V		General-purpose I^2C bus clock signal
92	I2C1_SDA	209	I/O	+3.3V		General-purpose I^2C bus data signal
94	UART4_TXD	138	O	+3.3V		UART4 port transmission signal
96	UART4_RXD	140	I	+3.3V		UART4 port receiving signal
98	WAKE1_MICO#	37	I	+3.3V		Active low Apalis module wake input signal
100	POWER_ENABLE_MOCI	24	O	+3.3V		Signal for enabling onboard peripherals' voltage rail
102	RESET_MOCI#	26	O	+3.3V		Active low reset output for the onboard peripherals
104	RESET_MICO#	28	I	+3.3V		Active low reset input for the Apalis module
106	GPIO1	1	I/O	+3.3V		General-purpose I/O
108	GPIO2	3	I/O	+3.3V		
110	GPIO3	5	I/O	+3.3V		
112	GPIO4	7	I/O	+3.3V		
114	GPIO5	11	I/O	+3.3V		
116	GPIO6	13	I/O	+3.3V		
118	GPIO7	15	I/O	+3.3V		
120	GPIO8	17	I/O	+3.3V		

2.12 Camera

There are three options to connect cameras to the Apalis Evaluation Board:

- Parallel Camera connector
- MIPI CSI Camera connector
- Type-specific Mezzanine Board connector

These interfaces allow for the connection of a wide variety of cameras.

Any of the available camera interfaces can be connected to the reference clock signal CAM1_MCLK provided by the Apalis module, if required.

The CAM1_MCLK signal can be connected to only one target. Simultaneous use of this signal on more than one camera connectors is not possible. Connection of the CAM1_MCLK signal can be changed by assembling and disassembling 0R resistors.

The following table describes the assembly options available on the Apalis Evaluation Board concerning the CAM1_MCLK signal connection:

Table 47: Camera Master Clock Assembly Options

Solution Selected	Assembly Options
CAM1_MCLK signal routed to the Parallel Camera connector	Assemble resistor R377, Disassemble resistors R324 and R379
CAM1_MCLK signal routed to the MIPI CSI Camera connector	Assemble resistor R324, Disassemble resistors R377 and R379
CAM1_MCLK signal routed to the Type-specific Mezzanine Board connector camera connector	Assemble resistor R379, Disassemble resistors R324 and R377

By default, the CAM1_MCLK signal is connected to the MIPI CSI Camera connector (X60), with resistor R324 assembled.

2.12.1 Parallel Camera

The Parallel Camera Interface on connector X22 is intended for applications requiring image capture capability from CMOS or CDD image sensors. This interface supports various operating modes, data widths, formats, and clocking schemes. For details, please see the relevant Apalis module datasheet.

To provide compatibility with the variety of different parallel camera interface standards, the data signals of this interface have been routed through a reconfigurable jumper array.

Only 8 of the 12 data bits are directly connected to the module. The other 4 data bit need to be connected through the Type-specific connector.

2.12.1.1 Parallel Camera Connector (X22)

Connector type: 2×12 Pin Header Male, 2.54 mm

Table 48: Parallel Camera Connector (X22)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up / Pull-down	Description
1	3.3V_SW		PWR	+3.3V		+3.3V power supply output
2	3.3V_SW		PWR	+3.3V		
3	PAR_CAM1_MCLK	193 (via R377)	O	+3.3V		Master clock output
4	CAM1_PCLK	191	I/O	+3.3V		Pixel clock
5	CAM1_HSYNC	197	I/O	+3.3V		Horizontal synchronization
6	CAM1_VSYNC	195	I/O	+3.3V		Vertical synchronization
7	CAM1_D0	187	I/O	+3.3V		Parallel data 0
8	CAM1_D1	185	I/O	+3.3V		Parallel data 1
9	CAM1_D2	183	I/O	+3.3V		Parallel data 2
10	CAM1_D3	181	I/O	+3.3V		Parallel data 3
11	CAM1_D4	179	I/O	+3.3V		Parallel data 4
12	CAM1_D5	177	I/O	+3.3V		Parallel data 5
13	CAM1_D6	175	I/O	+3.3V		Parallel data 6
14	CAM1_D7	173	I/O	+3.3V		Parallel data 7
15	I2C_CAM1_SCL	203	I/O	+3.3V	1.8K to 3.3V_SW	Parallel Camera I^2C bus Clock
16	I2C_CAM1_SDA	201	I/O	+3.3V	1.8K to 3.3V_SW	Parallel Camera I^2C bus Data
17	CAM1_D8		I/O	+3.3V		Parallel data 8, connected to X38, pin 24
18	CAM1_D9		I/O	+3.3V		Parallel data 9, connected to X38, pin 26
19	GND		PWR			
20	GND		PWR			
21	CAM1_D10		I/O	+3.3V		Parallel data 10, connected to X38, pin 28
22	CAM1_D11		I/O	+3.3V		Parallel data 11, connected to X38, pin 30
23	3.3V_SW		PWR	+3.3V		+3.3V power supply output
24	5V_SW		PWR	+5V		+5V power supply output

2.12.1.2 Camera Jumper Array (X57)

Connector type: 2×12 Pin Header Male, 2.54 mm

Table 49: Camera Jumper Array (X57)

SoM Side			Peripheral Side		I/O Type	Voltage
MXM3 Pin	Signal Name	Pin	Pin	Signal Name		
187	MXM3_187	A1	B1	CAM1_D0	I/O	+3.3V
185	MXM3_185	A2	B2	CAM1_D1	I/O	+3.3V
183	MXM3_183	A3	B3	CAM1_D2	I/O	+3.3V

Continued on next page

Table 49: Camera Jumper Array (X57) (Continued)

SoM Side			Peripheral Side		I/O Type	Voltage
MXM3 Pin	Signal Name	Pin	Pin	Signal Name		
181	MXM3_181	A4	B4	CAM1_D3	I/O	+3.3V
179	MXM3_179	A5	B5	CAM1_D4	I/O	+3.3V
177	MXM3_177	A6	B6	CAM1_D5	I/O	+3.3V
175	MXM3_175	A7	B7	CAM1_D6	I/O	+3.3V
173	MXM3_173	A8	B8	CAM1_D7	I/O	+3.3V
	CAM_MEZ_PIN24	A9	B9	CAM1_D8	I/O	+3.3V
	CAM_MEZ_PIN26	A10	B10	CAM1_D9	I/O	+3.3V
	CAM_MEZ_PIN28	A11	B11	CAM1_D10	I/O	+3.3V
	CAM_MEZ_PIN30	A12	B12	CAM1_D11	I/O	+3.3V

2.12.1.3 Camera Function Tap (X58)

Pinout identical to X57 Pins B1 to B12.

2.12.1.4 Camera MXM3 Breakout Area (X56)

Pinout identical to X57 Pins A1 to A12.

2.12.2 MIPI CSI Camera Interface

The MIPI CSI interface is available on the type-specific pins of some Apalis modules, for details check the datasheet of the relevant Apalis module. A part of the high-speed differential type-specific signals (TS_DIFF14 to TS_DIFF18) is shared between the MIPI CSI Camera connector X60 and the type-specific mezzanine board connector X38.

MIPI CSI is a high-speed point-to-point differential interface, therefore it can be connected only to one connector. To address this, the Apalis Evaluation Board has 0R resistors assembly options (R332 to R351) that allows routing these high-speed differential signals between the module and the type-specific mezzanine connector or between the module and the MIPI CSI camera connector.

The assembly options are shown in the table below:

Table 50: MIPI CSI Assembly Options

Solution Selected	Assembly Options
High-speed signals TS_DIFF14 to TS_DIFF18 are routed to the type-specific mezzanine connector (X38)	Assemble resistors R332 to R341, Disassemble resistors R342 to R351
High-speed signals TS_DIFF14 to TS_DIFF18 are routed to the MIPI CSI camera connector (X60)	Assemble resistors R342 to R351, Disassemble resistors R332 to R341

By default, TS_DIFF14 to TS_DIFF18 high-speed Apalis module signals are connected to the MIPI CSI camera connector (resistors R342 to R351 assembled).

2.12.2.1 MIPI CSI Camera Connector (X60)

Connector type: 24 Position FFC/FPC, vertical 0.5mm, Hirose FH12-24S-0.5SVA(54)

Table 51: MIPI CSI Camera Connector (X60)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	CSI_D0_N	155 (via R348)	I/O			Negative differential CSI data signal, lane 0
3	CSI_D0_P	157 (via R349)	I/O			Positive differential CSI data signal, lane 0
4	GND		PWR			
5	CSI_D1_N	149 (via R346)	I			Negative differential CSI data signal, lane 1
6	CSI_D1_P	151 (via R347)	I			Positive differential CSI data signal, lane 1
7	GND		PWR			
8	CSI_CLK_N	161 (via R350)	I			Negative differential CSI clock signal
9	CSI_CLK_P	163 (via R351)	I			Positive differential CSI clock signal
10	GND		PWR			
11	CSI_GPIO0_RST		O			Camera RESET
12	CSI_CAM1_MCLK	193 (via R324)	O			CSI camera master clock
13	I2C_CAM1_SCL		I/O	+3.3V	1.8k to +V3.3_SW	Camera I^2C bus Clock
14	I2C_CAM1_SDA		I/O	+3.3V	1.8k to +V3.3_SW	Camera I^2C bus Data
15	3.3V_SW		PWR	+3.3V		+3.3V switchable power supply output
16	CSI_D2_N	143 (via R344)	I			Negative differential CSI data signal, lane 2
17	CSI_D2_P	145 (via R345)	I			Positive differential CSI data signal, lane 2
18	GND		PWR			
19	CSI_D3_N	137 (via R342)	I			Negative differential CSI data signal, lane 3
20	CSI_D3_P	139 (via R343)	I			Positive differential CSI data signal, lane 3
21	5V_SW		PWR			+5V switchable power supply output
22	CSI_GPIO1		O	+3.3V		Camera Power Down
23	CSI_GPIO2		I	+3.3V		Camera Identification
24	CSI_GPIO3		O	+3.3V		Power Supply Control

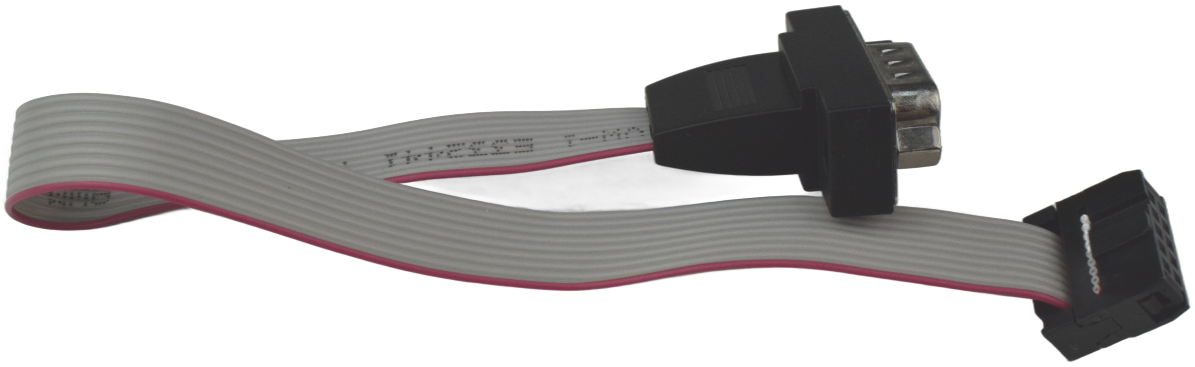
2.13 Digital and Analog I/O

2.13.1 Communication Interfaces

2.13.1.1 CAN

The Apalis Evaluation Board uses the ISO1042BDWR isolated CAN transceivers from Texas Instruments to implement two CAN FD interfaces in conjunction with the two CAN interfaces on the Apalis module supporting regular CAN up to 1Mbps and CAN FD up to 5Mbps data rate. The CAN interfaces are available on two 2×5 pin headers, X26 and X32. Pin header to D-Sub adapters can be used with the connectors X26 and X32.

Figure 4: 9-pin D-Sub to IDC adapter



The jumpers JP15, JP16, JP17, JP18, JP25, JP34, JP35, and JP36 provide hardware configuration for these interfaces:

Connector type: 8x 1×2Pin Header Male, 2.54 mm pitch

Table 52: CAN Configuration Jumpers

Jumper	Status	Function
JP25, JP36	CLOSED	CAN1 split terminated
JP34, JP35	CLOSED	CAN2 split terminated
JP15, JP16	CLOSED	CAN1 isolated power supply is connected to the connector X32
JP16, JP17	CLOSED	CAN2 isolated power supply is connected to the connector X26

The CAN transceivers power is switchable and can be controlled by software. For this purpose, signals CAN1_PWR_EN (MXM3_158) and CAN2_PWR_EN (MXM3_156) are used. Check the Apalis Evaluation Board schematic for details.

2.13.1.1.1 CAN1 Connector (X32)

Connector type: 2×5Pin Header Male, 2.54 mm pitch

Table 53: CAN1 Connector (X32)

Pin	Signal Name	I/O Type	Voltage	Description
1	NC			Not connected
2	CAN1_PGND	PWR		CAN_1 isolated GND
3	CAN1_L	I/O		Low-level CAN_1 bus line
4	CAN1_H	I/O		High-level CAN_1 bus line
5	CAN1_GND_ISO			Connected through 100 Ohm
6	NC			Not connected
7	NC			

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Table 53: CAN1 Connector (X32) (Continued)

Pin	Signal Name	I/O Type	Voltage	Description
8	CAN1_PW	PWR	+5V	CAN_1 isolated Power supply output
9	NC			Not connected
10	NC			

2.13.1.1.2 CAN2 Connector (X26)

Connector type: 2×5Pin Header Male, 2.54 mm pitch

Table 54: CAN1 Connector (X32)

Pin	Signal Name	I/O Type	Voltage	Description
1	NC			Not connected
2	CAN2_PGND	PWR		CAN_2 isolated GND
3	CAN2_L	I/O		Low-level CAN_2 bus line
4	CAN2_H	I/O		High-level CAN_2 bus line
5	CAN2_GND_ISO			Connected through 100 Ohm
6	NC			Not connected
7	NC			
8	CAN2_PW	PWR	+5V	CAN_2 isolated Power supply output
9	NC			Not connected
10	NC			

2.13.1.2 UART Interfaces

The Apalis Evaluation Board features 4 UART interfaces that are connected to the following connectors:

- UART1: connector X28 through an RS232 transceiver. It can also be optionally connected to a USB Debugger's built-in Serial transceiver based on the FTDI's FT4232HL bridge IC.
- UART2: connector X55 through an RS422/485 transceiver.
- UART3: second channel of the USB Debugger's built-in Serial transceiver.
- UART4: mezzanine connector X38. Refer to Type-Specific Mezzanine Board Connector.

2.13.1.2.1 RS232 Connector (X28)

Connector type: D-Sub 9-pin Male, Assmann A-DS 09 A/KG-T2S

Table 55: RS422/485 Connector (X55)

Pin	Signal Name	MXM3 Pin	I/O Type	Description
1	UART1_RS232_CON_DCD	124 (via IC7)	I	Data Carrier Detect (DCD)
2	UART1_RS232_CON_RXD	118 (via IC7)	I	Receive Data (RXD)
3	UART1_RS232_CON_TXD	112 (via IC7)	O	Transmit Data (TXD)
4	UART1_RS232_CON_DTR	110 (via IC7)	O	Data Terminal Ready (DTR)
5	GND		PWR	
6	UART1_RS232_CON_DSR	120 (via IC7)	I	Data Set Ready (DSR)
7	UART1_RS232_CON_RTS	114 (via IC7)	O	Request to Send (RTS)
8	UART1_RS232_CON_CTS	116 (via IC7)	I	Clear to Send (CTS)
9	UART1_RS232_CON_RI	122 (via IC7)	I	Ring Indicator (RI)

By changing the position of the Jumpers JP10, JP12, JP27, and JP28, it is possible to route the signals of the UART1 interface to the connector X28 (via the RS232 transceiver) or the USB Debugger's built-in Serial transceiver accessible via the X29 USB-C Connector.

Connector type: 4x 1×3Pin Header Male, 2.54 mm

Table 56: UART1 Configuration Jumpers

JP10, JP12, JP27 and JP28 Position	Description
1 - 2	UART1 interface routed to the connector X28 through the RS232 transceiver.
2 - 3	UART1 interface routed to the USB Debugger's built-in Serial transceiver (connector X29).

2.13.1.2.2 RS422/485 Connector (X55)

Connector type: D-Sub 9-pin Male, Assmann A-DS 09 A/KG-T2S

Table 57: RS232 connector (X28)

Pin	Signal Name	I/O Type	Description
1	GND	PWR	
2	NC		Not Connected
3	NC		
4	UART2_RS485_RXD+	I	
5	UART2_RS485_RXD-	I	
6	NC		Not Connected
7	NC		
8	UART2_RS485_TXD+	O	
9	UART2_RS485_TXD-	O	

The jumpers JP5, JP6, JP7, JP8, JP9, and JP11 provide hardware configuration for this interface:

Connector type: 1×2 Pin Header Male, 2.54 mm

Table 58: RS422/485 Configuration Jumpers

Jumper	Status	Function
JP7	CLOSED	ECHO disabled (the sender cannot read the message just sent)
JP5, JP8	CLOSED	Insert the 120ohm bus termination (for RS422)[1]
JP11	CLOSED	The upper RS422/485 interface is enabled
JP6, JP9	CLOSED	Half Duplex configuration
JP6, JP9	OPEN	Full Duplex configuration

[1] If JP6 and JP9 are closed, the RS422/485 interface is in the Half Duplex mode, then only one of the termination jumpers can be closed, either JP5 or JP8.

2.13.2 Digital Interfaces

2.13.2.1 Switches and LEDs

The Apalis Evaluation Board features:

- 8x LEDs:
  - 4x Green
  - 4x Red
- 4x Switches
- 4x Buttons

Interfaces to and from these devices are available on connector X34. They can be directly connected to the GPIO breakout connectors or additional hardware.

The buttons and switches are **not debounced**.

2.13.2.1.1 LEDs/Switches connector (X34)

Connector type: 2×10 Pin Header Female, 2.54 mm

Table 59: LEDs/Switches connector (X34)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down
1	GND	PWR		
2	3.3V_SW	PWR	+3.3V	
3	SWITCH_1	O	+3.3V	
4	LED_1	I	+3.3V	
5	SWITCH_2	O	+3.3V	100K to GND
6	LED_2	I	+3.3V	
7	SWITCH_3	O	+3.3V	

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Table 59: LEDs/Switches connector (X34) (Continued)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down
8	LED_3	I	+3.3V	
9	SWITCH_4	O	+3.3V	100K to GND
10	LED_4	I	+3.3V	
11	BUTTON_1	O	+3.3V	10K to GND
12	LED_5	I	+3.3V	100K to GND
13	BUTTON_2	O	+3.3V	10K to GND
14	LED_6	I	+3.3V	100K to GND
15	BUTTON_3	O	+3.3V	10K to 3.3V_SW
16	LED_7	I	+3.3V	100K to GND
17	BUTTON_4	O	+3.3V	10K to 3.3V_SW
18	LED_8	I	+3.3V	100K to GND
19	GND	PWR		
20	3.3V_SW	PWR	+3.3V	

By default, BUTTON_1 and BUTTON_2 have active-high configuration, while BUTTON_3 and BUTTON_4 are have active-low configuration. The buttons' configuration can be changed with different assembly options.

The following table describes the assembly options available:

Table 60: Button Assembly Options

Button	Selected Option	Assembly Options	
		Assemble	Disassemble
Button 1	**Active-High**[1]	R129 (10K) R126 (10R)	R221 R222
	Active-Low	R221 (10K) R222 (10R)	R129 R126
Button 2	**Active-High**[1]	R133 (10K) R130 (10R)	R357 R358
	Active-Low	R357 (10K) R358 (10R)	R133 R130
Button 3	Active-High	R137 (10K) R359 (10R)	R360 R136
	Active-Low[1]	R360 (10K) R136 (10R)	R137 R359
Button 4	Active-High	R141 (10K) R367 (10R)	R368 R140
	Active-Low[1]	R368 (10K) R140 (10R)	R141 R367

[1] Default Configuration

2.13.3 Analog Interfaces

The Analog outputs are implemented as Pulse Width Modulated (PWM) signals feeding discrete RC filters with a time constant of 3.3ms.

The Analog inputs are directly connected to the GPIO breakout area.

2.13.3.1 Analog I/O Connector (X14)

Connector type: 2×8 Pin Header Male, 2.54mm

Table 61: Analog I/O Connector (X14)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	AN1_ADC0	305	I	+3.3V		ADC input 0
2	AGND		PWR			Analog ground
3	AN1_ADC1	307	I	+3.3V		ADC input 1
4	AGND		PWR			Analog ground
5	AN1_ADC2	309	I	+3.3V		ADC input 2
6	AGND		PWR			Analog ground
7	AN1_TSWIP_ADC3	311	I	+3.3V		ADC input 3
8	AGND		PWR			Analog ground
9	ANALOG_OUT4	8	O	+3.3V	RC-filter (3.3ms)	Low-pass filtered PWM4 output
10	GND		PWR			
11	ANALOG_OUT3	6	O	+3.3V	RC-filter (3.3ms)	Low-pass filtered PWM3 output
12	GND		PWR			
13	ANALOG_OUT2	4	O	+3.3V	RC-filter (3.3ms)	Low-pass filtered PWM2 output
14	GND		PWR			
15	ANALOG_OUT1	2	O	+3.3V	RC-filter (3.3ms)	Low-pass filtered PWM1 output
16	GND		PWR			

2.14 Temperature Sensor

The Apalis Evaluation Board features the digital temperature sensor TMP75CIDGKR (IC50). The sensor is connected to the general-purpose I2C1 bus. The default I^2C address is `0x4F`. For details, please check the TMP75CIDGKR datasheet.

2.15 Real-Time Clock (RTC)

The Apalis Evaluation Board uses the ST Microelectronics M41T0M6 chip as an external RTC. The battery holder BAT1 is available on the Apalis Evaluation Board for RTC power backup.

Backup battery power can be delivered to either the internal RTC or the external RTC based on the jumper JP22 setting.

Connector type: 1×3 Pin Header Male, 2.54 mm Pitch

Table 62: RTC Configuration Jumper (JP22)

Jumper Position	Description
1 - 2	Internal RTC (available on Apalis Module)
2 - 3	External RTC (available on Evaluation Board)

For more details about the internal RTC, please refer to the relevant Apalis system-on-module datasheet.

2.15.1 Battery Holder (BAT1)

A 20 mm (diameter) coin cell/battery should be used with the Battery Holder (BAT1). The coin cell can provide power backup to the RTC circuits when the external power supply is not available.

Supported batteries: CR2032 or similar coin cells.

Connector type: Renata HU2032-LF

Table 63: Battery Holder (BAT1)

Pin	Signal Name	Voltage
1	VCC_BATT	+3.0V
2	GND	

2.16 JTAG

The Apalis Evaluation Board provides a JTAG interface to the JTAG port available on Apalis modules.

The X33 connector provides an interface to an external JTAG device via a standard 2.54mm shrouded and keyed header.

In addition, the Apalis Evaluation Board features a spring-loaded Pogo-pin connector (X59), positioned directly underneath the installed Apalis module, allowing direct connection with the Apalis module JTAG test points.

The Apalis Evaluation Board also has an onboard JTAG debugger feature. Please check the USB Debug section of this document and the Apalis Evaluation Board schematic for detailed information. The schematic is available on the Reference Designs page of the Toradex developer website.

If an external JTAG debugger is used with an Apalis Evaluation Board, jumper JP21 should be removed. Simultaneous use of the onboard and external JTAG Debugger is not allowed. Violating this requirement may damage Debuggers or the Apalis Evaluation Board. By default, jumper JP21 is not assembled on the Apalis Evaluation Board.

2.16.1 JTAG to Host Connector (X33)

Connector type: 2×10 Pin Shrouded and Keyed Header Male, 2.54mm

Table 64: JTAG to Host Connector (X33)

Pin	Signal Name	MXM3 Pin	I/O Type	Voltage	Description
1	VREF_JTAG		PWR	+1.8V/+3.3V	Reference voltage output for the JTAG adapter from the target CPU
2	VREF_JTAG		PWR	+1.8V/+3.3V	
3	JTAG_TRST#		I	+1.8V/+3.3V	Reset signal of the target JTAG port
4	GND		PWR		
5	JTAG_TDI		I	+1.8V/+3.3V	Test Data Input signal to the target CPU
6	GND		PWR		
7	JTAG_TMS		I	+1.8V/+3.3V	Test Mode Select signal to the target CPU
8	GND		PWR		
9	JTAG_TCK		I	+1.8V/+3.3V	Test Clock signal to the target CPU
10	GND		PWR		
11	JTAG_RTCK		O	+1.8V/+3.3V	Return Test Clock signal from the target CPU
12	GND		PWR		
13	JTAG_TDO		O	+1.8V/+3.3V	Test Data Output from the target CPU
14	GND		PWR		
15	JTAG_SYSRESET#	28 (via R22)	I	+3.3V	Apalis module Reset input (Not Connected)
16	GND		PWR		
17	NC				
18	GND		PWR		
19	NC				
20	GND		PWR		

2.16.2 JTAG to Apalis Connector (X59)

Connector type: 1×7 POGO pins, Mill-Max 821-22-007-10-000101

Table 65: JTAG to Apalis Connector (X59)

Pin	Signal Name	I/O Type	Voltage	Description
1	JTAG_TDI	O	+1.8V/+3.3V	Test Data Input signal to the target CPU
2	JTAG_TDO	I	+1.8V/+3.3V	Test Data Output from the target CPU
3	JTAG_TCK	O	+1.8V/+3.3V	Test Clock signal to the target CPU
4	JTAG_TRST#	O	+1.8V/+3.3V	Reset signal of the target JTAG port
5	JTAG_TMS	O	+1.8V/+3.3V	Test Mode Select signal to the target CPU
6	JTAG_RTCK	I	+1.8V/+3.3V	Return Test Clock signal from the target CPU
7	VREF_JTAG	PWR	+1.8V/+3.3V	Reference voltage output for the JTAG adapter from the target CPU

2.17 USB Debug

The Apalis Evaluation Board provides an onboard Universal USB Debugger (IC41). The debugger is based on the FT4232HL chip and offers the following features:

- 2x UART ports connected to Apalis Module UART1 and UART3 interfaces
- JTAG Debugger/Programmer
- 4x GPIO used for performing basic Evaluation Board control features: Power ON/OFF, Reset, etc.

The simplified USB Debug architecture is shown below.

Figure 5: USB Debug architecture.

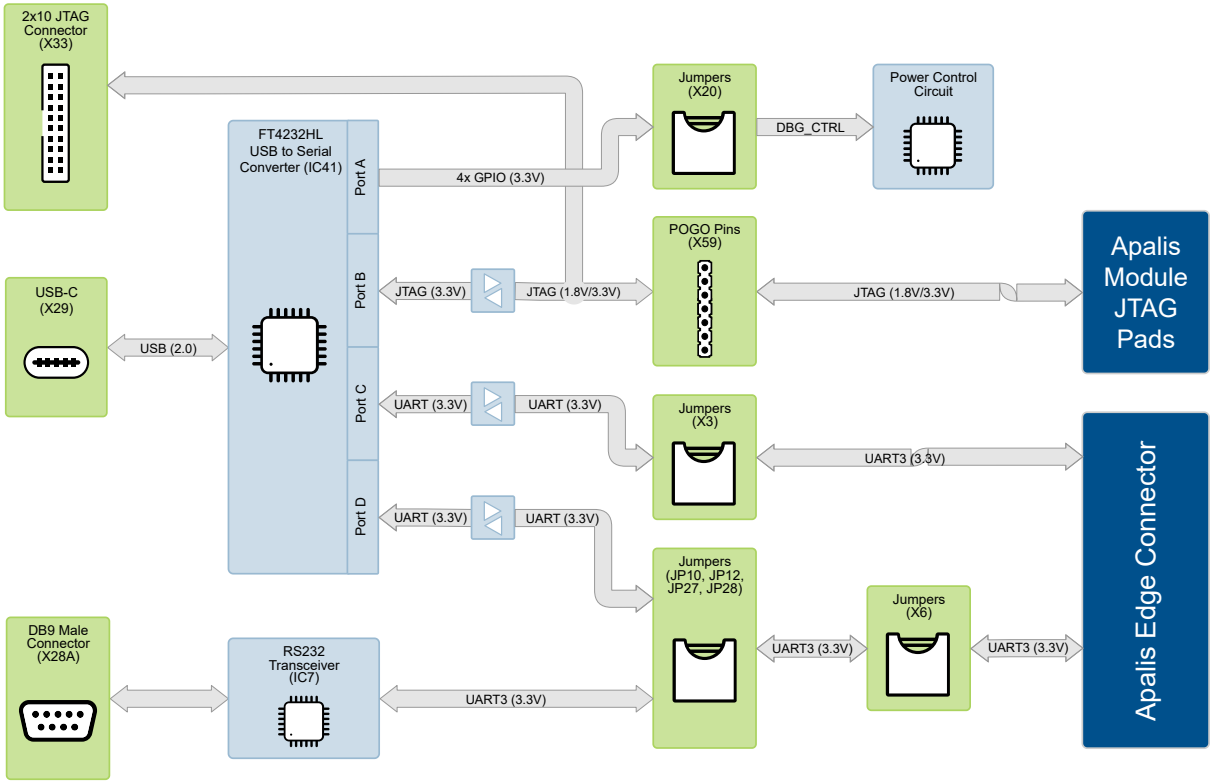

Table 66: FT4232HL IC Pin Assignments

Pin	Pin Name	I/O Type	Interface	Signal Name	Description
21	ADBUS4	O	GPIO	DBG_FORCE_OFF#	Apalis Evaluation Board FORCE OFF
22	ADBUS5	O		DBG_RESET#	Apalis Module RESET
23	ADBUS6	O		DBG_PWR_BTN#	Apalis Evaluation Board POWER ON/OFF
24	ADBUS7	O		DBG_RECOVERY#	Verdin Module RECOVERY mode
26	BDBUS0	O	JTAG	FTDI_JTAG_TCK	JTAG Test Mode Select
27	BDBUS1	O		FTDI_JTAG_TDI	JTAG Test Data Input
28	BDBUS2	I		FTDI_JTAG_TDO	JTAG Test Data Output
29	BDBUS3	O		FTDI_JTAG_TMS	JTAG Test Mode Set
			JTAG		

Continued on next page

Table 66: FT4232HL IC Pin Assignments (Continued)

Pin	Pin Name	I/O Type	Interface	Signal Name	Description
30	BDBUS4	O		FTDI_JTAG_TRST#	JTAG Test Mode Reset
34	BDBUS7	O		(LED34)	JTAG activity LED
38	CDBUS0	O	UART	UART3_RXD	Receiver Data of the Apalis module UART3
39	CDBUS1	I		UART3_TXD	Transmitter Data of the Apalis module UART3
48	DDBUS0	O	UART	UART1_FTDI_RXD	Receiver Data of the Apalis module UART1
52	DDBUS1	I		UART1_FTDI_TXD	Transmitter Data of the Apalis module UART1
53	DDBUS2	O		UART1_FTDI_CTS	Clear To Send signal of the Apalis UART1
54	DDBUS3	I		UART1_FTDI_RTS	Ready To Send signal of the Apalis UART1

The debug interface is accessible via the USB-C connector X29.

2.17.1 USB Debug Connector (X29)

Connector type: USB-C, Stewart SS-52400-003

Table 67: USB Debug Connector (X29)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
A1	GND	PWR			
A2	NC				Not Connected
A3	NC				
A4	5V_DBG	PWR	+5V		FTDI debugger power supply input
A5	USB_DBG_CC2			5.1k to GND	Type-C configuration channel signal 1[1]
A6	USB_DBG_CON_P	I/O			Positive Differential USB 2.0 Signal
A7	USB_DBG_CON_N	I/O			Negative Differential USB 2.0 Signal
A8	NC				Not Connected
A9	5V_DBG	PWR	+5V		FTDI debugger power supply input
A10	NC				Not Connected
A11	NC				
A12	GND	PWR			
B1	GND	PWR			
B2	NC				Not Connected
B3	NC				
B4	5V_DBG	PWR	+5V		FTDI debugger power supply input
B5	USB_DBG_CC1			5.1k to GND	Type-C configuration channel signal 2[1]
B6	USB_DBG_CON_P	I/O			Positive Differential USB 2.0 Signal
B7	USB_DBG_CON_N	I/O			Negative Differential USB 2.0 Signal
B8	NC				Not Connected
B9	5V_DBG	PWR	+5V		FTDI debugger power supply input
B10	NC				Not Connected

Continued on next page

Table 67: USB Debug Connector (X29) (Continued)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
B11	NC				
B12	GND	PWR			
S1/S2	GND_CHASSIS				
S3/S4	GND_CHASSIS				
S5/S6	GND_CHASSIS				

[1] The Connector and Board Configuration Channel (CC) signals are inverted intentionally. For more information, see the blog Adding USB-C to your Carrier Board Design.

The USB Debugger JTAG interface and all the JTAG connectors are connected as a daisy chain. The jumper JP21 controls the USB Debugger JTAG connection to the Apalis module.

Connector type: 1×2 Pin Header Male, 2.54 mm Pitch

Table 68: JTAG Jumper Configuration (JP21) - Not Assembled

Jumper Position	Description
OPEN	USB JTAG Debugger disconnected from the Apalis Module
CLOSED	USB JTAG Debugger connected to the Apalis Module

If an external JTAG debugger is used with an Apalis Evaluation Board, jumper JP21 should be removed. Simultaneous use of the onboard and external JTAG Debugger is not allowed. Violating this requirement may damage Debuggers or the Apalis Evaluation Board. By default, jumper JP21 is not assembled on the Apalis Evaluation Board.

2.18 Recovery Mode

The recovery mode feature allows for flashing of new firmware to Apalis Systems on Module.

The recovery signal of the Apalis SoMs is exposed at pin 63 (TS1) of the Apalis type-specific connector (X38).

The polarity of the RECOVERY signal is not consistent for the Apalis SoMs family.
Please check the Apalis Module datasheet before setting the RECOVERY signal polarity.

To configure the recovery signal polarity, the jumper JP29 is used:

Connector type: 1×3 Pin Header Male, 2.54 mm Pitch

Table 69: Recovery Mode Jumper Configuration (JP29)

Jumper Position	Description
1 - 2	Recovery signal polarity is Active-Low
2 - 3	Recovery signal polarity is Active-High

To put the Apalis SoM into the recovery mode, the following steps must be taken:

1. Set the “RECOVERY POLARITY” jumper (JP29).
2. Power on the board: Press and release the “ON/OFF” button (SW9).
3. Press and hold the “RECOVERY” button (SW11).
4. Press and release the “RESET” button (SW10).
5. Wait for a few seconds.
6. Release the “RECOVERY” button (SW11).

2.19 Low-speed I/O pins configuration

The low-speed I/O pins breakout connectors offer the flexibility to map the I/O pins of the Apalis module to on-board functionalities or to external hardware.

The factory setting is a straight-through jumper setting, with the X3-A row connected straight to the X3-B row, for example. This is also true for the connectors X6 and X9.

All signals residing on the male headers are also available on female connectors in parallel to allow easy measurement, probing, and re-routing.

To map the MXM3 pin with the corresponding SoC ball name, which is specific to individual Apalis modules, please refer to the applicable Apalis module datasheet.

2.19.1 Low-speed I/O pins 1 Male (X3)

Connector Type: 2×40Pin Male, 2.54mm

Table 70: Low-speed I/O pins 1 Male (X3)

SoM Side			Peripheral Side		I/O Type	Voltage	Pull-up/Pull-down	Description
MXM3 Pin	Signal Name	Pin	Pin	Signal Name				
	3.3V_SW	A1	B1	3.3V_SW	PWR	+3.3V		+3.3V switchable power supply output
35	MXM3_35	A2	B2	SATA1_ACT#	I/O	+3.3V		SATA activity signal
17	MXM3_17	A3	B3	GPIO8	I/O	+3.3V		General-purpose I/O
15	MXM3_15	A4	B4	GPIO7	I/O	+3.3V		
13	MXM3_13	A5	B5	GPIO6	I/O	+3.3V		
11	MXM3_11	A6	B6	GPIO5	I/O	+3.3V		
7	MXM3_7	A7	B7	GPIO4	I/O	+3.3V		
5	MXM3_5	A8	B8	GPIO3	I/O	+3.3V		
3	MXM3_3	A9	B9	GPIO2	I/O	+3.3V		
1	MXM3_1	A10	B10	GPIO1	I/O	+3.3V		
	GND	A11	B11	GND	PWR			
8	MXM3_8	A12	B12	PWM4	O	+3.3V		General-purpose PWM output
6	MXM3_6	A13	B13	PWM3	O	+3.3V		
4	MXM3_4	A14	B14	PWM2	O	+3.3V		
2	MXM3_2	A15	B15	PWM1	O	+3.3V		
	3.3V_SW	A16	B16	3.3V_SW	PWR	+3.3V		+3.3V switchable power supply output
12	MXM3_12	A17	B17	CAN1_RX	I	+3.3V		CAN1 receive signal
14	MXM3_14	A18	B18	CAN1_TX	O	+3.3V		CAN1 transmitting signal
16	MXM3_16	A19	B19	CAN2_RX	I	+3.3V		CAN2 receive signal
18	MXM3_18	A20	B20	CAN2_TX	O	+3.3V		CAN2 transmitting signal
158	MXM3_158	A21	B21	CAN1_PWR_EN	O	+1.8V/+3.3V		CAN1 transceiver enable output
156	MXM3_156	A22	B22	CAN2_PWR_EN	O	+1.8V/+3.3V		CAN2 transceiver enable output

Continued on next page

Table 70: Low-speed I/O pins 1 Male (X3) (Continued)

SoM Side			Peripheral Side		I/O Type	Voltage	Pull-up/Pull-down	Description
MXM3 Pin	Signal Name	Pin	Pin	Signal Name				
	GND	A23	B23	GND	PWR			
37	MXM3_37	A24	B24	WAKE1_MICO#	I	+3.3V	5.1k to 3.3V_SW	Active low Apalis module wake input signal
24	MXM3_24	A25	B25	POWER_ENABLE_MOCI	O	+3.3V	100k to GND	Signal for enabling onboard peripherals' voltage rail
26	MXM3_26	A26	B26	RESET_MOCI#	O	+3.3V		Active low reset output for the onboard peripherals
28	MXM3_28	A27	B27	RESET_MICO#	I	+3.3V		Active low reset input for the Apalis module
	GND	A28	B28	GND	PWR			
	3.3V_SW	A29	B29	3.3V_SW	PWR	+3.3V		+3.3V switchable power supply output
72	MXM3_72	A30	B30	USBO1_ID	PWR	+3.3V	10k to 3.3V_SW	ID pin of the USBO1 port used in DRP (OTG) mode
84	MXM3_84	A31	B31	USBH_EN	I	+3.3V	10k to GND	Enable signal for the bus voltage output in host mode for the USBH port
96	MXM3_96	A32	B32	USBH_OC#	I/O	+3.3V	10k to 3.3V_SW	Overcurrent condition input signal for the USBH port
262	MXM3_262	A33	B33	USBO1_OC#	I/O	+3.3V		Overcurrent condition input signal for the USBO1 port
274	MXM3_274	A34	B34	USBO1_EN	I/O	+3.3V	10k to GND	Enable signal for the bus voltage output in host mode for the USBO1 port
	3.3V_SW	A35	B35	3.3V_SW	PWR	+3.3V		+3.3V switchable power supply output
138	MXM3_138	A36	B36	UART4_TXD	O	+3.3V		UART4 port transmission signal
140	MXM3_140	A37	B37	UART4_RXD	I	+3.3V		UART4 port receive signal
134	MXM3_134	A38	B38	UART3_TXD	O	+3.3V		UART3 port transmission signal
136	MXM3_136	A39	B39	UART3_RXD	I	+3.3V		UART3 port receive signal
	GND	A40	B40	GND	PWR			

2.19.2 Low-speed I/O pins 1 Female (X2)

Connector Type: 1×40Pin Female, 2.54mm

Pinout identical to X3 Pins A1 to A40

2.19.3 Function 1 Female (X4)

Connector Type: 1×40Pin Female, 2.54mm

Pinout identical to X3 Pins B1 to B40

2.19.4 Low-speed I/O pins 2 Male (X6)

Connector Type: 2×40Pin Male, 2.54mm

Table 71: Low-speed I/O pins 2 Male (X6)

SoM Side			Peripheral Side		I/O Type	Voltage	Pull-up/Pull-down	Description
MXM3 Pin	Signal Name	Pin	Pin	Signal Name				
207	MXM3_207	B1	A1	I2C2_DDC_SCL	I/O	+3.3V	1.8k to 3.3V_SW	DDC Interface Clock
205	MXM3_205	B2	A2	I2C2_DDC_SDA	I/O	+3.3V	1.8k to 3.3V_SW	DDC Interface Data
217	MXM3_217	B3	A3	SPDIF_IN	I	+3.3V		SPDIF digital audio input
215	MXM3_215	B4	A4	SPDIF_OUT	O	+3.3V		SPDIF digital audio output
204	MXM3_204	B5	A5	DAP1_SYNC	I/O	+3.3V		I2S Field Select (Transmit Frame Sync)
202	MXM3_202	B6	A6	DAP1_D_IN	I	+3.3V		I2S Data Input
200	MXM3_200	B7	A7	DAP1_BIT_CLK	I/O	+3.3V		I2S Serial Clock (Transmit Bit Clock)
198	MXM3_198	B8	A8	DAP1_RESET#	O	+3.3V		I2S Audio codec RESET output
196	MXM3_196	B9	A9	DAP1_D_OUT	O	+3.3V		I2S Data Output
194	MXM3_194	B10	A10	DAP1_MCLK	O	+3.3V		I2S Master clock output
190	MXM3_190	B11	A11	SD1_CD#	I	+3.3V	10k to 3.3V_SW	SD1 Card Detection
188	MXM3_188	B12	A12	SD1_D1	I/O	+1.8V/+3.3V		SD1 Serial Data 1
186	MXM3_186	B13	A13	SD1_D0	I/O	+1.8V/+3.3V		SD1 Serial Data 0
184	MXM3_184	B14	A14	SD1_CLK	O	+1.8V/+3.3V		SD1 Serial Clock
180	MXM3_180	B15	A15	SD1_CMD	O	+1.8V/+3.3V		SD1 Serial Command
178	MXM3_178	B16	A16	SD1_D3	I/O	+1.8V/+3.3V		SD1 Serial Data 3
176	MXM3_176	B17	A17	SD1_D2	I/O	+1.8V/+3.3V		SD1 Serial Data 2
164	MXM3_164	B18	A18	MMC1_CD#	I	+3.3V	10k to 3.3V_SW	MMC1 Card Detection
162	MXM3_162	B19	A19	MMC1_D1	I/O	+1.8V/+3.3V		MMC1 Serial Data 1
160	MXM3_160	B20	A20	MMC1_D0	I/O	+1.8V/+3.3V		MMC1 Serial Data 0
	3.3V_SW	B21	A21	3.3V_SW		+3.3V		+3.3V switchable power supply output
	GND	B22	A22	GND				

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Table 71: Low-speed I/O pins 2 Male (X6) (Continued)

SoM Side			Peripheral Side		I/O Type	Voltage	Pull-up/Pull-down	Description
MXM3 Pin	Signal Name	Pin	Pin	Signal Name				
154	MXM3_154	B23	A23	MMC1_CLK	O	+1.8V/+3.3V		MMC1 Serial Clock
152	MXM3_152	B24	A24	SD1_PWR_CTRL	O	+1.8V/+3.3V		SD1 Card power control output
150	MXM3_150	B25	A25	MMC1_CMD	O	+1.8V/+3.3V		MMC1 Serial Command
148	MXM3_148	B26	A26	MMC1_PWR_CTRL	O	+1.8V/+3.3V		MMC/SD Card power power control output
146	MXM3_146	B27	A27	MMC1_D3	I/O	+1.8V/+3.3V		MMC1 Serial Data 3
144	MXM3_144	B28	A28	MMC1_D2	I/O	+1.8V/+3.3V		MMC1 Serial Data 2
132	MXM3_132	B29	A29	UART2_RXD	I	+3.3V		UART2 port Receive Data (RXD)
130	MXM3_130	B30	A30	UART2_CTS	I	+3.3V		UART2 port Clear to Send (CTS)
128	MXM3_128	B31	A31	UART2_RTS	O	+3.3V		UART2 port Request to Send (RTS)
126	MXM3_126	B32	A32	UART2_TXD	O	+3.3V		UART2 port Transmit Data (TXD)
124	MXM3_124	B33	A33	UART1_DCD	I	+3.3V		UART1 port Data Carrier Detect (DCD)
122	MXM3_122	B34	A34	UART1_RI	I	+3.3V		UART1 port Ring Indicator (RI)
120	MXM3_120	B35	A35	UART1_DSR	I	+3.3V		UART1 port Data Set Ready (DSR)
118	MXM3_118	B36	A36	UART1_RXD	I	+3.3V		UART1 port Receive Data (RXD)
116	MXM3_116	B37	A37	UART1_CTS	I	+3.3V		UART1 port Clear to Send (CTS)
114	MXM3_114	B38	A38	UART1_RTS	O	+3.3V		UART1 port Request to Send (RTS)
112	MXM3_112	B39	A39	UART1_TXD	O	+3.3V		UART1 port Transmit Data (TXD)
110	MXM3_110	B40	A40	UART1_DTR	O	+3.3V		UART1 port Data Terminal Ready (DTR)

2.19.5 Low-speed I/O pins 2 Female (X5)

Connector Type: 1×40Pin Female, 2.54mm

Pinout identical to X6 Pins B1 to B40

2.19.6 Function 2 Female (X7)

Connector Type: 1×40Pin Female, 2.54mm

Pinout identical to X6 Pins A1 to A40

2.19.7 Low-speed I/O pins 3 Male (X9)

Connector Type: 2×40Pin Male, 2.54mm

Table 72: Low-speed I/O pins 3 Male (X9)

SoM Side			Peripheral Side		I/O Type	Voltage	Pull-up/Pull-down	Description
MXM3 Pin	Signal Name	Pin	Pin	Signal Name				
301	MXM3_301	A1	B1	LCD1_B7	O	+3.3V		RGB LCD Blue pixel color bit 7
299	MXM3_299	A2	B2	LCD1_B6	O	+3.3V		RGB LCD Blue pixel color bit 6
297	MXM3_297	A3	B3	LCD1_B5	O	+3.3V		RGB LCD Blue pixel color bit 5
295	MXM3_295	A4	B4	LCD1_B4	O	+3.3V		RGB LCD Blue pixel color bit 4
293	MXM3_293	A5	B5	LCD1_B3	O	+3.3V		RGB LCD Blue pixel color bit 3
291	MXM3_291	A6	B6	LCD1_B2	O	+3.3V		RGB LCD Blue pixel color bit 2
289	MXM3_289	A7	B7	LCD1_B1	O	+3.3V		RGB LCD Blue pixel color bit 1
287	MXM3_287	A8	B8	LCD1_B0	O	+3.3V		RGB LCD Blue pixel color bit 0
283	MXM3_283	A9	B9	LCD1_G7	O	+3.3V		RGB LCD Green pixel color bit 7
281	MXM3_281	A10	B10	LCD1_G6	O	+3.3V		RGB LCD Green pixel color bit 6
279	MXM3_279	A11	B11	LCD1_G5	O	+3.3V		RGB LCD Green pixel color bit 5
277	MXM3_277	A12	B12	LCD1_G4	O	+3.3V		RGB LCD Green pixel color bit 4
275	MXM3_275	A13	B13	LCD1_G3	O	+3.3V		RGB LCD Green pixel color bit 3
273	MXM3_273	A14	B14	LCD1_G2	O	+3.3V		RGB LCD Green pixel color bit 2
271	MXM3_271	A15	B15	LCD1_G1	O	+3.3V		RGB LCD Green pixel color bit 1
269	MXM3_269	A16	B16	LCD1_G0	O	+3.3V		RGB LCD Green pixel color bit 0
265	MXM3_265	A17	B17	LCD1_R7	O	+3.3V		RGB LCD Red pixel color bit 7
263	MXM3_263	A18	B18	LCD1_R6	O	+3.3V		RGB LCD Red pixel color bit 6
261	MXM3_261	A19	B19	LCD1_R5	O	+3.3V		RGB LCD Red pixel color bit 5
259	MXM3_259	A20	B20	LCD1_R4	O	+3.3V		RGB LCD Red pixel color bit 4
257	MXM3_257	A21	B21	LCD1_R3	O	+3.3V		RGB LCD Red pixel color bit 3
255	MXM3_255	A22	B22	LCD1_R2	O	+3.3V		RGB LCD Red pixel color bit 2

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Table 72: Low-speed I/O pins 3 Male (X9) (Continued)

SoM Side			Peripheral Side		I/O Type	Voltage	Pull-up/Pull-down	Description
MXM3 Pin	Signal Name	Pin	Pin	Signal Name				
253	MXM3_253	A23	B23	LCD1_R1	O	+3.3V		RGB LCD Red pixel color bit 1
251	MXM3_251	A24	B24	LCD1_R0	O	+3.3V		RGB LCD Red pixel color bit 0
249	MXM3_249	A25	B25	LCD1_DE	O	+3.3V		RGB LCD Data enable signal output
247	MXM3_247	A26	B26	LCD1_HSYNC	O	+3.3V		RGB LCD Horizontal synchronization output
245	MXM3_245	A27	B27	LCD1_VSYNC	O	+3.3V		RGB LCD Vertical synchronization output
243	MXM3_243	A28	B28	LCD1_PCLK	O	+3.3V		RGB LCD Pixel clock signal output
239	MXM3_239	A29	B29	PWM_BKL1	O	+3.3V		Display brightness control PWM output
286	MXM3_286	A30	B30	BKL1_ON	O	+3.3V		Display backlight ENABLE output
235	MXM3_235	A31	B31	SPI2_CLK	O	+3.3V		SPI2 clock signal
233	MXM3_233	A32	B32	SPI2_CS	O	+3.3V		SPI2 chip select signal
231	MXM3_231	A33	B33	SPI2_MOSI	O	+3.3V		SPI2 master output signal
229	MXM3_229	A34	B34	SPI2_MISO	I	+3.3V		SPI2 master input signal
227	MXM3_227	A35	B35	SPI1_CS	O	+3.3V		SPI1 chip select signal
225	MXM3_225	A36	B36	SPI1_MOSI	O	+3.3V		SPI1 master output signal
223	MXM3_223	A37	B37	SPI1_MISO	I	+3.3V		SPI1 master input signal
221	MXM3_221	A38	B38	SPI1_CLK	O	+3.3V		SPI1 clock signal
211	MXM3_211	A39	B39	I2C1_SCL	I/O	+3.3V	1.8k to 3.3V_SW	General-purpose I^2C bus clock signal
209	MXM3_209	A40	B40	I2C1_SDA	I/O	+3.3V	1.8k to 3.3V_SW	General-purpose I^2C bus data signal

2.19.8 Low-speed I/O pins 3 Female (X8)

Connector Type: 1×40Pin Female, 2.54mm

Pinout identical to X9 Pins A1 to A40

2.19.9 Function 3 Female (X10)

Connector Type: 1×40Pin Female, 2.54mm

Pinout identical to X9 Pins B1 to B40

3 Operating Conditions

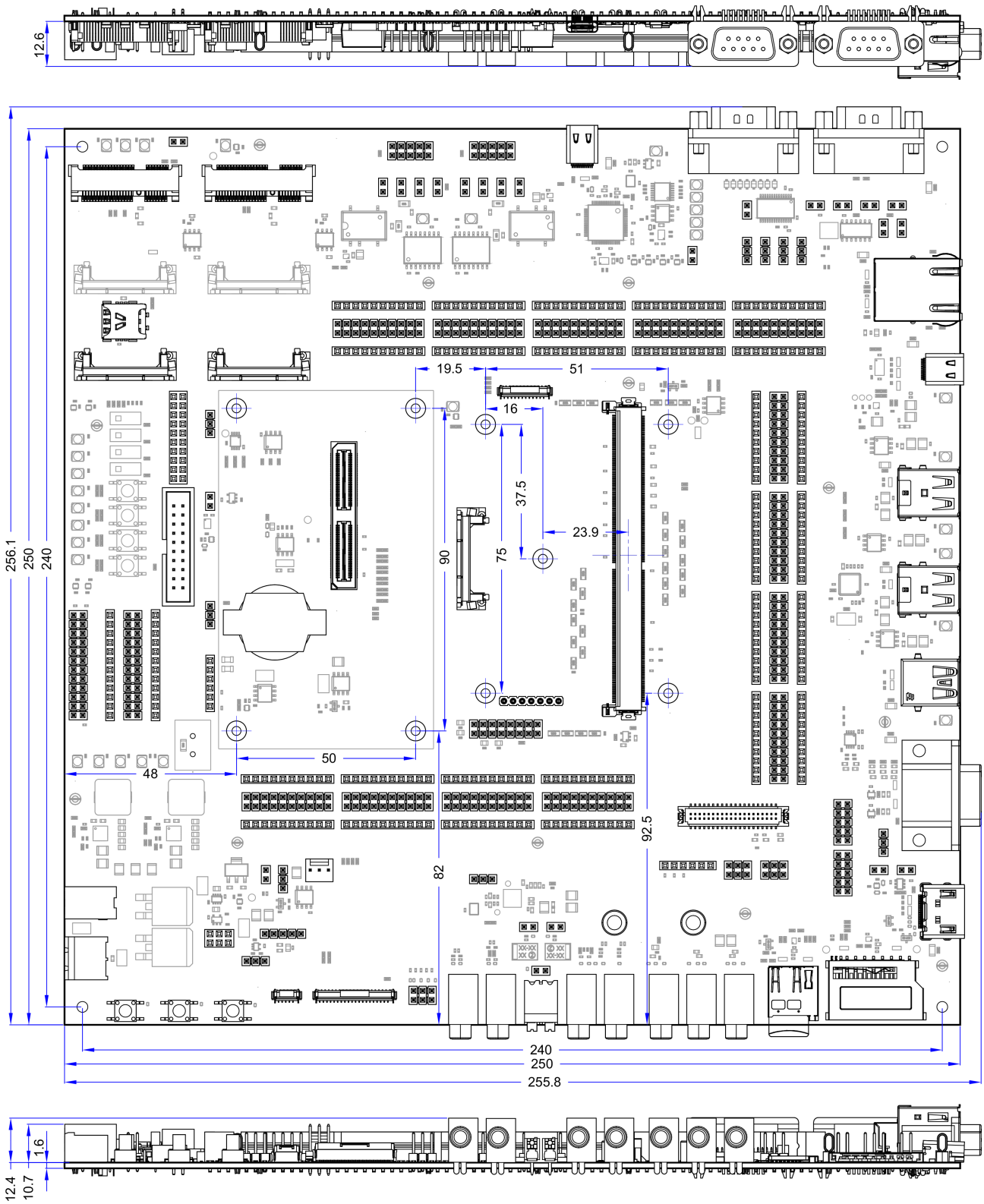
3.1 Operating Temperature Range

- 0 to +70°C

4 Mechanical Data

4.1 Apalis Evaluation Board Dimentions

Figure 6: Apalis Evaluation Board dimensions (in millimeters)



5 Design Data

The design data for Toradex carrier boards are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the carrier board design data, please use the web link below:

https://developer.toradex.com/carrier-board-design/reference-designs/#apalis-evaluation-board/

6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at: http://www.toradex.com/support/product-compliance

7 Device and Documentation Support

7.1 Trademarks

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