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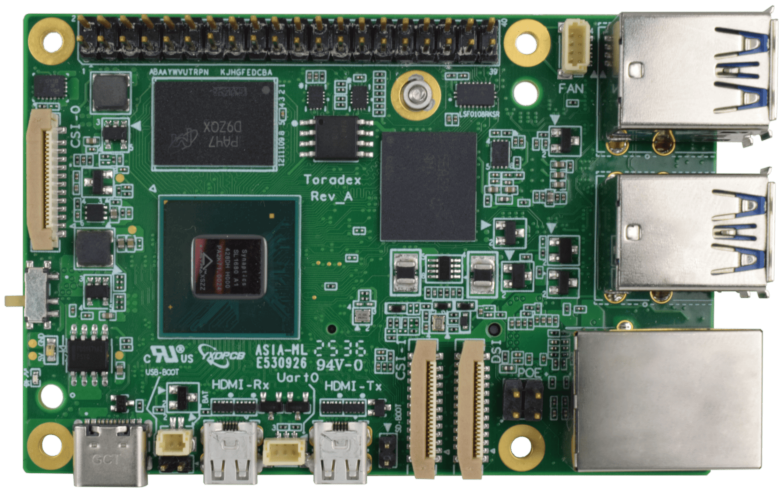
Luna SL1680 SBC

Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
03-Nov-2025	Rev. 0.1	V1.0	Initial documentation
10-Apr-2026	Rev. 0.2	V1.0	Section 2: Update top side connectors with the fan connector on Figure 2 and Table 4

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Abbreviation	Explanation
ADC	Analog to Digital Converter
BTB	Board To Board
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.

Continued on next page

Abbreviations (Continued)

Abbreviation	Explanation
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1 Introduction

1.1 Purpose of the Datasheet

This document describes the hardware characteristics and capabilities of the Luna SL1680 Single-Board Computer (SBC). It is intended as a technical reference for hardware designers, system integrators, and developers working with this product.

For the latest information regarding software features and integration, please visit the Luna SL1680 SBC product page:

https://www.toradex.com/single-board-computers/sl1680

1.2 Synaptics SL1680 System-on-Chip (SoC) Overview

The **Luna SL1680 Single-Board Computer (SBC)** is a platform designed for commercial and light industrial applications. It is intended for integration into end products, offering long-term reliability, extended lifetime, and built-in AI capabilities to meet edge computing requirements. At its core, the Luna SL1680 SBC features the **Synaptics SL1680 System-on-Chip (SoC)**, a high-performance processor designed for **AI-native edge IoT** applications. From a hardware perspective, the Luna SL1680 SBC maintains mechanical and electrical compatibility with a wide range of commercially available SBCs, enabling developers to upgrade to a more robust and AI-ready solution without significant redesign effort while preserving an optimal price-to-performance ratio.

Key characteristics of the Cortex®-A73 cores:

- **64-bit ARM®v8-A architecture quad-core ARM® Cortex®-A73** processor cluster.
- Enhanced integer and floating-point operation capabilities with dedicated **64 kB instruction** and **32 kB data caches per core**.
- A shared **1 MB L2 cache** that reduces memory latency and improves overall multicore efficiency.
- Support for **ARM® NEON SIMD** extensions and cryptographic instructions for accelerated media processing and security.
- Clock speed **up to 2.1 GHz**.
- **40,000 DMIPS** performance rating.

Supplementing the main CPU cluster, the SL1680 features an integrated **ARM® Cortex®-M3 processor** dedicated to security and system management tasks.

Key characteristics of the Cortex®-M3 core:

- Clock Speed: **250 MHz**.
- Primary Functions:
  - **Secure Boot** and trusted system initialization.
  - Hardware-accelerated **cryptographic operations**.
  - System monitoring and management tasks.
- Isolation: Operates independently from the main CPU cluster to ensure **secure execution**.

Table 1: CPU

Parameter	Luna SL1680 SBC 16GB LPDDR4
SoC	SL1680
Cortex-A73 Cores	4
L1 Instruction Cache per core	64 kB
L1 Data Cache per core	32 kB
L2 Cache shared between cores	1 MB
L3 Cache shared between cores	–
NPU Performance (TOPS)	>7.9 TOPS (INT8 dense)
GPU - FLOPs (FP32)	Imagination PowerVR Series9XE GE9920 - 45 GFLOPS
DRAM Controller	64-bit LPDDR4/LPDDR4x up to 3733 MT/s
Video Codec Support	Decode: AV1, H.265/264, VP8, VP9, MPEG-2
	Encode: H.264, VP8
Security Features	Secure Boot, Cryptographic accelerators
Multimedia Support	ISP with dual camera support, 4K video encode/decode
Power Management	DVFS support, Always-On domain with wake-up events

1.2.1 GPU and NPU Features

The GPU of the SoC offers a balanced combination of 2D/3D acceleration and compute performance. It supports widely used graphics APIs such as

- OpenGL® ES™ 1.1, 2.0, 3.0, 3.1, 3.2,
- OpenCL™ 1.2,
- Vulkan® 1.1,
- Andriod™ NN HAL,
- DirectFB,
- Renderscript.

This delivers responsive graphics, advanced user interfaces, and accelerated compute workloads within power-efficient constraints suitable for the Luna SL1680 SBC environment.

Table 2: GPU

Parameter	Luna SL1680 SBC
GPU Model	Imagination PowerVR Series9XE GE9920
2D Acceleration	Yes
3D Acceleration	Yes
FLOPs	FP32: 45 GFLOPS
L2 Cache	Not specified
MSAA anti-aliasing	up to 8x
OpenCL	up to 1.2

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Table 2: GPU (Continued)

Parameter	Luna SL1680 SBC
OpenGL ES	up to 3.2
Vulkan	1.1
DirectFB	Supported
Hardware Video Codec	H.264, H.265, VP8 (Encode/Decode)

Supplementing the GPU cluster, the SL1680 features an integrated **Neural Processing Unit** (**NPU**) dedicated to accelerating artificial intelligence (AI) and machine learning (ML) workloads. Delivering up to **7.9+ TOPS** of performance, being optimized for **TensorFlow Lite** inferencing through the Synaptics SyNAP toolkit.

1.2.2 Image Signal Processor (ISP)

The Synaptics SL1680 integrates a high-performance Image Signal Processor Subsystem (ispSS) for advanced camera and image processing applications. It supports dual-camera input and a wide range of image processing functions, optimized for embedded vision systems.

ISP Highlights:

- **Camera Support:**
  - **Dual MIPI CSI** interfaces (4-lane + 2-lane).
  - Lane speed up to **2.5 Gbps per lane**.
  - **Single-camera** video capture: **up to 4K @ 60 fps**.
  - **Dual-camera** video capture: **up to 4K @ 30 fps**.
- **Image Processing Features:**
  - **Multi-exposure** staggered DOL HDR (up to 3 exposures).
  - Local tone mapping, spatial and temporal noise reduction.
  - **Autofocus** (AF), **auto exposure** (AE), **auto white balance** (AWB).
- **Performance & Power Efficiency:**
  - 128-bit AMBA AXI-4 memory interface for high-throughput data handling
  - AMBA AHB interface for programmatic control and configuration

1.2.3 Video Post Processing (VPP)

The SL1680 integrates a Video Post Processing (VPP) module for high-fidelity multimedia output, supporting multiple video/graphics planes, flexible format conversions, and high-resolution display interfaces.

VPP Highlights:

- **Video/Graphics Support:**
  - Up to 4 video or graphics planes loaded from DRAM.
  - Flexible input/output format conversion, scaling, positioning, and blending.
- **Video Encoding/Decoding:**
  - **Decoding:** H.264, H.265, VP8.
  - **Encoding:** H.264, VP8.
- **Display Output:**
  - **HDMI TX:** UHD 3840x2160 @ 60 Hz (HDMI 2.1).
  - **MIPI DSI TX:** UHD 3840x2160 @ 30 Hz.

- **Video Input:**
  - **HDMI RX:** UHD 3840x2160 @ 60 Hz (HDMI 2.1).
- **Video Quality & Processing:**
  - **Input pixel format:** RAW (RGGB), 10/12-bit per pixel.
  - Supports **SDR - HDR conversions** for tone mapping.

1.3 Single-Board Computer Main Features

The Luna SL1680 SBC incorporates advanced processing, AI, multimedia, security, memory, connectivity, and I/O capabilities designed to meet demanding embedded application requirements. It offers **multimedia support** with an integrated ISP capable of handling up to **two cameras** and **VPU codecs** for efficient video processing. Security is reinforced through **secure boot** and **hardware cryptographic accelerators**, ensuring data integrity and protection. The system supports up to **4 GB of LPDDR4 RAM** on a 32-bit bus and up to **256 GB of eMMC flash storage** for robust performance and reliability. Additionally, it provides **optional wireless connectivity** with **Wi-Fi** and **Bluetooth**, using an **M.2 (Key E)** expansion slot, which may be used for other peripherals if not used by this module, complemented by a wide range of **I/O interfaces**, including **Micro-HDMI** (one input receiver and one output transmitter, **Gigabit Ethernet**, and **USB 3.x**).

1.3.1 Memory

The Luna SL1680 SBC integrates dual-channel LPDDR4x DRAM modules configured in a 32-bit wide interface to the SL1680 SoC. The memory subsystem is powered through dedicated voltage rails for core (VDD1, VDD2) and I/O (VDDQ) supplies, all monitored and regulated to meet LPDDR4x power sequencing requirements. The DRAM devices include on-die termination and advanced calibration capabilities to optimize signal integrity and timing margins.

Memory initialization follows strict power-up sequencing, as described in Power-Up Sequence, with simultaneous ramping of power rails ensuring data integrity and reliable self-refresh capability. The memory controller in SL1680 manages full training and calibration during boot, establishing the timing between the SoC and DRAM for seamless operation.

Key Features:

- **High-Speed Data Transfer:** Supports data rates up to approximately 4266 MT/s enabling efficient memory access.
- **Low Power Consumption:** Operates at 1.1 V core voltage and 1.8 V I/O voltage, including features such as on-die termination to reduce power usage.
- **Dual 16-bit Channels:** Enables a 32-bit wide data path through two independent channels, enhancing parallelism and throughput.
- **Advanced Timing:** Programmable read/write latencies and burst lengths supporting efficient data transfers.
- **High Capacity:** Available in densities up to 32 Gb per chip, supporting module capacities up to 16 GB or more.
- **Enhanced Reliability:** Optional on-chip ECC, signal integrity improvements, and optimized refresh schemes.
- **Light Industrial Grade:** Available variants support extended temperature ranges (−25 °C to +85 °C).

Performance Parameters

- Clock frequencies typically supporting up to 2133 MHz per channel (4266 MT/s data rate).
- Burst lengths of 16 or 32 transfers.
- Adaptive refresh mechanisms for energy efficiency.

1.3.2 Storage

The Luna SL1680 SBC integrates multiple non-volatile storage options, including an on-board eMMC device and an external serial EEPROM. The eMMC device offers capacities up to 256GB and connects directly to the SL1680 SoC through a dedicated high-speed MMC/SD interface, supporting standardized signal voltages, timings, and advanced modes such as error correction and partitioning. The external EEPROM is interfaced via a dedicated SPI bus, providing robust storage for configuration parameters and system calibration data. Both storage devices ensure reliable data retention and efficient access for operating system, applications, and system functions.

Storage initialization follows the JEDEC eMMC specification with controlled power-up sequences coordinated by the SoC's bootloader to guarantee data integrity. The interface supports advanced commands for enhanced performance and reliability features such as partitioning, secure erase, and trim operations.

Key Features

- On-board **eMMC flash** with multiple capacity options – up to **256 GB** eMMC flash storage.
- **EEPROM** connected via **SPI** for configuration and calibration data.
- **MicroSD card slot** for expandable storage.

1.4 Interfaces

The Luna SL1680 SBC offers a wide set of interfaces to accommodate diverse system requirements:

- General-purpose digital I/O (**GPIO**).
- **I²C**, **SPI**, and **UART** serial buses.
- **USB 2.0 / 3.1** ports.
- **Dual Micro-HDMI** (Type D) ports:
  - One output port.
  - One input port.
- **MIPI interfaces**:
  - One 22-pin FCC **MIPI DSI** (quad lane) for display.
  - Two 22-pin FCC **MIPI CSI**: one quad lane and one dual lane for camera.
- USB ports:
  - **Four USB-A** ports (USB 3.x).
  - **USB-C** port for power input and recovery mode.
- **Gigabit Ethernet** via RJ45 connector.
- **M.2 Key E** slot supporting **PCIe**, **SDIO**, **UART**, and **PCM** interfaces.

Other Connectors

- Commercially standard 40-pin GPIO header.
- UART console header (3.3 V logic level).
- Power button.
- Fan control header.
- RTC battery header/holder.

Table 3: Luna SL1680 SBC interfaces

Parameter	Luna SL1680 Single-Board Computer
Analog	
Analog Input	2x ADC channels (12-bit, 1.2 V full scale)
Audio	
Audio Interfaces	2x I^2S interface / 2x PDM
Camera	
MIPI CSI	2x (1x Quad Lane + 1x Dual Lane) up to 4K60p/4K30p support
Display	
HDMI	1x Receiver + 1x Transmitter
MIPI DSI	1x Quad Lane 4K30p/2K60p support
Low Speed	
GPIO	22 GPIOs available on 40-pin connector[1]
I^2C	1x[2]
PWM	4x PWM outputs[1]
SPI	1x
UART	3x[3]
Network	
Bluetooth	Support for Bluetooth 5.3[4]
Ethernet	1x GbE
Wi-Fi	Module dependent[4]
Storage	
SDIO/SD/MMC	2x 1x MicroSD slot + 1x built-in eMMC interface
USB	
USB 3.x *Host and Client*	4x SuperSpeed USB Type-A (Host)

[1] The number of pins accounts for the use of certain pins configured as alternate functions.
[2] Available on the M.2 PCIe connector.
[3] UART0 and UART2 accessible on the 40-pin connector, and UART3 available through the PCIe M.2 connector.
[4] Bluetooth and Wi-Fi connectivity are provided via a separate PCIe module and the specifications depend on the module.

1.5 Reference Documents

1.5.1 Synaptics SL1680

Additional details about the SL1680 SoC are available in the datasheet and reference manual provided by Synaptics.

https://www.synaptics.com/assets/product-brief/astra-sl1680-embedded-iot-processor

1.5.2 I/O Expanders

The Luna SL1680 SBC features two on-module I/O expanders, both being the FXL6408UMX from Onsemi.

https://www.onsemi.com/products/timing-logic-memory/standard-logic/i-o-expanders/fxl6408

1.5.3 Ethernet Transceiver

The Luna SL1680 SBC utilizes the RTL8211F-CG industrial-temperature, robust Gigabit Ethernet PHY transceiver from Realtek.

https://www.realtek.com/Product/Index?id=3975&cate_id=786

1.5.4 Real-Time Clock (RTC)

The Luna SL1680 SBC features the low-power Analog Devices DS1339AU+T real-time clock.

https://www.analog.com/en/products/ds1339a.html

1.5.5 Wi-Fi and Bluetooth Module

The Luna SL1680 SBC **WB variants** provide integrated wireless connectivity via an external **Wi-Fi and Bluetooth** module. The module is installed on the **M.2 (NGFF) socket, Key E**. The M.2 Key-E interface delivers PCIe and SDIO/UART signals required by the Wi-Fi/BT module and ensures broad compatibility with alternate wireless solutions that follow the same form factor.

Information about pre-certified antennas and cables are coming soon.

2 System Architecture Overview

2.1 Functional Overview

The Luna SL1680 SBC features a system architecture engineered to deliver high performance, efficient power utilization, and robust expandability. At its core, the design integrates a high-performance SoC coupled with dedicated power management circuitry, high-speed memory subsystems, and storage interfaces. Comprehensive connectivity options, including high-speed multimedia interfaces and versatile I/O expansion, enable seamless system integration across diverse embedded and edge computing applications.

2.1.1 SoC Overview (CPU, GPU, NPU)

At the core, the system-on-chip (SoC) features a quad-core ARM® Cortex®-A73 CPU delivering high processing throughput alongside an integrated Neural Processing Unit (NPU) capable of 7.9+ TOPS for AI acceleration. Graphics processing is handled by an Imagination PowerVR Series9XE GE9920 GPU, supporting high-performance 3D and multimedia workloads, including simultaneous image processing engines and video codecs.

2.1.2 PMIC and Power Architecture

The power management architecture includes a highly integrated PMIC configured to efficiently regulate multiple power rails required by the SoC and peripherals. The design ensures stable supply voltages with minimal noise and optimized power sequencing strategies supporting system reliability and extended battery life where applicable.

2.1.3 Memory Subsystem

The memory subsystem supports up to 16 GB of 32-bit LPDDR4 DRAM, providing ample bandwidth and low-latency access for demanding applications. The subsystem is architected for scalability and low power consumption, ensuring system stability and responsiveness.

2.1.4 Storage Devices

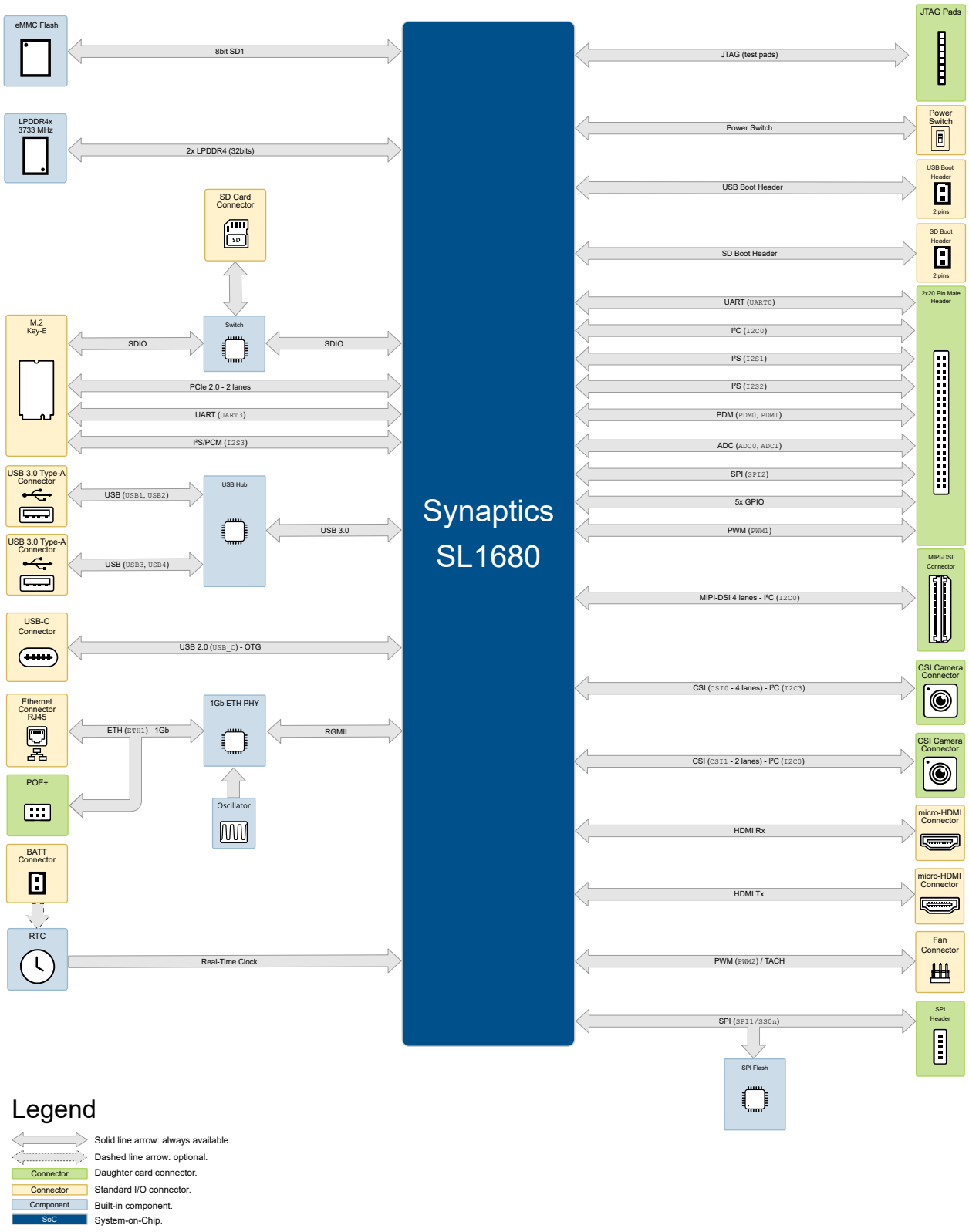
The Luna SL1680 SBC offers multiple storage options, including high-capacity on-board eMMC up to 256 GB for primary system and application data. Supplementing this is a 128 Mbit (16 MB) serial EEPROM connected via SPI for configuration and calibration data, alongside a microSD card slot for additional expandable storage needs.

2.1.5 Connectivity Controllers

The Luna SL1680 SBC incorporates a set of connectivity controllers that support a wide range of high-speed and peripheral interfaces. The platform provides Micro-HDMI output for display connectivity, Gigabit Ethernet for wired networking, multiple USB 3.x ports for high-throughput peripheral devices, and an M.2 (Key E) slot for expansion modules. Optional wireless functionality is available through PCIe-based modules supporting Wi-Fi and Bluetooth, enabling flexible integration of wireless networking and accessory solutions.

2.2 System Block Diagram

Figure 1: Block diagram



2.3 Connectors

Figure 2: Top side connectors

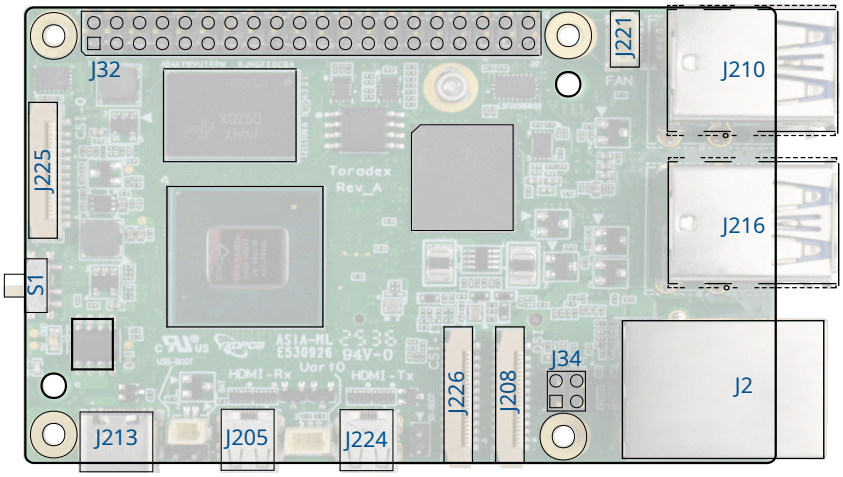


Table 4: List of top side connectors

Component	Part Number	Side	Description
Connector			
J2	HRK1-1B71PG5-36A1BB-1R	top	RJ45 connector with transformer
J32	CONN-DIP2R-40P-2R54	top	40-pin GPIO header with 2.54 mm pin spacing
J34	CONN4_2R_2R54	top	4-pin PoE header with 2.54 mm pin spacing
J205	MOLEX_467651301	top	Micro-HDMI receiver
J208	525592253	top	MIPI DSI
J210	USB-303WSD-BRY	top	Dual USB 3.0 Type-A ports, right-angle, RoHS
J216	USB-303WSD-BRY	top	Dual USB 3.0 Type-A ports, right-angle, RoHS
J221	BM04B-SRSS-TBT	top	Connector Header Surface Mount 4 position 0.039" (1.00mm)
J224	MOLEX_467651301	top	Micro-HDMI transmiter
J225	525592253	top	MIPI CSI – CSI0
J226	525592253	top	MIPI CSI – CSI1
Switch			
S1	SLW-682715-25A-SMT-TR	top	Power on/off switch

3 Luna SL1680 Main Connector

The Luna SL1680 SBC includes a comprehensive set of connectors and interfaces designed for flexibility and compatibility with common embedded ecosystems. The main connector is a standard 40-pin GPIO header, providing general-purpose I/O including power, ground, and peripheral signals.

The connection type (input, output, or input/output) is defined from the perspective of the Single-Board Computer or the System-on-Chip, unless stated otherwise.

3.1 Pin Assignment

The pin numbering of the Luna SL1680 SBC follows the industry-standard 40-pin GPIO header layout, ensuring straightforward compatibility with existing carrier boards and accessories. The pinout configuration is illustrated in Figure 3, while Table 5 details the functional assignments for each pin on the header.

Figure 3: 40-pin connector pinout

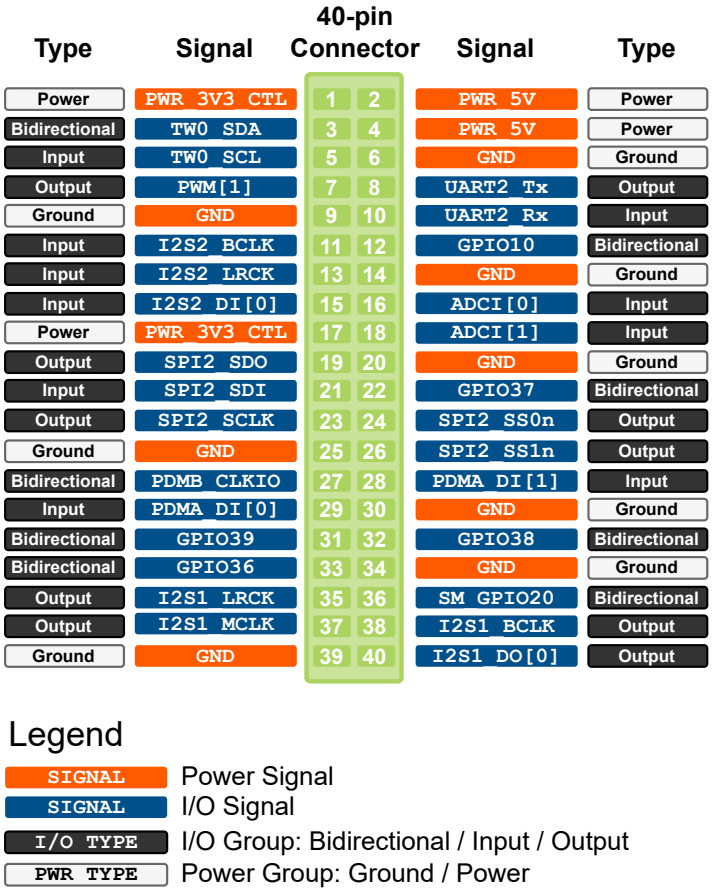


Table 5: 40 pin header

J32 pin	Luna SL1680 function	Alternate function	Reset status	Type	Description/Remarks
Odd Column					
1	PWR_3V3_CTL	–	–	PWR	3.3 V regulated power rail
3	TW0_SDA	MODE_1	InputInput[1]	I/O	I^2C data line (bidirectional) 2.2kΩ pull-up resistor
5	TW0_SCL	MODE_1	Input[1]	I	I^2C clock line (master-driven) 2.2kΩ pull-up resistor
7	PWM[1]	MODE_4	Input[1]	O	PWM channel output for control
9	GND	–	–	PWR	Ground reference
11	I2S2_BCLK	MODE_1	Input[1]	O	Bit clock for I^2S audio stream 470kΩ pull-down resistor
13	I2S2_LRCK	MODE_1	Input[1]	O	Frame clock for I^2S audio stream
15	I2S2_DI[0]	MODE_1	Input[1]	I	Data input line
17	PWR_3V3_CTL	–	–	PWR	3.3 V regulated power rail
19	SPI2_SDO	MODE_0	Input[2]	O	Serial data output (MOSI)
21	SPI2_SDI	MODE_0	Input[2]	I	Serial data input (MISO)
23	SPI2_SCLK	MODE_0	Input[2]	O	Serial clock
25	GND	–	–	PWR	Ground reference
27	PDMB_CLKIO	MODE_2	Input[2]	I/O	Clock for PDM interface B
29	PDMA_DI[0]	MODE_2	Input[1]	I	Data input channel 0 for PDM interface A
31	GPIO39	MODE_0	Input[1]	I/O	Configurable digital input/output
33	GPIO36	MODE_0	Input[1]	I/O	Configurable digital input/output
35	I2S1_LRCK	MODE_1	Input[1]	O	Frame clock
37	I2S1_MCLK	MODE_1	Input[1]	O	Master clock
39	GND	–	–	PWR	Ground reference
Even Column					
2	PWR_5V	–	–	PWR	Main 5 V power supply
4	PWR_5V	–	–	PWR	Main 5 V power supply
6	GND	–	–	PWR	Ground reference
8	UART2_Tx	MODE_5	Input	O	Serial transmit data
10	UART2_Rx	MODE_5	Input	I	Serial receive data
12	GPIO10	MODE_0	Input[1]	I/O	Configurable digital input/output
14	GND	–	–	PWR	Ground reference
16	ADCI[0]	–	Input[1]	I	Full-scale voltage: 1.2 V 1.5kΩ pull-up resistor
18	ADCI[1]	–	Input[1]	I	Full-scale voltage: 1.2 V 1.5kΩ pull-up resistor
20	GND	–	–	PWR	Ground reference
22	GPIO37	MODE_0	Input[1]	I/O	Configurable digital input/output
24	SPI2_SS0n	MODE_0	Input[2]	O	Chip select 0 (active low)
26	SPI2_SS1n	MODE_1	Input[2]	O	Chip select 1 (active low)
28	PDMA_DI[1]	MODE_2	Input	I	Data input channel 1 for PDM interface

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Table 5: 40 pin header (Continued)

J32 pin	Luna SL1680 function	Alternate function	Reset status	Type	Description/Remarks
30	GND	–	–	PWR	Ground reference
32	GPIO38	MODE_0	Input[1]	I/O	Configurable digital input/output
34	GND	–	–	PWR	Ground reference
36	SM_GPIO20	MODE_1	Input[1]	I/O	Configurable digital input/output 3.3 V signal (level shifter data rate: 100 Mbps)
38	I2S1_BCLK	MODE_1	Input[1]	O	Bit clock
40	I2S1_DO[0]	MODE_1	Input[1]	O	Data output line

[1] All GPIO-type pins default to input mode with internal or external pull-up resistors enabled at reset, ensuring defined logic levels without actively driving any pins high or low.
[2] Alternate function pins may be configured as inputs.

3.2 Function Multiplexing

Low-speed I/O pins on the LM 1680 SoC support **up to seven alternate functions**. Most of these pins can also be used as GPIOs (general-purpose I/O, sometimes referred to as digital I/O). For example, the signal connected to the pin 10 of the 40-pin header (J32) exposes the SoC alternate function **UART2_Rx**, which is the Luna SL1680 SBC standard function. In addition to this UART function, the pin can also be configured as:

- **SM_PWR_OK** (input): monitors power supply stability and indicates when power is stable and ready;
- **SM_SPI2_SS3n** (output): active-low chip select signal for the third slave device on SPI bus 2;
- **SM_GPIO** (input/output): configurable general-purpose digital input/output pin;
- **PWM[1]** (output): pulse-width modulation channel 1 output;
- **OS_TIMER** (output): outputs timer pulses used for system timing and scheduling functions;
- **SM_URT1_CTSn** (input): active-low clear-to-send flow control signal for UART interface 1.

Some alternate functions are available on more than one pin. Care must be taken to avoid assigning the same function to multiple pins simultaneously, as this can result in system instability or undefined behavior.

Table 6 lists all pins that support alternate functions, along with the alternate functions available for each pin. Alternate functions highlighted in bold indicate the primary interfaces selected for optimal compatibility.

Pin Reset Status
At reset, all GPIO-type pins default to **input mode** with internal or external pull-up resistors enabled, ensuring defined logic levels and preventing floating inputs. No GPIO pins are actively driven high or low by default.
All **alternate-function pins** are also initialized as inputs, maintaining a safe, high-impedance state until reconfigured by software.

Table 6: Alternate functions

J32 pin	Luna SL1680 SBC function	SoC ball name	Mode_0	Mode_1	Mode_2	Mode_3	Mode_4	Mode_5	Mode_6	Mode_7	MODE_STRAP
3	TW0_SDA	TW0_SDA	IO:GPIO[46]	**IO:TW0_SDA**	–	–	–	–	–	O:PHY_DBG[11]	–
5	TW0_SCL	TW0_SCL	IO:GPIO[47]	**IO:TW0_SCL**	–	–	–	–	–	O:PHY_DBG[11]	–
7	PWM[1]	SPI1_SS1n	IO:GPIO[53]	O:SPI1_SS1n	I:STS7_VALD	–	**O:PWM[1]**	–	–	O:PHY_DBG[14]	–
8	UART2_Tx	SM_SPI2_SS2n	O:MON_VDD1P8_OUT_1P05	O:SM_SPI2_SS2n	IO:SM_GPIO[15]	O:PWM[0]	O:SM_TIMER[0]	**O:URT2_TXD**	–	O:CLK_25M	–
10	UART2_Rx	SM_SPI2_SS3n	I:SM_PWR_OK	O:SM_SPI2_SS3n	IO:SM_GPIO[14]	O:PWM[1]	O:SM_TIMER[1]	**I:URT2_RXD**	–	I:SM_URT1_CTSn	–
11	I2S2_BCLK	I2S2_BCLK	IO:GPIO[12]	**IO:I2S2_BCLKIO**	IO:PDMA_CLKIO	–	–	–	–	–	–
12	GPIO10	I2S2_DI[1]	**IO:GPIO[10]**	I:I2S2_DI[1]	I:PDMA_DI[2]	I:STS4_VALD	–	–	–	–	–
13	I2S2_LRCK	I2S2_LRCK	IO:GPIO[13]	**IO:I2S2_LRCKIO**	–	–	–	–	–	–	–
15	I2S2_DI[0]	I2S2_DI[0]	IO:GPIO[11]	**I:I2S2_DI[0]**	I:PDMA_DI[3]	–	–	–	–	–	–
19	SPI2_SDO	SM_SPI2_SDO	**O:SM_SPI2_SDO**	IO:SM_GPIO[13] output only	O:URT2_RTSn	–	–	–	–	–	SM_STRP[1]
21	SPI2_SDI	SM_SPI2_SDI	**IO:SM_GPIO[12]**	I:URT2_CTSn	–	–	–	–	–	–	–
22	GPIO37	STS1_SD	**IO:GPIO[37]**	I:STS1_SD	O:PWM[2]	–	–	–	–	O:PHY_DBG[6]	–
23	SPI2_SCLK	SM_SPI2_SCLK	**O:SM_SPI2_SCLK**	IO:SM_GPIO[11]	–	–	–	–	–	–	–
24	SPI2_SS0n	SM_SPI2_SS0n	**O:SM_SPI2_SS0n**	IO:SM_GPIO[17] output only	–	–	–	–	–	O:PORB_AVDD33_LV	SM_STRP[2]
26	SPI2_SS1n	SM_SPI2_SS1n	IO:SM_GPIO[16] output only	**O:SM_SPI2_SS1n**	–	–	–	–	O:SM_URT1_RTSn	O:VDD_CPU_PORB	SM_STRP[3]
27	PDMB_CLKIO	I2S2_MCLK	IO:GPIO[7]	IO:I2S2_MCLK	**IO:PDMB_CLKIO**	–	O:HDMI_FBCLK	–	–	–	–
28	PDMA_DI[1]	I2S2_DI[2]	I2S2_DI[2]	I:I2S2_DI[2]	**I:PDMA_DI[1]**	I:STS4_CLK	–	–	–	–	–
29	PDMA_DI[0]	I2S2_DI[3]	IO:GPIO[8]	I:I2S2_DI[3]	**I:PDMA_DI[0]**	I:STS4_SD	–	–	–	–	–
31	GPIO39	STS1_CLK	**IO:GPIO[39]**	I:STS1_CLK	O:PWM[0]	–	–	–	–	O:PHY_DBG[4]	–
32	GPIO38	STS1_SOP	**IO:GPIO[38]**	I:STS1_SOP	O:PWM[1]	I:STS6_CLK	–	–	–	O:PHY_DBG[5]	–
33	GPIO36	STS1_VALD	**IO:GPIO[36]**	I:STS1_VALD	O:PWM[3]	I:STS6_SD	–	–	–	O:PHY_DBG[7]	–
35	I2S1_LRCK	I2S2_LRCK	IO:GPIO[13]	**IO:I2S2_LRCKIO**	–	–	–	–	–	–	–

Continued on next page

Table 6: Alternate functions (Continued)

J32 pin	Luna SL1680 SBC function	SoC ball name	Mode_0	Mode_1	Mode_2	Mode_3	Mode_4	Mode_5	Mode_6	Mode_7	MODE_STRAP
36	SM_GPIO20	SM_HDMI_TX_HPD	I:SM_HDMI_HPD	**IO:SM_GPIO[20]**	–	–	–	–	–	–	–
37	I2S1_MCLK	I2S2_MCLK	IO:GPIO[7]	**IO:I2S2_MCLK**	IO:PDMB_CLKIO	–	O:HDMI_FBCLK	–	–	–	–
38	I2S1_BCLK	I2S1_BCLK	IO:GPIO[20]	**IO:I2S1_BCLKIO**	O:PWM[1]	–	–	–	–	O:AVIO_DBG[1]	–
40	I2S1_DO[0]	I2S1_DO[1]	IO:GPIO[17]	**O:I2S1_DO[1]**	–	I:STS2_CLK	–	–	–	O:AVIO_DBG[5]	–

4 Camera and Video Interfaces

4.1 HDMI Interface

The Luna SL1680 SBC features two dedicated micro-HDMI (type D) ports:

- One Micro-HDMI output port capable of driving displays up to 4K resolution.
- One Micro-HDMI input port supporting video capture from compatible HDMI sources.

Both HDMI ports conform to standard HDMI 2.0 specs for audio/video transmission and HDCP content protection.

Table 7: HDMI summary by function

Function	Signals	Direction HDMI input (sink)	Direction HDMI output (source)	Remarks
TMDS video data	D0±, D1±, D2±	Input	Output	High-speed differential pairs
TMDS clock	CLK±	Input	Output	Differential clock from source
DDC (EDID / HDCP)	SCL, SDA	Input (SCL), I/O (SDA)	Output (SCL), I/O (SDA)	Open-drain bus
Hot Plug Detect	HPD	Input	Output	Sink to Source
+5 V Power from source	PWR5V	Input	Output	Source supplies 5.0 V to power the sink's EDID logic
CEC	CEC	I/O bidirectional	I/O bidirectional	Shared one-wire control bus
Shields / grounds	SHLD_x, GND	–	–	Reference and EMI protection

4.1.1 HDMI Input

The **Luna SL1680 SBC** includes a **high-performance HDMI 2.1 input interface** designed for video capture, multimedia processing, and AI-vision applications. It supports a wide range of modern HDMI features for high-resolution video, advanced color formats, and reliable interoperability with consumer and professional source devices.

Key features:

- **HDMI 2.1 compliance** with **HDR10** and **HLG** support
- Input resolutions up to **2160p@60 Hz** with **YUV 4:4:4** color sampling
- Support for **1080p@60 Hz** with **12-bit deep color**B
- **HDCP 2.3** for secure content protection
- **High Bit Rate (HBR) audio** input capability
- **Consumer Electronics Control (CEC)** for device interoperability
- **Dynamic HDR Metadata**, including **HDR10+**
- **Variable Refresh Rate (VRR)** for smooth motion rendering
- **Auto Lip Sync Correction** to maintain precise audio-video synchronization
- **Quick Media Switching (QMS)**, **Quick Frame Transport (QFT)**, and **Auto Low Latency Mode (ALLM)** for enhanced media and gaming responsiveness

Table 8: HDMI input interface

J205 pin	HDMI connector pin name	SL1680 ball name	Type (Voltage)	Description/Remarks
1	HPD	HDMITX_HPD/HDMITX-eARC_RXn	I (5.0 V)	Enhanced audio return channel - negative
2	NC	HDMITX-eARC_RXp	I (5.0 V)	Enhanced audio return channel - positive
3	D2+	HDMI_TX_TD2p	I (3.3 V)	TMDS data 2 positive
4	SHL_D2	–	PWR	Shield/Ground reference for D2 pair connected to the GND net
5	D2-	HDMI_TX_TD2n	I (3.3 V)	TMDS data 2 negative
6	D1+	HDMI_TX_TD1p	I (3.3 V)	TMDS data 1 positive
7	SHL_D1	–	PWR	Shield/Ground reference for D1 pair connected to the GND net
8	D1-	HDMI_TX_TD1n	I (3.3 V)	TMDS data 1 negative
9	D0+	HDMI_TX_TD0p	I (3.3 V)	TMDS data 0 positive
10	SHL_D0	–	PWR	Shield/Ground reference for D0 pair connected to the GND net
11	D0-	HDMI_TX_TD0n	I (3.3 V)	TMDS data 0 negative
12	CLK+	HDMI_TX_CKp	I (3.3 V)	Clock signal - positive
13	SHLD_C	–	PWR	Shield/Ground reference for clock pair connected to the GND net
14	CLK-	HDMI_TX_CKn	I (3.3 V)	Clock signal - negative
15	CEC	–	I/O (3.3 V)	Single-wire low-speed bus shared among HDMI devices open-drain - always referenced to 3.3 V
16	GND	–	PWR	
17	SCL	SM_TW2_SCL	I/O (3.3 V)	For EDID and HDCP communication; shared open-drain bus between source and sink level shifted to 5.0 V
18	SDA	SM_TW2_SDA	I/O (3.3 V)	
19	+5V	PWR_HDMITX_5V	PWR	Input

4.1.2 HDMI Output

The **Luna SL1680 SBC** features a high-performance **HDMI output interface** designed for advanced display and multimedia applications. It supports high-resolution video output, rich color formats, and the latest HDMI 2.1 features to ensure seamless integration with modern monitors, TVs, and AV equipment.

Key features:

- **HDMI 2.1 compliance** with full **HDR** support, including **HDR10+**
- Output resolutions up to **2160p@60 Hz** with **YUV 4:4:4** color sampling
- Support for **1080p@60 Hz** with **12-bit deep color**
- **HDCP 2.3** for secure content protection
- **High Bit Rate (HBR) audio** output capability
- **Consumer Electronics Control (CEC)** for device interoperability
- **Audio Return Channel (ARC)** and **Enhanced ARC (eARC)** support
- **Variable Refresh Rate (VRR)** for smoother visual performance
- **Auto Lip Sync Correction** to maintain precise audio-video synchronization
- **Quick Media Switching (QMS)**, **Quick Frame Transport (QFT)**, and **Auto Low Latency Mode (ALLM)** for optimized media and gaming experiences

Table 9: HDMI output interface

J224 pin	HDMI connector pin name	SL1680 ball name	Type (Voltage)	Description/Remarks
1	HPD	SM_HDMI_RX_HPD	O (5.0 V)	HDMI Hot Plug Detect Output, controlled by SM_HDMI_RX_PWR5V
2	NC	–	–	Not connected
3	D2+	HDMI_RX_D2p	I (3.3 V)	TMDS data 2 positive
4	SHL_D2	–	PWR	Shield/Ground reference for D2 pair connected to the GND net
5	D2-	HDMI_RX_D2n	I (3.3 V)	TMDS data 2 negative
6	D1+	HDMI_RX_D1p	I (3.3 V)	TMDS data 1 positive
7	SHL_D1	–	PWR	Shield/Ground reference for D1 pair connected to the GND net
8	D1-	HDMI_RX_D1n	I (3.3 V)	TMDS data 1 negative
9	D0+	HDMI_RX_D0p	I (3.3 V)	TMDS data 0 positive
10	SHL_D0	–	PWR	Shield/Ground reference for D0 pair connected to the GND net
11	D0-	HDMI_RX_D0n	I (3.3 V)	TMDS data 0 negative
12	CLK+	HDMI_RX_CKp	I (3.3 V)	Clock signal - positive
13	SHLD_C	–	PWR	Shield/Ground reference for clock pair connected to the GND net
14	CLK-	HDMI_RX_CKn	I (3.3 V)	Clock signal - negative
15	CEC	–	I/O (3.3 V)	Single-wire low-speed bus shared among HDMI devices open-drain - always referenced to 3.3 V
16	GND	–	PWR	
17	SCL	SM_TW2_SCL	I/O (5.0 V)	For EDID and HDCP communication; shared open-drain bus between source and sink level shifted to 5.0 V
18	SDA	SM_TW2_SDA	I/O (5.0 V)	
19	+5V	SM_HDMI_RX_PWR5V	PWR	

4.2 MIPI CSI and DSI Interfaces

The board includes dedicated MIPI interfaces to support camera and display integration:

- Two 22-pin FCC connectors for MIPI CSI camera inputs; one with quad-lane and one with dual-lane configuration.
- A 22-pin FCC connector providing a quad-lane MIPI DSI interface for display connections.

4.2.1 MIPI CSI Interfaces

The **Luna SL1680 SBC** integrates two **MIPI CSI-2 interfaces** for high-speed camera and image sensor connectivity, implemented through **Molex 52559-2253 FFC/FPC connectors** (designators **J225** and **J226**). Each connector provides **22 gold-plated contacts** on a **0.50 mm pitch**, ensuring low contact resistance and excellent signal integrity for high-speed differential signaling compliant with **MIPI CSI-2** standards.

These interfaces form the primary electrical and mechanical link between the SoC's camera inputs and external imaging modules, supporting **single- or dual-camera configurations** for **stereo capture**, **depth sensing**, or **multi-sensor systems**. The **3.9 mm low-profile** design enables compact system layouts ideal for embedded or space-constrained applications.

Both connectors employ a **slider-locking mechanism** that secures the flat-flex cable (FPC), ensuring stable contact and resistance to vibration or mechanical stress. Detailed pin assignments, signal descrip-

tions, and electrical characteristics for each connector are provided in Tables 10 and 11, connectors J225 and J226 respectively.

Table 10: MIPI CSI interface (CSI0) - port J225

J225 pin	SL1680 ball name	Type (Voltage)	Description/Remarks
1	PWR_3V3_CTL	PWR	Output
2	TW3_SDA	I/O (3.3 V)	I^2C clock for DSI display control interface
3	TW3_SCL	I (3.3 V)	I^2C data for DSI display control interface
4	GND	PWR	Connected to the GND net
5	SM-TW3.GPIO1_0	I/O (3.3 V)	Chip select from GPIO expander
6	SM-TW3.GPIO1_4	O (3.3 V)	Power on CSI0 from GPIO expander
7	GND	PWR	Connected to the GND net
8	MIPI_CSI0_D3p	I (1.8 V)	MIPI CSI data lane 3 positive differential pair for camera data
9	MIPI_CSI0_D3n	I (1.8 V)	MIPI CSI data lane 3 negative differential pair for camera data
10	GND	PWR	Connected to the GND net
11	MIPI_CSI0_D2p	I (1.8 V)	MIPI CSI data lane 2 positive differential pair for camera data
12	MIPI_CSI0_D2n	I (1.8 V)	MIPI CSI data lane 2 negative differential pair for camera data
13	GND	PWR	Connected to the GND net
14	MIPI_CSI0_CKp	I (1.8 V)	MIPI CSI clock lane 0 positive differential pair for camera clock
15	MIPI_CSI0_CKn	I (1.8 V)	MIPI CSI clock lane 0 negative differential pair for camera clock
16	GND	PWR	Connected to the GND net
17	MIPI_CSI0_D1p	I (1.8 V)	MIPI CSI data lane 1 positive differential pair for camera data
18	MIPI_CSI0_D1n	I (1.8 V)	MIPI CSI data lane 1 negative differential pair for camera data
19	GND	PWR	Connected to the GND net
20	MIPI_CSI0_D0p	I (1.8 V)	MIPI CSI data lane 0 positive differential pair for camera data
21	MIPI_CSI0_D0n	I (1.8 V)	MIPI CSI data lane 0 negative differential pair for camera data
22	GND	PWR	Connected to the GND net

Table 11: MIPI CSI interface (CSI1) - port J226

J226 pin	SL1680 ball name	Type (Voltage)	Description/Remarks
1	PWR_3V3_CTL	PWR	Output
2	TW0_SDA	I/O (1.8 V)	I^2C clock for DSI display control interface
3	TW0_SCL	I (1.8 V)	I^2C data for DSI display control interface
4	SM-TW3.GPIO1_6	O (3.3 V)	Chip select from GPIO expander
5	SM-TW3.GPIO1_7	IO (3.3 V)	Power on CSI1 from GPIO expander
6	–	–	Not connected
7	–	–	
8	–	–	
9	–	–	
10	–	–	
11	–	–	
12	–	–	
13	GND	PWR	Connected to the GND net
14	MIPI_CSI1_CKp	I (1.8 V)	MIPI CSI clock lane 0 positive differential pair for camera clock
15	MIPI_CSI1_CKn	I (1.8 V)	MIPI CSI clock lane 0 negative differential pair for camera clock
16	GND	PWR	Connected to the GND net
17	MIPI_CSI1_D1p	I (1.8 V)	MIPI CSI data lane 1 positive differential pair for camera data
18	MIPI_CSI1_D1n	I (1.8 V)	MIPI CSI data lane 1 negative differential pair for camera data
19	GND	PWR	Connected to the GND net
20	MIPI_CSI1_D0p	I (1.8 V)	MIPI CSI data lane 0 positive differential pair for camera data
21	MIPI_CSI1_D0n	I (1.8 V)	MIPI CSI data lane 0 negative differential pair for camera data
22	GND	PWR	Connected to the GND net

4.2.2 MIPI DSI Interface

The **Luna SL1680 SBC** provides a **MIPI DSI (Display Serial Interface)** for display connectivity, implemented through a **Molex 52559-2253 FFC/FPC connector** (designator **J208**). This connector features **22 gold-plated contacts** on a **0.50 mm pitch**, in compliance with **MIPI DSI** standards.

The DSI interface serves as the primary electrical and mechanical link between the SoC display output and external display modules, supporting

- **high-resolution panels** with
- **low-latency data transmission** and
- **robust signal integrity**.

The connector, with a **3.9 mm low-profile** form factor, incorporates a **slider-locking mechanism** to secure the flat-flex cable (FPC), preventing intermittent connections under vibration or mechanical stress.

Detailed pin assignments, signal descriptions, and electrical characteristics are provided in Table 12, which lists the pinout and corresponding **SL1680 signal mappings** for connector **J208**.

Table 12: MIPI DSI interface

J208 pin	SL1680 ball name	Type (Voltage)	Description/Remarks
1	PWR_3V3_CTL	PWR	Output
2	TW0_SDA	I/O (1.8 V)	I^2C clock for DSI display control interface
3	TW0_SCL	I (1.8 V)	I^2C data for DSI display control interface
4	GND	PWR	Connected to the GND net
5	SM-TW3.GPIO0_7	I/O (3.3 V)	DSI GPIO from GPIO expander
6	SM-TW3.GPIO0_1	O (3.3 V)	Power on DSI from GPIO expander
7	GND	PWR	Connected to the GND net
8	MIPI_DSI_D3p	O (1.8 V)	MIPI DSI data lane 3 positive differential pair for display data
9	MIPI_DSI_D3n	O (1.8 V)	MIPI DSI data lane 3 negative differential pair for display data
10	GND	PWR	Connected to the GND net
11	MIPI_DSI_D2p	O (1.8 V)	MIPI DSI data lane 2 positive differential pair for display data
12	MIPI_DSI_D2n	O (1.8 V)	MIPI DSI data lane 2 negative differential pair for display data
13	GND	PWR	Connected to the GND net
14	MIPI_DSI_CKp	O (1.8 V)	MIPI DSI clock positive lane differential pair for display clock
15	MIPI_DSI_CKn	O (1.8 V)	MIPI DSI clock negative lane differential pair for display clock
16	GND	PWR	Connected to the GND net
17	MIPI_DSI_D1p	O (1.8 V)	MIPI DSI data lane 1 positive differential pair for display data
18	MIPI_DSI_D1n	O (1.8 V)	MIPI DSI data lane 1 negative differential pair for display data
19	GND	PWR	Connected to the GND net
20	MIPI_DSI_D0p	O (1.8 V)	MIPI DSI data lane 0 positive differential pair for display data
21	MIPI_DSI_D0n	O (1.8 V)	MIPI DSI data lane 0 negative differential pair for display data
22	GND	PWR	Connected to the GND net

5 Peripheral Interfaces

The **Synaptics SL1680 SoC** features an extensive suite of peripheral interfaces. These interfaces enable scalable system integration, sensor interfacing, and high-speed data exchange across digital and analog domains.

Key interfaces:

- **Analog-to-Digital Converters (ADC):** Two high-resolution channels with a 1.2 V full-scale input for precise sensor data acquisition.
- **Digital Audio Interfaces:** Support for multi-channel **PCM audio**, advanced decoding, **Far-Field Voice (FFV)**, and **Keyword Detection**.
- **Pulse Width Modulation (PWM):** Configurable frequency and duty cycle for motor control, LED dimming, and general actuation.
- **Ethernet:** Integrated **RJ45 Gigabit Ethernet** interface (10/100/1000 Mbps) over **RGMII**, featuring auto-negotiation, diagnostics, and optional **PoE pass-through** (refer to Table 15).
- **General-Purpose I/O (GPIO):** A **40-pin header** providing configurable digital I/O, power rails, and multiplexed alternate functions (**UART**, **SPI**, **I²C**, **PWM**, **PCM**). Low-speed pins may support up to seven alternate functions.
- **GPIO Expanders:** Two **I²C-controlled 8-bit expanders (FXL6408UMX)** add further GPIO capacity, offering interrupt support, programmable pull-ups/-downs, reset control, and voltage-level translation.
- **PCI Express (M.2 Key E):** Expansion slot supporting **PCIe**, **SDIO**, **UART**, and **PCM** modules for wireless or peripheral connectivity in a standard mechanical form factor (see related tables for connector configurations).

5.1 ADC - Analog Digital Converter

The SL1680 features two independent ADC input channels, **ADCI0** and **ADCI1**, optimized for precise acquisition of analog sensor signals with integrated signal conditioning, operating at a sampling rate of up to **1 MSPS** (mega samples per second).

- Two independent ADC input channels (ADCI0 and ADCI1) with **up to 1.2 V** full-scale voltage.
- Designed for accurate acquisition of analog sensor signals with integrated signal conditioning.
- Pins dedicated on the 40-pin GPIO header: **Pin 16** (ADCI0) and **Pin 18** (ADCI1).

Table 13: Analog-to-Digital Converter (ADC) inputs

J32 pin	Luna SL1680 function	SL1680 ball name	Type	Description/Remarks
16	ADCI[0]	SM_ADCI[0]	Input	Voltage range: 0 to 1.2 V Resolution: 12 bits
18	ADCI[1]	SM_ADCI[1]	Input	

5.2 Digital Audio Interfaces

The Digital Audio Interfaces section provides detailed information on the Luna SL1680 SBC's support for advanced audio decoding and processing capabilities, including Far-Field Voice (FFV) and Keyword Detection. It supports multi-microphone inputs for high-quality voice capture and facilitates audio decompression across various formats. Audio post-processing functionality enhances the audio output for embedded IoT and multimedia applications. Audio data is transmitted and received via the synchronous digital audio lines on the 40-pin connector, enabling connectivity to external audio codec modules.

Audio Decoding/Processing

- Far-Field Voice (FFV) & Keyword Detection
- Microphone(s) input processing supported
- Audio decompression of various formats supported
- Audio post-processing

Table 14 enumerates the signal assignments, signal types, and functional descriptions for these interfaces, offering clarity and reference for integration and development work.

Table 14: Digital audio on 40-pin connector

J32 pin	Luna SL1680 function	SoC ball name	Alternate function	Description / Remarks
Primary function				
12	I2S2_DI	I2S2_DI	MODE_0	Bidirectional GPIO capable pin configurable as general-purpose I/O or as I2S2 data input
13	I2S2_LRCK	I2S2_LRCK	MODE_1	I2S2 left-right clock (word select) configurable as bidirectional GPIO
15	I2S2_DI	I2S2_DI	MODE_1	Dedicated I2S2 data input line
35	I2S1_LRCK	I2S2_LRCK	MODE_1	I2S1 left-right clock signal for audio frame synchronization supports alternate GPIO use
38	I2S1_BCLK	I2S1_BCLK	MODE_1	I2S1 bit clock for serial data timing configurable as bidirectional GPIO
Alternate function				
11	I2S2_BCLK	I2S2_BCLK	MODE_1	I2S2 bit clock output for synchronizing audio data transmission configurable as bidirectional GPIO
27	I2S2_MCLK	I2S2_MCLK	MODE_2	Master clock output for PDM microphone or I2S2 interface selectable via mode control
37	I2S1_MCLK	I2S2_MCLK	MODE_1	Master clock signal for I2S1 interface provides timing reference for external codec or DAC.
40	I2S1_DO	I2S1_DO	MODE_1	I2S1 digital audio output transmits serial data to external audio devices

5.3 Ethernet

One RJ45 Gigabit Ethernet jack is integrated to the single-board computer to provide wired network connectivity via a Reduced Gigabit Media Independent Interface (**RGMII**). This interface supports **10/100/1000 Mbps** speeds with auto-negotiation and standard diagnostic features. RGMII reduces pin count by employing time-multiplexed data signals and source-synchronous clocks, transmitting data on both clock edges at gigabit speeds. The interface ensures high-speed Ethernet connectivity with proper timing margin considerations in the physical layer design. Additionally, Power over Ethernet (**PoE**) pass-through capability is supported when using an optional dedicated adapter, allowing the SBC to be powered through the Ethernet network infrastructure where available. The pinout and respective signals for the Ethernet connector are detailed in Table 15.

Table 15: Ethernet connector (RJ45 - J2 connector)

J2 pin	Ethernet connector pin name	RTL8211f-cg ethernet transeiver	Description/Remarks
Common mode voltage reference			
4	TDCT0	–	Center taps of the transmit differential pairs
5	TDCT1	–	

Continued on next page

Table 15: Ethernet connector (RJ45 - J2 connector) (Continued)

J2 pin	Ethernet connector pin name	RTL8211f-cg ethernet transeiver	Description/Remarks
Ethernet data			
1	TD0+	MDIP0	Positive differential MDI signal
2	TD0-	MDIN0	Negative differential MDI signal
3	TD1+	MDIP1	Positive differential MDI signal
6	TD1-	MDIN1	Negative differential MDI signal
7	TD2+	MDIP2	Positive differential MDI signal
8	TD2-	MDIN2	Negative differential MDI signal
9	TD3+	MDIP3	Positive differential MDI signal
10	TD3-	MDIN3	Negative differential MDI signal
Leds			
15	LED1A	LED1/CFG_LDO0	
16	LED1K	–	Connected to the GND net through a 510Ω resistor
17	LED2A	–	Connected to the 3V3 power supply net through a 510Ω resistor
18	LED2K	LED2/CFG_LDO1	
Power-over-Ethernet (PoE) - J34			
11	VC1	–	Connected do the PoE Header (J34)
12	VC2	–	
13	VC3	–	
14	VC4	–	
Shield			
G1	SHIELD1	–	Connected to the GND net
G2	SHIELD2	–	
G3	G3	–	Not connected
G4	G4	–	

5.4 GPIO - General-Purpose Input/Output

The 40-pin GPIO header on the Luna SL1680 SBC follows a widely adopted pin assignment standard, ensuring broad compatibility with existing ecosystems and facilitating integration of external modules and accessories. Refer to Section 3.2 for more information about the pinout of the main GPIO connector.

The pinout provides:

- **Configurable GPIO lines:** Multiple general-purpose I/O pins that can be software-configured as digital inputs or outputs, supporting internal pull-up and pull-down resistor options.
- **Power supply rails:** Dedicated 3.3 V and 5 V output pins for powering external devices and interface circuitry.
- **Ground references:** Multiple ground pins distributed across the header to maintain signal integrity and minimize electrical noise.
- **Alternate function interfaces:** Multiplexed signal lines supporting UART, SPI, I^2C, PWM, PCM, and clock outputs, enabling direct connection to a wide range of peripherals.
- **SoC-integrated signals:** Select GPIOs are connected to internal SoC functions capable of interrupt

generation, event detection, and logic control, improving responsiveness in real-time applications.

Ground pins are positioned throughout the header to ensure robust electrical referencing and reduce the likelihood of ground loops in connected systems.

5.5 PCI Express (M.2 Key E) Expansion Slot

The Luna SL1680 SBC includes an **M.2 Key E slot** designed to support expansion modules utilizing **PCI Express, SDIO, UART, or PCM** interfaces.

This PCIe interface is **populated by default** with the Wi-Fi + Bluetooth module (refer to Section 1.5.5).
When not used for wireless connectivity, the slot can host a variety of **PCIe-compatible peripherals**, including alternative **Wi-Fi/Bluetooth modules** and other expansion devices.

The slot conforms to standard **M.2 Key E mechanical and electrical specifications**, ensuring seamless integration with third-party modules and reliable interoperability across various device ecosystems.

Table 16: PCI Express connector (M.2)

J17 pin	PCIe pin name	SL1680 ball name	Type (Voltage)	Description/Remarks
Upper contact (odd pins)				
1	GND	–	PWR	Connected to the GND net
3	USB_D+	–	I/O	Not connected
5	USB_D-	–	I/O	
7	GND	–	PWR	Connected to the GND net
9	SDIO_CLK	–	I (1.8 V)	Connected to TMUX1574RSVR (U61) multiplexer
11	SDIO_CMD	–	I/O (1.8 V)	
13	SDIO_DATA0	–	I/O (1.8 V)	Connected to TMUX1574RSVR (U60) multiplexer
15	SDIO_DATA1	–	I/O (1.8 V)	
17	SDIO_DATA2	–	I/O (1.8 V)	
19	SDIO_DATA3	–	I/O (1.8 V)	
21	SDIO_WAKE#	SM_TDI (GPIO[7])	O (1.8 V)	10kΩ pull-up resistor to PWR_1V8 net
23	SDIO_RESET#	–	I (1.8 V)	10kΩ pull-up resistor to PWR_M2-KEYE_VIO net logic level always up
33	GND	–	PWR	Connected to the GND net
35	PETp0	PCIe_TX0p	I/O (1.8 V)	0.1uF impedance control series capacitor
37	PETn0	PCIe_TX0n	I/O (1.8 V)	0.1uF impedance control series capacitor
39	GND	–	PWR	Connected to the GND net
41	PERp0	PCIe_RX0p	I/O (1.8 V)	
43	PERn0	PCIe_RX0n	I/O (1.8 V)	
45	GND	–	PWR	Connected to the GND net
47	REFCLKp0	PCIe_CLKp	O (1.8 V)	PCIe differential reference clock positive signal line
49	REFCLKn0	PCIe_CLKn	O (1.8 V)	PCIe differential reference clock negative signal line
51	GND	–	PWR	Connected to the GND net
53	CLKREQ0#		I/O (3.3 V)	10kΩ pull-up resistor to PWR_3V3 net through protection diode

Continued on next page

Table 16: PCI Express connector (M.2) (Continued)

J17 pin	PCIe pin name	SL1680 ball name	Type (Voltage)	Description/Remarks
55	PEWAKE0#	–	I/O (3.3 V)	10kΩ pull-up resistor to PWR_1V8 net
57	GND	–	PWR	Connected to the GND net
59	RESERVED/PETp1	PCIe_TX1p	O (1.8 V)	0.1uF impedance control series capacitor
61	RESERVED/PETn1	PCIe_TX1n	O (1.8 V)	0.1uF impedance control series capacitor
63	GND	–	PWR	Connected to the GND net
65	RESERVED/PERp1	PCIe_RX1p	I (1.8 V)	
67	RESERVED/PERn1	PCIe_RX1n	I (1.8 V)	
69	GND	–	PWR	Connected to the GND net
71	RESERVED/REFCLKp1	–	O (3.3 V)	Not connected
73	RESERVED/REFCLKn1	–	O (3.3 V)	Not connected
75	GND	–	PWR	Connected to the GND net
77	EP2	–	PWR	Connected to the GND net
Lower contact (even pins)				
2	3.3V	–	PWR (3.3 V)	Connected to PWR_3V3-M2-KEYE net
4	3.3V	–	PWR (3.3 V)	
6	LED1#(O,OD)	–	O	Not connected
8	PCM_CLK/I2S_SCK	I2S3_BCLK	I/O (1.8 V)	Serial bit clock for audio data timing
10	PCM_SYNC/I2S_WS	I2S3_LRCK	I/O (1.8 V)	Selects left or right audio channel
12	PCM_IN/I2S_SD_IN	I2S3_DI	O (1.8 V)	Serial audio data input line
14	PCM_OUT/I2S_SD_OUT	I2S3_DO	I (1.8 V)	Serial audio data output lineI2S3_LRCK
16	LED2#(O,OD)	–	O	Not connected
18	GND	–	PWR	Connected to the GND net
20	UART_WAKE#	–	O (3.3 V)	10kΩ pull-up resistor to PWR_1V8 net
22	UART_RXD	UART3_RXD	O (1.8 V)	Receives serial data from remote device
32	UART_TXD	UART3_TXD	I (1.8 V)	Transmits serial data to remote device
34	UART_CTS	UART3_CTSn	O (1.8 V)	Device may transmit, signal for flow control
36	UART_RTS	UART3_RTSn	I (1.8 V)	Requests permission to transmit data
38	VENDOR_DEFINED2 (VIO)	–		Connected to BRCM-WL_DEV_WAKE net
40	VENDOR_DEFINED4 (VIO_SD)	–	I (1.8 V)	Connected to M2-KEYE_SDIO-WAKEn net
42	VENDOR_DEFINED6 (HOST_W#)	–		10kΩ pull-up resistor to PWR_M2-KEYE_VIO net
44	COEX3	–	I/O (1.8 V)	Not connected
46	COEX2	–	I/O (1.8 V)	
48	COEX1	–	I/O (1.8 V)	
50	SUSCLK	–	I (3.3 V)	Frequency: 32 kHz
52	PERST0	–	I (3.3 V)	Connected to SM-TW3 (GPIO1_1) with a 100kΩ pull-up resistor to PWR_M2-KEYE_VIO net reset signal line
54	W_DISABLE2#	–	I (3.3 V)	Connected to SM-TW3 (GPIO1_5) with a 10kΩ pull-up resistor to PWR_M2-KEYE_VIO net GPIO Expander FXL6408UMX - active low (PDn)

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Table 16: PCI Express connector (M.2) (Continued)

J17 pin	PCIe pin name	SL1680 ball name	Type (Voltage)	Description/Remarks
56	W_DISABLE1#	–	I (3.3 V)	Connected to SM-TW3 (GPIO1_2) with a 10kΩ pull-up resistor to PWR_M2-KEYE_VIO net GPIO Expander FXL6408UMX - active low (PDn)
58	I2C_DATA	SM_TW3_SDA	I/O (3.3 V)	
60	I2C_CLK	SM_TW3_SCL	I (3.3 V)	
62	ALERT#	–	O (3.3 V)	Connected only to the test point TP98
64	RESERVED	–	–	Not connected
66	UIM_SWP/PERST1#	–	I (3.3 V)	Connected only to the test point TP161
68	UIM_POWER_SNK/CLKREQ1#	–	I (3.3 V)	Connected only to the test point TP162
70	UIM_PWR_SRC/GPIO01/PEWAKE1#	–	I/O (3.3 V)	Connected only to the test point TP163
72	3.3V	–	PWR (3.3 V)	Connected to PWR_3V3-M2-KEYE net
74	3.3V	–	PWR (3.3 V)	
76	EP1	–	PWR	Connected to the GND net

Table 17 lists the three recommended TE Connectivity configurations for the **PCIe Key E M.2 connector**, specifying the matching receptacle and standoff. These selections ensure proper mechanical alignment and height compatibility with the M.2 module.

Table 17: PCIe receptacle and stand-off matching

Choice No.	MFR: Part Number, Height RECP/Card	Stand-Off
1	TE : 2199230-4, H4.2mm / 2.48mm	SMTSO-M2-2.5ET
2	TE : 2199119-4, H3.2mm / 1.48mm	SMTSO-M2-1.5ET
3	TE : 2199125-4, H2.2mm / 0.63mm	SMTSO-M2-0.5ET

These options ensure proper mechanical fit and reliable connection for a variety of M.2 Key E modules.

Note that the mechanical mounting position (STO1) may overlap with the M.2 pin on the layout and should be verified during PCB design.

5.5.1 Pulse Code Modulation (PCM) Interfaces

The **Luna SL1680 SBC's Pulse Code Modulation (PCM) interface** provides a digital audio communication pathway for **high-quality signal transmission and reception**. It uses **standard I^2S protocol signals**, clock (PCM_CLK), frame sync (PCM_SYNC), data input (PCM_IN), and data output (PCM_OUT), ensuring broad compatibility with audio peripherals. The **PCM signals are available through dedicated pins on the 40-pin GPIO header**, allowing easy connection to audio codecs and telephony devices. Supporting synchronous serial data transfers, the interface enables stereo and voice communication while offering flexible pin multiplexing for integration with other system functions.

Table 18: Pulse Code Modulation (PCM) interface

PCIe pin	Luna SL1680 function	SL1680 ball name	PCM function	Type (Voltage)	Description/Remarks
8	I2S-SCK	I2S3_BCLK	PCM_CLK	I/O (1.8 V)	

Continued on next page

Table 18: Pulse Code Modulation (PCM) interface (Continued)

PCIe pin	Luna SL1680 function	SL1680 ball name	PCM function	Type (Voltage)	Description/Remarks
10	I2S-WS	I2S3_LRCK	PCM_SYNC	I/O (1.8 V)	
12	I2S-SD-IN	I2S3_DI	PCM_IN	O (1.8 V)	The direction of the signal is the opposite for the PCIe interface.
14	I2S-SD-OUT	I2S3_DO	PCM_OUT	I (1.8 V)	

5.5.2 Pulse Width Modulation (PWM) Interfaces

The Luna SL1680 SBC provides one primary PWM signal on the 40-pin main header for precise control applications, with two additional PWM channels available as alternate functions. These channels feature software-configurable frequency and duty cycle parameters, enabling fine control for tasks such as motor speed regulation, LED dimming, and actuator operation. Hardware support is available through dedicated pins and flexible pin multiplexing with other I/O functions, allowing seamless integration into a variety of embedded control systems.

Table 19: Pulse Width Modulation (PWM) outputs

J32 pin	Luna SL1680 function	SL1680 ball name	Type (Voltage)	Description/Remarks
Primary function				
7	PWM[1]	SPI1_SS1n	O (3.3 V)	Level-shifted to 3.3 V
Alternate function				
8	UATR2_Tx	SM_SPI2_SS2n	O (3.3 V)	Alternate function: Mode_3 (PWM[0]) level-shifted to 3.3 V
10	UART2_Rx	SM_SPI2_SS3n	O (3.3 V)	Alternate function: Mode_3 (PWM[1]) level-shifted to 3.3 V

5.6 USB Interfaces

The **Luna SL1680 SBC** provides multiple USB interfaces:

- **Four USB-A ports**, with the pinouts described in tables 20 and 21, supporting **USB 3.x** speeds, ideal for high-bandwidth peripherals such as external storage, cameras, and input devices.
- **One USB-C port**, with the pinout described in table 22, for **power input and device recovery**, supporting **5 V power delivery** and recovery mode for firmware flashing and system maintenance.

All USB ports include **overcurrent and short-circuit protection**.

Table 20: USB 3.0 connector pair A - connector J210

J210 pin	USB connector pin name	USB hub ball name	Description/Remarks
Down connector			
1	VBUS	–	Connected to VDP1 from AP2162AFGEG-7 power switch
2	DM	DM1	Connected to ESD protection device
3	DP	DP1	Connected to ESD protection device
4	GND	–	Connected to the GND net
5	SRDA_SSRX-	RXN_DS1	Connected to ESD protection device

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Table 20: USB 3.0 connector pair A - connector J210 (Continued)

J210 pin	USB connector pin name	USB hub ball name	Description/Remarks
6	SRDA_SSRX+	RXP_DS1	Connected to ESD protection device
7	GND_DRAIN	–	Connected to the GND net
8	SRDA_SSTX-	TXN_DS1	Connected to ESD protection device
9	SRDA_SSTX+	TXP_DS1	Connected to ESD protection device
Up connector			
10	VBUS1	–	Connected to VDP4 from AP2162AFGEG-7 power switch
11	DM1	DM4	Connected to ESD protection device
12	DP1	DP4	Connected to ESD protection device
13	GND1	–	Connected to the GND net
14	SRDA_SSRX1-	RXN_DS4	Connected to ESD protection device
15	SRDA_SSRX1+	RXP_DS4	Connected to ESD protection device
16	GND_DRAIN1	–	Connected to the GND net
17	SRDA_SSTX1-	TXN_DS4	Connected to ESD protection device
18	SRDA_SSTX1+	TXP_DS4	Connected to ESD protection device

Table 21: USB 3.0 connector pair B - connector J216

J216 pin	USB connector pin name	USB hub ball name	Description/Remarks
Down connector			
1	VBUS	–	Connected to VDP3 from AP2162AFGEG-7 power switch
2	DM	DM3	Connected to ESD protection device
3	DP	DP3	Connected to ESD protection device
4	GND	–	Connected to the GND net
5	SRDA_SSRX-	RXN_DS3	Connected to ESD protection device
6	SRDA_SSRX+	RXP_DS3	Connected to ESD protection device
7	GND_DRAIN	–	Connected to the GND net
8	SRDA_SSTX-	TXN_DS3	Connected to ESD protection device
9	SRDA_SSTX+	TXP_DS3	Connected to ESD protection device

Table 21: USB 3.0 connector pair B - connector J216 (Continued)

J216 pin	USB connector pin name	USB hub ball name	Description/Remarks
Up connector			
10	VBUS1	–	Connected to VDP2 from AP2162AFGEG-7 power switch
11	DM1	DM2	Connected to ESD protection device
12	DP1	DP2	Connected to ESD protection device
13	GND1	–	Connected to the GND net
14	SRDA_SSRX1-	RXN_DS2	Connected to ESD protection device
15	SRDA_SSRX1+	RXP_DS2	Connected to ESD protection device
16	GND_DRAIN1	–	Connected to the GND net
17	SRDA_SSTX1-	TXN_DS2	Connected to ESD protection device
18	SRDA_SSTX1+	TXP_DS2	Connected to ESD protection device

Table 22: USB-C connector

J213 pin	USB connector pin name	SoC ball name	Description/Remarks
A1	GND	–	
A4	VBUS	–	Connected to PWR_5V net through a fuse and a transistor switch circuit
A5	CC1	–	5.1kΩ pull-down
A6	DP1	USB2_Dp	Connected to ESD protection device
A7	DN1	USB2_Dn	Connected to ESD protection device
A8	SBU1	–	Not connected
A9	VBUS	–	Connected to PWR_5V net through a fuse and a transistor switch circuit
A12	GND	–	
B1	GND	–	
B4	VBUS	–	Connected to PWR_5V net through a fuse and a transistor switch circuit
B5	CC2	–	5.1kΩ pull-down
B6	DP2	USB2_Dp	Connected to ESD protection device
B7	DN2	USB2_Dn	Connected to ESD protection device
B8	SBU2	–	Not connected
B9	VBUS	–	Connected to PWR_5V net through a fuse and a transistor switch circuit
B12	GND	–	
Shell			
SH1	SHELL_GND	–	Connected to the GND net
SH2	SHELL_GND	–	
SH3	SHELL_GND	–	
SH4	SHELL_GND	–	

5.6.1 USB-C and Power Considerations

The **USB-C port (J213)** is primarily configured as a **power input interface**, with its **VBUS** line directly routed to the system's internal power management circuitry. The connector also supports **USB 2.0 data**

transfer via the **D+ (DP)** and **D− (DN)** lines, enabling peripheral communication with a host device.

The **CC1** and **CC2** pins are connected exclusively to **pull-down resistors**, in compliance with the USB Type-C specification for default downstream-facing ports (DFP). These resistors define the port's role as a downstream device, allowing the connected host to detect the port and provide standard VBUS power. No active Type-C controller circuitry is present on the CC lines; therefore, **power role negotiation is limited to the default USB-C behavior dictated by the pull-down resistor configuration**.

When connected to a host, the board functions as a **USB peripheral**, drawing power from the host and enabling bidirectional USB 2.0 data communication through the same interface. This arrangement supports simultaneous powering and data transfer without requiring active CC line management, ensuring compliance with standard USB-C connection behavior.

Powering via 40-pin Header
The board can be powered through the 40-pin expansion connector (**J32**) by supplying **5 V** to the corresponding power pin(s) and **GND** to the ground pins.

- When using this method, ensure that the supplied voltage matches the board's nominal **5 V input rail (PWR_5V)** and that proper **current limiting** and **reverse-protection** are provided externally.
- **Incorrect wiring or back-feeding may damage the board.**

5.7 Auxiliary Headers

5.7.1 Fan Control

The **Luna SL1680 SBC provides direct and precise control of a 4-wire PWM fan** via the **BM04B-SRSS-TBT header**. Fan modulation is achieved by routing the SoC's native **1.8 V PWM** (I2S1_DO2 in PWM alternate function mode, mapped to **GPIO16**) through a **SN74LVC1T45DRLR level shifter**, translating the control signal to industry-standard **5 V logic** required by most PWM fans. Real-time speed feedback is available via the tachometer signal, which is routed to **SPDIFI (GPIO4 alternate function)**.

The interface is engineered for **robust compatibility** with standard 4-wire fans, ensuring **reliable startup**, **variable speed modulation**, and **accurate RPM monitoring**. Power is supplied **directly from the SBC at regulated 5 V**.

Table 23: Fan control pinout and functional assignment

J221 pin	Luna SL1680 SBC Function	Fan Function	Description / Remarks
1	PWR_5V	PWR	5.0 V output[1]
2	PWM output derived from I2S1_DO2 alternate function mode PWM[2]	PWM	Logic-level shifted to 5V via SN74LVC1T45DRLR supports standard PWM control
3	GND	GND	Ground reference
4	SPDIFI alternate function mode GPIO4	tachometer	Fan tachometer input[1] open-drain, requires external pull-up if not present on fan

[1] From the Luna SL1680 SBC perspective.

6 Serial Communication and Debugging Interfaces

The **Luna SL1680 SBC** integrates a set of **serial communication and debugging interfaces** for system configuration, peripheral expansion, and low-level software development. These interfaces provide flexible connectivity options for sensors, actuators, and external controllers, as well as hardware-level access for firmware programming and diagnostics.

The available interfaces include:

- **I²C (Inter-Integrated Circuit):** Multi-master serial bus for low-speed peripheral communication and configuration.
- **SPI (Serial Peripheral Interface):** High-speed, full-duplex interface for connecting flash memory, sensors, and other digital peripherals.
- **UART (Universal Asynchronous Receiver/Transmitter):** Standard serial ports for console access, debugging, and device communication.
- **Real-Time Clock (RTC):** Dedicated interface for maintaining accurate system timekeeping, even during power-down conditions.

Together, these interfaces ensure versatile serial connectivity and robust debugging capabilities, supporting a wide range of embedded, industrial, and development use cases.

6.1 I²C

The **Luna SL1680 SBC** integrates multiple **I²C controllers** to provide communication channels essential for embedded applications. These controllers support both **general-purpose** and **dedicated subsystem interfaces**, enabling robust and flexible connectivity to a wide range of peripheral devices.

Key features:

- **One externally accessible I²C controller**, offering system-level connectivity for expansion and configuration devices.
- **Multiple general-purpose I²C ports** configurable for standard two-wire protocol communication with external components.
- **Dedicated I²C channels** for internal devices such as the PMIC, CSI and DSI interfaces.
- **Careful pin multiplexing considerations** apply to I²C interfaces, where sharing pins among various functions requires design attention to avoid conflicts.
- **Complete compatibility** with legacy and modern I²C peripherals, facilitating integration flexibility across diverse ecosystems.

Table 24 details the **I²C devices and their target addresses**, including both SoC-internal components and external peripherals, e.g., MIPI CSI/DSI connectors and the 40-pin header.

Table 24: I²C bus components

I²C/TWSI bus	Device/Remarks	Part Number (PN)	PCB designator	Target address (7-bit)
SM_TW3	GPIO EXPANDER I²C 8 bit	FXL6408UMX	U12	0x43
	GPIO EXPANDER I²C 8 bit	FXL6408UMX	U13	0x44
	Real-Time Clock	DS1339AU+T	U63	0x68
	External device connects to MIPI_CSI0 connector	–	J225	–
SM_TW2B	I²C step-Down voltage regulator 6A, 6V max default output voltage: 0.8V	TPS62870Y1QWRXSRQ1	U3	0x40
SOC_TW1B	I²C step-Down voltage regulator 6A, 6V max default output voltage: 0.8V	TPS62870Y1QWRXSRQ1	U2	0x40
SOC_TW0	External device connects to MIPI_CSI1 connector	–	J226	–
	External device connects to MIPI_DSI connector	–	J208	–
	External device connects to 40-pin Header	–	J32	–

6.1.1 Real-Time Clock

The **Luna SL1680 SBC** uses the **DS1339AU+T**, a low-power, **I²C serial real-time clock (RTC)** used for **time-keeping** and **calendar functions** in the system. The RTC module supports **backup power** through an external battery connected via the **BM02B-SRSS-TBT connector**, ensuring continuous operation during **power failures**.

The **I²C slave address** of the RTC component is:

- **0x68 (7-bit)** or
- **0xD0 (8-bit)**

complying with standard **RTC addressing** in embedded designs.

Table 25: Real-Time Clock (RTC) interface

RTC function	Luna SL1680 signal name	Description/Remarks
RTC_INTn	SM_TMS	RTC Interrupt with a 10kΩ pull-up resistor
RTC_SCL	SM_TW3_SCL	I²C Clock
RTC_SDA	SM_TW3_SDA	I²C Data

The RTC can be powered by an external source through the **BATT connector (J218)**, allowing it to retain time and date information when the main system power is off.

6.2 JTAG

The Luna SL1680 SBC provides access to the SoC's JTAG interface for low-level debugging. Although the JTAG signals are routed on the PCB, **the board does not include a dedicated JTAG connector**. Access to the interface is possible through designated test points on the board, where the standard JTAG signals are exposed.

Some JTAG signals are multiplexed with GPIO functions or boot configuration pins and may be disabled by default. In addition, the JTAG_SEL and TEST_EN control signals are held in a pull-down state, which keeps the JTAG interface inactive after reset. To enable JTAG operation, the appropriate control levels must be asserted according to the SoC's reference manual.

The JTAG interface operates at 1.8 V logic levels, corresponding to the SoC I/O domain. External JTAG probes must therefore be compatible with 1.8 V signaling or used in conjunction with a suitable level shifter.

The board holds the interface inactive by default (TEST_EN and JTAG_SEL pulled low and TRSTn/TCK weakly pulled), so one must actively assert the right control signals and use a 1.8 V-compatible probe (or proper level shifting).

Table 26 lists the JTAG signals available on the Luna SL1680 SBC and their corresponding functions.

Table 26: JTAG interface

Signal name	SoC net name	Description	Remarks
TCK	SM_TCK	Test Clock	Provides the clock signal for the JTAG state machine
TMS	SM_TMS	Test Mode Select	Controls the state machine operation
TDI	SM_TDI / SM_GPIO7	Test Data In	Serial input data to the device
TDO	SM_TDO / SM_GPO8	Test Data Out	Serial output data from the device
TRST	SM_TRSTn	Test Reset (Optional)	Asynchronous reset of the JTAG logic
TEST_EN	SM_TEST_EN	Enable test	Enables JTAG test mode when asserted high pulled down by default
JTAG_SEL	SM_JTAG_SEL	Select test	Selects JTAG interface mode; must be asserted high to activate JTAG pulled down by default
GND	GND	Ground	Common ground reference

6.3 SPI

The Synaptics SL1680 SoC includes **two SPI** (Serial Peripheral Interface) controllers that support high-speed synchronous serial communication for connecting various peripheral devices. On the single board computer, the pins related to the SPI2 interface are routed through a dedicated level shifter circuit. This level shifter translates the SoC's native 1.8 V SPI signal levels to 3.3 V suitable for the J32 40-pin connector, ensuring reliable and compatible interface signaling with external peripherals connected via this header.

Table 27: SPI interface

J32 pin	SL1680 ball name	Luna SL1680 function	Description/Remarks
23	SM_SPI2_SCLK	SPI2_SCLK	4.7kΩ pull-down
19	SM_SPI2_SDO	SPI2_SDO	–
21	SM_SPI2_SDI	SPI2_SDI	–
24	SM_SPI2_SS0n	SPI2_SS0n	–
26	SM_SPI2_SS1n	SPI2_SS1n	–

6.4 UART

The Luna SL1680 SBC provides **multiple UART** interfaces to accommodate diverse serial communication requirements, such as system debugging, peripheral interfacing, and module expansion. Table 28 presents a summary of the available UART interfaces, including the connector, voltage levels, and typical use cases; while Table 29 lists the corresponding electrical characteristics, detailing the logic levels, voltage threshBolds, and operational parameters for each interface.

Table 28: UART interface summary

UART	Connector	Signal Voltage	Typical Use	Remarks
UART0 (Console)	J219 (BM03B-SRSS-TBT)	3.3 V TTL	System console, debugging	Primary serial interface
UART2	J32 (40-pin header)	3.3 V TTL	Peripheral connection	General-purpose serial port
UART3	PCIe M.2 Connector	1.8 V (native SoC level)	M.2-based devices	Routed directly from SoC

Table 29: UART interface characteristics

Parameter	Symbol	Min	Typ	Max	Default values	Remarks
Logic high input voltage	VIH	0.7 × VDD	–	VDD	VDD = 3.3 V (UART0, UART2) VDD = 1.8 V (UART3)	
Logic low input voltage	VIL	0	–	0.3 × VDD		
Logic high output voltage	VOH	0.8 × VDD	–	VDD		
Logic low output voltage	VOL	0	–	0.2 × VDD		
Baud rate range	–	–	–	4 Mbps	–	Depends on SoC configuration

6.4.1 UART0 (Console Interface – J219)

- Serves as the **primary debug and console interface** for system bring-up, boot monitoring, and low-level diagnostics.
- The UART0 signals originate from the SL1680 SoC at **1.8 V logic levels** and are converted to **3.3 V** by a dedicated bidirectional **level shifter**.
- The design provides **robust noise immunity** and **protection for the SoC I/O domain**, allowing long-cable operation and compatibility with common USB-to-UART converters.
- The console interface is made available on connector **J219 (BM03B-SRSS-TBT)** with the following pinout:
  - **TX (Transmit):** Serial data output from the SoC console UART.
  - **RX (Receive):** Serial data input to the SoC console UART.
  - **GND (Ground):** System ground reference.
- The interface supports **asynchronous serial communication** with configurable parameters (baud rate, parity, stop bits). Default operation is **115200 bps, 8-N-1** for firmware console access.

6.4.2 UART2 (Peripheral Interface – J32, 40-pin Expansion Header)

- Provides an auxiliary UART channel for **user peripherals** via the 40-pin expansion connector **J32**.
- UART2 signals originate from the SoC's **1.8 V domain** and pass through a **dedicated level shifter** to **3.3 V**, ensuring compatibility with standard peripheral logic levels.
- Designed for **custom peripheral integration**, such as external MCUs, sensors, or communication modules, while preserving electrical protection and noise margin.
- Available signals:
  - **TX (Transmit):** Serial data output from the SoC peripheral UART.
  - **RX (Receive):** Serial data input to the SoC peripheral UART.
  - **CTS (Clear To Send):** Optional hardware flow control input to the SoC.
  - **RTS (Request To Send):** Optional hardware flow control output from the SoC.
  - **GND (Ground):** Common ground reference.

- Supports standard **asynchronous UART communication** with configurable baud rate, parity, stop

bits, and optional flow control.

6.4.3 UART3 (PCIe M.2 Interface)

- Routed internally to the **PCIe M.2 Key B connector**, providing a **serial communication channel** for devices on this interface.
- Operates at the **native 1.8 V logic level** of the SoC; external devices connected through M.2 must be 1.8 V compatible.
- Commonly used by **modems, GNSS, or wireless communication modules** integrated through the M.2 slot.
- Available signals:
  - **TX (Transmit):** Serial data output from the SoC UART3.
  - **RX (Receive):** Serial data input to the SoC UART3.
  - **GND (Ground):** Common ground reference.
- Supports **asynchronous serial communication**, typically used for control, logging, or diagnostic interfaces between the host and the M.2 device.

Table 30 summarizes the available UART interfaces on the Luna SL1680, detailing the corresponding signal names, pin numbers (relative to the respective connectors), and their connections to the respective SoC UART instances.

Table 30: UART interfaces

Pin number	Signal	Description	SoC-UART connection
UART0			
1	SM_URT0_RXD	Receive data to SoC UART	Connected to SL1680 UART0_RX shifted to 3.3V
2	SM_URT0_TXD	Transmit data from SoC UART	Connected to SL1680 UART0_TX shifted to 3.3V
3	GND	System ground	Ground reference
UART2			
8	UART2_Tx	Transmit data from SoC UART	Connected to SL1680 UART2_TX shifted to 3.3V
10	UART2_Rx	Receive data to SoC UART	Connected to SL1680 UART2_RX shifted to 3.3V
UART3			
20	M2-KEYE_UART-WAKEn	Wake-up signal from device	
22	M2-KEYE_UART-RXD	Receive data to SoC UART	Connected to SL1680 UART3 interface 1.8 V signals
32	M2-KEYE_UART-TXD	Transmit data from SoC UART	
34	M2-KEYE_UART-CTSn	Clear-to-send input to SoC	
36	M2-KEYE_UART-RTSn	Request-to-send output from SoC	

7 Test Points

Test points are distributed across the PCB to facilitate system validation, debugging, and signal integrity analysis during production and development. These test points provide convenient access to critical signals without disrupting normal system behavior.

Table 31: Test points

Test point ID	Connected signal	Purpose/Description and remarks
TP1	PWR_5V	Measure main 5V input voltage and stability
TP2	VCORE	Monitor SL1680 core voltage rail
TP3	RESET	Check reset signal timing
TP4	UART_TX	Monitor UART transmit line
TP5	GND	Ground reference point
TP98	ALERT#	PCIe interface 3.3 V output
TP161	UIM_SWP/PERST1#	PCIe reset signal
TP162	UIM_POWER_SNK/CLKREQ1#	PCIe clock request signal
TP163	UIM_PWR_SRC/GPIO1/PEWAKE1#	Serves multiple functions depending on boot and runtime configuration
TP170	PWR_5V_CTL	Measure the control signal that enables or disables the main 5 V power rail
TP171	PWR_3V3_CTL	Measure the control signal that enables or disables the 3.3 V power rail
TP172	PWR_1V8_CTL	Measure the control signal that enables or disables the 1.8 V power rail
TP173	PWR_3V3	Monitor the 3.3 V power line SY8832AIC DC-DC converter
TP174	PWR_1V8	Monitor the 1.8 V power line SY8832AIC DC-DC converter
TP181	PWR_SoC_VCORE	Monitor the 0.8 V rail for the SoC synchronous buck converter
TP182	PWR_SoC_VCPU	Monitor the 0.8 V rail for the SoC synchronous buck converter
TP183	PWR_VDDM_1V1&0V6 VDDQ(0V6)	0.6 V DC-DC converter output buck regulator output voltage
TP184	PWR_VDDM_1V8 VDD1(1V8)	DC-DC converter output buck regulator output monitor
TP186	PWR_VDDM_1V1 VDD2(1V1)	DC-DC converter output buck regulator stability confirmation
TP190	PWR_VDD_SM	Power and decoupling monitoring
TP201	PWR_CONN-USB-C_VBUS	Check voltage after input fuse
TP202	GND	Ground net
TP203	I2S1_DO[3]	Monitor the I2S1 digital audio data stream on the DO line
TP204	SM_EXPANDER0.GPIO5	GPIO expander U12 GPIO5
TP205	SM_TEST_EN	Enable system test modes
TP206	SM_JTAG_SEL	Selects the JTAG interface
TP207	SM_TRSTn	Test reset pin for the JTAG interface
TP208	SM_TCK	System manager test clock for the JTAG/debug interface clock input
TP209	USB2_ID	Detect the role of the device as host or peripheral

8 Power Management and Low Power Modes

8.1 USB-C Power Usage and Limitations

The **Luna SL1680 SBC** can be **powered directly from a computer through the USB-C connector** when flashing the module, provisioning the operating system, or performing light functional testing. In this mode, the USB-C interface provides both the 5V VBUS input and the USB 2.0 data connection required for **Recovery Mode**, allowing reprogramming of the device's non-volatile memory without the need for additional power sources.

From a hardware perspective, the USB~2.0 D+/D- lines remain active while VBUS is supplying power, and no circuitry in the design inhibits simultaneous data transfer and power input over USB-C. The port operates strictly as a USB-C device (UFP) with a fixed 5V sink role. It does not implement USB Power Delivery (USB-PD), does not participate in power negotiation, and cannot source power to downstream peripherals. As such, the available input current is limited to what a standard USB host or hub can supply.

TBA
For operation under **higher computational load** or when additional peripherals are attached, an external regulated power supply **must** be used. Detailed power-consumption characterization is currently in progress and will be included in subsequent revisions of this document. Corresponding recommendations for the appropriate power-supply specifications will be provided once this evaluation is complete.

8.2 Power Management

The Luna SL1680 SBC integrates a **power management architecture** designed to ensure reliable system startup, orderly shutdown, and robust protection against fault conditions. The **power control and monitoring signals** provide coordinated management of supply rails, enable power sequencing, and facilitate advanced functions such as recovery mode entry, wake-up events, and system status indication.

- **Primary Power Input (PWR_CONN–USB-C_VBUS)**
  The Luna SL1680 SBC is powered from a **USB Type-C connector**, serving as the main external power source. Power sequencing begins only after stable detection and validation of this voltage input.
- **Main System Rails (PWR_5V, PWR_3V3, PWR_1V8)**
  These rails supply the primary logic and peripheral domains of the board, feeding onboard regulators and interface components.
- **Core Power Rails (PWR_SoC_VCORE, PWR_SoC_VCPU)**
  Dedicated rails provide regulated voltages to the **SL1680 SoC** core and CPU domains. Stable voltage levels on these rails are critical to SoC functionality.
- **Memory Power Rails (PWR_VDDM_1V1&0V6, PWR_VDDM_1V1, PWR_VDDM_1V8)**
  Separate low-voltage supplies serve the LPDDR4x memory subsystem and associated I/O domains, ensuring proper timing and data integrity.

8.2.1 Power Control and Sequencing

- **Power Control Signals (PWR_3V3_CTL, PWR_1V8_CTL)**
  These control lines enable the 3.3 V and 1.8 V rails, respectively. Each are asserted before the associated domain powers up, ensuring proper sequencing of dependent components.
- **Power Button Interface (ON/OFF Signal)**
  - **Short press (< 5 s):** Initiates system power-on or orderly shutdown.
  - **Long press (> 5 s):** Forces a complete power-off, aligning with the SoC's documented behavior.
- **Power Sequencing** Startup is governed by a controlled power-up protocol. Each rail activates within a defined timing window to prevent latch-up, guarantee correct memory initialization, and stabilize all domains before logic enablement.

8.2.2 Protection and Reliability Features

To ensure fault tolerance and electrical safety, the Luna SL1680 SBC integrates multiple hardware protection mechanisms across its power domains:

- **Over-Voltage Protection (OVP)**
  Monitors output voltages and shuts down or clamps regulators if limits are exceeded, protecting sensitive SoC and memory circuits.
- **Under-Voltage Lockout (UVLO)**
  Prevents activation of power domains when input voltages fall below safe thresholds, avoiding undefined behavior or potential data corruption.
- **Over-Current Protection (OCP)**
  Limits current draw from DC-DC converters and regulators, mitigating short-circuit risks. Current-sense resistors allow accurate fault detection and monitoring.

8.3 Power Budget and Management Strategy

The Luna SL1680 SBC's power budget is derived from the maximum consumption of all major subsystems, including the **SL1680 SoC**, **LPDDR4x DRAM**, **eMMC storage**, **network PHYs**, and peripheral ICs, with safety margins for transient and peak conditions.

Dynamic power optimization is implemented through the **PMIC** and the SoC's internal controllers using **dynamic voltage and frequency scaling (DVFS)**.
Unused subsystems can be selectively powered down to minimize idle power consumption.

Continuous voltage and current monitoring provide real-time feedback to both hardware and firmware, allowing adaptive regulation based on workload, thermal conditions, and input source health.

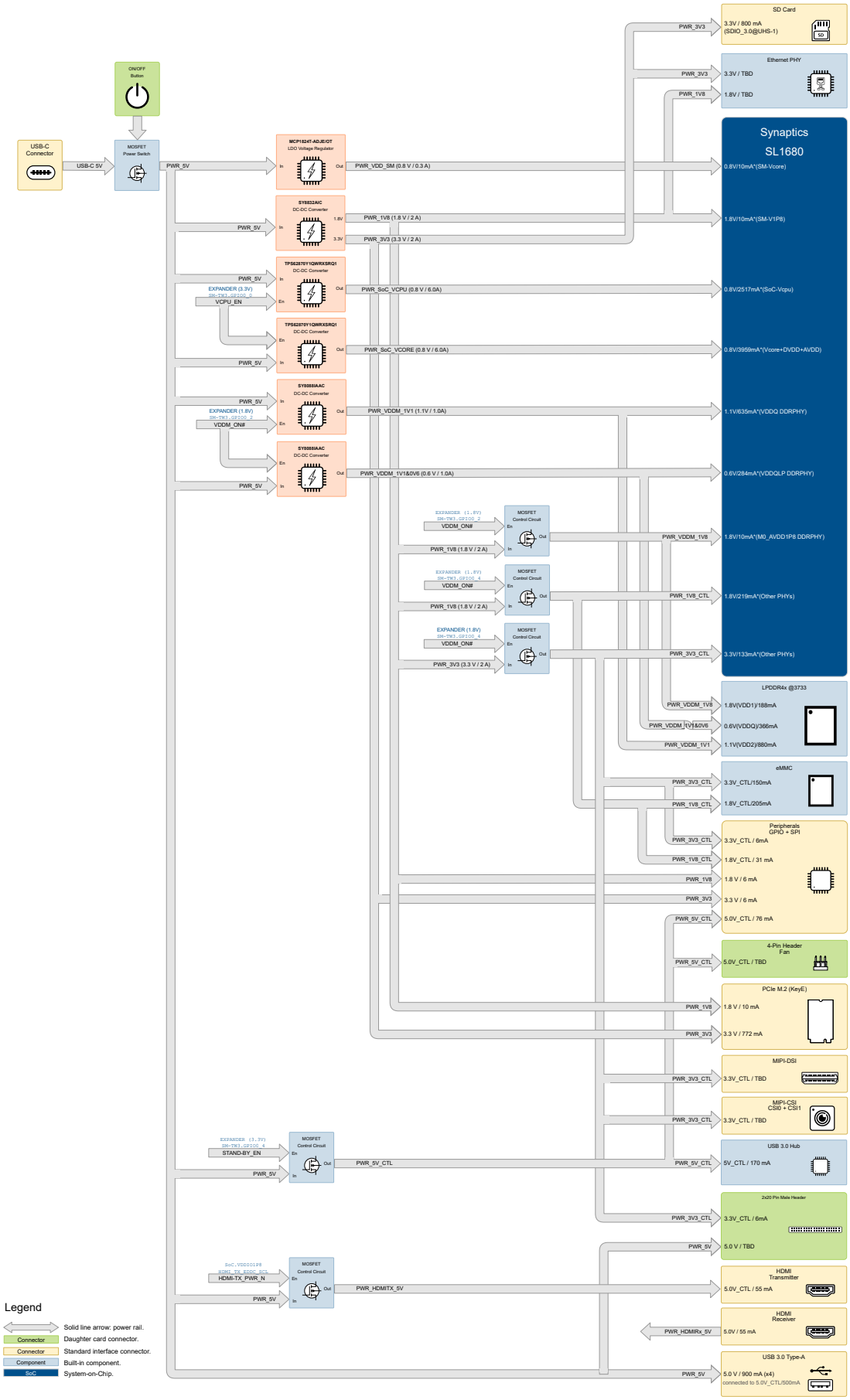
8.3.1 Power-Up Sequence for SL1680 SoC and LPDDR4x DRAM

The SL1680 SoC and its associated LPDDR4x memory modules require a coordinated power-up sequence to ensure reliable initialization and stable system operation.

1. Power Rail Ramp-Up
The main power rails (VDDCORE, VDDCPU, and VDDIO) are ramped simultaneously by the power management subsystem. DRAM supply lines (VDD1, VDD2, VDDQ) are given special attention, as they must reach stable voltage levels before memory initialization begins.
2. SoC Reset and Initialization
An external or internal reset ensures the SoC enters a defined safe state. All CPU cores and peripherals remain in reset until the power rails are stable.
3. PLL and Clock Stabilization
After reset de-assertion, the SoC's internal PLLs lock to their target frequencies. Stable clocks are then distributed to the CPU cores and memory controller, guaranteeing synchronized operation.
4. DRAM Reset and Training
Once the memory controller is powered and clocked, the LPDDR4x DRAM undergoes a reset sequence followed by initialization and calibration. This includes ZQ calibration to set impedance references and timing training to optimize signal integrity.
5. CPU and Peripheral Release
Following successful memory initialization and clock stabilization, the SoC releases CPU cores and peripherals from reset, allowing normal boot and runtime operation.

Figure 4 illustrates the full power distribution hierarchy, showing the primary rails, regulators, and downstream components. This helps visualize the sequencing described above.

Figure 4: Power tree



Power-Up Voltages Timing and Sequencing

1. **PWR_5V:** Initial input from VBUS and power-path controller.
2. **PWR_5V_stable:** Stabilizes the 5 V reference with minimal propagation delay.
3. **PWR_3V3 and PWR_3V3_CTL:** Enabled in the same PMIC phase group; provide primary IO supply.
4. **PWR_1V8 and PWR_1V8_CTL:** IO rails for analog and digital interfaces; ramp shortly after 3.3 V.
5. **PWR_VDDM_1V8:** Memory domain rail, sequenced after main IO rails.
6. **PWR_VDDM_1V1 and PWR_VDDM_0V6:** Low-voltage memory/mixed-signal rails; secondary outputs may slightly lag.
7. **PWR_SoC_VCPU and PWR_SoC_VCORE:** SoC core rails; last to ramp up to ensure all dependent subsystems are stable.

8.3.2 Reset and Power-On-Reset (POR)

SM_RSTIn (Reset Input)
The SM_RSTIn pin receives the system reset, typically from an external button, supervisory IC, or PMIC power-good signal. A 100 Ω resistor and 0.1 µF capacitor provide RC filtering to prevent spurious resets. A 2.2 kΩ pull-up ensures the line remains high during normal operation.

SM_POR_EN (POR Enable)
Controls whether the SoC's internal POR generator is active. Pulled up to 1.8 V to match the SoC I/O domain. Leaving it high enables POR; pulling it low bypasses it for test or debug scenarios.

All reset and POR signals are referenced to PWR_1V8, ensuring correct logic levels and protecting the SoC pins from voltage stress. Table 32 shows a summary of the POR signals.

Table 32: Power-On-Reset summary

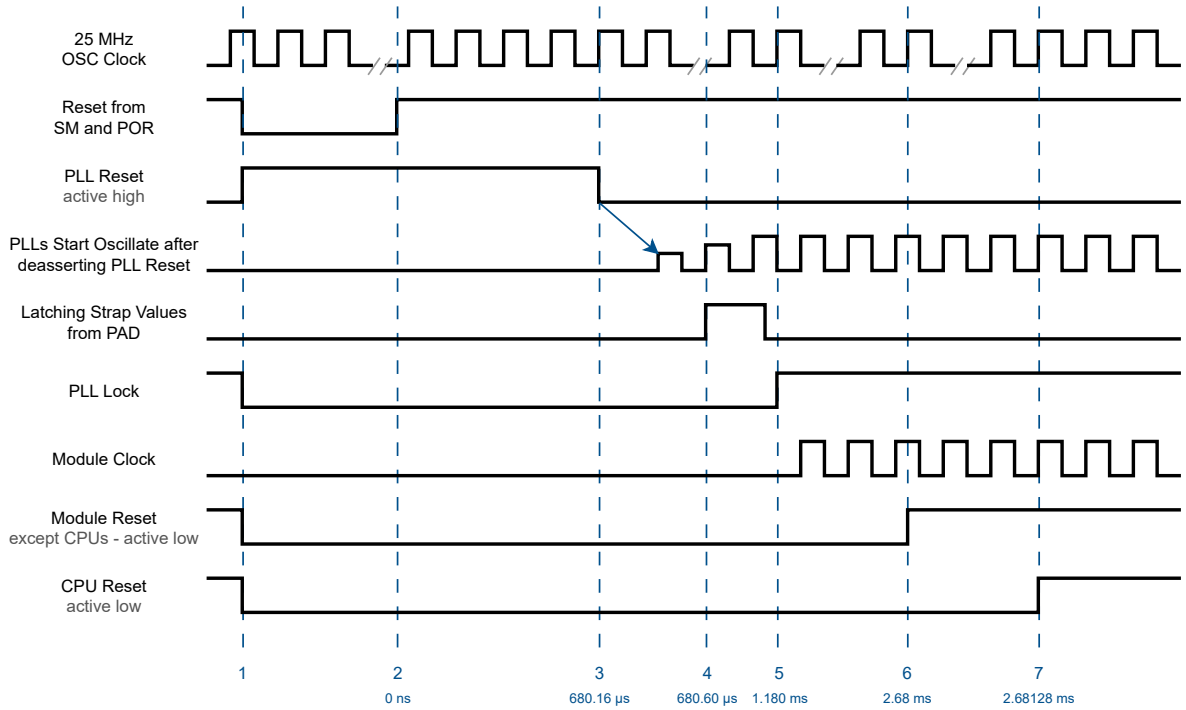
Signal	Function	Circuit Element	SoC Spec Reference
SM_RSTIn	Global reset input	RC filter, pull-up	External/system reset
SM_POR_EN	Enable POR circuitry	Pull-up, option DNS	Internal/external POR

Refer to Figure 5 for a detailed block diagram of the SL1680 power-up and reset timing.

System Power On and Reset Sequence

1. **25 MHz Oscillator Clock starts:** The external crystal oscillator generates the base system clock.
2. **System Reset and Power-On Reset released:** The Reset from SM (System Manager) and POR (Power-On Reset) are deasserted, allowing initialization to begin.
3. **PLL Reset deasserted:** Phase-Locked Loop (PLL) Reset transitions from active high to inactive, which enables the PLL circuitry.
4. **PLLs start oscillating:** After PLL Reset is deasserted, internal PLLs begin frequency synthesis and stabilization.
5. **Strap Values latched from PAD:** Configuration strapping values are read and latched from the board's PADs for proper system configuration.
6. **PLL Lock achieved:** PLL outputs stabilize, and the lock signal is asserted, allowing subsequent clocks to start.
7. **Module Clock and Resets released:** Module Clock starts oscillating, Module Reset (except CPUs) is released, and finally CPU Reset is released, allowing the CPU to begin executing.

Figure 5: Power-up sequence



8.3.3 GPIO Expanders

The Luna SL1680 SBC incorporates two **FXL6408UMX** GPIO expanders to extend the number of control and monitoring signals available to the system. These devices provide general-purpose digital I/O and within the Luna architecture they are primarily used to **control peripheral power-enable lines**, **monitor subsystem status**, and **coordinate low-power transitions** across various domains.

Each expander provides eight independently configurable pins that can operate as inputs or outputs, offering fine-grained control of power-relevant signals without increasing the processor's I/O load. Their interrupt capability allows immediate notification of state changes, enabling responsive wake-up events and efficient supervision of external components. Both hardware and software reset mechanisms ensure predictable behavior during system startup and recovery scenarios.

Highlights:

- Each pin is individually configurable as an input or output, with programmable default states and optional internal pull-ups/pull-downs.
- Outputs can source or sink up to **6 mA**, suitable for driving power-enable signals, reset lines, or status indicators.
- Supports **voltage-level translation** between the I^2C control interface and the controlled domains, allowing safe management of mixed-voltage peripherals.
- Operates at **I^2C speeds up to 400 kHz**, ensuring low-latency toggling of enable and reset signals during power sequencing.

- Low standby current (~**1.5 µA**) makes the expanders well-suited for **low-power and always-on** control tasks.

The GPIO expanders play a key role within the board's power-management strategy by providing reliable digital control points for regulators, switches, and other subsystems whose behavior must be coordinated during power-up, power-down, and runtime energy-saving modes.

Table 33: GPIO expanders

Expander	I²C	Address	Voltage	GPIO	Function	GPIO signaling
FXL6408UMX (U12)	SM-TW3	0x43 (7-bit)	3.3 V	GPIO0_0	VCPU/VCORE_ON#	0: Power ON VCPU/VCORE PMIC
						1: Power OFF
				GPIO0_1	PWR_ON_DSI	0: Power OFF
						1: Power ON
				GPIO0_2	VDDM_ON#	0: Power ON all VDDM PMICs (1V8/1V1/0V6)
						1: Power OFF
				GPIO0_3	VDDM-LPQ_OFF#	0: Power ON VDDM-LP PMICs (0V6)
						1: Power OFF
				GPIO0_4	STAND-BY_EN	0: Normal status
						1: Entry to Stand-By status with devices Powred down
				GPIO0_5	Not used	–
						–
				GPIO0_6	M2-PCIe_CLKREQ#	0: Triggered for M.2 PCIe Clock Request
						1: Idle
				GPIO0_7	GPIO_DSI	Reserved
						Reserved
FXL6408UMX (U13)	SM-TW3	0x44 (7-bit)	3.3 V	GPIO1_0	GPIO_CSI0	Reserved
						Reserved
				GPIO1_1	M2-PCIe_RST#	0: Assertion Reset for M.2 PCIe Module
						1: De-assertion
				GPIO1_2	M2-W_DISABLE1# (WL_REG_ON)	0: Assertion Disable to M.2 module by DISABLE1#
						1: De-assertion
				GPIO1_3	M2-W_HOST-WAKE# (BT_DEV_WAKE)	0: Assertion Wake from Host to M.2 module
						1: De-assertion
				GPIO1_4	PWR_ON_CSI0	0: Power OFF
						1: Power ON
				GPIO1_5	M2-W_DISABLE2# (BT_REG_ON)	0: Assertion Disable to M.2 module by DISABLE2#
						1: De-assertion
				GPIO1_6	GPIO_CSI1	Reserved
						Reserved
				GPIO1_7	PWR_ON_CSI1	0: Power OFF

Continued on next page

Table 33: GPIO expanders (Continued)

Expander	I²C	Address	Voltage	GPIO	Function	GPIO signaling
						1: Power ON

8.4 Low Power Modes

TBA
More information about low power modes will be available on the next releases of the datasheet.

9 Recovery Mode

Recovery Mode (USB Serial Loader) allows you to load new software onto the Luna SL1680 SBC even if the bootloader is corrupted or unable to start the system. This mode is not required during normal development, but it provides a reliable fallback mechanism when the module cannot boot on its own.

During system initialization, the SoC samples the **boot_src[1:0]** strap inputs to determine the primary boot source. These straps are latched exclusively during **cold power-up**, and their sampled logic levels dictate whether the ROM loader attempts to boot from SPI, eMMC, or enters the USB Serial Loader mode.

As summarized in Table 34, the module design applies weak **470 k**Ω pull resistors to define the default strap states, while headers **JP1** and **JP2** provide controllable override mechanisms. Installing the **JP2 recovery jumper** pulls **boot_src[0]** low, overriding the default strap level and forcing selection of the USB Serial Loader as the active boot path. Removing the jumper restores the default boot configuration on the next cold boot cycle.

Table 34: Boot Source Strap Definition

Jumper	Pad Name	Strap Name	Pull-Up/Pull-Down	Description
–	I2S2_MCLK	boot_src[0]	Pull-Down 470 kΩ	**CPU Boot Source bit[0].** Used in combination with boot_src[1] to select the device from which the ROM bootloader attempts to start the system. This signal is always pulled-down.
JP1	SPDIFO	boot_src[1]	Pull-Up 470 kΩ	**CPU Boot Source bit[1]**[1]**.** Boot mode selection: • 00: ROM boot from SPI; • 01: Reserved; • 10: ROM boot from eMMC; • 11: Direct boot from SPI (only with ENG_EN=1).
JP2	SPI1_SDO	software_strap[0]	Pull-Up 470 kΩ	**Straps for software usage.** ROM code will use this strap to decide booting from USB or not. • 0: Boot from USB; • 1: Boot from the device selected by boot_src. A low level on boot_src[1..0] during cold boot forces USB Serial Loader mode when the USB boot override circuit is enabled through header JP2.

[1] **JP1** sets the most significant bit.

10 Technical Specifications

10.1 Electrical Characteristics

The Luna SL1680 SBC expects a regulated 5 V input power supply with a typical current draw around 3 A, peaking during start-up or heavy load conditions up to 5 A (25 W). The power input circuitry includes undervoltage lockout (UVLO) at approximately 4.4 V and overvoltage protection (OVP) capable of withstanding transient surges up to 20 V on the USB-C power line for safety.

Power rails generated by on-board DC-DC converters and LDOs adhere to strict voltage tolerance limits, maintaining stable 3.3 V and other intermediate voltages as specified, with output variation restricted to ±5% typical.

All operating conditions including temperature ranges conform to industrial standards to ensure reliability in diverse environments.

Table 35: Power inputs - absolute maximum ratings

Parameter	Symbol	Minimum Value (Absolute)	Typical Value	Maximum Value (Absolute)	Unit
Main Power Supply Voltage	V_{IN}	4.75	5.00	5.25	V
Input Current (Max)	I_{IN}	–	3.00	5.00	A
USB-C Power Rail Voltage	V_{USB-C}	4.40 (UVLO)[1]	5.00	20.0 (OVP surge)[2]	V

[1] Undervoltage lockout: disables a device when the input voltage falls below a safe threshold.
[2] Overvoltage protection, specifically guards against transient voltage spikes.

Table 36: Operating conditions

Parameter	Symbol	Minimum Value	Typical Value	Maximum Value	Unit
Operating Temperature	T_{OP}	-40	25	85	°C
Storage Temperature	T_{STG}	-40	–	125	°C
DC-DC Converter Input Voltage	V_{DC-IN}	3.3	5.0	5.5	V
LDO Output Voltage	V_{LDO}	3.0	3.3	3.6	V

10.2 Mechanical Characteristics

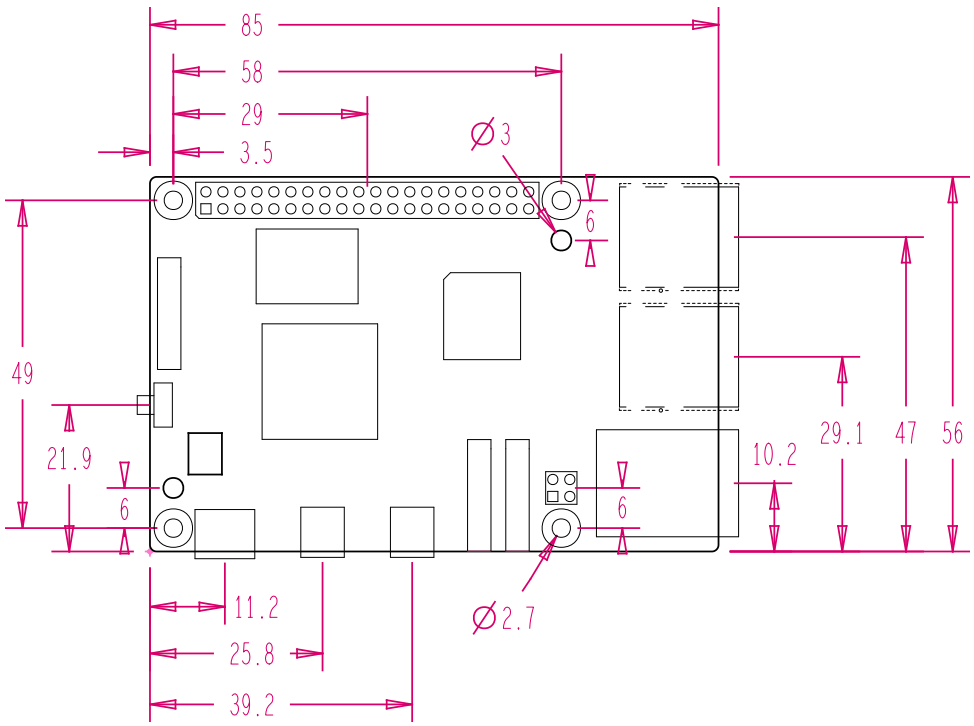
10.2.1 Mechanical Specifications and Dimensions

- Board dimensions: 85 mm × 56 mm × 17mm

Tolerance for all measures:
- ±0.1mm, unless otherwise specified.

Refer to Figure 6 for detailed mechanical dimensions and tolerances of the module.

Figure 6: Mechanical drawing



10.3 Thermal Specification

Thermal management is critical for ensuring optimal performance, reliability, and longevity of embedded computing platforms such as the Luna SL1680 SBC. Drawing from best practices used in Toradex's family of System on Modules and carrier boards, the thermal design guidelines and considerations described in Table 37 apply.

Table 37: Thermal operating parameters

Parameter	Symbol	Minimum Value	Typical Value	Maximum Value	Unit
Operating Temperature	T_{OP}	-40	25	85	°C
Storage Temperature	T_{STG}	-40	–	105	°C
Maximum Junction Temp.	T_J	–	95	105	°C
Recommended Ambient Temp.	T_{AMB}	-40	25	85	°C

Thermal Design Guidelines

- Apply thermal pads or pastes between hot components and heat spreaders or chassis.
- Avoid insulating materials between components and heat dissipation paths.
- Measure temperature at critical points during development using thermocouples or thermal cameras.
- Design firmware to implement thermal throttling and power management in response to elevated temperatures.
- Ensure board layout and system integration optimize thermal conductivity within mechanical constraints.

11 Device and Documentation Support

11.1 Product Compliance

TBA
More information about compliance will be available on the next releases of the datasheet.

11.2 Trademarks

TBA
More information about trademarks will be available on the next releases of the datasheet.

DISCLAIMER