

Revision History

Document Revisions

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1 Introduction

1.1 Purpose of the Datasheet

This document describes the hardware characteristics and capabilities of the Aquila iMX95 System-on-Module (SoM). It is intended as a technical reference for hardware designers, system integrators, and developers working with this module.

For information regarding currently supported software features and integration details, please refer to the Aquila iMX95 product page on the Toradex Developer Center:

<https://developer.toradex.com/hardware/aquila-som-family/modules/aquila-imx95>

1.2 Abbreviations

Table 1: Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface

Continued on next page

Table 1: Abbreviations (Continued)

Abbreviation	Explanation
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMI	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I ² C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI

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Table 1: Abbreviations (Continued)

Abbreviation	Explanation
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.3 Aquila SoM Family

The Aquila System-on-Module (SoM) family simplifies the design of modern embedded systems by encapsulating complex high-density circuitry and impedance-controlled layouts within a compact, production-ready module. This allows carrier board development to focus primarily on application-specific requirements, reducing overall design complexity and time-to-market.

Equipped with an optional Wi-Fi 7 and Bluetooth 5.3 interface, this SoM ensures cutting-edge connectivity. Its extensive range of interfaces spans from fundamental GPIOs to industry-standard I2C, I3C, SPI, USB, CAN FD, and UART buses. Furthermore, it accommodates advanced features like MIPI CSI camera interfaces, MIPI DSI display interface, and PCIe Gen3 ports.

The Aquila iMX95 module incorporates a Gigabit Ethernet PHY with IEEE1588 support directly on the module. For enhanced versatility, the SoC includes a second Ethernet MAC with an RGMII interface, enabling the addition of a Gigabit Ethernet PHY on the carrier board for dual Ethernet applications. A third Ethernet MAC with a SGMII/USXGMII interface is available for incorporating a 2.5 or 10-Gigabit Ethernet PHY on the carrier board.

For functional safety applications, the i.MX 95 SoC supports ISO 26262 ASIL-B and IEC 61508 SIL-2 compliance. A functional safety-ready Configure-to-Order (CTO) variant of the Aquila iMX95 SoM is available for systems requiring certified safety features, such as automotive, medical and industrial applications.

In summary, the Aquila iMX95 combines high performance, robust connectivity, and advanced feature integration in a scalable platform suitable for industrial, medical, automotive, and other demanding applications.

1.4 NXP i.MX 95 SoC

The Aquila iMX95 SoM is based on the NXP i.MX 95 family of System on Chips (SoCs).

The i.MX 95 family features up to 6 Cortex®-A55 (often shortened to A55) cores as the main processor cluster. These cores provide full 64-bit Arm®v8.2 support while maintaining seamless backward compatibility with 32-bit Arm®v7-A software. The A55 cores run at up to 1.8 GHz and include the following upgrades:

- Faster integer operations
- An enhanced floating-point unit (FPU)
- An L3 cache (in addition to L1 & L2) for improved multicore performance and reduced memory latency.

Additional processors in the heterogeneous multicore architecture include:

- 1x Cortex®-M7 (often shortened to M7), peaking up to 800 MHz.
- 1x Cortex®-M33 (often shortened to M33), peaking up to 333 MHz.

In addition to general-purpose MCUs use, the M33 and M7 cores can be configured as a safety island to support functional safety. This heterogeneous multicore architecture supports running real-time operating systems for time and safety-critical tasks.

The SoC also includes the following specialized processors and accelerators:

- **Mali-G310 GPU** from Arm®: Capable of up to 64 GFLOPs (FP32) and supports OpenCL™ 3.0, OpenGL® ES 3.2, Vulkan®1.3
- **Neural Processing Unit (NPU)**: Delivers up to 2.0 TOPS to significantly accelerate machine learning tasks
- **Video Processing Unit (VPU)**: Accelerates video decoding and encoding
- **Image Signal Processor (ISP)**: Supports both video and still image pipelines with image processing and color space conversion

The SoC even includes a new security enhancement: the EdgeLock® Secure Enclave—a fully isolated subsystem that supports functions such as secure boot, runtime attestation, trust provisioning, key management and other cryptographic operations. This dedicated security unit also simplifies certification for standards such as IEC 62443, US Cyber Trustmark and the Cyber Resilience Act.

1.4.1 Error Correcting Code (ECC)

The i.MX 95 series SoCs feature a Coherent 512 kB L3 cache with built-in Error Correcting Code (ECC) to enhance data integrity and reliability within the system. ECC functionality is critical for detecting and correcting single-bit errors in the cache memory, thereby preventing data corruption and improving system robustness in demanding applications. The i.MX 95 family features inline ECC for LPDDR4/LPDDR5 DRAM to improve system reliability and safety. For comprehensive information on ECC operations and principles, refer to the general ECC documentation available for NXP's i.MX 8 series processors ([AN13566](#)). This text serves as a supplement to the Cache and Memory Controller chapters in the i.MX 95 Applications Processor Reference Manual.

1.5 Main Features

1.5.1 CPU

The Aquila iMX95 integrates a high-performance CPU cluster based on up to six Arm® Cortex®-A55 cores. Each core runs at up to 1.8 GHz and supports the Armv8.2-A 64-bit architecture with backward compatibility for 32-bit Armv7-A applications.

Key enhancements of the Cortex-A55 cores include:

- improved integer processing performance;
- enhanced floating-point unit (FPU) for optimized mathematical operations;
- integrated L3 cache, in addition to L1 and L2, for reduced memory latency and improved multicore efficiency.

Table 2: CPU

Parameter	Aquila iMX95 Hexa 8GB WB IT	Aquila iMX95 Hexa 8GB IT	Aquila iMX95 Hexa 4GB WB IT	Aquila iMX95 Hexa 4GB IT	Aquila iMX95 Hexa 2GB ET
SoC	MIMX9596	MIMX9596	MIMX9596	MIMX9596	MIMX9596
A55 Cores	6	6	6	6	6
M7 Cores	1	1	1	1	1
M33 Cores	1	1	1	1	1

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Table 2: CPU (Continued)

Parameter	Aquila iMX95 Hexa 8GB WB IT	Aquila iMX95 Hexa 8GB IT	Aquila iMX95 Hexa 4GB WB IT	Aquila iMX95 Hexa 4GB IT	Aquila iMX95 Hexa 2GB ET
L1 Instruction Cache per core	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB
L1 Data Cache per core	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB	A55: 32 kB
L2 Cache per core	A55: 64 kB	A55: 64 kB	A55: 64 kB	A55: 64 kB	A55: 64 kB
L3 Cache shared between cores	A55: 512 kB	A55: 512 kB	A55: 512 kB	A55: 512 kB	A55: 512 kB
Data Tightly Coupled Memory	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB
Instruction Tightly Coupled Memory	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB	M7: 256 kB ¹ M33: 256 kB

¹ The sizes of Instruction Tightly Coupled Memory (ITCM) and Data Tightly Coupled Memory (DTCM) are configurable, with default values of 256 kB for ITCM and 256 kB for both ITCM DTCM. Both memories feature an ECC interface.

1.5.2 GPU

The module incorporates the Arm® Mali-G310 graphics processor, providing up to 64 GFLOPs (FP32). The GPU supports:

- OpenGL® ES 3.2
- Vulkan® 1.3
- OpenCL™ 3.0

This GPU delivers a balanced combination of performance and efficiency, enabling responsive graphics, advanced UI rendering, and compute acceleration for embedded and industrial applications.

Table 3: GPU

Parameter	Aquila iMX95 Hexa 8GB WB IT	Aquila iMX95 Hexa 8GB IT	Aquila iMX95 Hexa 4GB WB IT	Aquila iMX95 Hexa 4GB IT	Aquila iMX95 Hexa 2GB ET
GPU Model	Arm Mali-G310	Arm Mali-G310	Arm Mali-G310	Arm Mali-G310	Arm Mali-G310
2D Acceleration	Yes	Yes	Yes	Yes	Yes
3D Acceleration	Yes	Yes	Yes	Yes	Yes
FLOPs	FP32: 64	FP32: 64	FP32: 64	FP32: 64	FP32: 64
L2 Cache	128 kB	128 kB	128 kB	128 kB	128 kB
MSAA anti-aliasing	up to 4x	up to 4x	up to 4x	up to 4x	up to 4x
OpenCL	up to 2.2	up to 2.2	up to 2.2	up to 2.2	up to 2.2
OpenGL ES	up to 3.2	up to 3.2	up to 3.2	up to 3.2	up to 3.2
Vulkan	1.2	1.2	1.2	1.2	1.2

1.5.3 Interfaces

The Aquila iMX95 offers a wide set of interfaces to accommodate diverse system requirements:

- general-purpose digital I/O (GPIO);
- I²C, I³C, SPI, and UART serial buses;
- USB 2.0 / 3.2 Gen 1 ports;
- CAN FD (Flexible Data-rate);
- PCI Express Gen3;
- MIPI CSI and DSI for camera and display connectivity;
- Dual Gigabit Ethernet with IEEE 1588 support, and optional multi-Gigabit Ethernet via external PHYs.

Table 4: SoM interfaces

Parameter	Aquila iMX95 Hexa 8GB WB IT	Aquila iMX95 Hexa 8GB IT	Aquila iMX95 Hexa 4GB WB IT	Aquila iMX95 Hexa 4GB IT	Aquila iMX95 Hexa 2GB ET
Analog					
Analog Input	8	8	8	8	8
Audio					
Audio Interfaces	9 <i>I2S, PDM or S/PDIF</i>	9 <i>I2S, PDM or S/PDIF</i>	9 <i>I2S, PDM or S/PDIF</i>	9 <i>I2S, PDM or S/PDIF</i>	9 <i>I2S, PDM or S/PDIF</i>

Continued on next page

Table 4: SoM interfaces (Continued)

Parameter	Aquila iMX95 Hexa 8GB WB IT	Aquila iMX95 Hexa 8GB IT	Aquila iMX95 Hexa 4GB WB IT	Aquila iMX95 Hexa 4GB IT	Aquila iMX95 Hexa 2GB ET
Camera					
MIPI-CSI-2	1x Quad Lane	2x Quad Lane	2x Quad Lane	2x Quad Lane	2x Quad Lane
Display					
Display trollers	Con- Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)
DisplayPort	1x up to 4k via DSI to eDP converter	-	-	-	-
LVDS	1x (up to 1920x1080)	1x (up to 1920x1080)	1x (up to 1920x1080)	1x (up to 1920x1080)	1x (up to 1920x1080)
MIPI DSI	-	1x Quad Lane up to 4k	1x Quad Lane up to 4k	1x Quad Lane up to 4k	1x Quad Lane up to 4k
Low Speed					
CAN FD	5x	5x	5x	5x	5x
GPIO	14x + 92x	14x + 92x	14x + 92x	14x + 92x	14x + 92x
I ² C	8x	8x	8x	8x	8x
I ³ C	1x	1x	1x	1x	1x
JTAG	1x	1x	1x	1x	1x
PWM	22	22	22	22	22
OSPI	1x	1	1	1	1
QSPI	1x	1	1	1	1
SPI	6x	6x	6x	6x	6x
UART	8x	8x	8x	8x	8x
Network					
Bluetooth	Bluetooth 5.3	-	Bluetooth 5.3	-	-
USX/S/GMII (for 2.5 and 10 Gb Ethernet)	1x	1x	1x	1x	1x
Wi-Fi	2x2 Wi-Fi 7 (802.11be)	-	2x2 Wi-Fi 7 (802.11be)	-	-
Storage					
SDIO/SD/MMC	2x	2x	2x	2x	2x
USB					
USB 2.0 Host and Client	1x Host	2x Host	1x Host	2x Host	2x Host
USB 3.2 Gen 1 Host and Client	1x OTG Gen 1	1x OTG Gen 1	1x OTG Gen 1	1x OTG Gen 1	1x OTG Gen 1

1.5.4 Memory and Storage

The Aquila iMX95 offers multiple configurable memory and storage capacities to meet diverse application requirements, allowing designers to select the optimal balance of performance and non-volatile storage.

- **RAM Density:** Available configurations include 2GB, 4GB, 8GB, and 16GB of LPDDR5 memory, enabling scalable performance tailored to application requirements.
- **eMMC Storage Capacity:** Supported embedded eMMC options range from 4GB up to 256GB,

including 4GB, 8GB, 16GB, 32GB, 64GB, 128GB, and 256GB, providing flexibility in non-volatile storage according to system needs.

Table 5: Memory features

Parameter	Aquila iMX95 Hexa 8GB WB IT	Aquila iMX95 Hexa 8GB IT	Aquila iMX95 Hexa 4GB WB IT	Aquila iMX95 Hexa 4GB IT	Aquila iMX95 Hexa 2GB ET
eMMC					
eMMC Configuration	2D MLC ¹	2D MLC ¹	2D MLC ¹	2D MLC ¹	2D MLC ¹
eMMC Capacity	32GB	32GB	32GB	32GB	16GB
I²C EEPROM					
I ² C EEPROM Capacity	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits
RAM					
RAM Capacity	8GB	8GB	4GB	4GB	2GB
RAM Configuration <i>ctrl. × ch. × bits²</i>	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16	32-bit Dual Die 1 × 2 × 16
RAM Type	LPDDR5	LPDDR5	LPDDR5	LPDDR5	LPDDR5
RAM Speed	6400MT/s	6400MT/s	6400MT/s	6400MT/s	6400MT/s
Inline ECC	Yes	Yes	Yes	Yes	Yes

¹ Some eMMC partitions support Enhanced (SLC) mode.

² Controllers × channels per controller × bits per channel.

1.5.4.1 RAM – LPDDR5

The memory used in this system is LPDDR5 (Low Power Double Data Rate 5), a high-performance, low-power DRAM technology optimized for modern SoCs. LPDDR5 delivers enhanced data transfer rates and improved power efficiency, making it well-suited for applications in mobile, embedded, and industrial systems. This memory technology significantly advances over previous generations, enabling faster and more power-efficient access crucial for demanding tasks such as advanced multimedia processing, AI workloads, and real-time applications.

Key features are:

- **High-Speed Data Transfer:** LPDDR5 supports data rates up to 6400 MT/s (Mega Transfers per second), enabling rapid memory access and bandwidth.
- **Low Power Consumption:** Incorporates features such as dynamic voltage scaling, deep power-down modes, and improved clock gating to reduce power usage during idle or low-activity phases.
- **Enhanced Reliability:** Includes error correction and signal integrity enhancements for improved data accuracy under various operating conditions.
- **Wide I/O Interface:** Typically implemented with 16-bit or 32-bit wide data buses, supporting multiple channels for increased parallelism and throughput.
- **Advanced Timing and Command Structure:** Supports fine-grained refresh control, low-latency access, and new command encodings to optimize memory performance.

Performance Parameters

- **Clock Frequency:** Supports internal clock frequencies compatible with peak data rates, with phase-locked loop (PLL) circuits ensuring timing precision.
- **CAS Latency:** Programmable CAS latencies, typically ranging from 14 to 22 cycles, to balance

speed and power.

- **Refresh Schemes:** Adaptive per-bank and fine granularity refresh modes to optimize power consumption during refresh cycles.
- **Burst Length:** Supports burst lengths of 16 or 32 to enhance data transfer efficiency.

Electrical and Physical Characteristics

- **Memory Density:** Available in configurations ranging from 1Gb to 32Gb per chip, enabling module capacities suitable for 2GB up to 16GB or more.
- **Operating Voltage:** Core voltage in the range of approximately 1.1V ± 0.1V with I/O voltages standardized at 1.8V for interface signals.
- **Package Type:** BGA package optimized for automated assembly and thermal management.
- **Operating Temperature:** Industrial grade LPDDR5 variants support operation from -40°C to +85°C, ensuring reliability across harsh environments.

Integration Considerations

- **Interface Compatibility:** Designed for seamless integration with modern SoCs supporting LPDDR5 memory controllers, featuring compatibility layers for backward support with LPDDR4 standards where applicable.
- **Signal Integrity:** Requires careful PCB layout following controlled impedance and minimal crosstalk guidelines to preserve high-speed data integrity.
- **Memory Channel Configuration:** Supports single and dual-channel configurations offering flexibility in memory bandwidth and capacity scaling.
- **Power Management:** Interfaces with system PMICs for dynamic voltage and frequency scaling, enabling energy-efficient operation under variable workload demands.

Reliability and Safety

- **ECC Support:** Optional on-chip error-correcting code (ECC) support or system-level ECC implementation to detect and correct single-bit errors.
- **Thermal Management:** Designed to operate reliably under thermal stress with built-in temperature sensors for thermal throttling and system monitoring.
- **Built-in Self Test (BIST):** Supports built-in self-test features for manufacturing test and in-field diagnostics.

1.5.5 Physical

Table 6: Physical features

Parameter	Aquila iMX95
Module Dimensions	85.0 × 55.0 × 8.0 mm
Temperature Range	-40 °C to +85 °C
Shock / Vibration	EN 60068-2-6/50g 20ms

1.5.6 PCB

The Aquila iMX95 is designed with a 10-layer PCB to support signal routing, power distribution, and grounding requirements. This multi-layer configuration ensures optimal signal integrity, electromagnetic compatibility, and mechanical stability for the module.

1.6 Interface Overview

Features of the Aquila module are split into three distinct categories: **Always Compatible**, **Reserved** and **Module-specific**. The Always Compatible and Reserved pins are also referred to as the **Aquila Standard** pins. In addition to this definition, the i.MX 95 SoC supports alternate functions. These pins can operate as GPIOs but may be used for other purposes (e.g., UART).

Always Compatible interfaces are features that must be present on every SoM in the Aquila Family, ensuring upgradability and maximum scalability.

Reserved interfaces are defined features that may be absent on some SoM models due to unavailability. This may occur if a specific SoC does not support a particular interface or if an assembly option omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This ensures that any Aquila SoM can be reliably inserted into any Aquila carrier board without risk of damage due to incompatible Reserved pins.

A **Module-specific feature is not guaranteed to be functionally or electrically compatible across different Aquila modules**. When a carrier board design utilizes such module-specific features, other Aquila modules may not support these features and could assign different functions to the same pins, thereby limiting the range of compatible modules. This incompatibility between a system-on-module (SoM) and carrier board can result in loss of functionality or potentially cause hardware damage to either component. Furthermore, reliance on module-specific pins may restrict or prevent future system upgrades.

The **Alternate Functions** group refers to interfaces provided as additional functions on Always Compatible, Reserved, or Module-specific pins. These functions can be used only if the primary function of the pin is not in use.



Using **Module-Specific** signals introduces the risk of functional incompatibility and potential hardware damage when swapping modules. Designs relying on these pins may also limit or prevent future scalability across the Aquila family.

Whenever possible, prioritize **Always Compatible** interfaces in carrier board designs. This maximizes portability, simplifies software reuse, and preserves compatibility across future Aquila modules.

Table 7 lists the interfaces supported on the Aquila iMX95 module, along with the group in which each feature is provided: Always Compatible, Reserved, Module-specific or Alternate Function.

Table 7: X1 interfaces

Feature	Total	Always Compatible	Reserved	Module-specific or Alternate Function
Analog				
Analog Input <i>ADC</i>	8x	0x	4x	4x
Audio				
I ² S	4x	0x	2x	2x ¹
S/PDIF <i>RX and TX</i>	1x	0x	0x	1x ¹
PDM Mic Input	4x	0x	0x	4x ¹
Camera				
MIPI CSI-2	2x	0x	1x	1x ¹

Continued on next page

Table 7: X1 interfaces (Continued)

Feature	Total	Always Compatible	Reserved	Module-specific or Alternate Function
Display				
DisplayPort <i>on-SoM DSI to DP converter</i>	1x	0x	1x	0x
MIPI DSI	1x	0x	1x	0x
LVDS <i>dual channel</i>	1x	0x	0x	1x
Low Speed				
I ² C	8x	1x	3x	4x ¹
I3C	1x	1x	0x	0x
SPI	6x	1x	1x	4x ¹
UART	8x	3x	1x	4x ¹
PWM	22x	2x	2x	18x ¹
CAN FD	5x	0	4x	1x ¹
JTAG	1x	1x	0x	0x
QSPI	1x	0	1x	0x
OSPI	1x	0	0x	1x ¹
GPIO	106x	8x	6x	92x ¹
High-Speed				
PCIe Gen3	2x	1x	1x ²	0x
Network				
Gigabit Ethernet	1x	1x	0x	0x
RGMI I <i>for 2nd Gigabit Ethernet</i>	1x	0	0x	1x ¹
USX/S/GMI I <i>for 2.5 and 10 Gb Ethernet</i>	1x	0	1x	0x
Storage				
SD/SDIO/MMC	2x	1x	0x	1x ¹
USB				
USB 2.0 DRP	1x	1x	0x	0x
USB 2.0 Host	2x ²	1x	0x	1x ²
USB 3.2 Gen 1 OTG <i>SS Signals for USB 2.0 DRP</i>	1x	0	1x	0x

¹ Not all interfaces are exposed on dedicated board-to-board connector pins by default. Some features require enabling alternate functions on multiplexed pins via software configuration.

² Only on modules without Wi-Fi.

1.7 Reference Documents

1.7.1 Aquila Carrier Board Design Guide

To ensure compatibility with the Aquila module family, custom carrier boards must follow the Aquila Carrier Board Design Guide. Review this document thoroughly before beginning your design.

https://docs.toradex.com/116803-aquila_carrier_board_design_guide.pdf

1.7.2 Aquila Family Specification

This document outlines the specification that defines the Aquila Computer on Module family. It describes the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also explains the mechanical form factor, including key dimensions and potential thermal solutions.

<https://developer.toradex.com/hardware/aquila-som-family/aquila-family-specification>

1.7.3 Layout Design Guide

This document provides guidance on high-speed layout design and other factors that help ensure a correct carrier board layout on the first attempt.

<https://developer.toradex.com/carrier-board-design/carrier-board-design-guides/#custom-aquila-carrier-board>

1.7.4 Toradex Developer Center

The Toradex Developer Center is regularly updated with the latest product support information. It contains a wealth of additional resources.

Note that the Developer Center is shared across all Toradex products. Always verify that the information is applicable to the Aquila iMX95.

1.7.5 Aquila Carrier Board Schematics

Toradex provides complete schematics and an Altium project file that includes library symbols and IPC-7351-compliant footprints for the Aquila Development Board, as well as other carrier boards, free of charge. This resource is highly useful when designing your own carrier board.

<https://developer.toradex.com/hardware-resources/arm-family/carrier-board-design>

1.7.6 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring pin multiplexing on Aquila, Verdin, Apalis and Colibri modules. It also allows you to compare interfaces across different modules.

<https://developer.toradex.com/knowledge-base/pinout-designer>

1.7.7 NXP i.MX 95

Additional details about the NXP i.MX 95 SoC are available in the datasheet and reference manual provided by NXP.

<https://www.nxp.com/products/i.MX95>

1.7.8 EEPROM

The Aquila iMX95 includes an on-module I²C EEPROM: the M24C02-FMC6TG from STMicroelectronics.

<https://www.st.com/en/memories/m24c02-f.html>

1.7.9 I/O Expanders

The Aquila iMX95 features two on-module I/O expanders: the PCAL6416AHF and the PCAL6408AHKX from NXP.

<https://www.nxp.com/part/PCAL6416AHF>

<https://www.nxp.com/part/PCAL6408AHK>

1.7.10 Ethernet Transceiver

The Aquila iMX95 SoM utilizes the DP83867IRRGZR industrial-temperature, robust Gigabit Ethernet PHY transceiver from Texas Instruments.

<https://www.ti.com/product/DP83867IR>

1.7.11 PCB Temperature Sensor

The Aquila iMX95 can be assembled with an onboard PCB temperature sensor: the TI TMP1075DSGR.

<https://www.ti.com/product/TMP1075>

1.7.12 Real-Time Clock (RTC)

The Aquila iMX95 features the low-power Epson RX8130CE:B3 real-time clock.

<https://www5.epsondevice.com/en/products/rtc/rx8130ce.html>

1.7.13 TPM 2.0 Module

The Aquila iMX95 can be assembled with a Trusted Platform Module (TPM 2.0): the ST33KTPM2I3WBZA9 from STMicroelectronics. Complete documentation is available only under an NDA with STMicroelectronics.

<https://www.st.com/en/secure-mcus/st33ktpm2i.html>

1.7.14 Wi-Fi and Bluetooth Module

The WB versions of the Aquila iMX95 utilize a SX-PCEAX-SMT-SP host-based module that supports Wi-Fi 7, Bluetooth 5.3 and IEEE 802.15.4. This module uses two MHF4 antenna connectors.

<https://www.silextechnology.com/connectivity-solutions/embedded-wireless/sx-pceax>



Information about pre-certified antennas and cables are coming soon.

1.8 Naming Convention

This document follows a consistent naming convention. Pay close attention to punctuation and spacing in names. Do not confuse the NXP i.MX 95 SoC with the Toradex Aquila iMX95 SoM.

Table 8: Toradex naming conventions

Name	Description
i.MX 95	NXP i.MX 95 System on Chip family.
Aquila iMX95	Aquila module based on the i.MX 95 SoC. In this document, the term Aquila iMX95 refers to all versions of the module.
Aquila iMX95 Hexa 8GB WB IT	Aquila module based on the i.MX 95 SoC with 6 cores, 8 GB of RAM, Wi-Fi 7, Bluetooth and support for the industrial temperature range (IT).

1.8.1 Part Number Nomenclature

The part number nomenclature consists of a structured sequence of nine fields, each representing a specific configurable attribute of the device within the family. These fields encode key parameters such as RAM density, embedded eMMC storage capacity, DSI interface usage, integrated temperature sensor presence, Wi-Fi connectivity, and TPM security module inclusion. This arrangement enables precise identification and differentiation of variants based on their feature sets and functional capabilities. For clarification and detailed visualization, refer to Tables 9 and 10, which provides an illustrative example of the part number formation and the significance of each individual field.

Table 9: Part number nomenclature example

Family name	iMX95 segment	A-Core qty	RAM	eMMC	DSI usage	WiFi	TPM	Temperature
AQIMX95	9	6	-8G	-32G	-DP	-W7	-T	-IT

Table 10: Part number nomenclature options

Field	Options
Family name	
AQIMX95	Aquila iMX95 system-on-module
iMX95 segment	
9	NXP i.MX 95 19x19 system-on-chip
Cortex-A core quantity	
6	6 Cortex®-A55 cores
Ram density	
-2G	2 GB
-4G	4 GB
-8G	8 GB
-16G	16 GB
eMMC capacity	
-4G	4 GB
-8G	8 GB
-16G	16 GB
-32G	32 GB
-64G	64 GB
-128G	128 GB
-256G	256 GB
DSI usage	
-DP	DSI to DP converter (SN65DSI86)
-DSI	On DSI_1 of Aquila connector
-CSI	On CSI_2 of Aquila connector
Wi-Fi	
-W7	Wi-Fi 7 - Bluetooth 5.3
-W6E	Wi-Fi 6E - Bluetooth 5.2 (CT & WT only)

Continued on next page

Table 10: Part number nomenclature options (Continued)

Field	Options
-W5	Wi-Fi 5 - Bluetooth 5.3
-W0	No Wi-Fi/Bluetooth module
TPM	
-T	TPM 2.0 assembled
-N	TPM 2.0 not assembled
Temperature	
-IT	Industrial (-40 °C - 85 °C)
-ET	Extended (-25 °C - 85 °C)
-CT	Commercial (0 °C - 70 °C)

If your desired configuration is not available please get in touch with your Toradex sales representative mentioning the NPI part number desired.



Please note that the NPI part number nomenclature shown below does not reflect volume or sellable part numbers from Toradex. It should only be used to communicate your desired configuration.

1.9 Concept Configurations

[Section 1.5](#) displays an overview of the concept configurations. Interface counts shown are maximum supported; actual availability may vary by configuration and pin-muxing choices. We recommend using [Toradex Pinout Designer Tool](#) when designing your system.



The configurations shown below are as they are named merely concepts. They may or may not make it to be off the shelf products.

Table 11: Concept configurations

Features	Aquila iMX95 Hexa 8GB WB IT AQIMX9596-8G-32G-DP-W7-N-IT	Aquila iMX95 Hexa 8GB IT AQIMX9596-8G-32G-DSI-W0-N-IT	Aquila iMX95 Hexa 4GB WB IT AQIMX9596-4G-32G-CSI-W7-N-IT	Aquila iMX95 Hexa 4GB IT AQIMX9596-4G-32G-CSI-W0-N-IT	Aquila iMX95 Hexa 2GB ET AQIMX9596-2G-16G-DSI-W0-N-ET
CPU Details					
CPU Name	NXP MIMX9596	NXP MIMX9596	NXP MIMX9596	NXP MIMX9596	NXP MIMX9596
CPU Type	6x Arm Cortex®-A55	6x Arm Cortex®-A55	6x Arm Cortex®-A55	6x Arm Cortex®-A55	6x Arm Cortex®-A55
Microcontroller	1x Arm Cortex®-A55-M7 1x Arm Cortex®-M33	1x Arm Cortex®-A55-M7 1x Arm Cortex®-M33	1x Arm Cortex®-A55-M7 1x Arm Cortex®-M33	1x Arm Cortex®-A55-M7 1x Arm Cortex®-M33	1x Arm Cortex®-A55-M7 1x Arm Cortex®-M33
CPU Clock	1800 MHz (A55) 800 MHz (M7) 333 MHz (M33)	1800 MHz (A55) 800 MHz (M7) 333 MHz (M33)	1800 MHz (A55) 800 MHz (M7) 333 MHz (M33)	1800 MHz (A55) 800 MHz (M7) 333 MHz (M33)	1800 MHz (A55) 800 MHz (M7) 333 MHz (M33)
Memory					
RAM	8GB LPDDR5 (32 bits)	8GB LPDDR5 (32 bits)	4GB LPDDR5 (32 bits)	4GB LPDDR5 (32 bits)	2GB LPDDR5 (32 bits)
Flash	32GB eMMC	32GB eMMC	32GB eMMC	32GB eMMC	16GB eMMC
I²C EEPROM					
I ² C EEPROM Capacity	2 kbits 256 × 8 bits	2 kbits 256 × 8 bits	2 kbits 256 × 8 bits	2 kbits 256 × 8 bits	2 kbits 256 × 8 bits
Connectivity					
USB 3.2 Gen 1	1x OTG (Gen 1)	1x OTG (Gen 1)	1x OTG (Gen 1)	1x OTG (Gen 1)	1x OTG (Gen 1)
USB 2.0	1x Host	2x Host	1x Host	2x Host	2x Host
USX/S/GMII (for 2.5 and 10 Gb Ethernet)	1x	1x	1x	1x	1x
Gigabit Ethernet	1x	1x	1x	1x	1x
RGMII (for 2nd Gigabit Ethernet)	1x (alt)	1x (alt)	1x (alt)	1x (alt)	1x (alt)
Wi-Fi	2x2 Wi-Fi 7 (802.11be)	-	2x2 Wi-Fi 7 (802.11be)	-	-
Bluetooth	BT 5.3	-	BT 5.3	-	-
PCIe	1x (x1 Gen3)	2x (x1 Gen3)	1x (x1 Gen3)	2x (x1 Gen3)	2x (x1 Gen3)
I ² C	8x	8x	8x	8x	8x

Continued on next page

Table 11: Concept configurations (Continued)

Features	Aquila iMX95 Hexa 8GB WB IT AQIMX9596-8G-32G-DP-W7-N-IT	Aquila iMX95 Hexa 8GB IT AQIMX9596-8G-32G-DSI-W0-N-IT	Aquila iMX95 Hexa 4GB WB IT AQIMX9596-4G-32G-CSI-W7-N-IT	Aquila iMX95 Hexa 4GB IT AQIMX9596-4G-32G-CSI-W0-N-IT	Aquila iMX95 Hexa 2GB ET AQIMX9596-2G-16G-DSI-W0-N-ET
I ² C	1x	1x	1x	1x	1x
SPI	6x	6x	6x	6x	6x
QSPI	1x	1x	1x	1x	1x
OSPI	1x	1x	1x	1x	1x
UART	8x	8x	8x	8x	8x
PWM	22x	22x	22x	22x	22x
GPIO	14x + 92x	14x + 92x	14x + 92x	14x + 92x	14x + 92x
Analog Input	8x	8x	8x	8x	8x
SDIO/SD/MMC	2x	2x	2x	2x	2x
CAN FD	5x	5x	5x	5x	5x
JTAG	1x	1x	1x	1x	1x
Multimedia					
Display Controllers	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)
Video Decoder	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)
Video Encoder	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)	Yes (H.264/AVC and H.265/HEVC)
Neural Processing Unit (NPU)	Yes (2 TOPS)	Yes (2 TOPS)	Yes (2 TOPS)	Yes (2 TOPS)	Yes (2 TOPS)
DisplayPort	1x (up to 4k via DSI to eDP converter)	-	-	-	-
Display Serial Interface	-	1x Quad Lane MIPI DSI (up to 4k)	-	-	1x Quad Lane MIPI DSI (up to 4k)
LVDS	2x (up to 1920x1080)	2x (up to 1920x1080)	2x (up to 1920x1080)	2x (up to 1920x1080)	2x (up to 1920x1080)
Digital Audio	4x I ² S	4x I ² S	4x I ² S	4x I ² S	4x I ² S
S/PDIF (RX and TX)	1x	1x	1x	1x	1x
PDM Mic Input	4x	4x	4x	4x	4x

Continued on next page

Table 11: Concept configurations (Continued)

Features	Aquila iMX95 Hexa 8GB WB IT AQIMX9596-8G-32G-DP-W7-N-IT	Aquila iMX95 Hexa 8GB IT AQIMX9596-8G-32G-DSI-W0-N-IT	Aquila iMX95 Hexa 4GB WB IT AQIMX9596-4G-32G-CSI-W7-N-IT	Aquila iMX95 Hexa 4GB IT AQIMX9596-4G-32G-CSI-W0-N-IT	Aquila iMX95 Hexa 2GB ET AQIMX9596-2G-16G-DSI-W0-N-ET
2D Acceleration	Yes	Yes	Yes	Yes	Yes
3D Acceleration	Yes	Yes	Yes	Yes	Yes
Camera Serial Interface	1x Quad Lane MIPI CSI-2	1x Quad Lane MIPI CSI-2	2x Quad Lane MIPI CSI-2	2x Quad Lane MIPI CSI-2	1x Quad Lane MIPI CSI-2
Integrated ISP	Yes	Yes	Yes	Yes	Yes
Operating System					
Torizon	Q4 2025	Q4 2025	Q4 2025	Q4 2025	Q4 2025
Embedded Linux	Supported	Supported	Supported	Supported	Supported
Preinstalled OS	Toradex Easy Installer	Toradex Easy Installer	Toradex Easy Installer	Toradex Easy Installer	Toradex Easy Installer
Android	Contact Us	Contact Us	Contact Us	Contact Us	Contact Us
QNX	Coming Soon	Coming Soon	Coming Soon	Coming Soon	Coming Soon
FreeRTOS	Contact Us	Contact Us	Contact Us	Contact Us	Contact Us
Physical					
Size	85.0 x 55.0 mm	85.0 x 55.0 mm	85.0 x 55.0 mm	85.0 x 55.0 mm	85.0 x 55.0 mm
Temperature	-40 degC to 85 degC	-40 degC to 85 degC	-40 degC to 85 degC	-40 degC to 85 degC	-25 degC to 85 degC
Shock / Vibration	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms	EN 60068-2-6/50g 20ms
Power Dissipation	TBD ¹	TBD ¹	TBD ¹	TBD ¹	TBD ¹
Intended Use, Pricing, Availability	TBD ¹	TBD ¹	TBD ¹	TBD ¹	TBD ¹
Pricing	Contact Us	Contact Us	Contact Us	Contact Us	Contact Us
Minimum Product Commitment	2039	2039	2039	2039	2039

¹ Not available at the time of this document's publication.

1.10 Configure-To-Order (CTO) Options

In addition to the configurations above, customized versions of the module are available as Configure-To-Order (CTO) options. Refer to the [Section 1.8.1](#) for detailed guidance on specifying your desired module configuration.

2 Architecture Overview

The Aquila iMX95 System-on-Module integrates the NXP i.MX 95 SoC, high-speed memory, storage, connectivity subsystems, and supporting components on a compact PCB. This integration reduces design complexity for carrier boards while ensuring signal integrity, thermal stability, and compliance with industry standards.

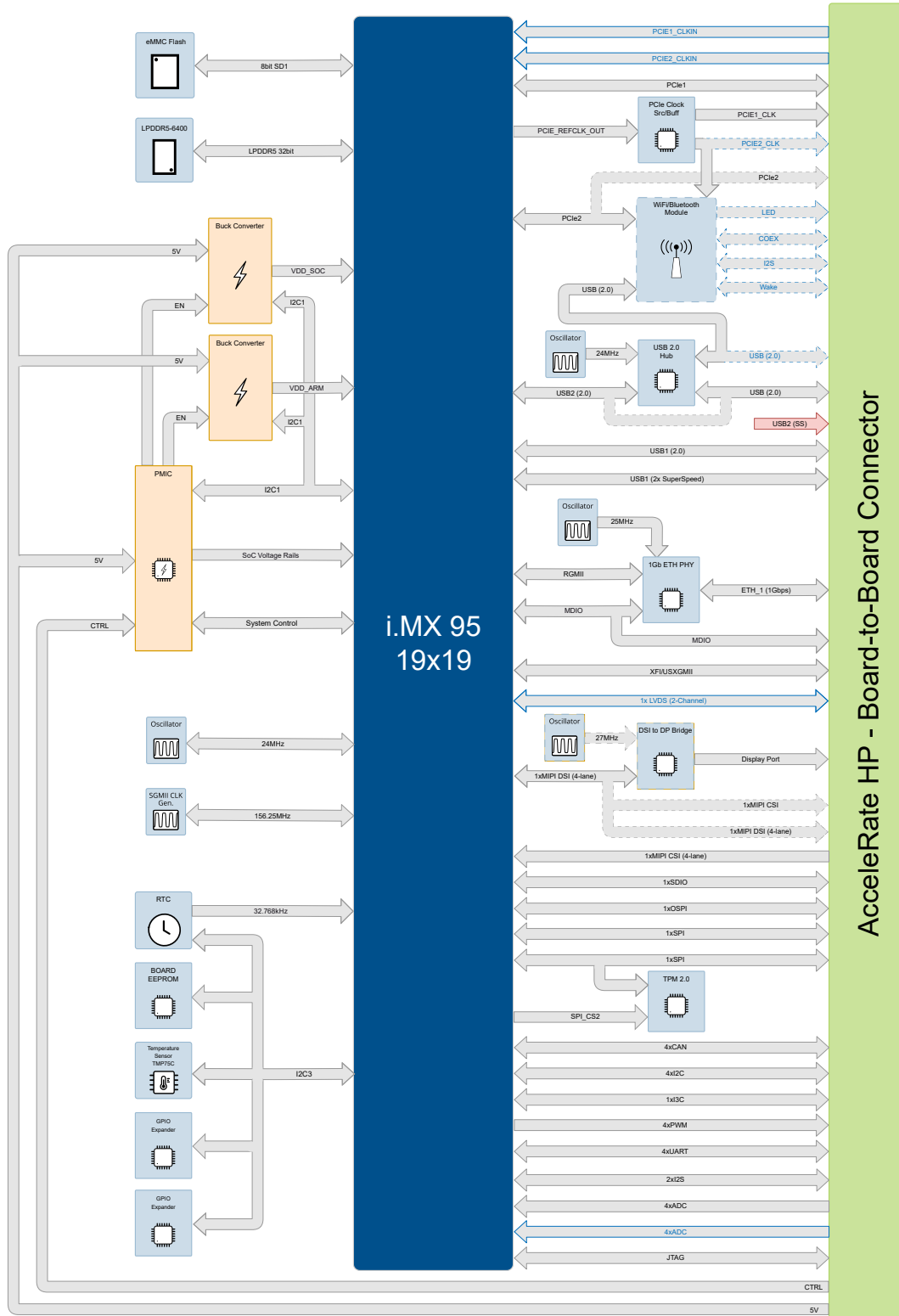
The overall architecture combines:

- **Application Processing:** Up to six Arm® Cortex®-A55 cores with shared L3 cache;
- **Real-Time Processing:** Arm® Cortex®-M7 and Cortex®-M33 cores for low-latency or safety-critical tasks;
- **Graphics & Multimedia:** Arm® Mali-G310 GPU, VPU, and ISP for display, video, and image processing;
- **AI Acceleration:** NPU delivering up to 2.0 TOPS for machine learning workloads;
- **Connectivity:** Integrated Gigabit Ethernet PHY, high-speed USB, PCIe Gen3, Wi-Fi 7, and Bluetooth 5.3;
- **Security:** EdgeLock® Secure Enclave and TPM 2.0 option;
- **System Infrastructure:** PMIC, I²C-based expanders, RTC, EEPROM, and thermal monitoring

The functional block diagram of the Aquila iMX95 SoM is shown in [Figure 1](#).

2.1 Block Diagram

Figure 1: Block diagram



Legend

- - - Dashed line. Assembly option.
- Blue line. Interface is available on the MSP pins.
- Red line. Interface is not available.

3 Aquila iMX95 Connector

3.1 Pin Numbering

The Aquila iMX95 uses a pin numbering scheme aligned with the mechanical layout of its board-to-board connector. This ensures straightforward mapping between SoM and carrier board designs.

- **Module Connector:** Samtec APF6-100-03.5-L-04-0-A-x
- **Recommended Carrier Board Mating Connector:** Samtec APM6-100-01.5-L-04-0-A-x

3.2 Pin Assignment

Tables 12 to 15 describe the main connector (X1) pinout and highlight the compatibility of each pin's function with the Aquila Family Specification. A detailed explanation of the compatibility groups defined in the specification is available in [Section 1.6](#).

Table 12: X1 pin assignment A

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
A01	SD_1_CD#	Yes	Always Compatible	SD2_CD_B (AD48)		Input with Pull-Down	
A02	SD_1_D1	Yes	Always Compatible	SD2_DATA1 (AC49)		Input with Pull-Down	
A03	SD_1_D0	Yes	Always Compatible	SD2_DATA0 (AC51)		Input with Pull-Down	
A04	GND	Yes	Always Compatible	GND			
A05	SD_1_CLK	Yes	Always Compatible	SD2_CLK (AB48)		Input with Pull-Down	
A06	SD_1_PWR_EN	Yes	Always Compatible	SD2_RESET_B (AD48)		Input with Pull-Down	
A07	SD_1_CMD	Yes	Always Compatible	SD2_CMD (AB52)		Input with Pull-Down	
A08	SD_1_D3	Yes	Always Compatible	SD2_DATA3 (AA49)		Input with Pull-Down	
A09	GND	Yes	Always Compatible	GND			
A10	SD_1_D2	Yes	Always Compatible	SD2_DATA2 (AA51)		Input with Pull-Down	
A11	GPIO_11_CSI_1	Yes	Always Compatible	SD2_VSELECT (AE51)		Input with Pull-Down	
A12	I2C_4_CSI1_SDA	Yes	Reserved	GPIO_IO30 (V46)		Input with Pull-Down	
A13	I2C_4_CSI1_SCL	Yes	Reserved	GPIO_IO31 (V48)		Input with Pull-Down	
A14	CTRL_MCLK_MOCI	Yes	Always Compatible	CCM_CLKO1 (AH20)		Output low	
A15	GND	Yes	Always Compatible	GND			
A16	CSI_1_D3_P	Yes	Reserved	MIPI_CSI1_D3_P (E11)			
A17	CSI_1_D3_N	Yes	Reserved	MIPI_CSI1_D3_N (E12)			
A18	GND	Yes	Always Compatible	GND			
A19	CSI_1_D2_P	Yes	Reserved	MIPI_CSI1_D2_P (E13)			
A20	CSI_1_D2_N	Yes	Reserved	MIPI_CSI1_D2_N (D14)			
A21	GND	Yes	Always Compatible	GND			
A22	CSI_1_CLK_P	Yes	Reserved	MIPI_CSI1_CLK_P (E15)			
A23	CSI_1_CLK_N	Yes	Reserved	MIPI_CSI1_CLK_N (F16)			

Continued on next page

Table 12: X1 pin assignment A (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
A24	GND	Yes	Always Compatible	GND			
A25	CSI_1_D1_P	Yes	Reserved	MIPI_CSI1_D1_P (E17)			
A26	CSI_1_D1_N	Yes	Reserved	MIPI_CSI1_D1_N (D18)			
A27	GND	Yes	Always Compatible	GND			
A28	CSI_1_D0_P	Yes	Reserved	MIPI_CSI1_D0_P (E19)			
A29	CSI_1_D0_N	Yes	Reserved	MIPI_CSI1_D0_N (F20)			
A30	GND	Yes	Always Compatible	GND			
A31	DSI_1_D3_N	Yes	Reserved	MIPI_DSICSI1_D3_N (C07)			Not connected for variants with DSI-to-DP bridge
A32	DSI_1_D3_P	Yes	Reserved	MIPI_DSICSI1_D3_P (B06)			Not connected for variants with DSI-to-DP bridge
A33	GND	Yes	Always Compatible	GND			
A34	DSI_1_D2_N	Yes	Reserved	MIPI_DSICSI1_D2_N (A09)			Not connected for variants with DSI-to-DP bridge
A35	DSI_1_D2_P	Yes	Reserved	MIPI_DSICSI1_D2_P (B08)			Not connected for variants with DSI-to-DP bridge
A36	GND	Yes	Always Compatible	GND			
A37	DSI_1_CLK_N	Yes	Reserved	MIPI_DSICSI1_CLK_N (C11)			Not connected for variants with DSI-to-DP bridge
A38	DSI_1_CLK_P	Yes	Reserved	MIPI_DSICSI1_CLK_P (B10)			Not connected for variants with DSI-to-DP bridge
A39	GND	Yes	Always Compatible	GND			
A40	DSI_1_D1_N	Yes	Reserved	MIPI_DSICSI1_D1_N (A13)			Not connected for variants with DSI-to-DP bridge
A41	DSI_1_D1_P	Yes	Reserved	MIPI_DSICSI1_D1_P (B12)			Not connected for variants with DSI-to-DP bridge
A42	GND	Yes	Always Compatible	GND			
A43	DSI_1_D0_N	Yes	Reserved	MIPI_DSICSI1_D0_N (C15)			Not connected for variants with DSI-to-DP bridge
A44	DSI_1_D0_P	Yes	Reserved	MIPI_DSICSI1_D0_P (B14)			Not connected for variants with DSI-to-DP bridge
A45	GND	Yes	Always Compatible	GND			
A46	DP_1_AUX-	Yes	Reserved		AUXN - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge

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Table 12: X1 pin assignment A (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
A47	DP_1_AUX+	Yes	Reserved		AUXP - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A48	GND	Yes	Always Compatible	GND			
A49	DP_1_LANE3-	Yes	Reserved		ML3N - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A50	DP_1_LANE3+	Yes	Reserved		ML3P - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A51	GND	Yes	Always Compatible	GND			
A52	DP_1_LANE2-	Yes	Reserved		ML2N - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A53	DP_1_LANE2+	Yes	Reserved		ML2P - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A54	GND	Yes	Always Compatible	GND			
A55	DP_1_LANE1-	Yes	Reserved		ML1N - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A56	DP_1_LANE1+	Yes	Reserved		ML1P - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A57	GND	Yes	Always Compatible	GND			
A58	DP_1_LANE0-	Yes	Reserved		ML0N - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A59	DP_1_LANE0+	Yes	Reserved		ML0P - DisplayPort Bridge		Not connected for variants without DSI-to-DP bridge
A60	GND	Yes	Always Compatible	GND			
A61	USB_1_SSRX1_N	Yes	Reserved	USB1_RX0_N (B20)			
A62	USB_1_SSRX1_P	Yes	Reserved	USB1_RX0_P (A21)			
A63	GND	Yes	Always Compatible	GND			
A64	USB_1_SSTX1_P	Yes	Reserved	USB1_TX0_N (E25)			
A65	USB_1_SSTX1_N	Yes	Reserved	USB1_TX0_P (D26)			
A66	GND	Yes	Always Compatible	GND			
A67	USB_1_SBU2	No	Reserved				Not connected
A68	USB_1_SBU1	No	Reserved				Not connected
A69	GND	Yes	Always Compatible	GND			

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Table 12: X1 pin assignment A (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
A70	USB_1_D_P	Yes	Reserved	USB1_D_P (C19)			
A71	USB_1_D_N	Yes	Reserved	USB1_D_N (B18)			
A72	GND	Yes	Always Compatible	GND			
A73	USB_1_SSRX2_N	Yes	Reserved	USB1_RX1_N (A17)			
A74	USB_1_SSRX2_P	Yes	Reserved	USB1_RX1_P (B16)			
A75	GND	Yes	Always Compatible	GND			
A76	USB_1_SSTX2_P	Yes	Reserved	USB1_TX1_P (E21)			
A77	USB_1_SSTX2_N	Yes	Reserved	USB1_TX1_N (D22)			
A78	GND	Yes	Always Compatible	GND			
A79	USB_2_SSTX1_N	No	Reserved				Not connected
A80	USB_2_SSTX1_P	No	Reserved				Not connected
A81	GND	Yes	Always Compatible	GND			
A82	USB_2_SSRX1_N	No	Reserved				Not connected
A83	USB_2_SSRX1_P	No	Reserved				Not connected
A84	GND	Yes	Always Compatible	GND			
A85	USB_2_D_N	Yes	Reserved	USB2_D_P (B24)	USB2_H_D_P		Connected to USB_2 interface or USB hub Assembly option
A86	USB_2_D_P	Yes	Reserved	USB2_D_N (A25)	USB2_H_D_N		Connected to USB_2 interface or USB hub Assembly option
A87	GND	Yes	Always Compatible	GND			
A88	ETH_1_MDI0_P	Yes	Always Compatible		TD_P_A - Ethernet RGMII		
A89	ETH_1_MDI0_N	Yes	Always Compatible		TD_M_A - Ethernet RGMII		
A90	GND	Yes	Always Compatible	GND			
A91	ETH_1_MDI1_P	Yes	Always Compatible		TD_P_B - Ethernet RGMII		

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Table 12: X1 pin assignment A (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
A92	ETH_1_MDI1_N	Yes	Always Compatible		TD_M_B - Ethernet RGMII		
A93	GND	Yes	Always Compatible	GND			
A94	ETH_1_MDI2_P	Yes	Always Compatible		TD_P_C - Ethernet RGMII		
A95	ETH_1_MDI2_N	Yes	Always Compatible		TD_M_C - Ethernet RGMII		
A96	GND	Yes	Always Compatible	GND			
A97	ETH_1_MDI3_P	Yes	Always Compatible		TD_P_D - Ethernet RGMII		
A98	ETH_1_MDI3_N	Yes	Always Compatible		TD_M_D - Ethernet RGMII		
A99	ETH_1_LED1	Yes	Always Compatible		LED0 - Ethernet RGMII		
A100	ETH_1_LED2	Yes	Always Compatible		LED2 - Ethernet RGMII		

Table 13: X1 pin assignment B

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
B01	GND	Yes	Always Compatible	GND			
B02	CSI_2_D3_P	Yes	Reserved	MIPI_DSICSI1_D3_P (B06)			Assembly option
B03	CSI_2_D3_N	Yes	Reserved	MIPI_DSICSI1_D3_N (C07)			Assembly option
B04	GND	Yes	Always Compatible	GND			
B05	CSI_2_D2_P	Yes	Reserved	MIPI_DSICSI1_D2_P (B08)			Assembly option
B06	CSI_2_D2_N	Yes	Reserved	MIPI_DSICSI1_D2_N (A09)			Assembly option
B07	GND	Yes	Always Compatible	GND			
B08	CSI_2_CLK_P	Yes	Reserved	MIPI_DSICSI1_CLK_P (B10)			Assembly option
B09	CSI_2_CLK_N	Yes	Reserved	MIPI_DSICSI1_CLK_N (C11)			Assembly option
B10	GND	Yes	Always Compatible	GND			
B11	CSI_2_D1_P	Yes	Reserved	MIPI_DSICSI1_D1_P (B12)			Assembly option
B12	CSI_2_D1_N	Yes	Reserved	MIPI_DSICSI1_D1_N (A13)			Assembly option
B13	GND	Yes	Always Compatible	GND			
B14	CSI_2_D0_P	Yes	Reserved	MIPI_DSICSI1_D0_P (B14)			Assembly option
B15	CSI_2_D0_N	Yes	Reserved	MIPI_DSICSI1_D0_N (C15)			Assembly option
B16	GND	Yes	Always Compatible	GND			
B17	GPIO_09_CSI_1	Yes	Reserved	SAI1_TXC (G51)		Input with Pull-Down	
B18	GPIO_10_CSI_1	Yes	Reserved	SAI1_RXD0 (H52)		Input with Pull-Down	
B19	GPIO_12_CSI_1	Yes	Reserved	SD3_DATA0 (AG49)		Input with Pull-Down	
B20	I2S_1_BCLK	Yes	Reserved	ENET2_TXC (AG23)		Input with Pull-Down	
B21	I2S_1_SYNC	Yes	Reserved	ENET2_TX_CTL (AF24)		Input with Pull-Down	
B22	I2S_1_D_OUT	Yes	Reserved	ENET2_RX_CTL (AH26)		Input with Pull-Down	
B23	I2S_1_D_IN	Yes	Reserved	ENET2_TD3 (AG29)		Input with Pull-Down	

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Table 13: X1 pin assignment B (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
B24	I2S_1_MCLK	Yes	Reserved	ENET2_RD2 (B24)		Input with Pull-Down	
B25	GND	Yes	Always Compatible	GND			
B26	I2S_2_BCLK	Yes	Reserved	SD3_DATA3 (AF52)		Input with Pull-Down	
B27	I2S_2_SYNC	Yes	Reserved	SD3_DATA2 (AE49)		Input with Pull-Down	
B28	I2S_2_D_OUT	Yes	Reserved	SD3_DATA1 (AH52)		Input with Pull-Down	
B29	I2S_2_D_IN	Yes	Reserved	SD3_CLK (AG51)		Input with Pull-Down	
B30	GND	Yes	Always Compatible	GND			
B31	UART_2_RXD	Yes	Always Compatible	GPIO_IO37 (Y52)		Input with Pull-Down	
B32	UART_2_CTS	Yes	Always Compatible	GPIO_IO10 (M48)		Input with Pull-Down	
B33	UART_2_TXD	Yes	Always Compatible	GPIO_IO36 (Y48)		Input with Pull-Down	
B34	UART_2_RTS	Yes	Always Compatible	GPIO_IO11 (M52)		Input with Pull-Down	
B35	UART_1_RXD	Yes	Always Compatible	GPIO_IO15 (P44)		Input with Pull-Down	
B36	UART_1_CTS	Yes	Always Compatible	GPIO_IO16 (P46)		Input with Pull-Down	
B37	UART_1_TXD	Yes	Always Compatible	GPIO_IO14 (N51)		Input with Pull-Down	
B38	UART_1_RTS	Yes	Always Compatible	GPIO_IO17 (P48)		Input with Pull-Down	
B39	GND	Yes	Always Compatible	GND			
B40	I2C_3_DSI1_SDA	Yes	Reserved	GPIO_IO12 (B40/C05)		Input with Pull-Down	Assembly option
B41	I2C_3_DSI1_SCL	Yes	Reserved	GPIO_IO13 (B41/C06)		Input with Pull-Down	Assembly option
B42	GPIO_17_DSI_1	Yes	Reserved	GPIO_IO07 (L51)		Input with Pull-Down	
B43	GPIO_18_DSI_1	Yes	Reserved	GPIO_IO09 (M46)		Input with Pull-Down	
B44	GPIO_19_DSI_1	Yes	Reserved	GPIO_IO33 (W45)		Input with Pull-Down	
B45	GPIO_20_DSI_1	Yes	Reserved	GPIO_IO34 (W49)		Input with Pull-Down	
B46	PWM_3_DSI	Yes	Reserved	GPIO_IO06 (L49)		Input with Pull-Down	

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Table 13: X1 pin assignment B (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
B47	GND	Yes	Always Compatible	GND			
B48	CAN_1_TX	Yes	Reserved	PDM_CLK (F46)		Input with Pull-Down	
B49	CAN_1_RX	Yes	Reserved	PDM_BIT_STREAM0 (B49)		Input with Pull-Down	
B50	CAN_2_TX	Yes	Reserved	GPIO_IO25 (T52)		Input with Pull-Down	
B51	CAN_2_RX	Yes	Reserved	GPIO_IO27 (U49)		Input with Pull-Down	
B52	GND	Yes	Always Compatible	GND			
B53	CAN_3_TX	Yes	Reserved	CCM_CLKO3 (AK20)		Input with Pull-Down	
B54	CAN_3_RX	Yes	Reserved	CCM_CLKO4 (AJ21)		Input with Pull-Down	
B55	CAN_4_TX	Yes	Reserved	GPIO_IO04 (K46)		Input with Pull-Down	
B56	CAN_4_RX	Yes	Reserved	GPIO_IO05 (L45)		Input with Pull-Down	
B57	GPIO_21_DP	Yes	Reserved	SD3_CMD (AF48)			
B58	PWM_4_DP	Yes	Reserved	GPIO_IO26 (U45)			
B59	DP0_HPD_R	Yes	Reserved		HPD - GPIO Expander A ¹		Assembly option
B60	QSPI_1_IO3	Yes	Reserved	XSPI1_DATA3 (AK48)		Input with Pull-Down	
B61	QSPI_1_IO2	Yes	Reserved	XSPI1_DATA2 (AJ47)		Input with Pull-Down	
B62	QSPI_1_CS2#	Yes	Reserved	CCM_CLKO2 (AF20)		Input with Pull-Down	
B63	QSPI_1_DQS	Yes	Reserved	XSPI1_DQS (AK44)		Input with Pull-Down	
B64	GND	Yes	Always Compatible	GND			
B65	QSPI_1_SCK	Yes	Reserved	XSPI1_SCLK (AJ43)		Input with Pull-Down	
B66	QSPI_1_CS1#	Yes	Reserved	XSPI1_SS0_B (AJ41)		Input with Pull-Down	
B67	QSPI_1_IO1	Yes	Reserved	XSPI1_DATA1 (AH46)		Input with Pull-Down	
B68	QSPI_1_IO0	Yes	Reserved	XSPI1_DATA0 (AJ45)		Input with Pull-Down	
B69	GND	Yes	Always Compatible	GND			

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Table 13: X1 pin assignment B (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
B70	OSPI_1_IO4	Yes	Reserved	XSPI1_DATA4 (AJ49)		Input with Pull-Down	
B71	OSPI_1_IO5	Yes	Reserved	XSPI1_DATA5 (AK50)		Input with Pull-Down	
B72	OSPI_1_IO6	Yes	Reserved	XSPI1_DATA6 (AJ51)		Input with Pull-Down	
B73	OSPI_1_IO7	Yes	Reserved	XSPI1_DATA7 (AH50)		Input with Pull-Down	
B74	USB_1_INT#	Yes	Always Compatible		P0_5 - GPIO Expander A ¹		
B75	USB_1_OC#	Yes	Always Compatible		P0_6 - GPIO Expander A ¹		
B76	USB_1_VBUS	Yes	Always Compatible	USB1_VBUS (E23)			
B77	USB_1_EN	Yes	Always Compatible		P2 - GPIO Expander B ²		
B78	USB_2_H_OC#	Yes	Always Compatible		P0_7 - GPIO Expander A ¹		
B79	USB_2_VBUS	Yes	Always Compatible	USB_2_VBUS (E27)			
B80	USB_2_H_EN	Yes	Always Compatible		P3 - GPIO Expander B ²		
B81	ETH_2_XGMII_INT#	Yes	Reserved		P1_0 - GPIO Expander A ¹		
B82	GND	Yes	Always Compatible	GND			
B83	ETH_2_XGMII_RX_N	Yes	Reserved	ETH_RX0_N (AK12)			
B84	ETH_2_XGMII_RX_P	Yes	Reserved	ETH_RX0_P (AJ13)			
B85	GND	Yes	Always Compatible	GND			
B86	ETH_2_XGMII_TX_N	Yes	Reserved	ETH_TX0_N (AK16)			
B87	ETH_2_XGMII_TX_P	Yes	Reserved	ETH_TX0_P (AJ17)			
B88	GND	Yes	Always Compatible	GND			
B89	ETH_2_XGMII_MDIO	Yes	Reserved	ENET2_MDIO		Input with Pull-Down	
B90	ETH_2_XGMII_MDC	Yes	Reserved	ENET2_MDC			
B91	CTRL_RECOVERY_MICO#	Yes	Always Compatible		PMIC		Connected to Recovery circuit
B92	CTRL_RESET_MICO#	Yes	Always Compatible		PMIC		Connected to Reset circuit

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Table 13: X1 pin assignment B (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
B93	CTRL_PWR_BTN_MICO#	Yes	Always Compatible		PMIC		Connected to PMIC circuit
B94	CTRL_FORCE_OFF_MOCI#	Yes	Always Compatible		PMIC		Connected to PMIC circuit
B95	CTRL_PWR_EN_MOCI	Yes	Always Compatible		PMIC		Connected to PMIC circuit
B96	PWR_1V8_MOCI	Yes	Always Compatible	+V1.8			
B97	VCC	Yes	Always Compatible	3.135 to 5.5 V			
B98	VCC	Yes	Always Compatible	3.135 to 5.5 V			
B99	VCC	Yes	Always Compatible	3.135 to 5.5 V			
B100	VCC_BACKUP	Yes	Always Compatible	VBAT			

¹ Available through the on-module GPIO Expander A (PCAL6416AHF).

² Available through the on-module GPIO Expander B (PCAL6408AHKX).

Table 14: X1 pin assignment C

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
C01	GPIO_13_CSI_2	Yes	Reserved		P0_0 - GPIO Expander A ¹	Pull-Down	
C02	GPIO_14_CSI_2	Yes	Reserved		P0_1 - GPIO Expander A ¹	Pull-Down	
C03	GPIO_15_CSI_2	Yes	Reserved		P0_2 - GPIO Expander A ¹	Pull-Down	
C04	GPIO_16_CSI_2	Yes	Reserved		P0_3 - GPIO Expander A ¹	Pull-Down	
C05	I2C_5_CSI2_SDA	Yes	Reserved	GPIO_IO12 (C05)		Input with Pull-Down	Assembly option
C06	I2C_5_CSI2_SCL	Yes	Reserved	GPIO_IO13 (C06)		Input with Pull-Down	Assembly option
C07	JTAG_1_TRST#	No	Reserved				Not connected
C08	JTAG_1_TDI	Yes	Always Compatible	DAP_TDI (AK24)		Input with Pull-Up	
C09	GND	Yes	Always Compatible	GND			
C10	JTAG_1_TDO	Yes	Always Compatible	DAP_TDO_TRACESWO (AJ23)		Input without Pull-Up/Down	
C11	JTAG_1_TCK	Yes	Always Compatible	DAP_TCLK_SWCLK (AG21)		Input with Pull-Down	
C12	JTAG_1_VREF	Yes	Always Compatible	+V1.8			
C13	JTAG_1_TMS	Yes	Always Compatible	DAP_TMS_SWDIO (AH22)		Input with Pull-Up	
C14	CTRL_TAMPER0	Yes	Always Compatible	TAMPER0 (F36)			
C15	CTRL_TAMPER1	Yes	Always Compatible	TAMPER1 (D38)			
C16	I2C_2_SDA	Yes	Always Compatible	ENET1_MDIO (AJ39)		Input with Pull-Down	
C17	I2C_2_SCL	Yes	Always Compatible	ENET1_MDC (AK40)		Input with Pull-Down	
C18	I2C_6_SDA	Yes	Reserved	GPIO_IO22 (T44)		Input with Pull-Down	
C19	I2C_6_SCL	Yes	Reserved	GPIO_IO23 (T46)		Input with Pull-Down	
C20	GPIO_04	Yes	Always Compatible	ENET2_TD0 (AG15)		Input with Pull-Down	
C21	GPIO_05	Yes	Always Compatible	ENET2_TD1 (AG27)		Input with Pull-Down	
C22	GPIO_06	Yes	Always Compatible	ENET2_TD2 (AF28)		Input with Pull-Down	
C23	GPIO_07	Yes	Always Compatible	ENET2_RXC (AJ25)		Input with Pull-Down	

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Table 14: X1 pin assignment C (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
C24	GPIO_08	Yes	Always Compatible	PDM_BIT_STREAM1 (H46)		Input with Pull-Down	
C25	PWM_1	Yes	Always Compatible	GPIO_IO24 (T48)		Input with Pull-Down	
C26	PWM_2	Yes	Always Compatible	GPIO_IO08 (M44)		Input with Pull-Down	
C27	GND	Yes	Always Compatible	GND			
C28	PCIE_2_L0_RX_P	Yes	Reserved	PCIE2_RX0_P (B34)			Not connected for variants with Wi-Fi+Bluetooth module
C29	PCIE_2_L0_RX_N	Yes	Reserved	PCIE2_RX0_N (C35)			Not connected for variants with Wi-Fi+Bluetooth module
C30	GND	Yes	Always Compatible	GND			
C31	PCIE_2_L1_RX_P	No	Reserved				Not connected
C32	PCIE_2_L1_RX_N	No	Reserved				Not connected
C33	GND	Yes	Always Compatible	GND			
C34	PCIE_2_CLKREQ#	Yes	Reserved	GPIO_IO35 (W51)			Not connected for variants with Wi-Fi+Bluetooth module
C35	PCIE_2_RESET#	Yes	Reserved		P1 - GPIO Expander B ²		Not connected for variants with Wi-Fi+Bluetooth module
C36	PCIE_WAKE#	Yes	Always Compatible		P0_4 - GPIO Expander A ¹	Input with Pull-Up	
C37	PCIE_1_CLKREQ	Yes	Always Compatible	GPIO_IO32 (V52)			
C38	PCIE_1_RESET#	Yes	Always Compatible		P0 - GPIO Expander B ²	Input with Pull-Down	
C39	GND	Yes	Always Compatible	GND			
C40	PCIE_1_L0_RX_P	Yes	Always Compatible	PCIE1_RX0_P (B28)			
C41	PCIE_1_L0_RX_N	Yes	Always Compatible	PCIE1_RX0_N (A29)			
C42	GND	Yes	Always Compatible	GND			
C43	PCIE_1_L1_RX_P	No	Reserved				Not connected
C44	PCIE_1_L1_RX_N	No	Reserved				Not connected
C45	GND	Yes	Always Compatible	GND			
C46	MSP_1_RX_P	-	Module-Specific	PCIE1_REF_PAD_CLK_P (B30)		Pull-Down	

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Table 14: X1 pin assignment C (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
C47	MSP_1_RX_N	–	Module-Specific	PCIE1_REF_PAD_CLK_N (C31)		Pull-Down	
C48	GND	Yes	Always Compatible	GND			
C49	MSP_2_RX_P	–	Module-Specific	PCIE2_REF_PAD_CLK_P		Pull-Down	
C50	MSP_2_RX_N	–	Module-Specific	PCIE2_REF_PAD_CLK_N		Pull-Down	
C51	GND	Yes	Always Compatible	GND			
C52	MSP_3_RX_P	–	Module-Specific		LAA_TX_EN - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C53	MSP_3_RX_N	–	Module-Specific		WL_TX_EN - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C54	GND	Yes	Always Compatible	GND			
C55	MSP_4_RX_P	–	Module-Specific	ADC_IN6 (B44)			
C56	MSP_4_RX_N	–	Module-Specific	ADC_IN7 (A45)			
C57	GND	Yes	Always Compatible	GND			
C58	MSP_5_RX_P	–	Module-Specific		LED1 - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C59	MSP_5_RX_N	–	Module-Specific		LED2 - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C60	GND	Yes	Always Compatible	GND			
C61	MSP_6_RX_P	–	Module-Specific		BT_I2S_0_SDI_GPIO - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C62	MSP_6_RX_N	–	Module-Specific		BT_I2S_0_SDO_GPIO - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C63	GND	Yes	Always Compatible	GND			
C64	MSP_7_RX_P	–	Module-Specific		BT_I2S_0_SCK_GPIO - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C65	MSP_7_RX_N	–	Module-Specific		BT_I2S_0_WS_GPIO - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C66	GND	Yes	Always Compatible	GND			
C67	MSP_8_RX_P	–	Module-Specific				Not connected
C68	MSP_8_RX_N	–	Module-Specific				Not connected
C69	GND	Yes	Always Compatible	GND			

Continued on next page

Table 14: X1 pin assignment C (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
C70	MSP_9_RX_P	–	Module-Specific				Not connected
C71	MSP_9_RX_N	–	Module-Specific				Not connected
C72	GND	Yes	Always Compatible	GND			
C73	MSP_10_RX_P	–	Module-Specific		LTE_COEX_TXD - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C74	MSP_10_RX_N	–	Module-Specific		LTE_COEX_RXD - Wi-Fi		Not connected for variants without Wi-Fi+Bluetooth module
C75	GND	Yes	Always Compatible	GND			
C76	MSP_11_RX_P	–	Module-Specific	EARC_P_UTIL (Y44)			
C77	MSP_11_RX_N	–	Module-Specific	EARC_N_HPDP (Y46)			
C78	GND	Yes	Always Compatible	GND			
C79	MSP_12_RX_P	–	Module-Specific	EARC_AUX (AA45)			
C80	MSP_12_RX_N	–	Module-Specific				Not connected
C81	GND	Yes	Always Compatible	GND			
C82	MSP_13_RX_P	–	Module-Specific				Not connected
C83	MSP_13_RX_N	–	Module-Specific				Not connected
C84	GND	Yes	Always Compatible	GND			
C85	MSP_14_RX_P	–	Module-Specific				Not connected
C86	MSP_14_RX_N	–	Module-Specific				Not connected
C87	GND	Yes	Always Compatible	GND			
C88	MSP_15_RX_P	–	Module-Specific				Not connected
C89	MSP_15_RX_N	–	Module-Specific				Not connected
C90	GND	Yes	Always Compatible	GND			
C91	MSP_16_RX_P	–	Module-Specific				Not connected
C92	MSP_16_RX_N	–	Module-Specific				Not connected

Continued on next page

Table 14: X1 pin assignment C (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
C93	GND	Yes	Always Compatible	GND			
C94	MSP_17_RX_P	–	Module-Specific				Not connected
C95	MSP_17_RX_N	–	Module-Specific				Not connected
C96	VCC	Yes	Always Compatible	3.135 to 5.5 V			
C97	VCC	Yes	Always Compatible	3.135 to 5.5 V			
C98	VCC	Yes	Always Compatible	3.135 to 5.5 V			
C99	VCC	Yes	Always Compatible	3.135 to 5.5 V			
C100	VCC	Yes	Always Compatible	3.135 to 5.5 V			

¹ Available through the on-module GPIO Expander A (PCAL6416AHF).

² Available through the on-module GPIO Expander B (PCAL6408AHKX).

Table 15: X1 pin assignment D

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
D01	ADC_1	Yes	Reserved	ADC_IN0 (A37)			
D02	ADC_2	Yes	Reserved	ADC_IN1 (B38)			
D03	ADC_3	Yes	Reserved	ADC_IN2 (C39)			
D04	ADC_4	Yes	Reserved	ADC_IN3 (A41)			
D05	CTRL_RESET_MOCI#	Yes	Always Compatible				Connected to Reset circuit
D06	CTRL_WAKE1_MICO#	Yes	Always Compatible	XSPI1_SS1_B (AH42)		Input with Pull-Down	
D07	I2C_1_SDA	Yes	Always Compatible	I2C2_SDA (E45)		Input with Pull-Down	
D08	I2C_1_SCL	Yes	Always Compatible	I2C2_SCL (E43)		Input with Pull-Down	
D09	SPI_1_CS	Yes	Always Compatible	GPIO_IO00 (J49)		Input with Pull-Down	
D10	SPI_1_MISO	Yes	Always Compatible	GPIO_IO01 (J51)		Input with Pull-Down	
D11	SPI_1_MOSI	Yes	Always Compatible	GPIO_IO02 (K48)		Input with Pull-Down	
D12	SPI_1_CLK	Yes	Always Compatible	GPIO_IO03 (K52)		Input with Pull-Down	
D13	GND	Yes	Always Compatible	GND			
D14	SPI_2_CLK	Yes	Reserved	GPIO_IO21 (R51)		Input with Pull-Down	
D15	SPI_2_MISO	Yes	Reserved	GPIO_IO19 (R45)		Input with Pull-Down	
D16	SPI_2_CS	Yes	Reserved	GPIO_IO18 (P52)		Input with Pull-Down	
D17	SPI_2_MOSI	Yes	Reserved	GPIO_IO20 (R49)		Input with Pull-Down	
D18	GND	Yes	Always Compatible	GND			
D19	UART_3_RXD	Yes	Always Compatible	UART1_RXD (E49)		Input with Pull-Down	
D20	UART_3_TXD	Yes	Always Compatible	UART1_TXD (F52)		Input with Pull-Down	
D21	UART_4_RXD	Yes	Always Compatible	UART2_RXD (E51)		Input with Pull-Down	
D22	UART_4_TXD	Yes	Always Compatible	UART2_TXD (F48)		Input with Pull-Down	
D23	GPIO_01	Yes	Always Compatible	ENET2_RD0 (AJ27)		Input with Pull-Down	

Continued on next page

Table 15: X1 pin assignment D (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
D24	GPIO_02	Yes	Always Compatible	ENET2_RD1 (AK28)		Input with Pull-Down	
D25	GPIO_03	Yes	Always Compatible	ENET2_RD3 (AH30)		Input with Pull-Down	
D26	GND	Yes	Always Compatible	GND			
D27	PCIE_2_CLK_P	Yes	Reserved		PCIe clock generator		Not connected for variants with Wi-Fi+Bluetooth module
D28	PCIE_2_CLK_N	Yes	Reserved		PCIe clock generator		Not connected for variants with Wi-Fi+Bluetooth module
D29	GND	Yes	Always Compatible	GND			
D30	PCIE_2_L0_TX_P	Yes	Reserved	PCIE2_TX0_P (E31)			Not connected for variants with Wi-Fi+Bluetooth module
D31	PCIE_2_L0_TX_N	Yes	Reserved	PCIE2_TX0_N (F32)			Not connected for variants with Wi-Fi+Bluetooth module
D32	GND	Yes	Always Compatible	GND			
D33	PCIE_2_L1_TX_P	No	-				Not connected
D34	PCIE_2_L1_TX_N	No	-				Not connected
D35	GND	Yes	Always Compatible	GND			
D36	PCIE_1_CLK_P	Yes	Reserved		CLK1_P		Connected to PCIe clock generator
D37	PCIE_1_CLK_N	Yes	Reserved		CLK1_N	Wi-Fi/Bluetooth	Connected to PCIe clock generator
D38	GND	Yes	Always Compatible	GND		Wi-Fi/Bluetooth	
D39	PCIE_1_L0_TX_P	Yes	Reserved	PCIE1_TX0_P (E29)			
D40	PCIE_1_L0_TX_N	Yes	Reserved	PCIE1_TX0_N (D30)			
D41	GND	Yes	Always Compatible	GND			
D42	PCIE_1_L1_TX_P	No	-				Not connected
D43	PCIE_1_L1_TX_N	No	-				Not connected
D44	GND	Yes	Always Compatible	GND			
D45	MSP_1_TX_P	No	-				Not connected
D46	MSP_1_TX_N	No	-				Not connected

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Table 15: X1 pin assignment D (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
D47	GND	Yes	Always Compatible	GND			
D48	MSP_2_TX_P	No	-				Not connected
D49	MSP_2_TX_N	No	-				Not connected
D50	GND	Yes	Always Compatible	GND			
D51	MSP_3_TX_P	-	-				Not connected
D52	MSP_3_TX_N	-	-				Not connected
D53	GND	Yes	Always Compatible	GND			
D54	MSP_4_TX_P	-	Module-Specific	ADC_IN4 (A41)			
D55	MSP_4_TX_N	-	Module-Specific	ADC_IN5 (B42)			
D56	GND	Yes	Always Compatible	GND			
D57	MSP_5_TX_P	-	Module-Specific				USB_3_OC# - Connected to USB circuit
D58	MSP_5_TX_N	-	Module-Specific				USB_3_EN - Connected to USB circuit
D59	GND	Yes	Always Compatible	GND			
D60	MSP_6_TX_P	-	Module-Specific		USB DP DN2 - USB Hub		Not connected for variants with Wi-Fi+Bluetooth module
D61	MSP_6_TX_N	-	Module-Specific		USB DM DN2 - USB Hub		Not connected for variants with Wi-Fi+Bluetooth module
D62	GND	Yes	Always Compatible	GND			
D63	MSP_7_TX_P	-	-				Not connected
D64	MSP_7_TX_N	-	-				Not connected
D65	GND	Yes	Always Compatible	GND			
D66	MSP_8_TX_P	-	Module-Specific	LVDS1_D0_P (B02)			
D67	MSP_8_TX_N	-	Module-Specific	LVDS1_D0_N (A03)			
D68	GND	Yes	Always Compatible	GND			
D69	MSP_9_TX_P	-	Module-Specific	LVDS1_D1_P (C01)			

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Table 15: X1 pin assignment D (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
D70	MSP_9_TX_N	–	Module-Specific	LVDS1_D1_N (C03)			
D71	GND	Yes	Always Compatible	GND			
D72	MSP_10_TX_P	–	Module-Specific	LVDS1_CLK_P (D02)			
D73	MSP_10_TX_N	–	Module-Specific	LVDS1_CLK_N (D04)			
D74	GND	Yes	Always Compatible	GND			
D75	MSP_11_TX_P	–	Module-Specific	LVDS1_D2_P (E01)			
D76	MSP_11_TX_N	–	Module-Specific	LVDS1_D2_N (E03)			
D77	GND	Yes	Always Compatible	GND			
D78	MSP_12_TX_P	–	Module-Specific	LVDS1_D3_P (F02)			
D79	MSP_12_TX_N	–	Module-Specific	LVDS1_D3_N (F04)			
D80	GND	Yes	Always Compatible	GND			
D81	MSP_13_TX_P	–	Module-Specific	LVDS0_D0_P (G07)			
D82	MSP_13_TX_N	–	Module-Specific	LVDS0_D0_N (G09)			
D83	GND	Yes	Always Compatible	GND			
D84	MSP_14_TX_P	–	Module-Specific	LVDS0_D1_P (F06)			
D85	MSP_14_TX_N	–	Module-Specific	LVDS0_D1_N (F08)			
D86	GND	Yes	Always Compatible	GND			
D87	MSP_15_TX_P	–	Module-Specific	LVDS0_CLK_P (B04)			
D88	MSP_15_TX_N	–	Module-Specific	LVDS0_CLK_N (A05)			
D89	GND	Yes	Always Compatible	GND			
D90	MSP_16_TX_P	–	Module-Specific	LVDS0_D2_P (D06)			
D91	MSP_16_TX_N	–	Module-Specific	LVDS0_D2_N (E07)			
D92	GND	Yes	Always Compatible	GND			

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Table 15: X1 pin assignment D (Continued)

X1 Pin	Aquila Specification Signal Name	Family Compatible Function	Aquila Specification Compatibility Group	SoC Function (Ball Name)	Non-SoC Ball Name	Reset State	Remarks
D93	MSP_17_TX_P	–	Module-Specific	LVDS0_D3_P (D08)			
D94	MSP_17_TX_N	–	Module-Specific	LVDS0_D3_N (E09)			
D95	VCC	Yes	Always Compatible	3.135 to 5.5 V			
D96	VCC	Yes	Always Compatible	3.135 to 5.5 V			
D97	VCC	Yes	Always Compatible	3.135 to 5.5 V			
D98	VCC	Yes	Always Compatible	3.135 to 5.5 V			
D99	VCC	Yes	Always Compatible	3.135 to 5.5 V			
D100	VCC	Yes	Always Compatible	3.135 to 5.5 V			

4 I/O Pins

4.1 Function Multiplexing

Low-speed I/O pins on the NXP i.MX 95 SoC support up to seven alternate functions. Most of these pins can also be used as GPIOs (general-purpose I/O, sometimes referred to as digital I/O).

For example, the i.MX 95 signal connected to X1 connector pin **D21** exposes the SoC alternate function **UART2_RXD**, which corresponds to the Aquila standard function **UART_4_RXD**. In addition to this UART function, the pin can also be configured as:

- UART1_CTS_B (Clear To Send, active low control input)
- SPI2_SOUT (Serial Data Out)
- TPM1_CH2 (TPM channel 2)
- SAI1_MCLK (SAI master clock)
- GPIO1_IO06 (GPIO)

Whenever possible, **it is strongly recommended to use functions that are compatible across all Aquila modules**. This ensures maximum compatibility with standard software and other modules in the Aquila Family.

Some alternate functions are available on more than one pin. **Care must be taken to avoid assigning the same function to multiple pins simultaneously**, as this can result in system instability or undefined behavior.

[Table 16](#) lists all pins that support alternate functions, along with the alternate functions available for each pin. Alternate functions highlighted in bold indicate the primary interfaces selected for optimal Aquila compatibility.

Table 16: Alternate functions

X1 pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
A01	SD2_CD_B	AD48	usdhc2.CD_B	netc.TMR_1588_TRIG1	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]		
A02	SD2_DATA1	AC49	usdhc2.DATA1	netc.TMR_1588_CLK	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]		
A03	SD2_DATA0	AC51	usdhc2.DATA0	netc.TMR_1588_PP2	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]		
A05	SD2_CLK	AB48	usdhc2.CLK	netc.TMR_1588_PP1	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]		
A06	SD2_RESET_B	AD52	usdhc2.RESET_B	lptmr2.ALT2		netc.TMR_1588_GCLK	flexio1.FLEXIO[7]	gpio3.IO[7]		
A07	SD2_CMD	AB52	usdhc2.CMD	netc.TMR_1588_TRIG2	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]		
A08	SD2_DATA3	AA49	usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT	netc.TMR_1588_ALARM1	flexio1.FLEXIO[6]	gpio3.IO[6]		
A10	SD2_DATA2	AA51	usdhc2.DATA2	netc.TMR_1588_PP3	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]		
A11	SD2_VSELECT	AE51	usdhc2.VSELECT	usdhc2.WP	lptmr2.ALT3		flexio1.FLEXIO[19]	gpio3.IO[19]		
A12	GPIO_IO30	V46	gpio2.IO[30]	i2c4.SDA	can5.TX					flexio1.FLEXIO[30]
A13	GPIO_IO31	V48	gpio2.IO[31]	i2c4.SCL	can5.RX					flexio1.FLEXIO[31]
A14	CCM_CLKO1	AH20	ccmsrcgpcmix.CLKO1	netc.TMR_1588_TRIG1			flexio1.FLEXIO[26]	gpio3.IO[26]		
B17	SAI1_TXC	G51	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]		
B18	SAI1_RXD0	H52	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]		
B19	SD3_DATA0	AG49	usdhc3.DATA0	flexspi.A_DATA[0]	sai5.TX_DATA[3]	sai5.RX_BCLK	flexio1.FLEXIO[22]	gpio3.IO[22]	xspi_slv.DATA[0]	
B20	ENET2_TXC	AG23	netc.ETH1_RGMII_TX_CLK	ccmsrcgpcmix.ENET_CLK_ROOT	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]		
B21	ENET2_TX_CTL	AF24	netc.ETH1_RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC	netc.ETH1_RMII_TX_EN	flexio2.FLEXIO[20]	gpio4.IO[20]		
B22	ENET2_RX_CTL	AH26	netc.ETH1_RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]	netc.ETH1_RMII_CRSDV	
B23	ENET2_TD3	AG29	netc.ETH1_RGMII_TXD[3]		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]		
B24	ENET2_RD2	AJ29	netc.ETH1_RGMII_RXD[2]	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]	netc.ETH1_RMII_RX_ER	
B26	SD3_DATA3	AF52	usdhc3.DATA3	flexspi.A_DATA[3]	sai5.RX_DATA[3]	sai5.TX_BCLK	flexio1.FLEXIO[25]	gpio3.IO[25]	xspi_slv.DATA[3]	
B27	SD3_DATA2	AE49	usdhc3.DATA2	flexspi.A_DATA[2]	sai5.RX_DATA[2]	sai5.TX_SYNC	flexio1.FLEXIO[24]	gpio3.IO[24]	xspi_slv.DATA[2]	
B28	SD3_DATA1	AH52	usdhc3.DATA1	flexspi.A_DATA[1]	sai5.RX_DATA[1]	sai5.TX_DATA[0]	flexio1.FLEXIO[23]	gpio3.IO[23]	xspi_slv.DATA[1]	

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Table 16: Alternate functions (Continued)

X1 pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
B29	SD3_CLK	AG51	usdhc3.CLK	flexspi_A_SCLK	sai5.TX_DATA[1]	sai5.RX_DATA[0]	flexio1.FLEXIO[20]	gpio3.IO[20]		xspi_slv.CLK
B31	GPIO_IO37	Y52	gpio5.IO[17]		uart7.RX		spi4.SCK			
B32	GPIO_IO10	M48	gpio2.IO[10]	spi3.SOUT			tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]
B33	GPIO_IO36	Y48	gpio5.IO[16]		uart7.TX		spi4.SOUT			
B34	GPIO_IO11	M52	gpio2.IO[11]	spi3.SCK			tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]
B35	GPIO_IO15	P44	gpio2.IO[15]	uart3.RX			spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]
B36	GPIO_IO16	P46	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]		uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]
B37	GPIO_IO14	N51	gpio2.IO[14]	uart3.TX			spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]
B38	GPIO_IO17	P48	gpio2.IO[17]	sai3.MCLK			uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]
B40/C05	GPIO_IO12	N45	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	flexio1.FLEXIO[12]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
B41/C06	GPIO_IO13	N49	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]		spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]
B42	GPIO_IO07	L51	gpio2.IO[7]	spi3.PCS1			spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]
B43	GPIO_IO09	M46	gpio2.IO[9]	spi3.SIN			tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]
B44	GPIO_IO33	W45	gpio5.IO[13]		uart6.RX		spi4.PCS1			
B45	GPIO_IO34	W49	gpio5.IO[14]		uart6.CTS_B		spi4.PCS0			
B46	GPIO_IO06	L49	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]		spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]
B48	PDM_CLK	F46	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]		can1.TX
B49	PDM_BIT_STREAM0	G45	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]		can1.RX
B50	GPIO_IO25	T52	gpio2.IO[25]	usdhc3.DATA1	can2.TX		tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]
B51	GPIO_IO27	U49	gpio2.IO[27]	usdhc3.DATA3	can2.RX		tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]
B53	CCM_CLK03	AK20	ccmsrcgpcmix.CLK03	netc.TMR_1588_TRIG2	can3.TX		flexio2.FLEXIO[28]	gpio4.IO[28]		
B54	CCM_CLK04	Aj21	ccmsrcgpcmix.CLK04	netc.TMR_1588_PP2	can3.RX		flexio2.FLEXIO[29]	gpio4.IO[29]		
B55	GPIO_IO04	K46	gpio2.IO[4]	tpm3.CH0	pdm.CLK	can4.TX	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]

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Table 16: Alternate functions (Continued)

X1 pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
B56	GPIO_IO05	L45	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	can4.RX	spi7.SIN	uart6.RX		flexio1.FLEXIO[5]
B57	SD3_CMD	AF48	usdhc3.CMD	flexspi.A_SS0_B	sai5.TX_DATA[2]	sai5.RX_SYNC	flexio1.FLEXIO[21]	gpio3.IO[21]	xspi_slv.CS	
B58	GPIO_IO26	U45	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	flexio1.FLEXIO[26]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC
B60	XSPI1_DATA3	AK48	flexspi.A_DATA[3]	sai2.TX_DATA[7]	sai4.RX_DATA[0]		xspi_slv.DATA[3]	gpio5.IO[3]		
B61	XSPI1_DATA2	AJ47	flexspi.A_DATA[2]	sai2.TX_DATA[6]	sai4.TX_DATA[0]		xspi_slv.DATA[2]	gpio5.IO[2]		
B62	CCM_CLK02	AF20	ccmsrcgpcmix.CLK02	netc.TMR_1588_PP1			flexio1.FLEXIO[27]	gpio3.IO[27]		
B63	XSPI1_DQS	AK44	flexspi.A_DQS	sai5.RX_SYNC	sai5.TX_DATA[2]	sai2.RX_DATA[6]	xspi_slv.DQS	gpio5.IO[8]		
B65	XSPI1_SCLK	AJ43	flexspi.A_SCLK	sai2.RX_DATA[4]	sai4.RX_SYNC	earc.hpd	xspi_slv.CLK	gpio5.IO[9]		
B66	XSPI1_SS0_B	AJ41	flexspi.A_SS0_B	sai2.RX_DATA[5]	sai4.RX_BCLK	earc.cec	xspi_slv.CS	gpio5.IO[10]		
B67	XSPI1_DATA1	AH46	flexspi.A_DATA[1]	sai2.TX_DATA[5]	sai4.TX_SYNC	sai4.TX_DATA[1]	xspi_slv.DATA[1]	gpio5.IO[1]		
B68	XSPI1_DATA0	AJ45	flexspi.A_DATA[0]	sai2.TX_DATA[4]	sai4.TX_BCLK	sai4.RX_DATA[1]	xspi_slv.DATA[0]	gpio5.IO[0]		
B70	XSPI1_DATA4	AJ49	flexspi.A_DATA[4]	sai5.TX_DATA[0]	sai5.RX_DATA[1]		xspi_slv.DATA[4]	gpio5.IO[4]		
B71	XSPI1_DATA5	AK50	flexspi.A_DATA[5]	sai5.TX_SYNC	sai5.RX_DATA[2]	sai2.RX_DATA[6]	xspi_slv.DATA[5]	gpio5.IO[5]		
B72	XSPI1_DATA6	AJ51	flexspi.A_DATA[6]	sai5.TX_BCLK	sai5.RX_DATA[3]	sai2.RX_DATA[7]	xspi_slv.DATA[6]	gpio5.IO[6]		
B73	XSPI1_DATA7	AH50	flexspi.A_DATA[7]	sai5.RX_DATA[0]	sai5.TX_DATA[1]		xspi_slv.DATA[7]	gpio5.IO[7]		
B89	ENET2_MDIO	AJ31	netc.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]		
B90	ENET2_MDC	AK32	netc.MDC	uart4.DCB_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]		
C08	DAP_TDI	AK24	dap.TDI	mqs2.LEFT	netc.TMR_1588_ALARM1	can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX	
C10	DAP_TDO_TRACESWO	AJ23	dap.TDO_TRACESWO	mqs2.RIGHT	netc.TMR_1588_ALARM2	can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX	
C11	DAP_TCLK_SWCLK	AG21	dap.TCLK_SWCLK			can4.RX	flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B	
C13	DAP_TMS_SWDIO	AH22	dap.TMS_SWDIO			can4.TX	flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B	
C16	ENET1_MDIO	AJ39	netc.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]		
C17	ENET1_MDC	AK40	netc.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]		

Continued on next page

Table 16: Alternate functions (Continued)

X1 pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
C18	GPIO_IO22	T44	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	can5.TX	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]
C19	GPIO_IO23	T46	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	can5.RX	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]
C20	ENET2_TD0	AG25	netc.ETH1_RGMII_TXD[0]	uart4.TX	sai2.RX_DATA[3]	sai4.TX_DATA[0]	flexio2.FLEXIO[19]	gpio4.IO[19]		netc.ETH1_RMII_TXD[0]
C21	ENET2_TD1	AG27	netc.ETH1_RGMII_TXD[1]	uart4.RTS_B	sai2.RX_DATA[2]	sai4.TX_BCLK	flexio2.FLEXIO[18]	gpio4.IO[18]		netc.ETH1_RMII_TXD[1]
C22	ENET2_TD2	AF28	netc.ETH1_RGMII_TXD[2]	netc.ETH1_RMII_REF50_CLK ¹ ccmsrcgpcmix.ENET_REF_CLK_ROOT ²	sai2.RX_DATA[1]	sai4.TX_SYNC	flexio2.FLEXIO[17]	gpio4.IO[17]		
C23	ENET2_RXC	AJ25	netc.ETH1_RGMII_RX_CLK	netc.ETH1_RMII_RX_ER	sai2.TX_DATA[1]	sai4.RX_SYNC	flexio2.FLEXIO[23]	gpio4.IO[23]		
C24	PDM_BIT_STREAM1	H46	pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT3	gpio1.IO[10]		
C25	GPIO_IO24	T48	gpio2.IO[24]	usdhc3.DATA0			tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]
C26	GPIO_IO08	M44	gpio2.IO[8]	spi3.PCS0			tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]
C34	GPIO_IO35	W51	gpio5.IO[15]	pcie2.CLKREQ_B	uart6.RTS_B		spi4.SIN			
C37	GPIO_IO32	V52	gpio5.IO[12]	pcie1.CLKREQ_B	uart6.TX		spi4.PCS2			
D06	XSPI1_SS1_B	AH42	flexspi.A_SS1_B	sai5.RX_BCLK	sai5.TX_DATA[3]	sai2.RX_DATA[7]		gpio5.IO[11]		
D07	I2C2_SDA	E45	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]		
D08	I2C2_SCL	E43	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B	
D09	GPIO_IO00	J49	gpio2.IO[0]	i2c3.SDA			spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]
D10	GPIO_IO01	J51	gpio2.IO[1]	i2c3.SCL			spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]
D11	GPIO_IO02	K48	gpio2.IO[2]	i2c4.SDA			spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]
D12	GPIO_IO03	K52	gpio2.IO[3]	i2c4.SCL			spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]
D14	GPIO_IO21	R51	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	flexio1.FLEXIO[21]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK
D15	GPIO_IO19	R45	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	flexio1.FLEXIO[19]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]
D16	GPIO_IO18	P52	gpio2.IO[18]	sai3.RX_BCLK			spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]
D17	GPIO_IO20	R49	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]		spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]
D19	UART1_RXD	E49	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0	vpu.UART_RX	gpio1.IO[4]		

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Table 16: Alternate functions (Continued)

X1 pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
D20	UART1_TXD	F52	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1	vpu.UART_TX	gpio1.IO[5] or ccmsrcgpcmix.BOOT_MODE[0]		
D21	UART2_RXD	E51	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]		
D22	UART2_TXD	F48	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7] or ccmsrcgpcmix.BOOT_MODE[1]		
D23	ENET2_RD0	AJ27	netc.ETH1_RGMII_RXD[0]	uart4.RX	sai2.TX_DATA[2]	sai4.RX_BCLK	flexio2.FLEXIO[24]	gpio4.IO[24]		netc.ETH1_RMII_RXD[0]
D24	ENET2_RD1	AK28	netc.ETH1_RGMII_RXD[1]	spdif1.IN	sai2.TX_DATA[3]	sai4.RX_DATA[0]	flexio2.FLEXIO[25]	gpio4.IO[25]		netc.ETH1_RMII_RXD[1]
D25	ENET2_RD3	AH30	netc.ETH1_RGMII_RXD[3]	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]		
-	GPIO_IO28	U51	gpio2.IO[28]	i2c3.SDA	can3.TX					flexio1.FLEXIO[28]
-	GPIO_IO29	V44	gpio2.IO[29]	i2c3.SCL	can3.RX					flexio1.FLEXIO[29]
-	ENET1_TX_CTL	AF32	netc.ETH0_RGMII_TX_CTL	uart3.DTR_B	netc.ETH0_RMII_TX_EN		flexio2.FLEXIO[6]	gpio4.IO[6]		
-	ENET1_TD3	AG37	netc.ETH0_RGMII_TXD[3]		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]		
-	ENET1_TD2	AF36	netc.ETH0_RGMII_TXD[2]	netc.ETH0_RMII_REF50_CLK ¹ ccmsrcgpcmix.ENET_REF_CLK_ROOT ²	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]		
-	ENET1_TD1	AG35	netc.ETH0_RGMII_TXD[1]	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]		i3c2.PUR_B netc.ETH0_RMII_TXD[1]
-	ENET1_TD0	AG33	netc.ETH0_RGMII_TXD[0]	uart3.TX	netc.ETH0_RMII_TXD[0]		flexio2.FLEXIO[5]	gpio4.IO[5]		
-	ENET1_TXC	AG31	netc.ETH0_RGMII_TX_CLK	ccmsrcgpcmix.ENET_CLK_ROOT			flexio2.FLEXIO[7]	gpio4.IO[7]		
-	ENET1_RX_CTL	AH34	netc.ETH0_RGMII_RX_CTL	uart3.DSR_B	netc.ETH0_RMII_CRS_DV	usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]		
-	ENET1_RXC	AJ33	netc.ETH0_RGMII_RX_CLK	netc.ETH0_RMII_RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]		
-	ENET1_RD0	AJ35	netc.ETH0_RGMII_RXD[0]	uart3.RX	netc.ETH0_RMII_RXD[0]		flexio2.FLEXIO[10]	gpio4.IO[10]		
-	ENET1_RD1	AK36	netc.ETH0_RGMII_RXD[1]	uart3.CTS_B	netc.ETH0_RMII_RXD[1]	lptmr2.ALT1	flexio2.FLEXIO[11]	gpio4.IO[11]		
-	ENET1_RD2	AJ37	netc.ETH0_RGMII_RXD[2]		netc.ETH0_RMII_RX_ER	lptmr2.ALT2	flexio2.FLEXIO[12]	gpio4.IO[12]		
-	ENET1_RD3	AH38	netc.ETH0_RGMII_RXD[3]			lptmr2.ALT3	flexio2.FLEXIO[13]	gpio4.IO[13]		
-	SD1_CLK	AG39	usdhc1.CLK				flexio1.FLEXIO[8]	gpio3.IO[8]		
-	SD1_CMD	AF40	usdhc1.CMD				flexio1.FLEXIO[9]	gpio3.IO[9]		

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Table 16: Alternate functions (Continued)

X1 pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
-	SD1_DATA0	AG45	usdhc1.DATA0				flexio1.FLEXIO[10]	gpio3.IO[10]		
-	SD1_DATA1	AE45	usdhc1.DATA1				flexio1.FLEXIO[11]	gpio3.IO[11]		
-	SD1_DATA2	AD46	usdhc1.DATA2				flexio1.FLEXIO[12]	gpio3.IO[12]		
-	SD1_DATA3	AG43	usdhc1.DATA3	flexspi.A_SS1_B			flexio1.FLEXIO[13]	gpio3.IO[13]		
-	SD1_DATA4	AF44	usdhc1.DATA4	flexspi.A_DATA[4]			flexio1.FLEXIO[14]	gpio3.IO[14]		xspi_slv.DATA[4]
-	SD1_DATA5	AG47	usdhc1.DATA5	flexspi.A_DATA[5]	usdhc1.RESET_B		flexio1.FLEXIO[15]	gpio3.IO[15]		xspi_slv.DATA[5]
-	SD1_DATA6	AD44	usdhc1.DATA6	flexspi.A_DATA[6]	usdhc1.CD_B		flexio1.FLEXIO[16]	gpio3.IO[16]		xspi_slv.DATA[6]
-	SD1_DATA7	AC45	usdhc1.DATA7	flexspi.A_DATA[7]	usdhc1.WP		flexio1.FLEXIO[17]	gpio3.IO[17]		xspi_slv.DATA[7]
-	SD1_STROBE	AG41	usdhc1.STROBE	flexspi.A_DQS			flexio1.FLEXIO[18]	gpio3.IO[18]		xspi_slv.DQS
-	I2C1_SCL	D48	i2c1.SCL	i3c1.SCL	uart1.DCB_B	tpm2.CH0		gpio1.IO[0]		
-	I2C1_SDA	D52	i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]		
-	SAI1_TXFS	G49	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]		
-	SAI1_TXD0	H48	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]		
-	WDOG_ANY	J45	wdog1.WDOG_ANY	fccu.eout1				gpio1.IO[15]		
-	FCCU_ERR0	K44	fccu.eout0							

¹ Input pin.

² Output pin.

Bold text: Alternate function that provides maximum compatibility between modules of the Aquila family.

Rows in : Pin used to determine boot mode at power-on reset. It is output-only because it is isolated from the SoM's board-to-board connector by a 3-state buffer.

After reset, it operates according to the selected alternate function.

4.2 Pin Control

The alternate function of each pin can be configured independently. Each pin has a Pad Mux register where various settings can be defined (note that some settings may not be available for certain pins). The register is named IOMUXC_SW_MUX_CTL_PAD_x, where x corresponds to the name of the i.MX 95 pin.

Table 17: Pad control register

Bit	Field	Description	Remarks
31-5	Reserved		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enable	Force the selected mux mode input path.
3	Reserved		
2-0	MUX_MODE	000 Select mux mode: ALT0 mux port 001 Select mux mode: ALT1 mux port 010 Select mux mode: ALT2 mux port 011 Select mux mode: ALT3 mux port 100 Select mux mode: ALT4 mux port 101 Select mux mode: ALT5 mux port (GPIO) 110 Select mux mode: ALT6 mux port	Check Section 4.1 for the available alternate function of the pin.

Each pin also has an associated register that allows configuration of pull-up/pull-down resistors, drive strength, and other electrical settings. This register is named IOMUXC_SW_PAD_CTL_PAD_x, where x corresponds to the name of the i.MX 95 pin. Note that some settings may not be available on all pins.

Input functions available on more than one physical pin require an additional input multiplexer. This multiplexer is configured using a register named IOMUXC_x_SELECT_INPUT, where x corresponds to the name of the input function.

Table 18: Pad mux register

Bit	Field	Description
31-28	APC_LCK	APC lock bits APC_LCK[3:0] are lock bits for APC[3:0], they are one-to-one mapped: APC_LCK[3] locks APC[3] APC_LCK[2] locks APC[2] APC_LCK[1] locks APC[1] APC_LCK[0] locks APC[0] Once an APC_LCK lock bit is set, the corresponding APC data bit cannot be changed. APC_LCK bits are sticky bits, which means that once they are set to 1, they cannot be set to 0 unless reset is performed.
27-24	APC	Domain Access Field The Domain Access bits control whether the corresponding domain can access the IOMUX registers. When set to 1, the corresponding domain cannot access the IOMUX register. When set to 0, the corresponding domain can access the IOMUX register. Select one out of next values for pad: <PAD_NAME> 0000 ... 1111
23-16	Reserved	

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Table 18: Pad mux register (Continued)

Bit	Field	Description
15-13	SMIC	<p>Safe Mode Control Bypasses pin safe-stating:</p> <ul style="list-style-type: none"> • When SMC is enabled, pin safe-stating is allowed. FCCU fault reaction disables the pin by keeping the OBE field value to 1'b0. • When SMC is disabled, pin safe-stating by FCCU fault reaction is bypassed and does not affect the pin. <p>Pin safe-stating is managed per application domains. Accordingly, SMC manages pin safe-state bypassing by application domains.</p> <ul style="list-style-type: none"> 000b - Disabled on all four application domains 001b - Enabled safe stating for application domain 1 010b - Enabled safe stating for application domain 2 011b - Enabled safe stating for application domain 1 and application domain 2 100b - Enabled safe stating for application domain 3 101b - Enabled safe stating for application domain 1 and application domain 3 110b - Enabled safe stating for application domain 2 and application domain 3 111b - Enabled safe stating for all application domains
12	HYS	<p>Schmitt trigger Field Select one out of next values for pad: SAI1_TXD0</p> <ul style="list-style-type: none"> 0b - No Schmitt input 1b - Schmitt input
11	OD	<p>Open Drain Field Select one out of next values for pad: SAI1_TXD0</p> <ul style="list-style-type: none"> 0b - Open Drain Disable 1b - Open Drain Enable
10	PD	<p>Pull Down Field Select one out of next values for pad: SAI1_TXD0</p> <ul style="list-style-type: none"> 0b - Not pull down 1b - Pull down
9	PU	<p>Pull Up Field Select one out of next values for pad: SAI1_TXD0</p> <ul style="list-style-type: none"> 0b - No pull up 1b - Pull up
8-7	FSEL1	<p>Slew Rate Field Select one out of next values for pad: SAI1_TXD0</p> <ul style="list-style-type: none"> 00b - 01b - 10b - Slight Fast Slew Rate 11b - Fast Slew Rate
6-1	DSE	<p>Drive Strength Field Select one out of next values for pad: SAI1_TXD0</p> <ul style="list-style-type: none"> 00_0000b - No drive 00_0001b - x1 00_0011b - x2 00_0111b - x3 00_1111b - x4 01_1111b - x5 11_1111b - X6
0	Reserved	

For more information about the available register settings, refer to the [i.MX 95 Reference Manual¹](#).

4.3 Pin Reset Status

After a reset, i.MX 95 pins can be in different modes. Most are pulled low, while some are in a high-impedance state or pulled high. Refer to [Section 3.2](#) for a complete list of the reset states of each pin. Once the bootloader is running, pins and their states can be reconfigured.



Pin reset states are only guaranteed during the release of the reset signal. During the power-up sequence, pin states may be undefined until the corresponding I/O bank voltage is enabled on the module.

¹<https://www.nxp.com/products/i.MX95>

5 Interface Description

5.1 ADC – Analog to Digital Converter

The NXP i.MX 95 integrates a 12-bit Successive Approximation Register (SAR) ADC module featuring up to eight external single-ended analog input channels, along with internal monitoring inputs. The SAR ADC supports a maximum sampling rate of 1 MS/s and offers flexible clock configuration. It operates in multiple conversion modes, including One-Shot and Scan, and supports interrupt- or DMA-driven data acquisition.

Additional capabilities include configurable internal or external trigger sources, hardware presampling, built-in self-test functions, and programmable watchdog thresholds. The ADC also incorporates offset and gain calibration mechanisms to ensure measurement accuracy.

Table 19: ADC pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	I/O <i>SoM perspective</i>	Description
D01	ADC_1	ADC_IN0	ALTO ¹	I	Analog input 1
D02	ADC_2	ADC_IN1	ALTO ¹	I	Analog input 2
D03	ADC_3	ADC_IN2	ALTO ¹	I	Analog input 3
D04	ADC_4	ADC_IN3	ALTO ¹	I	Analog input 4
D54	ADC_5	ADC_IN4	ALTO ¹	I	Analog input 5
D55	ADC_6	ADC_IN5	ALTO ¹	I	Analog input 6
C55	ADC_7	ADC_IN6	ALTO ¹	I	Analog input 7
C56	ADC_8	ADC_IN7	ALTO ¹	I	Analog input 8

¹ This pin has no alternate functions.

5.2 CAN – Controller Area Network

The i.MX 95 integrates a single FlexCAN controller that is fully compliant with CAN FD (Flexible Data-Rate), as defined by ISO 11898-1:2015 and CAN Specification 2.0 Part B. Key features include:

- Support for standard and extended data frames with payloads up to 64 bytes
- Bit rate switching (BRS) for CAN FD
- Error state indication and full CAN FD protocol compatibility
- Flexible message buffer configuration, dynamically adjustable based on payload size; larger payloads reduce buffer count
- Legacy RX FIFO (6-frame capacity) and Enhanced RX FIFO (20-frame capacity), both with DMA support
- Listen-only and programmable loopback modes for self-test, diagnostics and passive monitoring
- High-resolution timestamping via a dedicated 32-bit free-running timer, optionally synchronized to an external time tick
- Maskable interrupts with individual flags for message buffers and FIFO, supporting interrupt-driven or DMA-based data handling

Table 20: CAN pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM perspective</i>	Description
CAN1						
B48	CAN_1_TX	PDM_CLK	ALT6	CAN1_TX	O	CAN port 1 transmit pin
B49	CAN_1_RX	PDM_BIT_STREAM0	ALT6	CAN1_RX	I	CAN port 1 receive pin
CAN2						
B50	CAN_2_TX	GPIO_IO25	ALT2	CAN2_TX	O	CAN port 2 transmit pin
B51	CAN_2_RX	GPIO_IO27	ALT2	CAN2_RX	I	CAN port 2 receive pin
CAN3						
B53	CAN_3_TX	CCM_CLK03	ALT2	CAN3_TX	O	CAN port 3 transmit pin
B54	CAN_3_RX	CCM_CLK04	ALT2	CAN3_RX	I	CAN port 3 receive pin
CAN4						
B55	CAN_4_TX	GPIO_IO04	ALT3	CAN4_TX	O	CAN port 4 transmit pin
B56	CAN_4_RX	GPIO_IO05	ALT3	CAN4_RX	I	CAN port 4 receive pin

The remaining interfaces are available as alternate functions on other pins. The [Toradex Pinout Designer²](#) tool can help verify pin multiplexing, especially for alternate functions that are not part of the standard Aquila specification.

5.3 Digital Audio Interfaces

The i.MX 95 SoC features six Synchronous Audio Interfaces (SAIs) that support a variety of audio protocols including I²S, AC'97, TDM, and Codec/DSP. In this SOM, the SAI signals SAI1_TXC and SAI1_RXD0 are exposed on pins B17 (GPIO_09_CSI_1) and B18 (GPIO_10_CSI_1), respectively. These signals fall into the category of **Alternate Functions**, meaning they share the pins with other functions selectable through pin multiplexing.

The remaining SAI interfaces are available on other pins as alternate functions. The Toradex Pinout Designer tool can assist in verifying the pin multiplexing configuration, particularly for alternate functions not defined in the standard Aquila specification.

Table 21: I²S pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM in controller mode</i>	Description
I2S_1						
B20	I2S_1_BCLK	ENET2_IO16	ALT2	SAI2_TX_BCLK	O	Transmit bit clock
B21	I2S_1_SYNC	ENET2_IO26	ALT2	SAI2_TX_SYNC	O	Transmit frame sync
B22	I2S_1_D_OUT	ENET2_IO21	ALT2	SAI2_TX_DATA0	O	Data output
B23	I2S_1_D_IN	ENET2_IO20	ALT2	SAI2_RX_DATA0	I	Data input
B24	I2S_1_MCLK	ENET2_IO17	ALT2	SAI2_MCLK	O	Audio controller clock

Continued on next page

²<https://developer.toradex.com/carrier-board-design/pinout-designer/>

Table 21: I²S pins (Continued)

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM in controller mode</i>	Description
I2S_2						
42	I2S_2_BCLK	SD3_DATA3	ALT3	SAI5_TX_BCLK	O	Transmit bit clock
44	I2S_2_SYNC	SD3_DATA3	ALT3	SAI5_TX_SYNC	O	Transmit frame sync
46	I2S_2_D_OUT	SD3_DATA1	ALT3	SAI5_TX_DATA0	O	Data output
48	I2S_2_D_IN	SD3_CLK	ALT3	SAI5_RX_DATA0	I	Data input

5.3.1 SAI Used as AC'97

The SAI interface can be configured for AC'97 compatibility. The AC'97 audio interface does not require an additional I²C bus for control communication, as the codec is controlled directly through the AC'97 interface.

The AC'97 codec requires a master reference clock, which can be provided either by one of the SAI master clock outputs or by an external crystal or oscillator.



Some codecs use unconventional pin naming: for example, a device may label its data input pin as SDATA_OUT and its data output pin as SDATA_IN. These names refer to the signals they should connect to on the host, not to the actual signal direction.

Table 22: SAI in AC'97 mode

SoC port name	Codec signal name	I/O <i>SoM perspective</i>	Description
SAIx.RX_DATA[0]	SDATA_IN	I	Audio Serial Input to i.MX 95 from the codec.
SAIx.TX_DATA[0]	SDATA_OUT	O	Audio Serial Output from i.MX 95 to the codec.
SAIx.TX_SYNC	SYNC	O	Audio Sync
SAIx.TX_BCLK	BIT_CLK	I	Audio Bit Clock
GPIOx	RESET#	O	Master H/W Reset. Any GPIO can be used.

5.3.2 MICFIL – PDM Microphone Interface

The i.MX 95 SoC supports up to four PDM microphone input signals. PDM (Pulse-Density Modulation) is a widely used digital interface for transmitting audio from microphones to the SoC. The PDM bitstream is time-multiplexed and carries audio data for two channels (left and right), allowing up to eight microphones to be connected.

Since PDM is not part of the standard Aquila interface, these signals are available only as alternate functions. As a result, PDM microphone support is not guaranteed to be compatible across different Aquila modules. The I/O column in [Table 23](#) reflects the signals when the SoM is configured in controller mode.

Table 23: PDM pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
Microphone Input						
B36	UART_1_CTS	GPIO_IO16	ALT2	PDM_BIT_STREAM2	I	Microphone data input channel 2
B40	I2C_3_DSI1_SCL	GPIO_IO12	ALT2	PDM_BIT_STREAM2	I	Microphone data input channel 2
B41	I2C_3_DSI1_SDA	GPIO_IO13	ALT2	PDM_BIT_STREAM3	I	Microphone data input channel 3
B46	PWM_3_DSI	GPIO_IO19	ALT2	PDM_BIT_STREAM3	I	Microphone data input channel 3
B49	CAN_1_RX	PDM_BIT_STREAM0	ALT0	PDM_BIT_STREAM0	I	Microphone data input channel 0
B56	CAN_4_RX	GPIO_IO05	ALT2	PDM_BIT_STREAM0	I	Microphone data input channel 0
B58	PWM_4_DP	GPIO_IO26	ALT2	PDM_BIT_STREAM1	I	Microphone data input channel 1
C05	I2C_3_DSI1_SDA	GPIO_IO12	ALT2	PDM_BIT_STREAM2	I	Microphone data input channel 2
C06	I2C_3_DSI1_SCL	GPIO_IO13	ALT2	PDM_BIT_STREAM3	I	Microphone data input channel 3
C24	PWM_2	GPIO_IO08	ALT0	PDM_BIT_STREAM1	I	Microphone data input channel 1
D15	SPI_2_MISO	GPIO_IO19	ALT2	PDM_BIT_STREAM3	I	Microphone data input channel 3
D17	SPI_2_MOSI	GPIO_IO20	ALT2	PDM_BIT_STREAM0	I	Microphone data input channel 0
Serial Clock						
B48	CAN_1_TX	PDM_CLK	ALT0	PDM_CLK	O	Serial clock
B55	CAN_4_TX	GPIO_IO04	ALT2	PDM_CLK	O	Serial clock
D14	SPI_2_CLK	GPIO_IO21	ALT2	PDM_CLK	O	Serial clock

5.3.3 S/PDIF – Sony-Philips Digital Interface

The S/PDIF interface supports both input and output. The input controller can digitally recover the clock from the incoming stream and conforms to the AES/EBU IEC 60958 standard.

S/PDIF is not part of the Aquila standard, meaning its signals are only available as alternate functions on other interface pins. As a result, S/PDIF support is not guaranteed to be compatible across different Aquila modules. The I/O column in [Table 24](#) reflects the signals flow when the SoM is configured in controller mode.

Table 24: S/PDIF pins

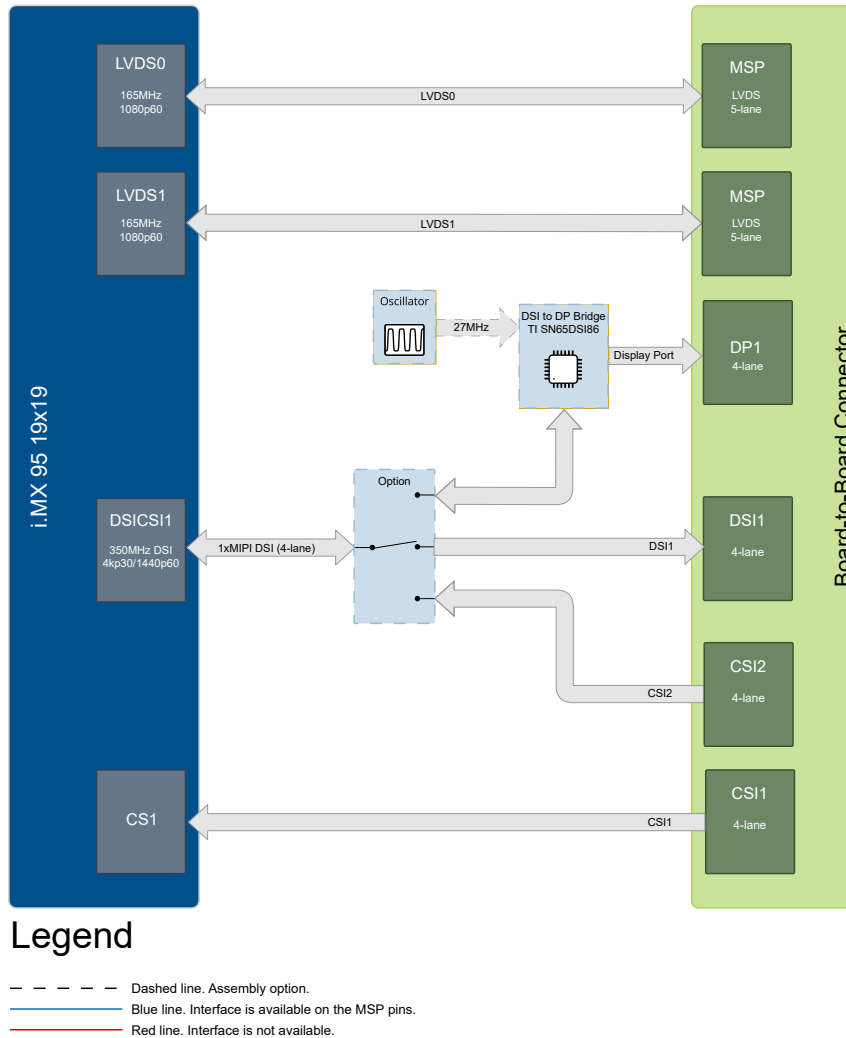
X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C18	I2C_6_SDA	GPIO_IO22	ALT2	SPDIF1_IN	I	Audio input
C19	I2C_6_SCL	GPIO_IO23	ALT2	SPDIF1_OUT	O	Audio output
D24	GPIO_02	ENET2_RD1	ALT1	SPDIF1_IN	I	Audio input
D25	GPIO_03	ENET2_RD3	ALT1	SPDIF1_OUT	O	Audio output
D25	GPIO_03	ENET2_RD3	ALT2	SPDIF1_IN	I	Audio input

5.4 Displays

The Aquila iMX95 features a single display controller with two display engines, enabling simultaneous driving of up to three displays: one MIPI-DSI interface and two LVDS interfaces. Both LVDS displays are required to share the same resolution and timing parameters. [Figure 2](#) shows the block diagram of the Aquila iMX95 display subsystem, which allows flexible, high-resolution display configurations optimized

for demanding applications.

Figure 2: Displays block diagram



HDMI port is not natively supported on the Aquila iMX95 SoM. However, HDMI can be enabled with a DSI-to-HDMI bridge solution on the carrier board.

Display Engines:

- One MIPI-DSI interface
- One LVDS interface supporting two LVDS displays (both must share identical resolution and timing)

DisplayPort Bridge:

- A dedicated DisplayPort bridge converts MIPI-DSI signals to DisplayPort output if required.

The MIPI-DSI and DisplayPort interfaces are defined as Reserved Aquila interfaces, ensuring compatibility across Aquila modules. In contrast, the LVDS signals are located on module-specific pins, making LVDS usage potentially incompatible with other Aquila modules.

For maximum interoperability, the MIPI-DSI and DisplayPort interfaces are recommended. Should LVDS

displays be necessary alongside other Aquila modules, implementing a MIPI-DSI to LVDS bridge on the carrier board is advised.

LVDS Interface:

- Two 1080p60 LVDS transmitters, configurable as either two 4-lane or one 8-lane LVDS channels
- Both LVDS displays must use matching resolution and timing parameters

MIPI-DSI Interface:

- Single 4-lane interface operating at up to 350 MHz per lane (2.5 Gbps/lane)
- Supports up to 4Kp30 or 3840×1440p60 resolutions

DSICSI1 Signal Usage Options

The DSICSI1 signals on the Aquila iMX95 module offer three distinct configuration possibilities, selectable by module NPI:

1. MIPI Display Serial Interface (MIPI DSI - DSI1): utilizes pins A31, A32, A34, A35, A37, A38, A40, A41, A43, and A44 for a standard 4-lane MIPI DSI display interface.
2. DisplayPort Bridge (DP_1): converts MIPI DSI signals to DisplayPort output using pins A46, A47, A49, A50, A52, A53, A55, A56, A58, and A59.
3. Camera Serial Interface (CSI2): configured as a CSI2 interface on pins B02, B03, B05, B06, B08, B09, B11, B12, B14, and B15 for camera input.



These configuration options are predetermined by the module NPI at the assembly stage. Customers must select the correct NPI according to their required interface, as these options cannot be modified or reconfigured on the customer side post-purchase.

Please refer to [Section 1.8.1](#) for detailed information on the Part Number nomenclature.

5.4.1 DisplayPort Bridge

The SN65DSI86ZXHR is a high-performance bridge device designed to convert MIPI Display Serial Interface (DSI) signals to DisplayPort output. This component enables the integration of DSI-based systems with DisplayPort-compatible displays, supporting high-resolution and high-refresh-rate video transmission. By handling protocol conversion and signal integrity, the SN65DSI86ZXHR provides a flexible and reliable solution for bridging the gap between MIPI DSI sources and DisplayPort displays.

Table 25: DisplayPort interface signals

X1 Pin	Aquila standard function	SoC ball name	SoC alternate function	I/O	Description/Remarks
A47	DP_1_AUX+	- ¹	-	I/O	Positive differential, bidirectional auxiliary channel used for device control
A46	DP_1_AUX-	- ¹	-	I/O	Negative differential, bidirectional auxiliary channel used for device control
A50	DP_1_LANE3+	- ¹	-	O	Positive of differential pair that carries high-speed, unidirectional serialized video and audio data
A49	DP_1_LANE3-	- ¹	-	O	Negative of differential pair that carries high-speed, unidirectional serialized video and audio data
A53	DP_1_LANE2+	- ¹	-	O	Positive of differential pair that carries high-speed, unidirectional serialized video and audio data

Continued on next page

Table 25: DisplayPort interface signals (Continued)

X1 Pin	Aquila standard function	SoC ball name	SoC alternate function	I/O	Description/Remarks
A52	DP_1_LANE2-	⁻¹	-	O	Negative of differential pair that carries high-speed, unidirectional serialized video and audio data
A56	DP_1_LANE1+	⁻¹	-	O	Positive of differential pair that carries high-speed, unidirectional serialized video and audio data
A55	DP_1_LANE1-	⁻¹	-	O	Negative of differential pair that carries high-speed, unidirectional serialized video and audio data
A59	DP_1_LANE0+	⁻¹	-	O	Positive of differential pair that carries high-speed, unidirectional serialized video and audio data
A58	DP_1_LANE0-	⁻¹	-	O	Negative of differential pair that carries high-speed, unidirectional serialized video and audio data
Control Signals					
-	CTRL_DP_BRIDGE_EN	⁻²	-	-	10 kΩ pull-up resistor.
-	I2C_SOM_SCL	GPIO_IO29	ALT1	-	I ² C interface, intended for controlling DSI bridges.
-	I2C_SOM_SDA	GPIO_IO28	ALT1	-	

¹ Available through the on-module DisplayPort Bridge (SN65DSI86ZXHR).

² Available through the on-module GPIO Expander B (PCAL6408AHKX).

5.4.2 DSI

Table 26: DSI interface signals

X1 pin	Aquila standard function	SoC ball name	SoC alternate function	I/O	Description
A38	DSI_1_CLK_P	MIPI_DSICSI1_CLK_P	ALT0	O	Positive differential DSI Interface clock
A37	DSI_1_CLK_N	MIPI_DSICSI1_CLK_N	ALT0	O	Negative differential DSI Interface clock
A44	DSI_1_D0_P	MIPI_DSICSI1_D0_P	ALT0	O	Positive differential DSI Interface data lane 0
A43	DSI_1_D0_N	MIPI_DSICSI1_D0_N	ALT0	O	Negative differential DSI Interface data lane 0
A41	DSI_1_D1_P	MIPI_DSICSI1_D1_P	ALT0	O	Positive differential DSI Interface data lane 1
A40	DSI_1_D1_N	MIPI_DSICSI1_D1_N	ALT0	O	Negative differential DSI Interface data lane 1
A35	DSI_1_D2_P	MIPI_DSICSI1_D2_P	ALT0	O	Positive differential DSI Interface data lane 2
A34	DSI_1_D2_N	MIPI_DSICSI1_D2_N	ALT0	O	Negative differential DSI Interface data lane 2
A32	DSI_1_D3_P	MIPI_DSICSI1_D3_P	ALT0	O	Positive differential DSI Interface data lane 3
A31	DSI_1_D3_N	MIPI_DSICSI1_D3_N	ALT0	O	Negative differential DSI Interface data lane 3
Control Interface					
B41	I2C_3_DSI_SCL	GPIO_IO13	ALT6	I/O	I ² C interface, intended to be used as DDC or for controlling DSI bridges
B40	I2C_3_DSI_SDA	GPIO_IO12	ALT6	I/O	
B46	PWM_3_DSI	GPIO_IO06	ALT0	O	Display backlight brightness control.
B42	GPIO_17_DSI_1	GPIO_IO07	ALT0	I/O	DSI_1_INT#; Interrupt input, intended to be used as hotplug detect or for interrupt messages from DSI bridges on carrier board. DSI_1_BKL_EN; Display backlight enable
B43	GPIO_18_DSI_1	GPIO_IO09	ALT0	I/O	
B44	GPIO_19_DSI_1	GPIO_IO33	ALT0	I/O	
B45	GPIO_20_DSI_1	GPIO_IO34	ALT0	I/O	

5.4.3 LVDS

The native LVDS signals are located on module-specific pins. This means the LVDS interface may not be available on other Aquila modules or, if present, may not use the same pins. If an LVDS display is required and compatibility with other Aquila Family modules is important, consider implementing a MIPI DSI to LVDS bridge on the carrier board, provided the carrier supports it.

Native LVDS Support:

- Aquila iMX95 supports native LVDS video output up to 24-bit color depth.
- Resolution and Channel Configuration: 2x 1080p60 LVDS Tx (2x 4-lane or 1x 8-lane)

Table 27: LVDS interface signals

X1 pin	SoC ball name	SoC alternate function	I/O	Description
Channel 0				
D87	LVDS0_CLK_N	- ¹	O	LVDS clock lane, N polarity signal, channel 0
D88	LVDS0_CLK_P	- ¹	O	LVDS clock lane, P polarity signal, channel 0
D82	LVDS0_D0_N	- ¹	O	LVDS data lane 0, N polarity signal, channel 0
D81	LVDS0_D0_P	- ¹	O	LVDS data lane 0, P polarity signal, channel 0
D85	LVDS0_D1_N	- ¹	O	LVDS data lane 1, N polarity signal, channel 0
D84	LVDS0_D1_P	- ¹	O	LVDS data lane 1, P polarity signal, channel 0
D91	LVDS0_D2_N	- ¹	O	LVDS data lane 2, N polarity signal, channel 0
D90	LVDS0_D2_P	- ¹	O	LVDS data lane 2, P polarity signal, channel 0
D94	LVDS0_D3_N	- ¹	O	LVDS data lane 3, N polarity signal, channel 0
D93	LVDS0_D3_P	- ¹	O	LVDS data lane 3, P polarity signal, channel 0
Channel 1				
D73	LVDS1_CLK_N	- ¹	O	LVDS clock lane, N polarity signal, channel 1
D72	LVDS1_CLK_P	- ¹	O	LVDS clock lane, P polarity signal, channel 1
D67	LVDS1_D0_N	- ¹	O	LVDS data lane 0, N polarity signal, channel 1
D66	LVDS1_D0_P	- ¹	O	LVDS data lane 0, P polarity signal, channel 1
D70	LVDS1_D1_N	- ¹	O	LVDS data lane 1, N polarity signal, channel 1
D69	LVDS1_D1_P	- ¹	O	LVDS data lane 1, P polarity signal, channel 1
D76	LVDS1_D2_N	- ¹	O	LVDS data lane 2, N polarity signal, channel 1
D75	LVDS1_D2_P	- ¹	O	LVDS data lane 2, P polarity signal, channel 1
D79	LVDS1_D3_N	- ¹	O	LVDS data lane 3, N polarity signal, channel 1
D78	LVDS1_D3_P	- ¹	O	LVDS data lane 3, P polarity signal, channel 1

¹ Dedicated to the LVDS interface and does not support alternate functions.

5.5 Ethernet

The Aquila standard provides two Ethernet ports leveraging the i.MX 95 SoC's dual Ethernet controllers, each with a unique MAC address. The first port is a 10/100/1000 Mbit media-dependent interface (MDI) that includes an on-module Ethernet PHY—the TI DP83867—and features advanced Time-Sensitive Networking (TSN) capabilities. The second port is a gigabit media-independent interface (RGMII) available on the module's board-to-board connector pins, supporting connection to an external Ethernet PHY. While this second controller does not support TSN, both Ethernet controllers support Energy Effi-

cient Ethernet (EEE), Ethernet Audio Video Bridging (AVB), and precision time synchronization compliant with IEEE 1588.

Table 28: Media-Dependent Interface Ethernet pins

X1 pin	Aquila specification signal name	DP83867 signal name	I/O <i>SoM perspective</i>	Description
Lane 0				
A88	ETH_1_MDI0_N	TD_M_A	I/O	Negative differential MDI signal
A89	ETH_1_MDI0_P	TD_P_A	I/O	Positive differential MDI signal
Lane 1				
A91	ETH_1_MDI1_P	TD_P_B	I/O	Positive differential MDI signal
A92	ETH_1_MDI1_N	TD_M_B	I/O	Negative differential MDI signal
Lane 2				
A94	ETH_1_MDI2_N	TD_M_C	I/O	Negative differential MDI signal
A95	ETH_1_MDI2_P	TD_P_C	I/O	Positive differential MDI signal
Lane 3				
A97	ETH_1_MDI3_P	TD_P_D	I/O	Positive differential MDI signal
A98	ETH_1_MDI3_N	TD_M_D	I/O	Negative differential MDI signal
LED control				
A99	ETH_1_LED_2	LED_0	O	Low when a link (any speed) is established
A100	ETH_1_LED_1	LED_2	O	Toggles during RX/TX activity

The TI DP83867 is a high-performance, low-power Ethernet PHY transceiver integrated on the system-on-module to support 10/100/1000 Mbps IEEE 802.3 compliant Ethernet communication. It features adaptive equalization and low latency MAC interface. The DP83867 supports RGMII, RMII, and SGMII interfaces, enabling flexible connectivity with the SoC while providing intelligent power management for efficient system-level energy consumption. Integrated loopback and diagnostic capabilities facilitate system debugging and compliance testing, making it ideal for applications requiring high reliability and throughput.

If only Fast Ethernet (10/100 Mbit) connectivity is required, providing two lanes are sufficient, allowing MDI2 and MDI3 signals to remain unconnected. Designers should consult the [Aquila Carrier Board Design Guide](#) for proper implementation. The i.MX 95 SoC's Gigabit Ethernet MAC integrates an accurate IEEE 1588-compliant timer for precise clock synchronization. This controller supports Audio Video Bridging (AVB), Time-Sensitive Networking (TSN), and includes external synchronization pins accessible via alternate functions. The on-module Texas Instruments DP83867 Ethernet PHY's interrupt signal (INT#) is routed to the P1_2 pin of the PCAL6416AHF I/O Expander for system integration.

The signals of the second Ethernet MAC are available as RGMII signals on the module board-to-board connector pins B81, B83, B84, B86, B87, B89, and B90, enabling the use of a dedicated external Ethernet PHY on the carrier board for dual Ethernet applications. This offers flexibility for specialized networking scenarios requiring two independent Ethernet ports.

Table 29: RGMII pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM perspective</i>	Description
Interrupt line						
B81	ETH_2_XGMII_INT#	-	ALT5	-	I	Interrupt signal from Ethernet PHY configuration and status connected to the GPIO Expander A
Receive interface						
B83	ETH_2_XGMII_RX0_N	ETH_RX0_N	ALT0 ¹	-	I	Negative differential XGMII signal
B84	ETH_2_XGMII_RX0_P	ETH_RX0_P	ALT0 ¹	-	I	Positive differential XGMII signal
Transmit interface						
B86	ETH_2_XGMII_TX0_N	ETH_TX0_N	ALT0 ¹	-	I	Negative differential XGMII signal
B87	ETH_2_XGMII_TX0_P	ETH_TX0_P	ALT0 ¹	-	I	Positive differential XGMII signal
Management interface						
B89	ETH_2_XGMII_MDIO	ENET2_MDIO	ALT0	NETC_MDIO	I/O	Bidirectional Management Data I/O for PHY configuration and status
B90	ETH_2_XGMII_MDC	ENET2_MDC	ALT0	NETC_MDIC	O	Management data clock signal

¹ This pin has no alternate functions.

5.5.1 ENET2 Used as I²S

The NXP i.MX 95 SoC has a second Ethernet interface connection (ENET2) which can alternatively function as an I²S (I2S1) interface. In the Aquila standard configuration, ENET2 is assigned by default to operate as I2S1. The following signals correspond to this I²S interface implementation.

Table 30: ENET2 as I²S interface

X1 pin	SoC port name	I ² S signal name	I/O <i>SoM perspective</i>	Description
B20	ENET2.TXC	I2S_1_BCLK	O	Bit clock serial continuous clock
B21	ENET2.TX_CTL	I2S_1_SYNC	I/O	Frame sync for channel alignment
B22	ENET2.RX_CTL	I2S_1_D_OUT	O	Serial Data Output line
B23	ENET2.TD3	I2S_1_D_IN	I	Serial Data Input line
B24	ENET2.RD2	I2S_1_MCLK	I	Master clock for synchronization

The remaining signals of the ENET2 interface are configured as general-purpose I/Os (GPIOs) and are routed to the board-to-board connector. Refer to [Table 31](#) for the detailed signal mapping.

Table 31: ENET2 as I²S interface

X1 pin	SoC port name	GPIO signal name	Description
D23	ENET2.RD0	GPIO_01	
D24	ENET2.RD1	GPIO_02	
D25	ENET2.RD3	GPIO_03	
C20	ENET2.TD0	GPIO_04	General Purpose Input/Output (GPIO) pins from the second Ethernet interface
C21	ENET2.TD1	GPIO_05	
C22	ENET2.TD2	GPIO_06	
C23	ENET2.RXC	GPIO_07	

5.6 FlexSPI – Flexible Serial Peripheral Interface

In addition to the standard SPI controller (referred to as LPSPI in NXP documentation), the i.MX 95 SoC integrates a Flexible SPI Controller (FlexSPI) with one SPI channel supporting up to two external devices. This interface supports single, dual, quad, and octal data transfer modes, enabling versatile communication. FlexSPI is designed for efficient access to NAND and NOR flash memories compliant with the QuadSPI standard.

The Aquila standard defines a QuadSPI interface featuring a single channel with two chip select signals intended for up to two memory devices, assigned within the Reserved pin class. Both chip selects are exposed via the FlexSPI controller; however, on the Aquila iMX95 module, the pin designated as the second chip select in the Reserved class is implemented as a general-purpose input/output (GPIO) without native chip select functionality. Consequently, direct hardware-driven control of the second chip select at this pin is not available. Use of this second chip select requires either software-driven bitbanging—which is typically impractical for flash memory devices—or reassignment to an alternate pin with chip select capability.

In addition, the Aquila iMX95 supports an octal mode operation by providing four supplementary data lines at the Reserved pin locations, rather than through alternate functions. This design approach ensures interface compatibility within the Aquila family, allowing the FlexSPI controller to leverage expanded data bandwidth in octal SPI mode where supported.



Octal SPI functionality, including these additional data pins, may not be implemented on all Aquila modules.

Table 32: FlexSPI modes

SoC function	Single mode	Dual mode	Quad mode	Octal mode
XSPI1_DATA0	TX	Bi-dir	Bi-dir	Bi-dir
XSPI1_DATA1	RX	Bi-dir	Bi-dir	Bi-dir
XSPI1_DATA2	-	-	Bi-dir	Bi-dir
XSPI1_DATA3	-	-	Bi-dir	Bi-dir
XSPI1_DATA4	-	-	-	Bi-dir
XSPI1_DATA5	-	-	-	Bi-dir
XSPI1_DATA6	-	-	-	Bi-dir
XSPI1_DATA7	-	-	-	Bi-dir

Table 33: QSPI signal pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM perspective</i>	Description
Data strobe						
B63	QSPI_1_DQS	XSPI1_DQS	ALT0	FLEXSPI_A_DQS	I	Data Strobe signal, required by some high-speed DDR devices
Clock						
B65	QSPI_1_CLK	XSPI1_SCLK	ALT0	FLEXSPI_A_SCLK	O	Serial Clock
Chip select						
B66	QSPI_1_CS#	XSPI1_SS0_B	ALT0	FLEXSPI_A_SS0_B	O	Chip Select 0
B67	CTRL_WAKE_MICO#	XSPI1_SS1_B	ALT0	FLEXSPI_A_SS1_B	O	Chip Select 1
Data lines						
B68	QSPI_1_IO0	XSPI1_DATA0	ALT0	FLEXSPI_A_DATA0	I/O	Serial data line 0
B67	QSPI_1_IO1	XSPI1_DATA1	ALT0	FLEXSPI_A_DATA1	I/O	Serial data line 1
B61	QSPI_1_IO2	XSPI1_DATA2	ALT0	FLEXSPI_A_DATA2	I/O	Serial data line 2
B60	QSPI_1_IO3	XSPI1_DATA3	ALT0	FLEXSPI_A_DATA3	I/O	Serial data line 3
B70	QSPI_1_IO4	XSPI1_DATA4	ALT0	FLEXSPI_A_DATA4	I/O	Serial data line 4
B71	QSPI_1_IO5	XSPI1_DATA5	ALT0	FLEXSPI_A_DATA5	I/O	Serial data line 5
B72	QSPI_1_IO6	XSPI1_DATA6	ALT0	FLEXSPI_A_DATA6	I/O	Serial data line 6
B73	QSPI_1_IO7	XSPI1_DATA7	ALT0	FLEXSPI_A_DATA7	I/O	Serial data line 7

Table 34: FlexSPI pins available via alternate functions

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM perspective</i>	Description
Clock						
B29	eMMc_CLK	SD3_CLK	ALT1 ¹	FLEXSPI_A_SCLK	O	Serial Clock
Chip select						
B57	eMMC_CMD	SD3_CMD	ALT1 ¹	FLEXSPI_A_SS0_B	O	Chip Select 0
Data lines						
B19	GPIO_12_CS01	SD3_DATA0	ALT1 ¹	FLEXSPI_A_DATA0	I/O	Serial data line 0
B28	I2S_2_D_OUT	SD3_DATA1	ALT1 ¹	FLEXSPI_A_DATA1	I/O	Serial data line 1
B27	I2S_2_SYNC	SD3_DATA2	ALT1 ¹	FLEXSPI_A_DATA2	I/O	Serial data line 2
B26	I2S_2_BCLK	SD3_DATA3	ALT1 ¹	FLEXSPI_A_DATA3	I/O	Serial data line 3

¹ For detailed mapping and configuration of the FlexSPI pins available through alternate functions, refer to the [Pinout Designer Tool](#).

5.7 GPIO – General-Purpose Input/Output

The Aquila Standard provides 23 dedicated General-Purpose Input/Output (GPIO) pins, of which four are allocated to the MIPI CSI camera interface and two to the MIPI DSI display interface.

Beyond these dedicated GPIOs, additional multifunctional pins can be repurposed as GPIOs when their primary functions are inactive. However, to ensure optimal compatibility and standard compliance across the Aquila family, it is strongly recommended to prioritize the use of the 23 dedicated GPIO

pins before employing alternate-function pins for general-purpose I/O.

Table 35: GPIO pins - Aquila Specification

X1// Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	Remarks
General-purpose					
D23	GPIO_01	ENET2_RD0	ALT5	GPIO_IO24	
D24	GPIO_02	ENET2_RD1	ALT5	GPIO_IO25	
D25	GPIO_03	ENET2_RD3	ALT5	GPIO_IO27	
C20	GPIO_04	ENET2_TD0	ALT5	GPIO_IO19	
C21	GPIO_05	ENET2_TD1	ALT5	GPIO_IO18	
C22	GPIO_06	ENET2_TD2	ALT5	GPIO_IO17	
C23	GPIO_07	ENET2_RXC	ALT5	GPIO_IO23	
C24	GPIO_08	PDM_BIT_STREAM1	ALT5	GPIO_IO10	
Reserved GPIO for MIPI CSI camera interface					
B17	GPIO_09_CSI_1	SAI1_TXC	ALT5	GPIO_IO12	
B18	GPIO_10_CSI_1	SAI1_RXD0	ALT5	GPIO_IO14	
A11	GPIO_11_CSI_1	SD2_VSELECT	ALT5	GPIO_IO19	
B19	GPIO_12_CSI_1	SD3_DATA0	ALT5	GPIO_IO22	
C01	GPIO_13_CSI_2	¹	-	-	100 kΩ pull-down resistor
C02	GPIO_14_CSI_2	¹	-	-	100 kΩ pull-down resistor
C03	GPIO_15_CSI_2	¹	-	-	100 kΩ pull-down resistor
C04	GPIO_16_CSI_2	¹	-	-	100 kΩ pull-down resistor
C06	I2C_5_CSI2_SCL	GPIO_IO13	ALT0	GPIO_IO13	Assembly Option
C05	I2C_5_CSI2_SDA	GPIO_IO12	ALT0	GPIO_IO12	Assembly Option
Reserved GPIO for MIPI DSI camera interface					
B42	GPIO_17_DSI_1	GPIO_IO07	ALT0	GPIO_IO07	
B43	GPIO_18_DSI_1	GPIO_IO09	ALT0	GPIO_IO09	
B44	GPIO_19_DSI_1	GPIO_IO33	ALT0	GPIO_IO33	
B45	GPIO_20_DSI_1	GPIO_IO34	ALT0	GPIO_IO34	
Reserved GPIO for DisplayPort interface					
B57	GPIO_21_DP	SD3_CMD	ALT5	GPIO_IO21	

¹ Available through the on-module GPIO Expander A (PCAL6416AHF).

Note the reset state of the GPIO pins: after a reset, the i.MX 95 pins may be configured in different modes. Most pins are pulled low, while some are high-impedance or pulled high. Once the bootloader is running, the pins and their states can be reconfigured. The reset state is only guaranteed during the release of the reset signal.

5.7.1 GPIO Wakeup

In principle, all GPIOs can be used to wake the Aquila iMX95 module from a suspended state. In the Aquila Standard, pin D06 is the default wake-up source. Only this pin is guaranteed to be wake-up compatible across Aquila modules. If carrier board compatibility with other Aquila modules is required,

use only this pin for wake-up functionality.

Table 36: GPIO wakeup pins

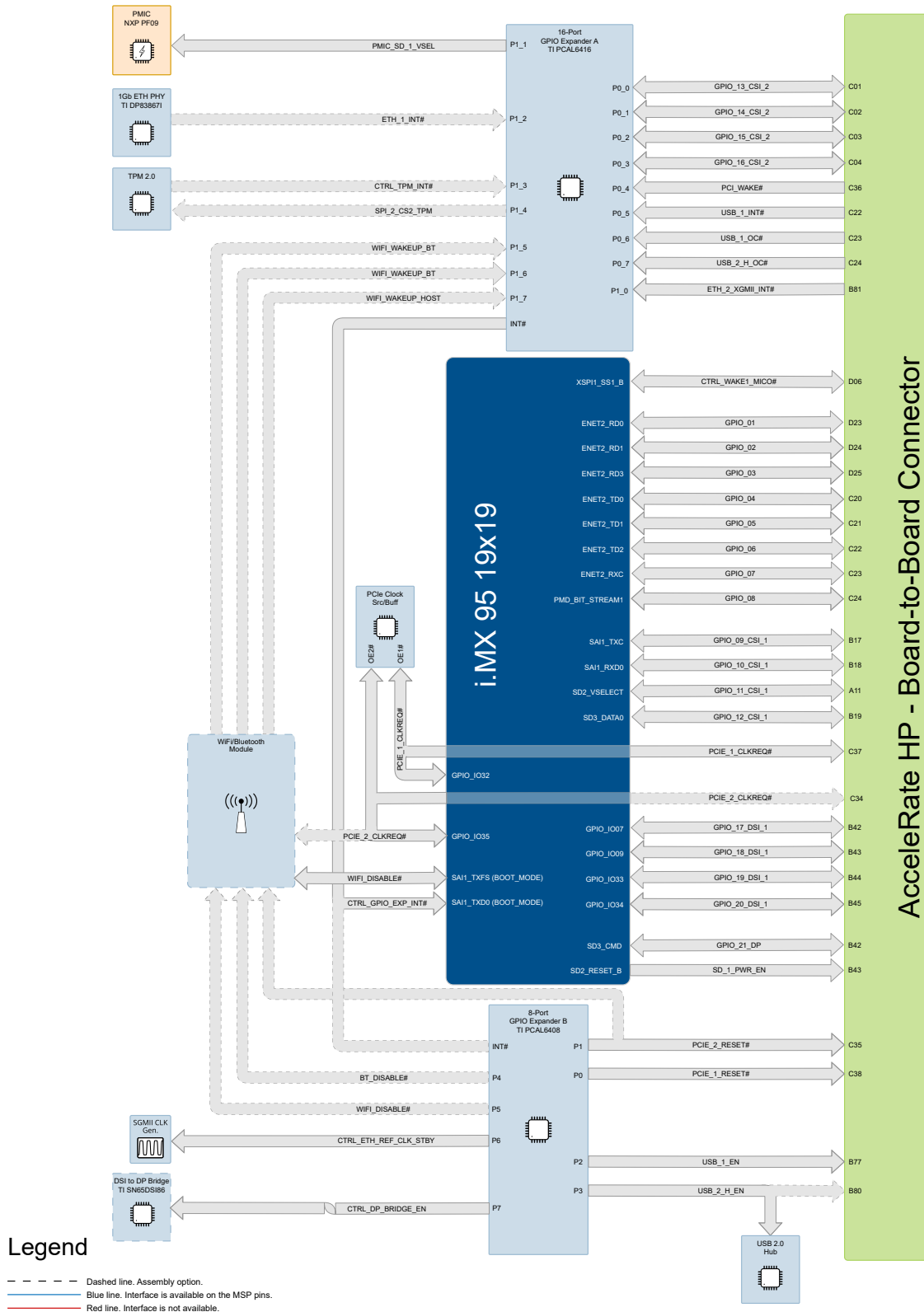
X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM perspective</i>	Description
D06	CTRL_WAKE1_MICO# ¹	XSPI1_SS1_B	ALT5	GPIO1_IO11	I/O	Default external wake-up signal

¹ There are no pull resistors on the module and the signal can be left floating on carrier boards if the wake feature is disabled in the software.

5.7.2 GPIO Expanders

The Aquila iMX95 leverages two GPIO expanders, the PCAL6416AHF and PCAL6408AHKX, to enhance its module functionality and maintain compatibility within the Aquila family. These expanders boost the number of available input/output pins via an I²C interface, enabling more flexible peripheral integration and efficient handling of I/O demands. [Figure 3](#) shows the block diagram of the Aquila iMX95 GPIO expanders subsystem.

Figure 3: GPIO expanders block diagram



The PCAL6416AHF is a 16-bit general-purpose GPIO expander. Its capabilities include bidirectional voltage-level translation, supporting communication between I²C buses and I/O pins operating at different voltage levels ranging from 1.65 V to 5.5 V. This makes it highly flexible for interfacing with multiple types of sensors, switches, LEDs, and other peripherals. It features programmable pull-up and pull-down resistors, interrupt generation for input state changes, and configurable output drive strengths up to 25 mA. The device simplifies design in mixed-signal environments by managing the voltage compatibility and reducing the need for additional components. However, its limitations include operating only at I²C speeds up to 400 kHz and requiring careful handling of interrupt masking to avoid spurious signals.

The PCAL6408AHKX is an 8-bit I²C-bus GPIO expander ideal for applications needing fewer I/O pins compared to 16-bit models. It extends I/O capabilities with 8 bidirectional ports, featuring programmable polarity inversion, input latching, and interrupt generation. Suited for space-constrained or simpler expansions, it supports power supply voltages from 1.65 V to 5.5 V and includes built-in voltage-level translation for mixed-voltage system integration. Operating within Fast-mode I²C limits (up to 400 kHz), it may restrict throughput in high-speed systems. The device offers programmable pull-up/pull-down resistors and configurable output drive strength up to 25 mA, enabling direct LED driving. Limitations include the I²C speed cap and the need to manage interrupt masking carefully to prevent spurious signals.

5.8 I²C/I³C Inter-Integrated Circuit

The NXP i.MX 95 System on Chip (SoC) integrates eight I²C controllers. Of these, **six controllers are accessible for external use**, while two have dedicated roles or limitations. Specifically, the I2C1 port is reserved for communication with the on-module Power Management IC (PMIC) and is not externally available. The eight I²C controllers are categorized as follows:

- one “Always Compatible” I²C/I³C interface for general-purpose applications;
- four “Reserved” interfaces dedicated to specific functions including the MIPI CSI-1 and CSI-2 camera inputs and the MIPI DSI display interface; and
- three “Module Specific” ports.

Among the “Module Specific” ports, the fifth I²C port is only accessible via alternate pin functions and may not be compatible across the Aquila module family, limiting its interoperability. The “Always Compatible” I²C interface serves as a general-purpose bus suitable for a wide range of devices such as real-time clocks (RTCs), sensors, and SMB-compliant system management devices.

In addition to I²C, the NXP i.MX 95 integrates one I³C controller that provides enhanced communication capabilities with improved speed and efficiency, categorized as “Always Compatible” within the Aquila standard. This dual presence of I²C and I³C buses ensures comprehensive support for legacy and advanced peripheral devices.

The NXP i.MX 95 SoC features eight I²C controllers. The fifth and sixth I²C ports are only available as alternate functions of other pins. Therefore, these interfaces may not be compatible with other Aquila modules.

Table 37: I²C/I³C Signal pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I ² C/I ³ C port	Remarks
D08	I2C_1_SDA	I2C2_SDA	ALT0	I2C2_SDA	I ² C2	Generic I ² C
D07	I2C_1_SCL	I2C2_SCL	ALT0	I2C2_SCL	I ² C2	
C16	I2C_2_SDA	ENET_MDIO	ALT2	I3C2_SDA	I ³ C2	Generic I ² C Always Compatible

Continued on next page

Table 37: I²C/I³C Signal pins (Continued)

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I ² C/I ³ C port	Remarks
C17	I2C_2_SCL	ENET_MDC	ALT2	I3C2_SDA	I ³ C2	
B40	I2C_3_DSI1_SDA	GPIO_IO12	ALT6	I2C8_SDA	I ² C8	I ² C port for the DSI interface. Intended to be used as DDC or for controlling DSI bridges on the carrier board
B41	I2C_3_DSI1_SCL	GPIO_IO13	ALT6	I2C8_SCL	I ² C8	
A12	I2C_4_CSI1_SDA	GPIO_IO30	ALT1	I2C4_SDA	I ² C4	Dedicated DDC port for CSI
A13	I2C_4_CSI1_SCL	GPIO_IO31	ALT1	I2C4_SCL	I ² C4	
C05	I2C_5_CSI2_SDA	GPIO_IO12	ALT6	I2C8_SDA	I ² C8	I ² C port for the camera interface
C06	I2C_5_CSI2_SCL	GPIO_IO13	ALT6	I2C8_SCL	I ² C8	
C18	I2C_6_SDA	GPIO_IO22	ALT6	I2C5_SDA	I ² C5	Generic I ² C
C19	I2C_6_SCL	GPIO_IO23	ALT6	I2C5_SCL	I ² C5	

Note: the I2C_5_CSI2 and I2C_3_DSI1 share the same SoC pin because the DSI interface can be used as a CSI interface.

Table 38: I²C/I³C additional signal pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I ² C/I ³ C port	Description/Remarks
I²C 2						
D07	I2C_1_SDA	I2C2_SDA	ALT0	I2C2_SDA	I2C2	Additional I2C2 port
D08	I2C_1_SCL	I2C2_SCL	ALT0	I2C2_SCL	I2C2	
I²C 4						
A12	I2C_4_CSI1_SDA	GPIO_IO30	ALT1	I2C4.SDA	I2C4	Additional I2C4 port
A13	I2C_4_CSI1_SCL	GPIO_IO31	ALT1	I2C4.SCL	I2C4	
I²C 5						
D09	SPI_1_CS	GPIO_IO00	ALT6	I2C5.SDA	I2C5	Alternate pins for the I2C5 port
D10	SPI_1_MISO	GPIO_IO01	ALT6	I2C5.SCL	I2C5	
I²C 6						
D11	SPI_1_MOSI	GPIO_IO02	ALT6	I2C6.SDA	I2C6	Additional I2C6 port
D12	SPI_1_CLK	GPIO_IO03	ALT6	I2C6.SCL	I2C6	
B55	CAN_4_TX	GPIO_IO04	ALT6	I2C6.SDA	I2C6	
B56	CAN_4_RX	GPIO_IO05	ALT6	I2C6.SCL	I2C6	
I²C 7						
B46	PWM_3_DSI	GPIO_IO06	ALT6	I2C7.SDA	I2C7	Additional I2C7 port
B42	GPIO_17_DSI_1	GPIO_IO07	ALT6	I2C7.SCL	I2C7	
C26	PWM_2	GPIO_IO08	ALT6	I2C7.SDA	I2C7	
B43	GPIO_18_DSI_1	GPIO_IO09	ALT6	I2C7.SCL	I2C7	

Continued on next page

Table 38: I²C/I³C additional signal pins (Continued)

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I ² C/I ³ C port	Description/Remarks
I²C 8						
B32	UART_2_CTS	GPIO_IO10	ALT6	I2C8.SDA	I2C8	Additional I2C8 port
B34	UART_2_RTS	GPIO_IO11	ALT6	I2C8.SCL	I2C8	
B40/C05	I2C_3/5_DS11/CSI2_SDA	GPIO_IO12	ALT6	I2C8.SDA	I2C8	
B41/C06	I2C_3/5_DS11/CSI2_SCL	GPIO_IO13	ALT6	I2C8.SCL	I2C8	
I³C 1						
D07	I2C_1_SDA	I2C2_SDA	ALT1	I3C1.PUR	-	Control of pull-up resistors on the I3C1 bus lines
D08	I2C_1_SCL	I2C2_SCL	ALT6	I3C1.PUR_B	-	
I³C 2						
C16	I2C_2_SDA	ENET1_MDIO	ALT2	I3C2.SDA	I3C2	Additional I3C2 port
C17	I2C_2_SCL	ENET1_MDC	ALT2	I3C2.SCL	I3C2	
A05	SD_1_CLK	SD2_CLK	ALT2	I3C2.SDA	I3C2	
A01	SD_1_CD#	SD2_CD_B	ALT2	I3C2.SCL	I3C2	
A06	SD_1_CMD	SD2_CMD	ALT2	I3C2.PUR	-	Control of pull-up resistors on the I3C2 bus lines
A06	SD_1_CMD	SD2_CMD	ALT3	I3C2.PUR_B	-	

Table 39 shows the addresses of the on-board I²C components.

Table 39: I²C addresses

Component	Part Number	SoC function names	I ² C Address
Buck Converter A	MPF5302AMMAAES	GPIO_IO28/GPIO_IO29	0x29
Buck Converter B	MPF5301AMMABES	GPIO_IO28/GPIO_IO29	0x2A
DisplayPort Bridge	SN65DSI86ZXHR	GPIO_IO28/GPIO_IO29	0x2C
EEPROM	M24C02-FMC6TG	GPIO_IO28/GPIO_IO29	0x50
GPIO Expander A	PCAL6416AHF	GPIO_IO28/GPIO_IO29	0x21
GPIO Expander B	PCAL6408AHKX	GPIO_IO28/GPIO_IO29	0x20
Power Management IC (PMIC)	MPF0900AMBA1ES	I2C1_SCL/I2C1_SDA	0x08
Real-Time Clock (RTC)	RX8130CE:B3	GPIO_IO28/GPIO_IO29	0x32
Temperature Sensor	TMP1075	GPIO_IO28/GPIO_IO29	0x48

5.8.1 EEPROM

The Aquila iMX95 integrates the M24C02-FMC6TG EEPROM, a 2kB (256 x 8-bit) electrically erasable programmable memory device. This EEPROM uses a standard I²C interface for communication. Packaged in an UDFDN-8 form factor (2 mm x 3 mm), it supports an operating temperature range of -40°C to +85°C.

Key electrical characteristics include:

- a supply voltage of 3.3 V (inside the admissible range of 1.7 V to 5.5 V),
- low active current consumption typically around 4 mA, and

- a standby current below 1 μA , enabling energy-efficient operation.

The device guarantees endurance of 4,000,000 write cycles and data retention of over 200 years, ensuring long-term reliability for configuration data, calibration parameters, or system logs. The M24C02-FMC6TG is ideal for non-volatile memory storage in systems requiring low power and robust performance.

5.8.2 Real-Time Clock (RTC)

The Aquila iMX95 module features an Real-Time Clock (RTC) IC on the module. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for timekeeping. When the main power supply is available, the RTC is powered from that rail. However, to retain RTC functionality when the main power is off, a coin cell must be connected to the VCC_BACKUP supply pin (pin B100).

While the module's main voltage is available, the onboard RTC can recharge a supercapacitor or rechargeable battery via the VCC_BACKUP pin. The available charging current is very low ($<500 \mu\text{A}$ at 3 V). If higher charging current is required, an external charging circuit can be implemented on the carrier board.



When using the RTC's recharging capability, a current-limiting resistor of at least 47 k Ω must be placed between the battery and the VCC_BACKUP pin. **Using a lower resistance may prevent the module from booting.**

5.8.3 Temperature Sensor

The Aquila iMX95 uses the TMP1075 digital local temperature sensor for precise monitoring of PCB temperatures within the range of -55°C to 125°C . It communicates via an I²C interface, enabling integration with the module's microcontroller. The sensor features low power consumption, operates at a supply voltage of 3.3V (inside the range of 2.7 V to 5.5 V that can be used by the temperature sensor module), and provides high accuracy with minimal temperature offset and drift.

Alternate parts:

- OnSemi NCT75MNR2G
- OnSemi NCT375MNR2G

5.9 JTAG

The JTAG interface, designated as "Always Compatible," is generally not required for programming modules within the Aquila family. However, it remains a valuable tool for in-depth debugging of the Arm[®] Cortex[®]-M7 core and advanced diagnostics of the Arm[®] Cortex[®]-A cores.

The i.MX 95 SoC does not include a dedicated JTAG reset input (JTAG_TRST#). Contrary to some implementations, the TRST# pin on the module board-to-board connector is not connected internally to the module's reset signal (RESET_MOCI#) or any other reset line. Therefore, asserting TRST# affects only the JTAG TAP state machine without triggering a full system reset.

For runtime console access and debug purposes, UART_3 is typically used for the main CPUs' (Arm[®] Cortex[®]-A55) console, while UART_4 is dedicated to debugging the real-time MCU cores (Arm[®] Cortex[®]-M7 and Arm[®] Cortex[®]-M33).



Instead of relying on the JTAG port, the module can be reprogrammed using Recovery Mode over the USB interface. For reliable flashing and debugging via Recovery Mode, it is strongly recommended to keep the USB_1 interface accessible, even if it is not used during regular production operation.

Table 40: JTAG pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C07	JTAG_1_TRST#	-	-	-	-	Not connected
C08	JTAG_1_TDI	DAP_TDI	ALT0	DAP_TDI	I ¹	Test Data In
C10	JTAG_1_TDO	DAP_TDO_TRACESWO	ALT0	DAP_TDO_TRACESWO	O ¹	Test Data Out
C11	JTAG_1_TCK	DAP_TCLK_SWCLK	ALT0	DAP_TCLK_SWCLK	I ¹	Test Clock
C12	JTAG_1_VREF	-	-	-	O	1.8V output reference for the debugger
C13	JTAG_1_TMS	DAP_TMS_SWDIO	ALT0	DAP_TMS_SWDIO	I ¹	Test Mode Select

¹ From the perspective of the SoM.

5.10 MIPI CSI – MIPI Camera Serial Interface

The Aquila iMX95 supports one quad-lane MIPI CSI interface. The interface is fully compatible with single, dual, and quad-lane CSI camera configurations. The physical layer employed is the MIPI D-PHY specification version 1.2, ensuring high-speed, low-power serial data transmission. When the Display Serial Interface (DSI) is utilized, only one CSI interface remains active, as the DSI shares the Combo Rx/Tx D-PHY with the second CSI-2 host controller, mapping both within the Camera domain.

Ten GPIOs are reserved for the MIPI CSI camera interfaces (four for each interface, and additional two for control lines). Details are available in [Table 35](#).



The second CSI interface configuration is an assembly option that requires the correct module NPI. Modules equipped with the DisplayPort (DP) bridge feature are not eligible for the second CSI interface. Please verify the module configuration at the time of purchase to ensure the availability of the second CSI interface.

Features

Key features include scalable lane configurations from one to four data lanes, with data rates up to 5 Gbps per lane. This supports high-definition video capture scenarios such as 4Kp60 fps on a single CSI interface, dual 4Kp30 fps streams, two 1080p60 fps cameras, or up to four 1080p30 fps cameras utilizing MIPI virtual channel multiplexing. The interface adheres to the MIPI Alliance CSI-2 Version 2.1 standard and supports unidirectional master operation. A broad range of image formats is supported, including YUV420 (8-bit and 10-bit), YUV422 (8-bit and 10-bit), multiple RGB formats (444, 555, 565, 666, 888), and RAW formats with bit depths from 6 to 20 bits. User-defined byte-based data packets and generic 8-bit long packet types are also supported, providing extensive protocol flexibility.

Table 41: MIPI CSI1 interface

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	I/O	Description
A22	CSI_1_CLK_P	MIPI_CSI1_CLK_P	- ¹	I	Positive differential CSI interface clock signal
A23	CSI_1_CLK_N	MIPI_CSI1_CLK_N	- ¹	I	Negative differential CSI interface clock signal
A28	CSI_1_D0_P	MIPI_CSI1_D0_P	- ¹	I	Positive differential CSI interface data signal, lane 0
A29	CSI_1_D0_N	MIPI_CSI1_D0_N	- ¹	I	Negative differential CSI interface data signal, lane 0
A25	CSI_1_D1_P	MIPI_CSI1_D1_P	- ¹	I	Positive differential CSI interface data signal, lane 1
A26	CSI_1_D1_N	MIPI_CSI1_D1_N	- ¹	I	Negative differential CSI interface data signal, lane 1

Continued on next page

Table 41: MIPI CSI1 interface (Continued)

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	I/O	Description
A19	CSI_1_D2_P	MIPI_CSI1_D2_P	- ¹	I	Positive differential CSI interface data signal, lane 2
A20	CSI_1_D2_N	MIPI_CSI1_D2_N	- ¹	I	Negative differential CSI interface data signal, lane 2
A16	CSI_1_D3_P	MIPI_CSI1_D3_P	- ¹	I	Positive differential CSI interface data signal, lane 3
A17	CSI_1_D3_N	MIPI_CSI1_D3_N	- ¹	I	Negative differential CSI interface data signal, lane 3

¹ Dedicated to the MIPI CSI interface and does not support alternate functions.

Table 42: MIPI CSI2 interface

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	I/O	Description
B08	CSI_2_CLK_P	MIPI_DSICSI1_CLK_P	- ¹	O	Positive differential CSI Interface clock
B09	CSI_2_CLK_N	MIPI_DSICSI1_CLK_N	- ¹	O	Negative differential CSI Interface clock
B14	CSI_2_D0_P	MIPI_DSICSI1_D0_P	- ¹	I	Positive differential CSI Interface data lane 0
B15	CSI_2_D0_N	MIPI_DSICSI1_D0_N	- ¹	I	Negative differential CSI Interface data lane 0
B11	CSI_2_D1_P	MIPI_DSICSI1_D1_P	- ¹	I	Positive differential CSI Interface data lane 1
B12	CSI_2_D1_N	MIPI_DSICSI1_D1_N	- ¹	I	Negative differential CSI Interface data lane 1
B05	CSI_2_D2_P	MIPI_DSICSI1_D2_P	- ¹	I	Positive differential CSI Interface data lane 2
B06	CSI_2_D2_N	MIPI_DSICSI1_D2_N	- ¹	I	Negative differential CSI Interface data lane 2
B02	CSI_2_D3_P	MIPI_DSICSI1_D3_P	- ¹	I	Positive differential CSI Interface data lane 3
B03	CSI_2_D3_N	MIPI_DSICSI1_D3_N	- ¹	I	Negative differential CSI Interface data lane 3

¹ Dedicated to the MIPI CSI/DSI interfaces and does not support alternate functions.

In addition to the MIPI CSI-2 interface pins, the Aquila offers a dedicated I²C interface for the camera.

Table 43: Additional CSI interface signals

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	I/O	Remarks
C05	I2C_5_CSI2_SDA	GPIO_IO12	-	I/O	Control signal
C06	I2C_5_CSI2_SCL	GPIO_IO13	-	I/O	Control signal

5.11 PCI Express

The NXP i.MX 95 SoC incorporates two single-lane PCI Express (PCIe) interfaces, fully compliant with the PCIe 3.0 base specification. Each PCIe lane supports data rates up to 8 Gb/s (Gen3), providing high-speed connectivity for peripheral devices. The interface maintains backward compatibility with PCIe Gen2 (5 Gb/s) and Gen1 (2.5 Gb/s) standards to ensure broad interoperability with a wide range of PCIe devices.

A 100 MHz PCIe reference clock is internally generated by the SoC and made available to peripherals via dedicated pins on the module's board-to-board connector. All necessary source terminations and clock signal conditioning components are provided on the Aquila module to facilitate robust signal integrity and reliable operation.

Due to the high-speed nature of PCIe signaling, careful attention to layout and design practices is critical. Users are strongly advised to consult the Aquila Carrier Board Design Guide and Layout Design Guide for detailed recommendations and requirements to ensure optimal PCIe interface performance.

Table 44: PCIe 1 interface signals

X1 pin	Aquila signal name	SoC function name	SoC alternate function	I/O	Description
C47 ¹	PCIE1_REF_PAD_CLK_N	PCIE1_REF_PAD_CLK_N	- ²	O	Negative differential 100MHz reference clock signal Sourced by a reference clock oscillator
C46 ¹	PCIE1_REF_PAD_CLK_P	PCIE1_REF_PAD_CLK_P	- ²	O	Positive differential 100MHz reference clock signal Sourced by a reference clock oscillator
C41	PCIE_1_L0_RX_N	PCIE1_RX0_N	- ²	I	Negative differential receive data signal, lane 0
C40	PCIE_1_L0_RX_P	PCIE1_RX0_P	- ²	I	Positive differential receive data signal, lane 0
D40	PCIE_1_L0_TX_N	PCIE1_TX0_N	- ²	O	Negative differential transmit data signal, lane 0
D39	PCIE_1_L0_TX_P	PCIE1_TX0_P	- ²	O	Positive differential transmit data signal, lane 0
-	PCIE_1_RESET#	-	- ²	O	Dedicated reset output for PCIe connected on the P0 pin of the GPIO Expander B

¹ Module Specific pin with 10 kΩ pull-down resistor.

² Dedicated to the PCI Express interface and does not support alternate functions.

For modules that do not feature the Wi-Fi/Bluetooth module, a second PCIe interface is present. [Table 45](#) present the PCIe 2 interface pins on the X1 connector.

Table 45: PCIe 2 interface signals

X1 pin	Aquila signal name	SoC ball name	SoC function name	I/O	Description
C50	PCIE2_REF_PAD_CLK_N	A33 ¹	PCIE2_REF_PAD_CLK_N	O	Negative differential 100 MHz reference clock signal sourced by a reference clock oscillator
C49	PCIE2_REF_PAD_CLK_P	B32 ¹	PCIE2_REF_PAD_CLK_P	O	Positive differential 100 MHz reference clock signal sourced by a reference clock oscillator
C29	PCIE_2_L0_RX_N	C35	PCIE2_RX0_N	I	Negative differential receive data signal, lane 0
C28	PCIE_2_L0_RX_P	B34	PCIE2_RX0_P	I	Positive differential receive data signal, lane 0
D31	PCIE_2_L0_TX_N	F32	PCIE2_TX0_N	O	Negative differential transmit data signal, lane 0
D30	PCIE_2_L0_TX_P	E31	PCIE2_TX0_P	O	Positive differential transmit data signal, lane 0
C35	PCIE_2_RESET#	- ²	-	O	Dedicated reset output for PCIe Connected on the P0 pin of the GPIO Expander B.
D27	PCIE_2_CLK_X1_P	- ³	-	O	Positive differential 100 MHz reference clock signal sourced by a reference clock oscillator
D28	PCIE_2_CLK_X1_N	- ³	-	O	Negative differential 100 MHz reference clock signal sourced by a reference clock oscillator

¹ Module Specific pin with 10 kΩ pull-down resistor.

² Connected through GPIO Expander B (PCAL6408AHKX).

³ Connected through clock generator/buffer (LMKDB1102REYR).

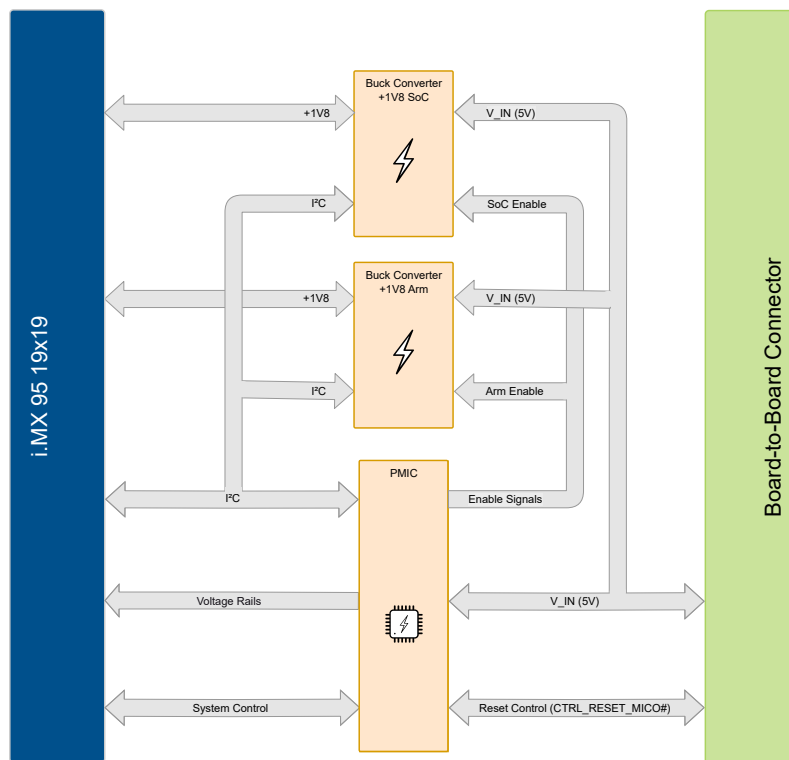
5.12 Power Supply

All Aquila modules are powered by a single voltage VCC and an optional low-current backup power supply for purposes such as Real Time Clock (RTC) support. The main power supply offers an input voltage of 5V ±5%. The Aquila form factor is specified for a maximum sustained power consumption

of up to 26W and a maximum peak power consumption of up to 40W for the SoMs. Most of the GPIO-capable I/O pins run on a 1.8V logic level. The Aquila module provides a reference 1.8V output for the I/O rails (PWR_1V8_MOCI). The module provides up to 250mA on this pin. Carrier boards may use this module output rail directly as the only 1.8V supply for their peripherals. This saves complexity and costs on the carrier board. The carrier board needs to ensure that the maximum amount of current drawn from the PWR_1V8_MOCI output pin does not exceed 250mA. Drawing a higher current can lead to instability and damage to the module power supply.

The block diagram of the Power Supply for the Aquila iMX95 and its main signals are depicted on [Figure 4](#).

Figure 4: Power supply block diagram



5.12.1 Digital Supply

The carrier board is responsible for supplying power to the Aquila iMX95 module via the X1 connector. The SoM integrates a MPF0900AMBA1ES Power Management IC (PMIC), which coordinates power distribution across the module. This PMIC, in conjunction with a combination of switched-mode and linear voltage regulators, manages and regulates the various power rails required by the SoM to ensure stable and optimized operation.

Table 46: Power pins

X1 pin	Aquila signal name	I/O	Description	Remarks
B97, B98, B99, C96, C97, C98, C99, C100, D95, D96, D97, D98, D99, D100	VCC	I	4.75V to 5.25V main power supply. 5.00V ± 5%.	Use decoupling capacitors on the carrier board ¹
A4, A9, A15, A18, A21, A24, A27, A30, A33, A36, A39, A42, A45, A48, A51, A57, A60, A63, A66, A69, A72, A75, A78, A81, A84, A87, A90, A93, A96 B1, B4, B7, B10, B13, B16, B25, B30, B39, B47, B52, B64, B69, B82, B85, B88 C9, C27, C30, C33, C39, C42, C45, C48, C51, C54, C57, C60, C63, C66, C69, C72, C75, C78, C81, C84, C87, C90, C93 D13, D18, D26, D29, D32, D35, D38, D41, D44, D47, D50, D53, D56, D59, D62, D65, D68, D71, D74, D77, D80, D83, D86, D89, D92	GND	I	Digital Ground.	
B100	VCC_BACKUP	I	RTC Power supply can be connected to a backup battery.	Can be left unconnected if the internal RTC is not used. VCC, not VCC_BACKUP, powers the SNVS supplies of the SoC

¹ Refer to the Aquila Design Guide.

5.12.2 Power Management Signals

The power management signals allow the carrier board to power on/off, reset, and wake up the module, and may force the module into recovery mode. The signals also indicate to the carrier board when to power off the main power rail and peripherals.

When the RSTB signal is asserted low, the PMIC initiates an orderly power-down sequence, followed by a power-up sequence upon release of the CTRL_RESET_MICO# signal, which may be left floating if unused. The module includes a dedicated power button input (CTRL_PWR_BTN_MICO#) connected directly to the SoC's ONOFF pin. A short press (<5 seconds) triggers power-up if the module is off or generates an interrupt if running—behavior contingent on the operating system—while a long press (>5 seconds) forces a power-down sequence regardless of OS state. To guarantee automatic boot, a pulse generator on the module simulates a short power button press upon main power rail application.

Power rails for the onboard Ethernet PHY can be fully disabled to save power, with the INT/PWDN input functioning as an interrupt controlled by the ETH_1_INT# signal. The Wi-Fi module's power rails are not independently switchable but include a power-down pin activated by asserting WL_EN and W_DISABLE2_L low, which reduces current consumption to approximately 0.6 mA. The Wi-Fi module features an internal power-on reset and requires firmware download after each power-up cycle. The PCIe reset input is driven by a GPIO expander and resets the entire Wi-Fi. The CTRL_FORCE_OFF_MOCI# signal, generated by the PMIC to disable the main power rail, is delayed by approximately 1.5 seconds after power off to prevent premature assertion during reset cycles; this delay may vary based on module and temperature conditions.

Table 47: Power management pins

X1 pin	Aquila signal name	I/O	Type	Remarks
B91	CTRL_RECOVERY_MICO#	I	OD 1.8V	Shorting the pin to ground during power-up puts the module into recovery mode. The module includes a 10 kΩ pull-up resistor, so the pin can be left floating on the carrier board
B92	CTRL_RESET_MICO#	I	OD 1.8V	Open-drain input. It resets the module when pulled low on the carrier board. This module includes a 100 kΩ pull-up resistor to the 1.8 V BBSM rail. It can be left floating on the carrier board
B93	CTRL_PWR_BTN_MICO#	I	OD 1.8V	Pulling the pin low for a long duration shuts down the module, while a short pull-down turns on the module from the off state. The pin is an open-drain input with a 100 kΩ pull-up resistor to the 1.8 V BBSM rail on the module. It can be left floating on the carrier board
B94	CTRL_FORCE_OFF_MOCI#	O	OD 5V	Output used to force shutdown of the main power rail. Must be ignored for the first 400 ms of power-up. The signal is 5 V tolerant and can be pulled up to 1.8 V, 3.3 V, or 5 V by the carrier board. It can be left floating
B95	CTRL_PWR_EN_MOCI	O	1.8V	Enable signal for the power rails of carrier board peripherals. It remains high during sleep modes
D05	CTRL_RESET_MOCI# ¹	O	OD 3.3V	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# signal is not asserted. The output is open-drain and does not include a pull-up resistor on the module. The signal is 3.3 V tolerant, and the carrier board can pull it up to 1.8 V or 3.3 V. It can be left floating on the carrier board
D06	CTRL_WAKE1_MICO#	I	1.8V	Wake-capable pin that allows the system to resume from sleep mode. There are no pull resistors on the carrier board. The pin can be left floating if the wake feature is disabled in software. It functions as a regular SoC GPIO

¹ This signal is an open-drain signal without pull-up resistors on the module. Since the pin is 5V tolerant, the carrier board can pull it up to 1.8V, 3.3V, or 5V

5.12.3 I²C Addresses

The power management components, including the PMIC MPF0900AMBA1ES and the Buck converters MPF5301AMMABES and MPF5302AMMAAES, are interfaced via the SoC's I²C1 bus. This I²C bus is not connected to the board-to-board connector and is accessible only through the SoC.

- MPF0900AMBA1ES - I²C address 0×08
- MPF5301AMMABES - I²C address 0×2A
- MPF5302AMMAAES - I²C address 0×29

5.13 PWM

The NXP i.MX 95 SoC integrates six Timer/PWM Modules within the Always-On (AON) domain, each featuring a 32-bit counter and six channels, providing a total of 36 PWM-capable channels across the SoC. Each Timer/PWM pin supports a selectable prescaler with division factors of 1, 2, 4, 8, 16, 32, 64, or 128, and multiple PWM modes including Edge-Aligned PWM (EPWM), Center-Aligned PWM (CPWM), and Combined PWM with dead time insertion. Channels are individually configurable to operate as PWM outputs, input capture, or output compare functions, and support DMA requests and interrupts. The TPM modules operate efficiently in low-power and debug modes, with asynchronous clocking enabling continued timer operations during such states.



To prevent confusion with other acronyms, this datasheet uses the abbreviation TPM exclusively to denote the Trusted Platform Module. References to timer or PWM signals using TPM follow only the SoC manufacturer's original pin names or alternate functions. All other instances of TPM pertain strictly to the Trusted Platform Module.

The Aquila Standard includes four PWM signals:

- PWM_1 and PWM_2, classified as Always Compatible, serve as general-purpose PWM outputs;

- PWM_3_DSI and PWM_4_DP belong to the Reserved class, with PWM_3_DSI dedicated to MIPI DSI display backlight inverter control and PWM_4_DP assigned to DisplayPort backlight control.

Additionally, 17 other PWM outputs from the i.MX 95 are available via alternate functions. It is therefore recommended to prioritize usage of the dedicated PWM pins over PWM_4_DP for maximum compatibility across different Aquila modules.

Table 48: Always compatible PWM pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM in controller mode</i>	Description
C25	PWM_1	GPIO_IO24	ALT4	TPM3_CH3	I	General Purpose PWM
C26	PWM_2	GPIO_IO08	ALT4	TPM3_CH0	O	General Purpose PWM

Table 49: Reserved PWM pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O <i>SoM in controller mode</i>	Description
B46	PWM_3_DSI ¹	GPIO_IO06	ALT1	TPM5_CH0	I	General Purpose PWM
B58	PWM_4_DP ¹	GPIO_IO26	ALT4	TPM5_CH3	O	General Purpose PWM

¹ These two PWM pins share the same timer module (TPM5/PWM5), requiring them to operate at the same frequency.

The additional PWM signals are not guaranteed to be pin-compatible with other Aquila modules.

Table 50: Additional PWM pins

X1 pin	Aquila specification signal name	SoC ball name	Soc alternate function	SoC alternate function name	I/O	Description/Remarks
PWM1						
B49	CAN_1_RX	PDM_BIT_STREAM0	ALT3	TPM1_EXTCLK	I	External clock input for PWM1
D19	UART_3_RXD	UART1_RXD	ALT3	TPM1_CH0	I/O	Channel 0
D20	UART_3_TXD	UART1_TXD	ALT3	TPM1_CH1	O	Channel 1 ¹
D21	UART_4_RXD	UART2_RXD	ALT3	TPM1_CH2	I/O	Channel 2
D22	UART_4_TXD	UART2_TXD	ALT3	TPM1_CH3	O	Channel 3 ¹
PWM2						
C24	GPIO_08	PDM_BIT_STREAM1	ALT3	TPM2_EXTCLK	I	External clock input for PWM2
-	PMIC_I2C_SCL	I2C1_SCL	ALT3	TPM2_CH0	-	Not connected to X1 pins
-	PMIC_I2C_SDA	I2C1_SDA	ALT3	TPM2_CH1	-	
D08	I2C_1_SCL	I2C2_SCL	ALT3	TPM2_CH2		Channel 2
D07	I2C_1_SDA	I2C2_SDA	ALT3	TPM2_CH3		Channel 3
PWM3						
B43	GPIO_18_DSI_1	GPIO_IO09	ALT4	TPM3_EXTCLK	I	External clock input for PWM3
B55	CAN_4_TX	GPIO_IO04	ALT1	TPM3_CH0	I/O	Channel 0

Continued on next page

Table 50: Additional PWM pins (Continued)

X1 pin	Aquila specification signal name	SoC ball name	Soc alternate function	SoC alternate function name	I/O	Description/Remarks
D17	SPI_2_MOSI	GPIO_IO20	ALT6	TPM3_CH1	I/O	Channel 1
B40/C05	I2C_3/5_DSI1/CSI2_SDA	GPIO_IO12	ALT1	TPM3_CH2	I/O	Channel 2
PWM4						
B32	UART_2_CTS	GPIO_IO10	ALT4	TPM4_EXTCLK	I	External clock input for PWM4
B56	CAN_4_RX	GPIO_IO05	ALT1	TPM4_CH0	I/O	Channel 0
D14	SPI_2_CLK	GPIO_IO21	ALT6	TPM4_CH1	I/O	Channel 1
B41/C06	I2C_3/5_DSI1/CSI2_SCL	GPIO_IO13	ALT1	TPM4_CH2	I/O	Channel 2
B50	CAN_2_TX	GPIO_IO25	ALT4	TPM4_CH3	I/O	Channel 3
PWM5						
B34	UART_2_RTS	GPIO_IO11	ALT4	TPM5_EXTCLK	I	External clock input for PWM5
C18	I2C_6_SDA	GPIO_IO22	ALT4	TPM5_CH1	I/O	Channel 1
D16	SPI_2_CS	GPIO_IO18	ALT6	TPM5_CH2	I/O	Channel 2
PWM6						
C18	I2C_6_SDA	GPIO_IO22	ALT5	TPM6_EXTCLK	I	External clock input for PWM6
C19	I2C_6_SCL	GPIO_IO23	ALT4	TPM6_CH1	I/O	Channel 1
D15	SPI_2_MISO	GPIO_IO19	ALT6	TPM6_CH2	I/O	Channel 2
B51	CAN_2_RX	GPIO_IO27	ALT4	TPM6_CH3	I/O	Channel 3

¹ This pin also functions as a strapping pin and must be used with caution to avoid unintended configuration or behavior during module initialization.

5.14 SPI

The NXP i.MX 95 SoC includes six SPI interfaces, referred to as Enhanced Configurable Serial Peripheral Interfaces (ECSPI) in NXP documentation:

- 1x Always Compatible (One SPI interface is available on the Aquila module as an Always Compatible interface)
- 1x Reserved (One SPI interface is available on the Aquila module as a Reserved interface)
- 4x Module Specific / Alternate function (The other four SPI interfaces are available as alternate functions on other interface pins)

The LPSPI_1 and LPSPI_2 instances are part of the Always-On domain, meaning they remain powered even in low-power modes. These instances **support only controller mode and cannot operate as peripherals**. The remaining SPI instances belong to the Wakeup domain, which allows them to be reactivated by events during low-power states. These instances **support both controller and peripheral modes**.

Both the Always Compatible and Reserved SPI interfaces feature a single chip select pin. The Always Compatible port supports up to 60 Mbps in master write mode and up to 30 Mbps in master read mode, while maximum speeds on other instances may be lower. These full-duplex synchronous serial interfaces enable robust communication between the Aquila module and connected peripherals. Users should consult the NXP i.MX 95 datasheet for detailed electrical and timing specifications.

Table 51: Always compatible SPI pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D09	SPI_1_CS	GPIO_IO00	ALT4	SPI6_PCS0	O	Peripheral select
D10	SPI_1_MISO	GPIO_IO01	ALT4	SPI6_SIN	I	Controller input, peripheral output
D11	SPI_1_MOSI	GPIO_IO02	ALT4	SPI6_SOUT	O	Controller output, peripheral input
D12	SPI_1_CLK	GPIO_IO03	ALT4	SPI6_SCK	O	Serial clock

Table 52: SPI reserved pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D16	SPI_2_CS	GPIO_IO18	ALT4	SPI5_PCS0	O	Peripheral select
D15	SPI_2_MISO	GPIO_IO19	ALT4	SPI5_SIN	I	Controller input, peripheral output
D17	SPI_2_MOSI	GPIO_IO20	ALT4	SPI5_SOUT	O	Controller output, peripheral input
D14	SPI_2_CLK	GPIO_IO21	ALT4	SPI5_SCK	O	Serial clock

Table 53: SPI signals available as alternate functions

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
SPI1						
B17	GPIO_09_CSL1	SAI1_TXC	ALT2	SPI1_SIN	I	Controller input, peripheral output
B18	GPIO_10_CSL1	SAI1_RXD0	ALT2	SPI1_SOUT	O	Controller output, peripheral input
B49	CAN_1_RX	PDM_BIT_STREAM0	ALT2	SPI1_PCS1	O	Peripheral select 1
SPI2						
C24	GPIO_08	PDM_BIT_STREAM1	ALT2	SPI2_PCS1	O	Peripheral select 1
D19	UART_3_RXD	UART1_RXD	ALT2	SPI2_SIN	I	Controller input, peripheral output
D20	UART_3_TXD	UART1_TXD	ALT2	SPI2_PCS0	O	Peripheral select 0
D21	UART_4_RXD	UART2_RXD	ALT2	SPI2_SOUT	O	Controller output, peripheral input
D22	UART_4_TXD	UART2_TXD	ALT2	SPI2_SCK	O	Serial clock
SPI3						
B32	UART_2_CTS	GPIO_IO10	ALT1	SPI3_SOUT	O	Controller output, peripheral input
B34	UART_2_RTS	GPIO_IO11	ALT1	SPI3_SCK	O	Serial clock
B42	GPIO_17_DSI_1	GPIO_IO07	ALT1	SPI3_PCS1	O	Peripheral select 1
B43	GPIO_18_DSI_1	GPIO_IO09	ALT1	SPI3_SIN	I	Controller input, peripheral output
C26	PWM_2	GPIO_IO08	ALT1	SPI3_PCS0	O	Peripheral select 0
SPI4						
B36	UART_1_CTS	GPIO_IO16	ALT5	SPI4_PCS2	O	Peripheral select 2
B38	UART_1_RTS	GPIO_IO17	ALT5	SPI4_PCS1	O	Peripheral select 1
B44	GPIO_19_DSI_1	GPIO_IO33	ALT5	SPI4_PCS1	O	Peripheral select 1
B45	TSP_26	GPIO_IO34	ALT5	SPI4_PCS0	O	Peripheral select 0

Continued on next page

Table 53: SPI signals available as alternate functions (Continued)

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C37	PCIE_1_CLKREQ#	GPIO_IO32	ALT4	SPI4_PCS2	O	Peripheral select 2
D14	SPI_2_CLK	GPIO_IO21	ALT5	SPI4_SCK	O	Serial clock
D15	SPI_2_MISO	GPIO_IO19	ALT5	SPI4_SIN	I	Controller input, peripheral output
D16	SPI_2_CS	GPIO_IO18	ALT5	SPI4_PCS0	O	Peripheral select 0
D17	SPI_2_MOSI	GPIO_IO20	ALT5	SPI4_SOUT	O	Controller output, peripheral input
SPI5						
B51	CAN_2_RX	GPIO_IO27	ALT6	SPI5_PCS1	O	Peripheral select 1
D14	SPI_2_CLK	GPIO_IO21	ALT4	SPI5_SCK	O	Serial clock
D15	SPI_2_MISO	GPIO_IO19	ALT4	SPI5_SIN	I	Controller input, peripheral output
D16	SPI_2_CS	GPIO_IO18	ALT4	SPI5_PCS0	O	Peripheral select 0
D17	SPI_2_MOSI	GPIO_IO20	ALT4	SPI5_SOUT	O	Controller output, peripheral input
SPI6						
C25	PWM_1	GPIO_IO24	ALT6	SPI6_PCS1	O	Peripheral select 1
D09	SPI_1_CS	GPIO_IO00	ALT4	SPI6_PCS0	O	Peripheral select 0
D10	SPI_1_MISO	GPIO_IO01	ALT4	SPI6_SIN	O	Controller input, peripheral output
D11	SPI_1_MOSI	GPIO_IO02	ALT4	SPI6_SOUT	O	Controller output, peripheral input
D12	SPI_1_CLK	GPIO_IO03	ALT4	SPI6_SCK	O	Serial clock
SPI7						
B42	GPIO_17_DSI_1	GPIO_IO07	ALT4	SPI7_SCK	O	Serial clock
B46	PWM_3_DSI	GPIO_IO06	ALT4	SPI7_SOUT	O	Controller output, peripheral input
B50	CAN_2_TX	GPIO_IO25	ALT6	SPI7_PCS1	O	Peripheral select 1
B55	CAN_4_TX	GPIO_IO04	ALT4	SPI7_PCS0	O	Peripheral select 0
B56	CAN_4_RX	GPIO_IO05	ALT4	SPI7_SIN	I	Controller input, peripheral output
SPI8						
B35	UART_1_RXD	GPIO_IO15	ALT4	SPI8_SCK	O	Serial clock.
B37	UART_1_TXD	GPIO_IO14	ALT4	SPI8_SOUT	O	Controller output, peripheral input
B40/C05	I2C_3/5_DSI1/CSI2_SDA	GPIO_IO12	ALT4	SPI8_PCS0	O	Peripheral select 0
B41/C06	I2C_3/5_DSI1/CSI2_SCL	GPIO_IO13	ALT4	SPI8_SIN	O	Controller input, peripheral output
B58	PWM_4_DP	GPIO_IO26	ALT6	SPI8_PCS1	O	Peripheral select 1

5.15 Trusted Platform Module (TPM)

The Aquila iMX95 SoM uses the ST33KTPM2I3WBZA9 Trusted Platform Module (TPM) delivering robust, hardware-based security functions in full compliance with the TPM 2.0 standard. It enables secure generation, storage, and management of cryptographic keys, facilitating trusted boot processes, platform integrity measurement, and strong authentication mechanisms to protect against unauthorized access and system tampering.

Supporting a comprehensive set of cryptographic algorithms including RSA, ECC, and SHA, the module ensures compatibility with a wide range of security protocols and applications. The module's design focuses on low power consumption and high reliability, making it well-suited for embedded, industrial, IoT, and edge computing environments where platform trustworthiness and data security are critical.

Additionally, the TPM features advanced tamper-resistance measures and secure cryptographic accelerators to safeguard sensitive operations against physical and logical attacks. Its integration simplifies the implementation of hardware-rooted security, enabling system designers to build secure systems that comply with industry standards and regulatory requirements.

The block diagram of the TPM and its main signals are depicted on [Figure 5](#).

Figure 5: Trusted Platform Module (TPM) block diagram

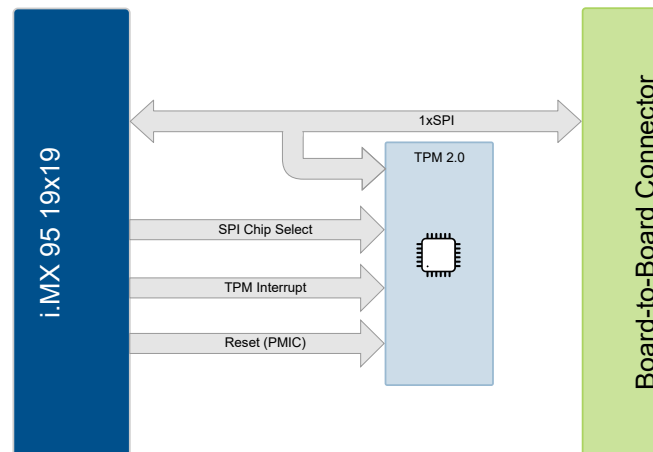


Table 54: TPM signals

Aquila specification signal name	TPM – QFN32 ball name	SoC ball name	Remarks
CTRL_TPM_INT#	SPI_PIRQ#/I2C_PIRQ#	–	Connected to P1_3 of the GPIO Expander A (PCAL6416AHF)
PMIC_RESET_1V8	SPI_RST#	–	Connected to the PMIC reset circuit
SPI_2_CS2_TPM	SPI_CS#	–	Connected to P1_4 of the GPIO Expander A (PCAL6416AHF)
SPI_2_MISO	MISO	GPIO_IO19	Board-to-Board connector pin D15
SPI_2_MOSI	MOSI	GPIO_IO20	Board-to-Board connector pin D17
SPI_2_CLK	SPI_CLK	GPIO_IO21	Board-to-Board connector pin D14

5.16 UART

The NXP i.MX 95 SoC includes eight UART interfaces, with the Aquila family specification providing access as follows:

- **UART_1 and UART_2:** General-purpose UARTs. The RX and TX signals are located in the Always Compatible section, while the RTS and CTS signals for hardware flow control reside in the Reserved section.
- **UART_3:** Located in the Always Compatible section, primarily intended as the main OS terminal debug port for the Arm® Cortex®-A55 cores. While reconfigurable for general use, it is recommended to reserve this interface for debugging.
- **UART_4:** In the Reserved section, generally dedicated to the real-time operating system running on the Cortex®-M7 core, but can also serve as a general-purpose UART.
- **Additional four UARTs:** Available only as alternate functions of other pins. These are not module-specific signals and may have limited compatibility.

The UART interfaces provide serial communication supporting full-duplex operation with standard NRZ format and programmable baud rates independent of the bus clock. They feature interrupt handling, hardware parity, receiver wake-up and address-matching capabilities for data exchange.

UART Features

- Programmable baud rates with 13-bit modulo divider and oversampling ratio from 4× to 32×, supporting asynchronous operation and low-power modes.
- Multiple interrupt sources including transmit empty, receive full, parity/framing/noise errors, break detection (LIN), and receiver wake-up methods.
- Hardware flow control support (RTS/CTS), configurable data character length, stop bits, independent FIFOs for transmit/receive with configurable watermarks, and optional IrDA RZI signaling.

Table 55: Always available UART pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
UART 1						
B35	UART_1_RX	GPIO_IO15	ALT1	UART3_RX	I	Receive data of general-purpose UART_1
B37	UART_1_TXD	GPIO_IO14	ALT1	UART3_TX	O	Transmit data of general-purpose UART_1
B38	UART_1_RTS	GPIO_IO17	ALT4	UART3_RTS_B	O	Request to Send of general-purpose UART_1
B36	UART_1_CTS	GPIO_IO16	ALT4	UART3_CTS_B	I	Clear to Send of general-purpose UART_1
UART 2						
B31	UART_2_RXD	GPIO_IO37	ALT2	UART7_RX	I	Receive data of general-purpose UART_2
B33	UART_2_TXD	GPIO_IO36	ALT2	UART7_TX	O	Transmit data of general-purpose UART_2
B34	UART_2_RTS	GPIO_IO11	ALT5	UART7_RTS_B	O	Request to Send of general-purpose UART_2
B32	UART_2_CTS	GPIO_IO10	ALT5	UART7_CTS_B	I	Clear to Send of general-purpose UART_2
UART 3						
D19	UART_3_RXD	UART1_RXD	ALT0	UART1_RX	I	Receive data of A55 debug UART_3
D20	UART_3_TXD	UART1_TXD	ALT0	UART1_TX	O	Transmit data of A55 debug UART_3

Table 56: Reserved UART pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D21	UART_4_RXD	UART2_RXD	ALT0	UART2_RX	I	Received Data of M7 debug UART_4
D22	UART_4_TXD	UART2_TXD	ALT0	UART2_TX	O	Transmitted Data of M7 debug UART_4

Table 57: UART additional pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
UART 1						
B17	GPIO_09_CSL_1	SAI1_TXC	ALT3	UART1_DSR_B	I	Indicates modem readiness to communicate, active low
D21	UART4_RXD	UART2_RXD	ALT1	UART1_CTS_B	O	Data set ready signal it is used by the peripheral to request data
UART 2						
B18	GPIO_10_CSL_1	SAI1_RXD0	ALT3	UART2_DSR_B	I	Indicates modem readiness to communicate, active low.
D07	I2C_1_SDA	I2C2_SDA	ALT2	UART2_RIN_B	I	Ring indicator signal it notifies of an incoming connection
D08	I2C_1_SCL	I2C2_SCL	ALT2	UART2_DCB_B	I	Data carrier detect signal it indicates the peripheral has received a valid signal
UART 3						
C16	I2C_2_SDA	ENET1_MDIO	ALT1	UART3_RIN_B	O	Ring indicator signal it notifies of an incoming connection
C17	I2C_2_SCL	ENET1_MDC	ALT1	UART3_DCB_B	I	Data carrier detect signal it indicates the peripheral has received a valid signal
B35	UART_1_RXD	GPIO_IO15	ALT1	UART3_RX	I	Receives data from the peripheral
B37	UART_1_TXD	GPIO_IO14	ALT1	UART3_TX	O	Transmits data to the peripheral
B36	UART_1_CTS	GPIO_IO16	ALT4	UART3_CTS_B	I	Data set ready signal it is used by the peripheral to request data
B38	UART_1_RTS	GPIO_IO17	ALT4	UART3_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data
UART 4						
B35	UART_1_RXD	GPIO_IO15	ALT6	UART4_RX	I	Transmits data to the peripheral
B37	UART_1_TXD	GPIO_IO14	ALT6	UART4_TX	O	Receives data from the peripheral
C20	GPIO_04	ENET_TD0	ALT1	UART4_TX	O	Receives data from the peripheral
B89	ETH_2_XGMII_MDIO	ENET2_MDIO	ALT1	UART4_RIN_B	O	Ring indicator signal it notifies of an incoming connection
B90	ETH_2_XGMII_MDC	ENET2_MDC	ALT1	UART4_DCB_B	I	Data carrier detect signal it indicates the peripheral has received a valid signal
B22	I2S_1_D_OUT	ENET2_RX_CTL	ALT1	UART4_DSR_B	I	Indicates modem readiness to communicate, active low
D23	GPIO_01	ENET2_RD0	ALT1	UART4_RX	I	Receives data from the peripheral
B36	UART_1_CTS	GPIO_IO16	ALT6	UART4_CTS_B	I	Data set ready signal it is used by the peripheral to request data
B21	I2S_1_SYNC	ENET2_TX_CTL	ALT1	UART4_DTR_B	O	Data terminal ready signal it indicates the host is ready to communicate
B38	UART_1_RTS	GPIO_IO17	ALT6	UART4_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data
C21	GPIO_05	ENET2_TD1	ALT1	UART4_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data

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Table 57: UART additional pins (Continued)

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
B24	I2S_1_MCLK	ENET2_RD2	ALT1	UART4_CTS_B	I	Data set ready signal it is used by the peripheral to request data
UART 5						
D09	SPI_1_CS	GPIO_IO00	ALT5	UART5_TX	O	Transmits data to the peripheral
D10	SPI_1_MISO	GPIO_IO01	ALT5	UART5_RX	I	Receives data from the peripheral
D11	SPI_1_MOSI	GPIO_IO02	ALT5	UART5_CTS_B	I	Data set ready signal it is used by the peripheral to request data
D12	SPI_1_CLK	GPIO_IO03	ALT5	UART5_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data
C13	JTAG_1_TMS	DAP_TMS_SWDIO	ALT6	UART5_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data
C08	JTAG_1_TDI	DAP_TDI	ALT6	UART5_RX	I	Receives data from the peripheral
C11	JTAG_1_TCK	DAP_TCLK_SWCLK	ALT6	UART5_CTS_B	I	Data set ready signal it is used by the peripheral to request data
C10	JTAG_1_TDO	DAP_TDO_TRACESWO	ALT6	UART5_TX	O	Transmits data to the peripheral
UART 6						
B56	CAN_4_RX	GPIO_IO05	ALT5	UART6_RX	I	Receives data from the peripheral
B55	CAN_4_TX	GPIO_IO04	ALT5	UART6_TX	O	Transmits data to the peripheral
B46	PWM_3_DSI	GPIO_IO06	ALT5	UART6_CTS_B	I	Data set ready signal it is used by the peripheral to request data
B42	GPIO_17_DSI_1	GPIO_IO07	ALT5	UART6_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data
C37	PCIE_1_CLKREQ#	GPIO_IO32	ALT2	UART6_TX	O	Transmits data to the peripheral
B44	GPIO_19_DSI_1	GPIO_IO33	ALT2	UART6_RX	I	Receives data from the peripheral
B45	GPIO_20_DSI_1	GPIO_IO34	ALT2	UART6_CTS_B	I	Data set ready signal it is used by the peripheral to request data
C34 ¹	PCIE_2_CLKREQ#	GPIO_IO35		UART6_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data
UART 7						
C26	PWM_2	GPIO_IO08	ALT5	UART7_TX	O	Transmits data to the peripheral
B43	GPIO_18_DSI_1	GPIO_IO09	ALT5	UART7_RX	I	Receives data from the peripheral
B32	UART_2_CTS	GPIO_IO10	ALT5	UART7_CTS_B	I	Data set ready signal it is used by the peripheral to request data
B34	UART_2_RTS	GPIO_IO11	ALT5	UART7_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data
B33	UART_2_TXD	GPIO_IO36	ALT2	UART7_TX	O	Transmits data to the peripheral
B31	UART_2_RXD	GPIO_IO37	ALT2	UART7_RX	I	Receives data from the peripheral
UART 8						
B40	I2C_3_DSI1_SDA	GPIO_IO12	ALT5	UART8_TX	O	Transmits data to the peripheral
C05	I2C_5_CSI2_SDA	GPIO_IO12	ALT5	UART8_TX	O	Transmits data to the peripheral
B41	I2C_3_DSI1_SCL	GPIO_IO13	ALT5	UART8_RX	I	Receives data from the peripheral

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Table 57: UART additional pins (Continued)

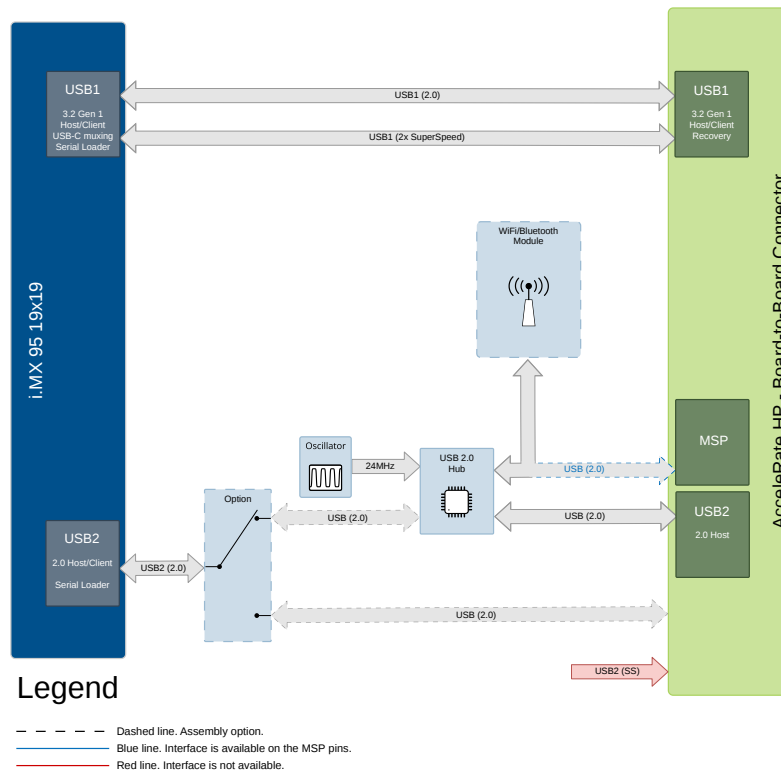
X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C06	I2C_5_CS12_SCL	GPIO_IO13	ALT5	UART8_RX	I	Receives data from the peripheral
B37	UART_1_TXD	GPIO_IO14	ALT5	UART8_CTS_B	I	Data set ready signal it is used by the peripheral to request data
B35	UART_1_RXD	GPIO_IO15	ALT5	UART8_RTS_B	O	Request To Send signal it is used by the host to indicate it wants to send data

¹ Available only on modules without Wi-Fi.

5.17 USB

The Aquila iMX95 module features two native USB ports: one USB Host port and one USB OTG (On-The-Go) port supporting both host and client modes. To expand connectivity, the module integrates a built-in USB hub (TUSB4020BIPHPR), increasing the total number of available USB ports. One of the USB 2.0 downstream ports of this hub is routed to support Bluetooth functionality within the integrated Wi-Fi + Bluetooth adapter. Figure 6 shows the block diagram of the Aquila iMX95 USB subsystem.

Figure 6: USB block diagram



In the Aquila standard:

- USB_1 is the OTG port, recommended for serial mode (recovery mode) usage. It supports SuperSpeed signals necessary for USB 3.1 Gen 1 operation; however, these SuperSpeed signals are available on module-specific pins, which may affect compatibility.
- USB_2 is a host-only port providing USB 2.0 speeds without SuperSpeed support.

Table 58: USB overview

Aquila USB port	Speed capabilities (SoC)	Role capabilities (SoC)	Speed according to Aquila standard	Role according to Aquila standard	Recovery mode
USB_1	USB 3.2 Gen 1	Host and client	USB 3.2 Gen 1	OTG (host and client)	Supported
USB_2	USB 2.0	Host	USB 2.0	Host only	Not supported

The i.MX 95 USB controller and PHY support USB Type-C with dual sets of SuperSpeed SerDes lanes (RX0/TX0 and RX1/TX1). The **first set (RX0/TX0) is guaranteed to be compatible** with other modules in the Aquila family supporting USB 3.2 Gen 1. The second set (RX1/TX1) is routed to module-specific pins, so compatibility with other modules is not guaranteed.

A built-in USB hub (TUSB4020BIPHR) expands connectivity by providing additional downstream ports. One of those ports is often used to carry the Bluetooth interface from an integrated Wi-Fi + Bluetooth adapter.

Table 59: USB1 interface pins

X1 pin	Aquila specification signal name	SoC ball name	SoC function name	I/O	Description
A70	USB_1_D_P	USB1_D_P	USB1_D_P	I/O	Positive differential USB Signal
A71	USB_1_D_N	USB1_D_N	USB1_D_N	I/O	Negative differential USB Signal
B76	USB_1_VBUS	USB1_VBUS	USB1_VBUS	I	Use this pin to detect if VBUS is present. This pin is a 5V input.
-	USB_1_ID	USB1_ID	USB1_ID	I	Use this pin to detect the ID pin if you use the port in OTG mode. This is a regular GPIO not connected
A61	USB_1_SSRX1_N	USB1_RX0_N	USB1_RX0_N	I	Negative differential receiving signal for USB SuperSpeed
A62	USB_1_SSRX1_P	USB1_RX0_P	USB1_RX0_P	I	Positive differential receiving signal for USB SuperSpeed
A64	USB_1_SSTX1_P	USB1_TX0_P	USB1_TX0_P	O	Positive differential transmission signal for USB SuperSpeed
A65	USB_1_SSTX1_N	USB1_TX0_N	USB1_TX0_N	O	Negative differential transmission signal for USB SuperSpeed
A74	USB_1_SSRX2_P	USB1_RX1_P	USB1_RX1_P	I	Positive differential receiving signal for USB SuperSpeed
A73	USB_1_SSRX2_N	USB1_RX1_N	USB1_RX1_N	I	Negative differential receiving signal for USB SuperSpeed
A76	USB_1_SSTX2_P	USB1_TX1_P	USB1_TX1_P	O	Positive differential transmission signal for USB SuperSpeed
A77	USB_1_SSTX2_N	USB1_TX1_N	USB1_TX1_N	O	Negative differential transmission signal for USB SuperSpeed
B74	USB_1_INT#	¹	-	I	Interrupt request signal.
B75	USB_1_OC#	¹	-	I	USB over-current, this pin can signal an over-current condition in the USB supply of the USB_1 interface
B77	USB_1_EN	²	-	O	This pin enables the external USB voltage supply for the USB_1 interface

¹ Available through the on-module GPIO Expander A (PCAL6416AHF).

² Available through the on-module GPIO Expander B (PCAL6408AHKX) and uses a pull-up resistor of 100 kΩ.

5.17.1 USB Hub

The TUSB4020BIPHR is available as an assembly option. It is a two-port USB 2.0 hub controller from Texas Instruments designed to expand a single USB port into multiple downstream ports. It supports high-speed (480 Mbps), full-speed, and low-speed USB data transfers, operating over an extended industrial temperature range (–40 °C to 85 °C). The device supports individual or grouped power switching and offers overcurrent protection for downstream ports, enhancing reliability and safety. Its integrated oscillator supports connection to a crystal or an external clock for precise timing.

Features:

- Two downstream USB 2.0 ports with high/full/low-speed support
- Multi-Transaction Translator (MTT) for simultaneous USB speeds
- Individual or ganged power switching with overcurrent protection
- USB Battery Charging 1.2 and Chinese Telecom charging (YD/T 1591-2009) support
- Industrial temperature range (-40 °C to 85 °C)
- Automatic charger detection and transparent BC/CDP/DCP modes
- Integrated oscillator with crystal or external clock input
- Wide supply voltage range (1.1 V and 3.3 V logic)
- RoHS compliant; suitable for consumer and industrial USB applications

5.18 uSDHC – Ultra Secured Digital Host Controller

The i.MX 95 SoC provides three SDIO interfaces:

- **SDIO 1:** Used internally for the eMMC flash.
- **SDIO 2:** Exposed on the module board-to-board connector as the Always Compatible Aquila SD® Memory Card Interface.
- **SDIO 3:** Used as GPIO and I2S pins.

Table 60: SDIO interfaces

SoC SDIO interface	Max bus width	Description
USDHC1	8-bit	Connected to the internal eMMC boot device. Not available on the module board-to-board connector
USDHC2	4-bit	Exposed as the Always Compatible Aquila SD® interface
USDHC3	4-bit	Used as GPIO and I2S interfaces. Including the CMD and CLK pins

Features:

- Supports SD Memory Card Specification versions 2.0 and 3.0
- Supports SDIO Card Specification versions 2.0 and 3.0
- Complies with MMC System Specification versions 4.2, 4.3, 4.4, 4.41, 5.0, and 5.1
- Supports addressing SD 3.0 and SDXC cards up to 2 TB capacity
- Supports SPI mode for legacy compatibility
- Supports SD UHS-I mode up to 208 MHz with 1.8 V I/O signaling
- Supports dual I/O voltage modes of 3.3 V and 1.8 V, with dynamic switching during initialization for UHS-I compliance
- The SD interface in the Always Compatible class supports both I/O voltage levels. No external pull-up resistors are required on the carrier board, as pull-up resistors are provided on the module.

The Aquila module's SD interface supports both 3.3 V and 1.8 V I/O voltage levels required for SD Memory Card compliance. The 3.3 V level is mandatory for standard SD card operation, while UHS-I class cards mandate support for 1.8 V signaling to achieve higher bus speeds. The interface can dynamically switch between these voltage levels during card initialization.

The Always Compatible SD interface supports dual I/O voltages and automatically switches to 1.8 V when operating in UHS-I mode. To meet SD specifications, the I/O signals default to 3.3 V but shift to 1.8 V for UHS-I operation. No external pull-up resistors are needed on the carrier board for the SDIO signals (CMD, DATA lines, and CLK) as these are integrated within the SoC or located on the module PCB.

Table 61: SDIO specification

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MB/s	3.3 V	SD Standard
High Speed	50 MHz	25 MB/s	3.3 V	SD Standard
SDR12	25 MHz	12.5 MB/s	1.8 V	UHS-I
SDR25	50 MHz	25 MB/s	1.8 V	UHS-I
DDR50	50 MHz (DDR)	50 MB/s	1.8 V	UHS-I
SDR50	100 MHz	50 MB/s	1.8 V	UHS-I
SDR104	208 MHz	104 MB/s	1.8 V	UHS-I

The SDIO power block I/O voltage on the Aquila iMX95 module can be independently configured from other I/O blocks, with all SDIO signals changing voltage levels simultaneously. The Always Compatible SD interface (USDHC2) I/O voltage is supplied by the PMIC's LDO2 output. Voltage selection is managed via the dedicated PMIC_SD_1_VSEL signal, controlled by the GPIO Expander A (PCAL6416AHF) on pin P1_1, which interfaces directly with the PMIC to switch between supported voltage levels seamlessly.

Table 62: SDIO Always available interface (USDHC2)

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
A01	SD_1_CD#	SD2_CD_B	ALT0	USDHC2_CD_B	I	Card detect
A05	SD_1_CLK	SD2_CLK	ALT0	USDHC2_CLK	O	Clock output
A07	SD_1_CMD	SD2_CMD	ALT0	USDHC2_CMD	I/O	SDIO command line
A03	SD_1_DATA0	SD2_DATA0	ALT0	USDHC2_DATA0	I/O	Data line 0
A02	SD_1_DATA1	SD2_DATA1	ALT0	USDHC2_DATA1	I/O	Data line 1
A10	SD_1_DATA2	SD2_DATA2	ALT0	USDHC2_DATA2	I/O	Data line 2
A08	SD_1_DATA3	SD2_DATA3	ALT0	USDHC2_DATA3	I/O	Data line 3
A06	SD_1_PWR_EN	SD2_RESET_B	ALT0	USDHC2_RESET_B	I	SD reset signal
A11	GPIO_11_CSI_1	SD2_VSELECT	ALT0	USDHC2_VSELECT	I	Voltage level control signal

Table 63: SDIO Available USDHC3 interface

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
B29	I2S_2_D_IN	SD3_CLK	ALT0	USDHC3_CLK	O	Clock output

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Table 63: SDIO Available USDHC3 interface (Continued)

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description ¹
B57	GPIO_21_DP	SD3_CMD	ALT0	USDHC3_CMD	I/O	SDIO command line
B19	GPIO_12_CSI_1	SD3_DATA0	ALT0	USDHC3_DATA0	I/O	Data line 0
B28	I2S_2_D_OUT	SD3_DATA1	ALT0	USDHC3_DATA1	I/O	Data line 1
B27	I2S_2_SYNC	SD3_DATA2	ALT0	USDHC3_DATA2	I/O	Data line 2
B26	I2S_2_BCLK	SD3_DATA3	ALT0	USDHC3_DATA3	I/O	Data line 3

¹ When used as SDIO (SD3) interface.

Table 64: SDIO available as alternate functions

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C18	I2C_6_SDA	GPIO_IO22	ALT1	USDHC3_CLK	O	Clock output
C19	I2C_6_SCL	GPIO_IO23	ALT1	USDHC3_CMD	I/O	SDIO command line
C25	PWM_1	GPIO_IO24	ALT1	USDHC3_DATA0	I/O	Data line 0
B50	CAN_2_TX	GPIO_IO25	ALT1	USDHC3_DATA1	I/O	Data line 1
B58	PWM_4_DP	GPIO_IO26	ALT1	USDHC3_DATA2	I/O	Data line 2
B51	CAN_2_RX	GPIO_IO27	ALT1	USDHC3_DATA3	I/O	Data line 3

¹ When used as SDIO (SD3) interface.

5.19 Wi-Fi and Bluetooth

The Aquila iMX95 is available with optional on-module Wi-Fi and Bluetooth interfaces. The Wi-Fi/Bluetooth module is connected via the PCIe2 interface for high-speed Wi-Fi data transfer, while the Bluetooth signals are routed separately through a USB interface. This separation occurs because it is common for Bluetooth protocols to use USB interfaces for their data and control signaling, which simplifies integration and ensures compatibility with standard Bluetooth stacks in operating systems. Additionally, routing Bluetooth over USB simplifies development and driver support, enabling simultaneous operation of Wi-Fi and Bluetooth functions without interference or bandwidth contention on the PCIe channel.



Assembly Options and Part Numbers

Please refer to [Section 1.8.1](#) for ensuring the correct assembly option for your application.

Features:

- Wi-Fi 7 IEEE 802.11a/b/g/n/ac/ax
- Dual-Band 5 GHz and 2.4 GHz
- 320 MHz channel bandwidth doubles capacity over Wi-Fi 6's 160 MHz channels
- 20/40/80 MHz channel bandwidth
- Supports simultaneous station, access point and P2P modes
- Bluetooth BR/EDR and Bluetooth Low Energy 5.3
- Dual antenna for simultaneous Wi-Fi and Bluetooth/802.15.4 operation

To save energy, the Wi-Fi and the Bluetooth capabilities can be disabled separately, using the signals WIFI_DISABLE# and BT_DISABLE#, respectively.

Table 65: Wi-Fi/Bluetooth interface to the SoC

Aquila specification signal name	SX-PCEAX-SMT-SP Pin name	SoC ball name	Remarks
Wi-Fi interface			
PCIE_WIFI_TX_P	HMT_PCIE_RXP0	PCIE2_TX0_P	
PCIE_WIFI_TX_N	HMT_PCIE_RXN0	PCIE2_TX0_N	
PCIE_WIFI_RX_P	HMT_PCIE_TXP0	PCIE2_RX0_P	
PCIE_WIFI_RX_N	HMT_PCIE_TXN0	PCIE2_RX0_N	
PCIE_REFCLK_WIFI_P	HMT_PCIE_REFCLKP	PCIE_REF_OUT_CLK_P	

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Table 65: Wi-Fi/Bluetooth interface to the SoC (Continued)

Aquila specification signal name	SX-PCEAX-SMT-SP Pin name	SoC ball name	Remarks
PCIE_REFCLK_WIFI_N	HMT_PCIE_REFCLKN	PCIE_REF_OUT_CLK_N	
PCIE_WAKE_WIFI#	PEWAKE0_L	- ¹	10 kΩ pull-up resistor
PCIE_2_CLKREQ#	CLKREQ0_L	GPIO_IO35	
PCIE_2_RESET#	PERST0_L	- ²	100 kΩ pull-down resistor
Bluetooth interface			
USB_WIFI_D_P	BT_USB_DP	- ³	
USB_WIFI_D_N	BT_USB_DM	- ³	
Control signals			
WIFI_DISABLE#	WL_EN	- ²	10 kΩ pull-up resistor
BT_DISABLE#	WL_DISABLE2_L	- ²	10 kΩ pull-up resistor

¹ Available through the on-module GPIO Expander A (PCAL6416AHF).

² Available through the on-module GPIO Expander B (PCAL6408AHKX).

³ Available through the on-module USB hub (TUSB4020BIPHPR).

The Aquila iMX95 module integrates Wi-Fi and Bluetooth functionality with dedicated control and wake signals as follows:

- **Enable Signals:** Two input signals, WIFI_DISABLE# and BT_DISABLE#, control the enablement of the Wi-Fi and Bluetooth radios respectively. Both signals are connected to 1.8 V and remain asserted by default, ensuring the radios are enabled continuously.
- **Wake-up Outputs:** Two wake output signals, WIFI_WAKEUP_HOST and WIFI_WAKE_BT, provide host wake-up capabilities for Wi-Fi and Bluetooth functions. These signals connect to the module pins BT_WAKEUP_HOST and WAKE_BT respectively and are exclusively routed through the board-to-board connector.
- **Firmware Dependency:** The availability and behavior of sleep and wake functions depend on the firmware loaded into the onboard u-blox Wi-Fi + Bluetooth module, affecting power management and host interaction.

Table 66 lists the Wi-Fi/Bluetooth interface signals accessible via the board-to-board connector.

Table 66: Wi-Fi/Bluetooth pins on board-to-board connector

X1 pin	Aquila function	SX-PCEAX-SMT-SP function	Remarks
PCIe pins			
D27	PCIE_2_CLK_P	PCIE_REFCLK_WIFI_P	
D28	PCIE_2_CLK_N	PCIE_REFCLK_WIFI_N	
D30	PCIE_2_L0_TX_P	PCIE_WIFI_TX_P	One lane with reference clock reserved interface
D31	PCIE_2_L0_TX_N	PCIE_WIFI_TX_N	
C28	PCIE_2_L0_RX_P	PCIE_WIFI_RX_P	
C29	PCIE_2_L0_RX_N	PCIE_WIFI_RX_N	

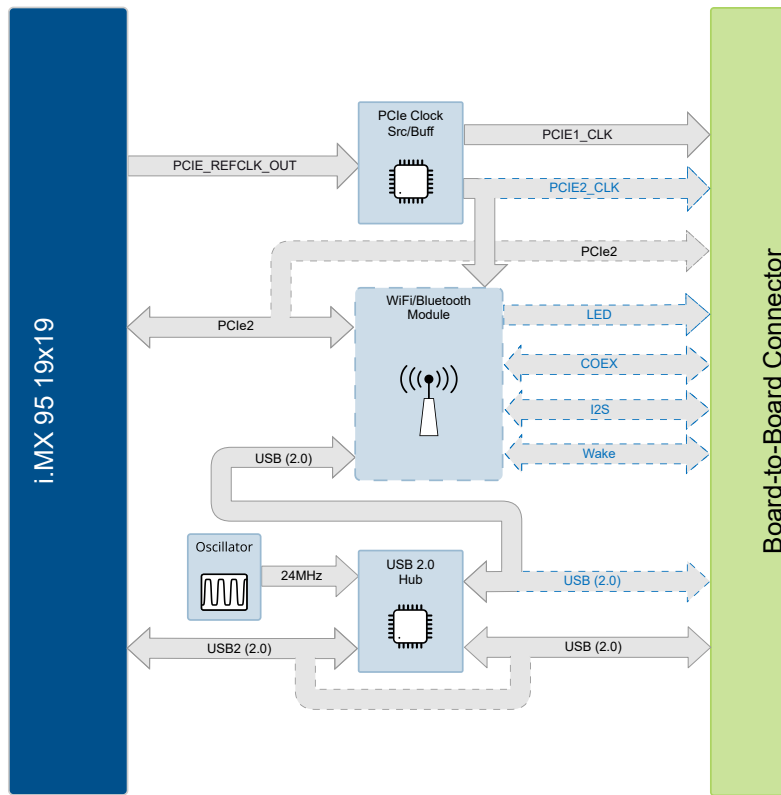
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Table 66: Wi-Fi/Bluetooth pins on board-to-board connector (Continued)

X1 pin	Aquila function	SX-PCEAX-SMT-SP function	Remarks
Module-specific pins			
C46	MSP_1_RX_P	PCIE1_REF_PAD_CLK_P	10kΩ pull-down
C47	MSP_1_RX_N	PCIE1_REF_PAD_CLK_N	10kΩ pull-down
C49	MSP_2_RX_P	PCIE2_REF_PAD_CLK_P	10kΩ pull-down
C50	MSP_2_RX_N	PCIE2_REF_PAD_CLK_N	10kΩ pull-down
C52	MSP_3_RX_P	WIFI_LAA_TX_EN	
C53	MSP_3_RX_N	WIFI_WL_TX_EN	
C58	MSP_5_RX_P	WIFI_LED1#	
C59	MSP_5_RX_N	WIFI_LED2#	
C61	MSP_6_RX_P	WIFI_I2S_SDI	10kΩ pull-down
C62	MSP_6_RX_N	WIFI_I2S_SDO	
C64	MSP_7_RX_P	WIFI_I2S_SCK	10kΩ pull-down
C65	MSP_7_RX_N	BT_SYNC	
C67	MSP_8_RX_P		Not connected
C68	MSP_8_RX_N		Not connected
C70	MSP_9_RX_P		Not connected
C71	MSP_9_RX_N		Not connected
D60	MSP_6_TX_P	USB_WIFI_D_P	Connected via the USB hub
D61	MSP_6_RX_P	USB_WIFI_D_N	Connected via the USB hub

The block diagram of the Wi-Fi and Bluetooth module, along with its connection to the USB Hub, is shown in [Figure 7](#).

Figure 7: Wi-Fi/Bluetooth block diagram



Legend

- - - - - Dashed line. Assembly option.
- Blue line. Interface is available on the MSP pins.
- Red line. Interface is not available.



The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. Please consult the relevant regional guidelines for detailed compliance information. Contact us for any questions or support related to certification and usage.

6 Test Points

The Aquila iMX95 system on module includes a comprehensive set of test points (TPs) that facilitate debugging, signal monitoring, and system validation during development and production. These test points provide direct access to critical signals such as power rails, communication interfaces, clock outputs, and control lines, enabling precise measurement and troubleshooting without disrupting normal module operation.

Each test point is identified by a unique label (e.g., TP01, TP02) and corresponds to specific signals, including PMIC control signals, eMMC interface lines, I²C buses, and various power supply voltages. Some test points incorporate external pull-up or pull-down resistors, which are detailed in the specification, to ensure signal stability and proper logic levels during testing.

Table 67: Test points

Test point	Aquila specification signal name	Non-SoC Pin - Component	Remarks
TP01	PMIC_I2C_SCL	–	2.2 kΩ pull-up
TP02	PMIC_I2C_SDA	–	2.2 kΩ pull-up
TP03	+V1.8	SW3LXA/SW3LXB - PMIC	
TP04	PMIC_PF09_VDDOTP	–	100 kΩ pull-down
TP05	–	VDDOTP/XFAILB - PMIC	4.7 kΩ pull-down
TP06	+V0.8	SW2LXA/SW2LXB - PMIC	
TP07	+V1.05_DDR	SW5LXA/SW5LXB - PMIC	
TP08	+V0.5_DDR	SW4LXA/SW4LXB - PMIC	
TP09	+VDD_SOC	LX - MPF5302AMMAAES	
TP10	+VDD_ARM	LX - MPF5301AMMABES	
TP11	eMMC_STROBE	DS - eMMC	
TP12	eMMC_CLK	CLK - eMMC	
TP13	eMMC_DATA0	DAT0 - eMMC	
TP14	I2C_SOM_SCL_3V3	SCL - Temperature Sensor	2.2 kΩ pull-up
TP15	I2C_SOM_SDA_3V3	SDA - Temperature Sensor	2.2 kΩ pull-up
TP16	–	CLK_OUT - Ethernet	
TP17	+V_IN	–	
TP18	+V3.3	SW1LXA/SW1LXB - PMIC	
TP19	+V0.8	SW2LXA/SW2LXB - PMIC	
TP20	+V1.8_BBSM	VAON - PMIC	
TP21	+V1.8	SW3LXA/SW3LXB - PMIC	
TP22	–	LDO1OUT - PMIC	Not used
TP23	+V0.5_DDR	SW4LXA/SW4LXB - PMIC	
TP24	+V3.3_1.8_SD	LDO2OUT - PMIC	
TP25	+VDD_SOC	LDO3OUT	
TP26	+V1.05_DDR	SW5LXA/SW5LXB - PMIC	
TP27	+VDD_SOC	LX - MPF5302AMMAAES	
TP28	+VDD_ARM	LX - MPF5301AMMABES	

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Table 67: Test points (Continued)

Test point	Aquila specification signal name	Non-SoC Pin - Component	Remarks
TP29	PMIC_PGOOD	-	10 kΩ pull-up
TP30	PMIC_I2C_SCL	-	10 kΩ pull-up
TP31	PMIC_I2C_SDA	-	10 kΩ pull-up
TP32	PMIC_FSOB	-	10 kΩ pull-up
TP33	PMIC_ON	-	100 kΩ pull-down
TP34	PMIC_STBY	-	100 kΩ pull-down
TP35	PMIC_RESET_CPU	-	100 kΩ pull-up
TP36	PMIC_PF53_SOC_EN	-	100 kΩ pull-down
TP37	PMIC_PF53_ARM_EN	-	100 kΩ pull-down
TP38	-	AMUX - PMIC	
TP39	PMIC_RESET_1V8	-	10 kΩ pull-up
TP40	PMIC_WDOG	-	10 kΩ pull-up
TP41	PMIC_PF09_INT_B	-	10 kΩ pull-up
TP42	-	PGOOD - MPF5302AMMAAES	10 kΩ pull-up
TP43	-	PGOOD - MPF5301AMMABES	10 kΩ pull-up
TP44	+V1.2_DP	SW - TPS62A02 (Buck)	
TP45	+V2.5_ETH	OUT - TLV75525P (Buck)	
TP46	+V1.8_DP	VCCIO - SN65DSI86ZXHR	

7 Low Power Modes



Missing Content

More information about power consumption will be available on the next release of the datasheet.

8 Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Aquila iMX95 even when the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in recovery mode, the USB_1 interface is used to connect it to a host computer. You will find additional information at our Developer Center:

<https://developer.toradex.com/hardware/hardware-resources/recovery-mode/imx-ti-recovery-mode>

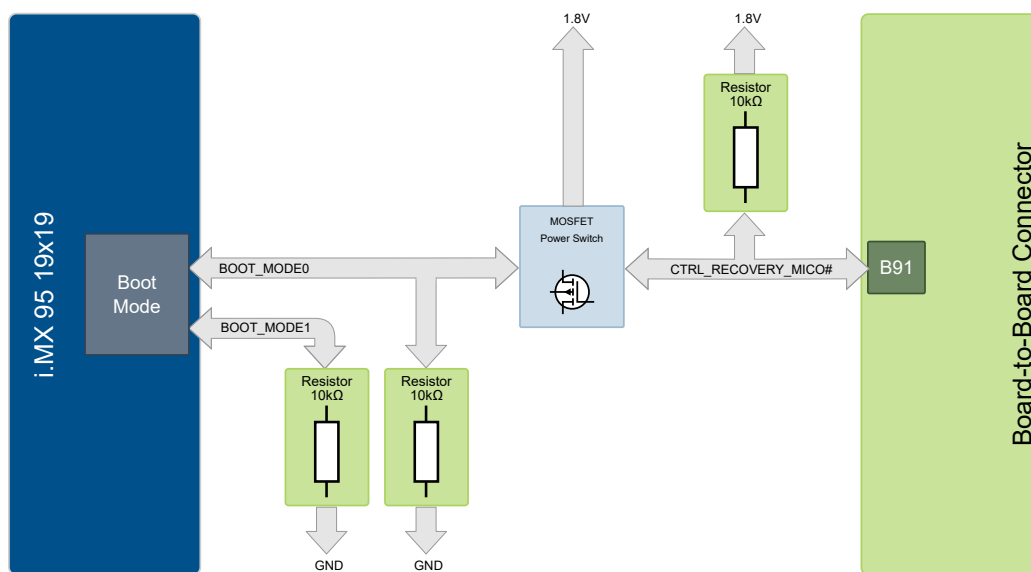
In order to enter recovery mode, the dedicated recovery pin needs to be pulled down with $\leq 1k\Omega$ during the initial power-on (cold boot) of the module. The CTRL_RECOVERY_MICO# function on the board-to-board connector pin B91 is standardized in the Aquila module specifications. It is highly recommended to add at least a test point on the carrier board to the pin B91 to be able to enter recovery mode. There is no need for a pull-up resistor on the carrier board.



Make sure that there is no bootable SD card plugged into the slot.

Otherwise, the module will try to boot from the external SD card instead of going into the USB serial loader.

Figure 8: Recovery mode block diagram



Legend

- - - - - Dashed line. Assembly option.
- Blue line. Interface is available on the MSP pins.
- Red line. Interface is not available.

9 Known Issues



There are no known issues.

10 Technical Specifications

10.1 Absolute Maximum Ratings

Table 68: Absolute maximum ratings

Symbol	Description	Minimum	Maximum	Unit
VCC	Main power supply	-0.3	6.0	V
VCC_BACKUP	RTC power supply	-0.3	6.0	V
IO_1.8V	SoC IO pins with 1.8V logic level	-0.3	2.1	V
IO_3.3V	SoC IO pins with 3.3V logic level (SDIO)	-0.3	3.6	V
ADC	ADC analog input	-0.3	3.6	V
USB_1_VBUS	Input voltage at USB_1_VBUS	-0.3	6.0	V

10.2 Recommended Operation Conditions

Table 69: Recommended operation conditions

Symbol	Description	Minimum	Typical	Maximum	Unit
VCC	Main power supply	4.75	5.00	5.25	V
VCC_BACKUP	RTC power supply	1.10	3.00	5.50	V

10.2.1 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Aquila product family. Following those recommendations ensures that the carrier board being designed will be compatible with all existing and future Aquila modules. For details, please refer to the [Aquila Carrier Board Design Guide](#) or the [Aquila Family Specification](#).

10.2.2 Power Ramp-Up Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Aquila module standard. This specification can be found in the [Aquila Carrier Board Design Guide](#).



Extra care must be taken to minimize backfeeding, as residual voltages on the PMIC power rails can prevent the module from powering up. The PMIC is sensitive to such voltages and may halt the boot sequence before initiating voltage ramp-up. While the i.MX 95 SoC employs a PMIC that does not monitor residual voltage—allowing boot even if voltages exceed 200 mV—it is still strongly advised to reduce backfeeding to ensure reliable operation.

10.3 Mechanical Characteristics

SoM Outline Dimensions

- 85mm x 55mm x 8mm



Tolerance for all measures:

- $\pm 0.1\text{mm}$, unless otherwise specified.

Refer to Figures 9 and 10 for detailed mechanical dimensions and tolerances of the module.

Figure 9: Module dimensions (top view)

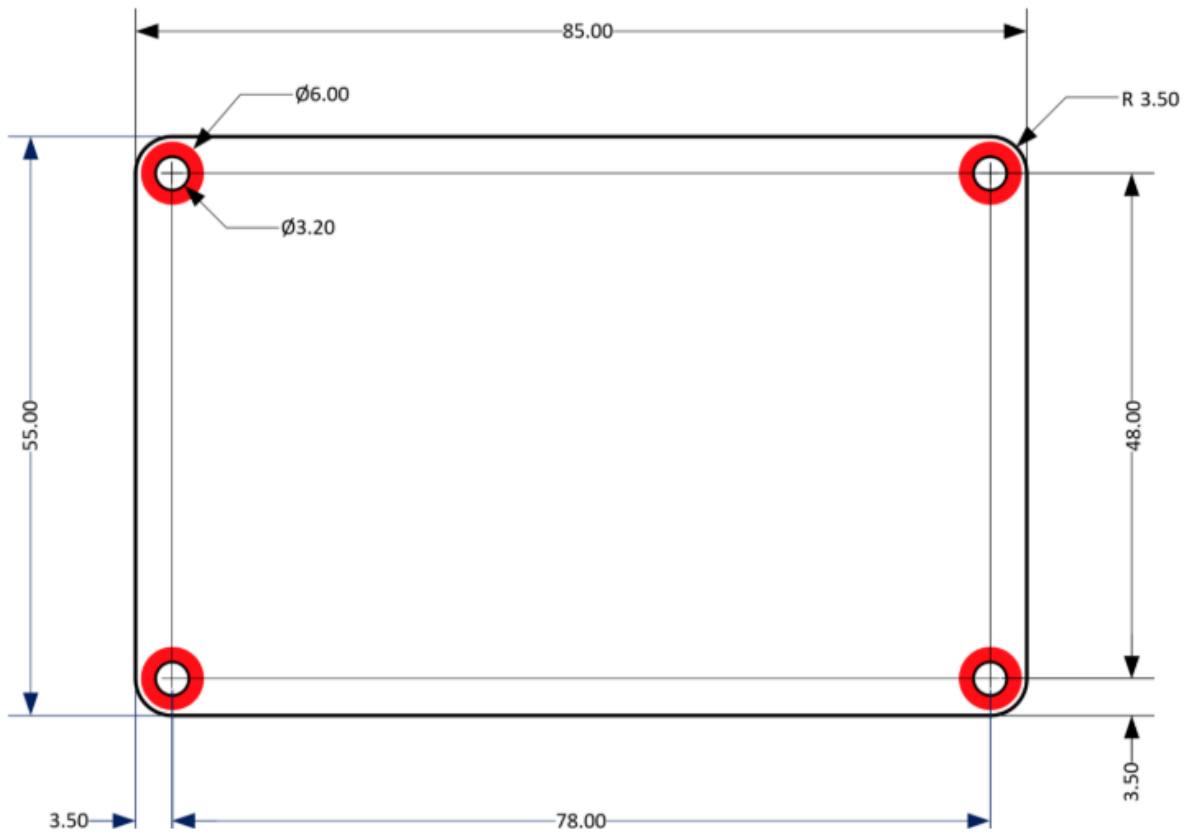
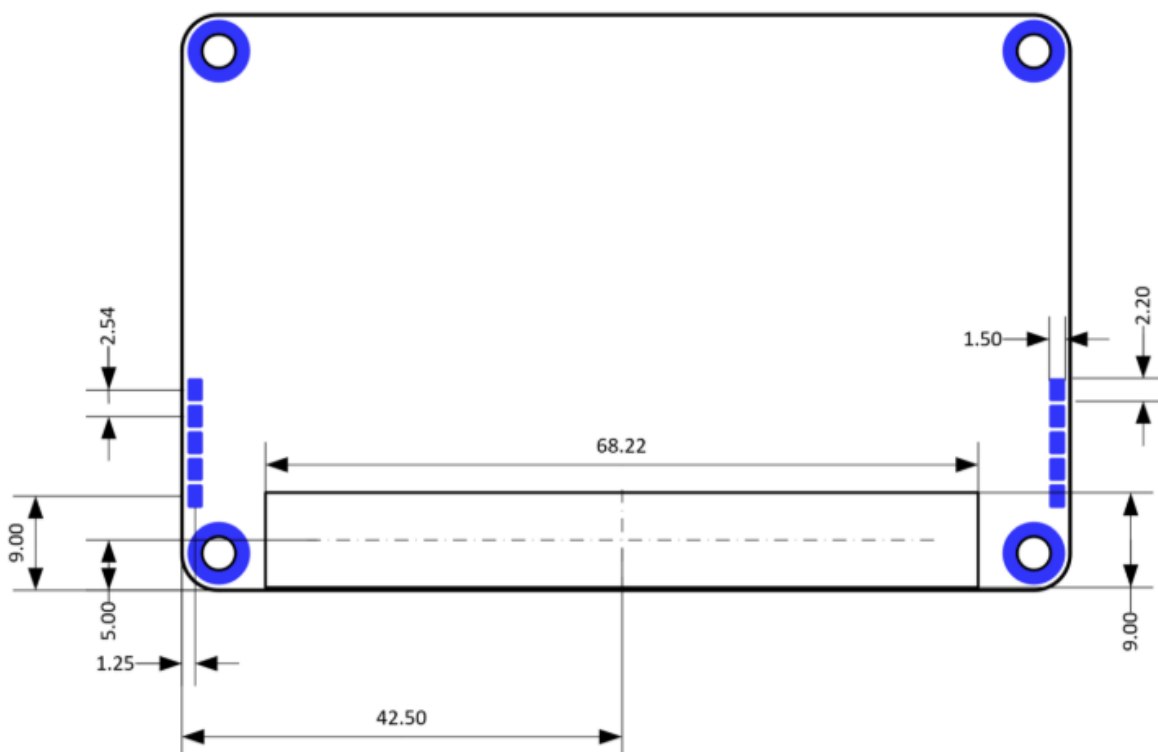


Figure 10: Module dimensions (bottom view)



10.3.1 Sockets for the Aquila Modules

The Aquila modules use Samtec’s Accelerate HP (High-Performance Array) Board-to-Board connector for state-of-the-art robustness and reliability. This connector has 400 pins in a 100×4 organization with a 0.635mm pitch. The board-to-board connector is available to Toradex customers for custom carrier board designs, both during development and production. Volume pricing is also available. For more information, see [Aquila Carrier Board Connector](#)³.

Table 70: Board-to-Board connector models

PN (Module Side)	Solder Balls	Remarks
Samtec APF6-100-03.5-L-04-0-A-FR	No	
Samtec APF6-100-03.5-L-04-2-TR	Yes	No alignment pins

Mating parts for the Carrier side can have two stacking height options:

- 5 mm stacking height
- 10 mm stacking height

Table 71: Mating Board-to-Board connector models

PN (Module Side)	Solder Balls	Stacking Height	Remarks
Samtec APM6-100-01.5-L-04-0-A-FR	No	5mm	
Samtec APM6-100-01.5-L-04-2-TR	Yes	5mm	No alignment pins
Samtec APM6-100-06.5-L-04-0-A-FR	No	10mm	
Samtec APM6-100-06.5-L-04-2-TR	Yes	10mm	No alignment pins



The above PNs indicate 10 µm gold contacts. For 30 µm gold please change the -L- option to -S-.

The following table compares the different mating parts options. The connector height is the stacking height of the connector. The board-to-board distance is the nominal space between the carrier board and the module. The column “Component Height Carrier Board” indicates the recommended maximum height of components underneath the module.

Table 72: Board-to-Board connector stacking height

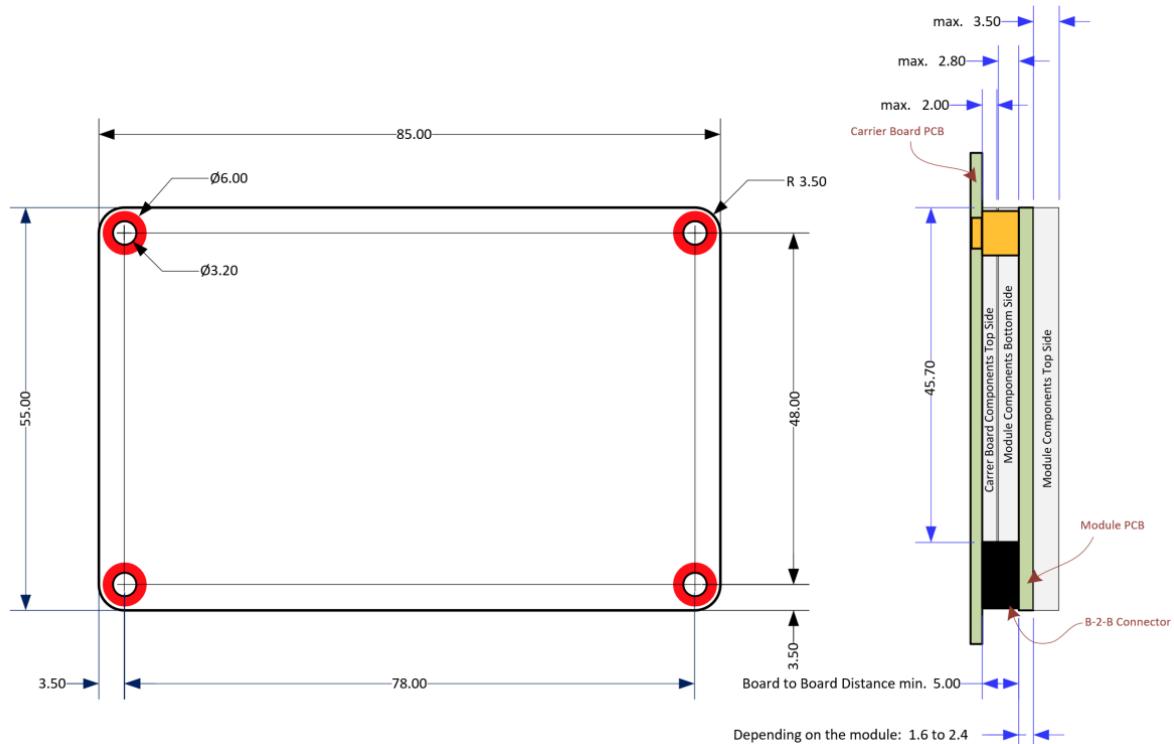
Connector Height	Board-to-Board distance	Component Height Carrier Board	Remarks
5mm	5 mm	2 mm	Recommended stacking height for Aquila modules
10mm	10 mm	8 mm	Recommended for special cases where high components under the module are required

To ensure mechanical compatibility with current and future Aquila modules and module revisions, it is recommended to reserve the full component height allowance specified for the module on the carrier board. Even if the module does not fully utilize the allotted component height, additional components should not be placed between the module and the carrier board. [Figure 11](#) shows the module dimensions including the specified stacking height to assist in carrier board design.

³<https://www.toradex.com/accessories/aquila-carrier-board-connector>

If system design requires components taller than 2 mm in this area, it is advisable to select a connector with an increased stacking height to maintain mechanical integrity and compatibility.

Figure 11: Module stacking dimensions



10.4 Thermal Specification

The Aquila iMX95 incorporates **DVFS (Dynamic Voltage and Frequency Scaling) and thermal throttling**, enabling the system to dynamically adjust operating frequency and voltage based on workload and temperature. The i.MX 95 SoC features DVFS for both the CPU cluster and the GPU. This allows the Aquila iMX95 to deliver higher performance with lower average power consumption compared to other solutions.

Aquila iMX95 modules include embedded temperature sensors that monitor die (junction) temperature and determine whether core throttling is required to prevent overheating. If the temperature reaches the maximum permitted threshold, the system automatically shuts down.

General thermal and performance considerations:

- **Heat dissipation is less critical if peak performance is used only briefly**, as advanced power management reduces power consumption when full performance is not needed.
- **Lower die temperatures reduce power consumption**, due to lower leakage currents during idle states. For example, an increase in die temperature from 25 °C to 125 °C can increase leakage by a factor of 10.
- **Effective thermal solutions improve performance**, as better heat dissipation enables the module to operate closer to its peak capability for longer durations.

Table 73: Thermal Specification – Aquila iMX95

Description	Minimum	Typical	Maximum	Unit
Operating temperature range	-40 ¹		85 ²	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 95 only ($R_{\theta JA}$) ³		21.10		°C/W
Thermal Resistance Junction-to-Top of i.MX 95 chip case ($R_{\theta JCTop}$) ³		0.98		°C/W

¹ The validation of the Wi-Fi module is currently pending. All other components are rated for the full -40 °C to 85 °C range.

² Depends on the cooling solution.

³ Tested on a high-K JEDEC four-layer board, as defined by JEDEC Standard JESD51-2A. Board mounted horizontally, natural convection.

11 Product Compliance

Up-to-date information about product compliance—such as RoHS, CE, UL 94, Conflict Minerals, REACH, and others—can be found [on our website](#)⁴.

⁴<https://www.toradex.com/support/product-compliance>

12 Device and Documentation Support

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