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Verdin AM62P V1.0

HW Datasheet

Preliminary – Subject to Change

Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
01-Jul-2025	Rev. 0.1	V1.0	Initial release

Contents

List of Tables

1 Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the Verdin AM62P. For information on the actual features supported by software, please refer to the relevant SoM product page on the Toradex Developer website:

https://developer.toradex.com/hardware/verdin-som-family/modules/verdin-am62p

1.2 Verdin SoM Family

The Verdin System on Module (SoM) family eliminates much of the complexity associated with modern-day electronic design. Complicated circuitry such as high-speed impedance-controlled layouts with high component density is encapsulated on the SoM. This allows the customer to create a carrier board that focuses solely on application-specific electronics, making the project substantially less complex.

The Verdin module takes this one step further and implements an interface pinout that allows direct connection of real-world I/O ports without the need to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high-speed serial technologies that require impedance-controlled differential pairs. Direct Breakout™ allows them to easily route such interfaces to common connectors in a simple, robust fashion.

The Verdin SoM features a wide input voltage range that allows it to be powered from a broad range of power sources (e.g., directly from a USB power supply or a single lithium cell). Due to increasing transistor density and the need for more power-efficient devices, the I/O voltage level is trending to decrease from 3.3V to 1.8V. For this reason, the Verdin family of SoMs supports a 1.8V I/O voltage level only. Both the wide input voltage range and the 1.8V I/O voltage make the power supply designs for a Verdin carrier board simple, easy, and cost-efficient. These features altogether make the Verdin family of SoMs perfectly suited for battery-powered applications as well.

1.3 TI AM62P SoC

The Verdin AM62P SoM is based on the Texas Instruments AM62P-Q1™ family of System on Chips (SoCs), it features up to four Cortex®-A53 (often shortened to A53) cores as the main processor cluster. The cores provide complete 64-bit Arm®v8-A support while maintaining seamless backward compatibility with 32-bit Arm®v7-A software. The A53 cores run at up to 1.4GHz and feature improved integer operations, floating-point unit (FPU), and Arm® Neon™ SIMD extension.

In addition to the main CPU complex, the AM62P also offers a Cortex®-R5F (often shortened to R5F) processor designed to meet SIL-2 safety requirements. The R5F runs at up to 800MHz and may be used to run safety tasks or as a general-purpose MCU. This heterogeneous multicore system allows for running additional real-time operating systems for time- and security-critical tasks.

The AM62P family features inline ECC (error-correcting code) for the LPDDR4 DRAM for high system reliability and safety.

The AM62P features the *PowerVR® BXS 4-64 MC1* graphics processing unit (GPU). The GPU is capable of up to 50GFLOPs and supports OpenGL® ES 3.2 and Vulkan® 1.2.

1.4 Main Features

1.4.1 CPU

Table 1: CPU Features

Parameter	Verdin AM62P Quad 2GB WB IT
SoC	AM62P54CVMHIAMHR
CPU Name	TI AM62P54
A53 Cores	4
R5F Cores	1
CPU Clock	A53: 1.4GHz R5F: 800MHz
Security (HSM)	Yes
Neon SIMD	Yes
L1 Instruction Cache (per core)	A53: 32kB
L1 Data Cache (per core)	A53: 32kB
L2 Cache (shared)	A53: 512kB
Tightly Coupled Memory	R5F: 256kB

1.4.2 GPU

Table 2: GPU Features

Parameter	Verdin AM62P Quad 2GB WB IT
GPU	Yes
2D Acceleration	Yes
3D Acceleration	Yes
GPU Model	PowerVR® BXS 4-64 MC1
Frequency	800MHz
FLOPs	50 GFLOPs
OpenGL ES	3.2
Vulkan	1.2

1.4.3 Interfaces

Table 3: Features Interfaces

Parameter	Verdin AM62P Quad 2GB WB IT
Analog	
Analog Input	4
Audio	
Digital Audio	2x McASP (I2S or TDM)
Camera	
MIPI CSI-2	1x Quad Lane
Display	
Display Controllers	Dual
LVDS	1x up to 1920x1080
MIPI DSI	1x Quad Lane
Low Speed	
CAN FD	4
GPIO	90
I²C	5
JTAG	1
PWM	3
QSPI/OSPI	1
SPI	5
UART	8
Network	
Bluetooth	5.3
Ethernet	GBE with TSN + 2ⁿ RGMII
Wi-Fi	Dual-band 1x1 802.11ax
Storage	
SDIO/SD/MMC	2
USB	
USB 2.0 Host	1
USB 2.0 OTG	1

1.4.4 Memory

Table 4: Memory Features

Parameter	Verdin AM62P Quad 2GB WB IT
eMMC	
eMMC Configuration	2D MLC
eMMC Capacity	16GB
I²C EEPROM	
I²C EEPROM Capacity	2kbit (256 × 8bits)
RAM	
RAM Capacity	2GB
RAM Configuration (ctrl. × ch. × bits)	32-bit, Single rank, 1 × 1 × 32
RAM Type	LPDDR4
RAM Speed	3733MT/s
Inline ECC	Yes

1.4.5 Physical

Table 5: Physical Features

Parameter	Verdin AM62P Quad 2GB WB IT
Module Dimensions	69.6 x 35.0 x 5.0 mm
Temperature Range	–40°C to +85°C
Shock / Vibration	EN 60068-2-6/50g 20ms
Power Dissipation	TBD

1.5 Interface Overview

Features of the Verdin module are split into three distinct categories: “Always Compatible”, “Reserved”, and “Module-specific”. The “Always Compatible” and “Reserved” pins are also referred to as the “Verdin Standard” pins.

Additionally to this definition, the AM62P SoC allows for alternate functions. As an example, many pins can, apart from their primary function, also work as GPIOs.

“Always Compatible” interfaces are features that shall be present on each SoM in the Verdin Family. Customers can count on upgradability and maximum scalability regarding these interfaces.

“Reserved” interfaces are features that are defined and reserved but possibly missing on some SoM models due to lack of availability. It could be that a particular SoC does not provide a specific interface or that there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means any Verdin SoM can be reliably inserted into any Verdin carrier board without causing damage due to incompatible “Reserved” pins.

A “Module-specific” feature is a feature that is not guaranteed to be functionally or electrically compatible between modules. Suppose a carrier board design uses such features. In that case, it is possible that other modules in the Verdin module family do not provide these features and instead provide other features on the associated pins. In this case, Verdin modules that are suitable for use in the carrier board design may be restricted. An incompatible SoM/carrier board combination may disable all functionality or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

The alternate functions group means that an interface is provided as an additional function on an “Always Compatible”, “Reserved”, or “Module-specific” pin. These functions can only be used if the primary function of the pin is not used.

Table 6 shows the interfaces that are supported on the Verdin AM62P module along with the group in which that feature is provided: “Always Compatible”, “Reserved”, “Module-specific”, or alternate function.

Table 6: X1 interfaces

Feature	Total	“Always Compatible”	“Reserved”	“Module-specific” or Alternate Function
Analog				
Analog input	4	0	4	0
Audio				
I^2S	2	0	2	0
Camera				
MIPI CSI-2	1	0	1	0
Display				
LVDS	1	0	0	1
MIPI DSI	1^{DSI}	0	1^{DSI}	0
Low Speed				
CAN FD	$2+2^{R5F}$	0	$1+1^{R5F}$	$1+1^{R5F}$
GPIO	$94+10^{nWB}$	10	$4+10^{nWB}$	80
I^2C	4	1	3	0

Continued on next page

Table 6: X1 interfaces (Continued)

Feature	Total	"Always Compatible"	"Reserved"	"Module-specific" or Alternate Function
JTAG	1	0	1	0
OSPI	1[OSPI]	0	0	1[OSPI]
PWM	6	1	2	3
QSPI	1	0	1	0
SPI	5	1	0	4
UART	9+1[PRU]	3	1	5+1[PRU]
Network				
Gigabit Ethernet	1	1	0	0
RGMII *for 2nd Gigabit Ethernet*	1	0	1	0
Storage				
SDIO/SD/MMC	1+1[nWB,1V8]	1	0	1[nWB,1V8]
USB				
USB 2.0 Host	1	1	0	0
USB 2.0 OTG	1	1	0	0

1V8: 1.8V-only interface, may require a level shifter on the carrier board.
DSI: See the DSI availability in Table 3 on page 7.
R5F: Interrupts are available only on R5F core. Requires software polling on A53 cores which may reduce throughput.
nWB: On models without Wi-Fi/Bluetooth module.
OSPI: The OSPI is an extension to the QSPI interface, using the QSPI pins and module specific pins.
PRU: Only accessible to the Programmable Real-Time Subsystem (PRUSS).

1.6 Reference Documents

1.6.1 Verdin Carrier Board Design Guide

A custom carrier board should follow the Verdin Carrier Board Design Guide to make the board compatible with the Verdin module family. Please study this document in detail before starting your carrier board design.

https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

1.6.2 Verdin Family Specification

This document outlines the specification which defines the Verdin Computer-on-Module family. It describes the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also explains the mechanical form factor, including key dimensions and possible thermal solutions.

https://docs.toradex.com/109262-verdin-family-specification.pdf

1.6.3 Layout Design Guide

This document contains information on high-speed layout design, along with additional factors that help ensure the carrier board layout is correct the first time.

https://docs.toradex.com/102492-layout-design-guide.pdf

1.6.4 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information on a regular basis. You can find an abundance of additional information there.

Please note that the Developer Center is shared across all Toradex products. You should always verify whether the information provided is valid and relevant for the Verdin AM62P.

https://developer.toradex.com

1.6.5 Verdin Carrier Board Schematics

We provide complete schematics plus an Altium project file which includes library symbols and IPC-7351 compliant footprints for the Verdin Development Board, as well as other carrier boards, free of charge. This resource is of great help when designing your own carrier board.

https://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.6.6 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin, Apalis, and Colibri Modules. The tool allows comparing the interfaces across different modules.

https://developer.toradex.com/knowledge-base/pinout-designer

1.6.7 TI AM62P

You may find additional details about the TI AM62P SoC in the Datasheet and Reference Manual provided by Texas Instruments.

AM62P:
https://www.ti.com/product/AM62P-Q1

1.6.8 Enabling Low Power Embedded Systems With AM62P Processors

TI's White Paper explaining low power modes, active power management, and analyzing power consumption on the AM62P SoC.

https://www.ti.com/lit/wp/sprad41/sprad41.pdf

1.6.9 ADC

Verdin AM62P utilizes a Texas Instrument TLA2024 12-bit, four-channel, I²C analog-to-digital converter.

https://www.ti.com/product/TLA2024

1.6.10 EEPROM

The Verdin AM62P has an on-module I²C EEPROM, the M24C02-FMC6TG from STMicroelectronics.

https://www.st.com/en/memories/m24c02-f.html

1.6.11 Ethernet Transceiver

The Verdin AM62P SoM utilizes the DP83867IR Industrial Temperature, robust gigabit Ethernet PHY transceiver from Texas Instruments.

https://www.ti.com/product/DP83867IR

1.6.12 PCB Temperature Sensor

The Verdin AM62P can be assembled with a PCB temperature sensor, the TI TMP1075DSGR.

https://www.ti.com/product/TMP1075

1.6.13 RTC

The Verdin AM62P features a low-power Epson RX8130CE real-time clock.

https://www5.epsondevice.com/en/products/rtc/rx8130ce.html

1.6.14 TPM 2.0 Module

The Verdin AM62P can be assembled with a Trusted Platform Module (TPM 2.0), the ST33KTPM2I from STMicroelectronics. The complete documentation is only available under a STMicroelectronics NDA.

https://www.st.com/en/secure-mcus/st33ktpm2xspi.html

1.6.15 Wi-Fi and Bluetooth Module

The WB versions of the Verdin AM62P utilize an u-blox MAYA-W260-00B Host-based multiradio module with Wi-Fi 6 802.11a/b/g/n/ac/ax dual-band and BT/BLE 5.3. This module uses two U.FL antennas.

https://www.u-blox.com/en/product/maya-w2-series

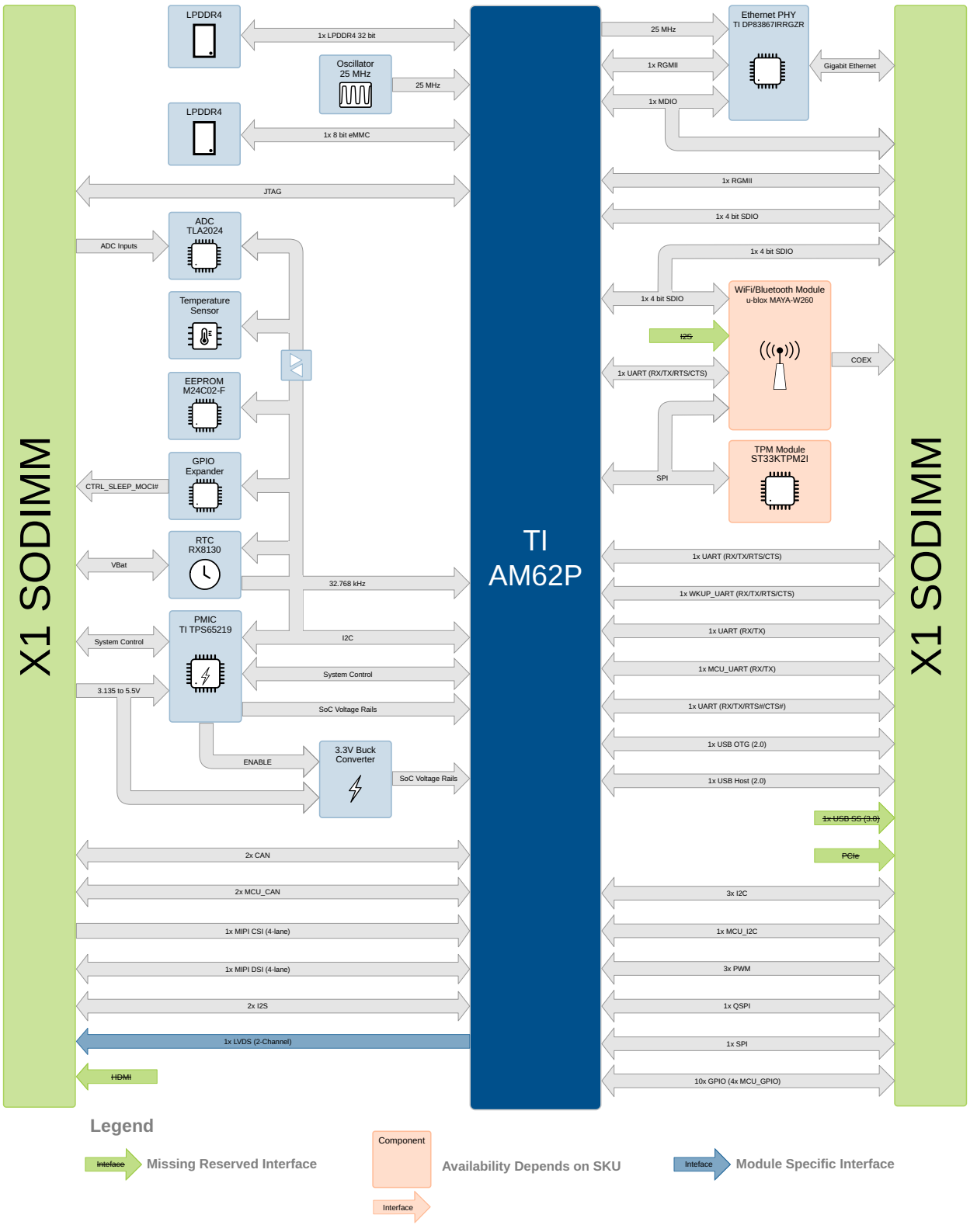
Information on pre-certified antennas and cables can be found here:

https://developer.toradex.com/hardware/hardware-resources/peripherals/wireless/wi-fi-cables-and-antennas-for-toradex-modules/

2 Architecture Overview

2.1 Block Diagram

Figure 1: Block Diagram



3 Verdin AM62P Connector

3.1 Pin Numbering

The Verdin module follows the same pin numbering scheme as the SODIMM DDR4 standard. Pins on the top side of the module have an odd number, while the pins on the bottom side have an even number.

Figure 2: Pin numbering (top)

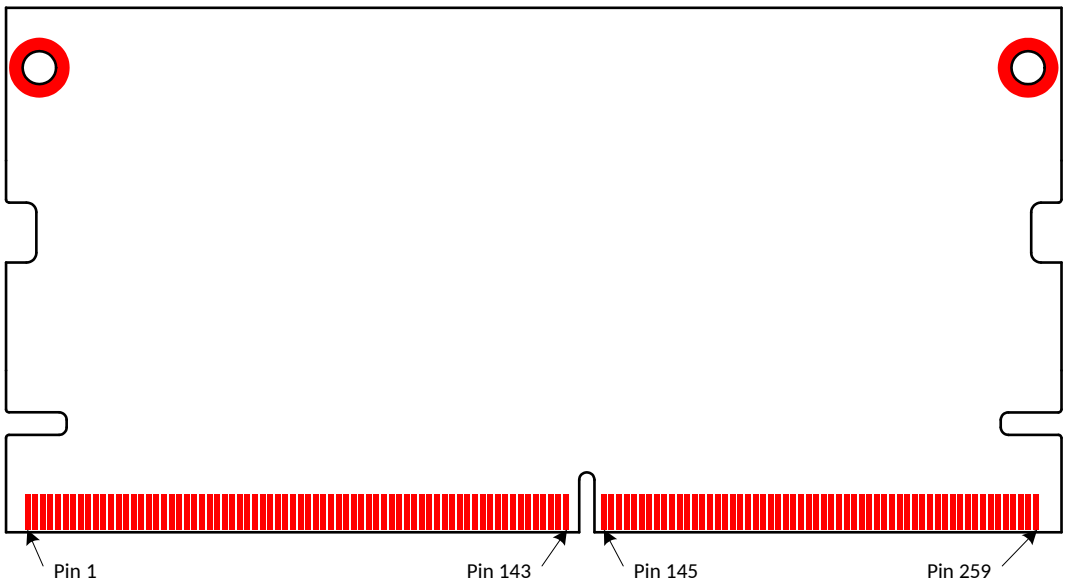
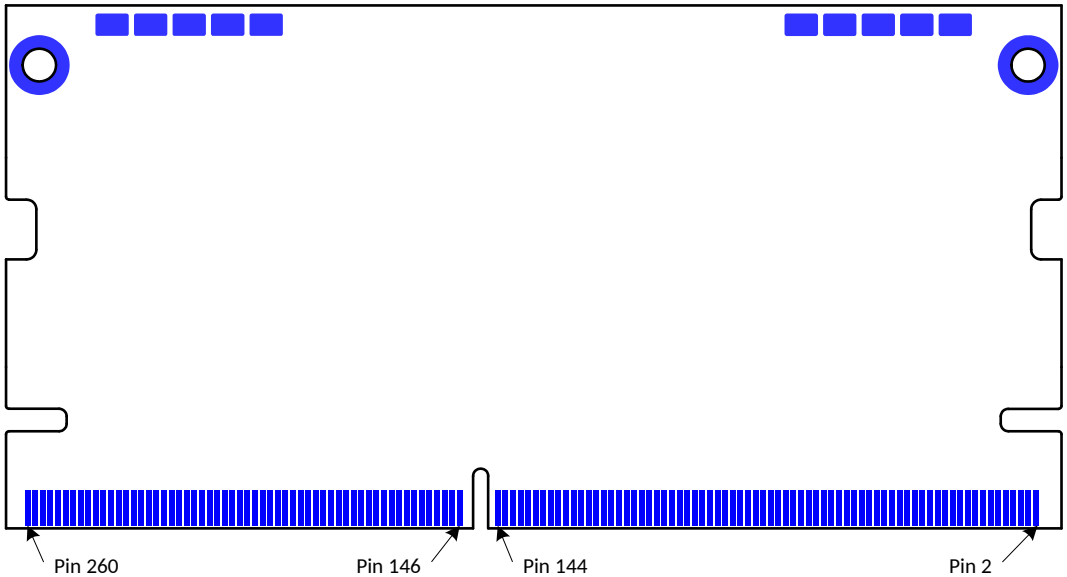


Figure 3: Pin numbering (bottom)



3.2 Pin Assignment

Table 7 and Table 8 describe the main connector (X1) pinout and highlight the pins' function compatibility with the family specification. A detailed explanation about the family specification compatibility groups is available in section 1.5 on page 9.

Table 7: X1 pin assignment - top side - odd pins

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
1	JTAG_1_TDI	Yes	Always Compatible	TDI		
3	JTAG_1_TRST#	Yes	Always Compatible	TRSTn		
5	JTAG_1_TDO	Yes	Always Compatible	TDO		
7	JTAG_1_VREF	Yes	Always Compatible		1.8V	Reference output, 10mA max.
9	JTAG_1_TCK	Yes	Always Compatible	TCK		
11	GND	Yes	Always Compatible		GND	
13	JTAG_1_TMS	Yes	Always Compatible	TMS		
15	PWM_1	Yes	Always Compatible	MMC2_SDWP		
17	DSI_1_INT#	Yes	Reserved	GPMC0_WAIT1		
19	PWM_3_DSI	Yes	Reserved	SPI0_CS1		
21	DSI_1_BKL_EN	Yes	Reserved	GPMC0_WPn		
23	DSI_1_D3_N	Yes	Reserved	DSI0_TXN3		
25	DSI_1_D3_P	Yes	Reserved	DSI0_TXP3		
27	GND	Yes	Always Compatible		GND	
29	DSI_1_D2_N	Yes	Reserved	DSI0_TXN2		
31	DSI_1_D2_P	Yes	Reserved	DSI0_TXP2		
33	GND	Yes	Always Compatible		GND	
35	DSI_1_CLK_N	Yes	Reserved	DSI0_TXCLKN		
37	DSI_1_CLK_P	Yes	Reserved	DSI0_TXCLKP		
39	GND	Yes	Always Compatible		GND	
41	DSI_1_D1_N	Yes	Reserved	DSI0_TXN1		
43	DSI_1_D1_P	Yes	Reserved	DSI0_TXP1		
45	GND	Yes	Always Compatible		GND	

Continued on next page

Table 7: X1 pin assignment - top side - odd pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
47	DSI_1_D0_N	Yes	Reserved	DSI0_TXN0		
49	DSI_1_D0_P	Yes	Reserved	DSI0_TXP0		
51	GND	Yes	Always Compatible		GND	
53	I2C_2_DSI_SDA	Yes	Reserved	I2C1_SDA		
55	I2C_2_DSI_SCL	Yes	Reserved	I2C1_SCL		
57	I2C_3_HDMI_SDA	Yes	Reserved	MCU_I2C0_SDA		
59	I2C_3_HDMI_SCL	Yes	Reserved	MCU_I2C0_SCL		
61	HDMI_1_HPD	No	Reserved	MCU_UART0_CTSn		HDMI not supported on Verdin AM62P
63	HDMI_1_CEC	No	Reserved	MCU_UART0_RTSn		HDMI not supported on Verdin AM62P
65	GND	Yes	Always Compatible		GND	
67	HDMI_1_TXC_N	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
69	HDMI_1_TXC_P	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
71	GND	Yes	Always Compatible		GND	
73	HDMI_1_TXD0_N	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
75	HDMI_1_TXD0_P	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
77	GND	Yes	Always Compatible		GND	
79	HDMI_1_TXD1_N	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
81	HDMI_1_TXD1_P	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
83	GND	Yes	Always Compatible		GND	
85	HDMI_1_TXD2_N	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
87	HDMI_1_TXD2_P	No	Reserved		NC	Not connected, HDMI not supported on Verdin AM62P
89	GND	Yes	Always Compatible		GND	
91	CSI_1_MCLK	Yes	Reserved	WKUP_CLKOUT0		

Continued on next page

Table 7: X1 pin assignment - top side - odd pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
93	I2C_4_CSI_SDA	Yes	Reserved	UART0_RTSn		
95	I2C_4_CSI_SCL	Yes	Reserved	UART0_CTSn		
97	GND	Yes	Always Compatible		GND	
99	CSI_1_D3_P	Yes	Reserved	CSI0_RXP3		
101	CSI_1_D3_N	Yes	Reserved	CSI0_RXN3		
103	GND	Yes	Always Compatible		GND	
105	CSI_1_D2_P	Yes	Reserved	CSI0_RXP2		
107	CSI_1_D2_N	Yes	Reserved	CSI0_RXN2		
109	GND	Yes	Always Compatible		GND	
111	CSI_1_CLK_P	Yes	Reserved	CSI0_RXCLKP		
113	CSI_1_CLK_N	Yes	Reserved	CSI0_RXCLKN		
115	GND	Yes	Always Compatible		GND	
117	CSI_1_D1_P	Yes	Reserved	CSI0_RXP1		
119	CSI_1_D1_N	Yes	Reserved	CSI0_RXN1		
121	GND	Yes	Always Compatible		GND	
123	CSI_1_D0_P	Yes	Reserved	CSI0_RXP0		
125	CSI_1_D0_N	Yes	Reserved	CSI0_RXN0		
127	GND	Yes	Always Compatible		GND	
129	UART_1_RXD	Yes	Always Compatible	MCASP0_AFSR		
131	UART_1_TXD	Yes	Always Compatible	MCASP0_ACLKR		
133	UART_1_RTS	Yes	Always Compatible	MCASP0_AXR2		
135	UART_1_CTS	Yes	Always Compatible	MCASP0_AXR3		
137	UART_2_RXD	Yes	Always Compatible	WKUP_UART0_RXD		

Continued on next page

Table 7: X1 pin assignment - top side - odd pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
139	UART_2_TXD	Yes	Always Compatible	WKUP_UART0_TXD		
141	UART_2_RTS	Yes	Always Compatible	WKUP_UART0_RTSn		
143	UART_2_CTS	Yes	Always Compatible	WKUP_UART0_CTSn		
145	GND	Yes	Always Compatible		GND	
147	UART_3_RXD	Yes	Always Compatible	UART0_RXD		
149	UART_3_TXD	Yes	Always Compatible	UART0_TXD		
151	UART_4_RXD	Yes	Reserved	MCU_UART0_RXD		
153	UART_4_TXD	Yes	Reserved	MCU_UART0_TXD		
155	USB_1_EN	Yes	Always Compatible	USB0_DRVVBUS		
157	USB_1_OC#	Yes	Always Compatible	GPMC0_ADVn_ALE		
159	USB_1_VBUS	Yes	Always Compatible	USB0_VBUS		Voltage Divider on the Module.
161	USB_1_ID	Yes	Always Compatible	GPMC0_CLK		
163	USB_1_D_N	Yes	Always Compatible	USB0_DM		
165	USB_1_D_P	Yes	Always Compatible	USB0_DP		
167	GND	Yes	Always Compatible		GND	
169	USB_2_SSTX_N	No	Reserved		NC	Not connected
171	USB_2_SSTX_P	No	Reserved		NC	Not connected
173	GND	Yes	Always Compatible		GND	
175	USB_2_SSRX_N	No	Reserved		NC	Not connected
177	USB_2_SSRX_P	No	Reserved		NC	Not connected
179	GND	Yes	Always Compatible		GND	
181	USB_2_D_N	Yes	Always Compatible	USB1_DM		
183	USB_2_D_P	Yes	Always Compatible	USB1_DP		

Continued on next page

Table 7: X1 pin assignment - top side - odd pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
185	USB_2_EN	Yes	Always Compatible	USB1_DRVVBUS		
187	USB_2_OC#	Yes	Always Compatible	GPMC0_CSn0		
189	ETH_2_RGMII_INT#	Yes	Reserved	GPMC0_CSn1		
191	ETH_2_RGMII_MDIO	Yes	Reserved	MDIO0_MDIO		Shared with on-module PHY.
193	ETH_2_RGMII_MDC	Yes	Reserved	MDIO0_MDC		Shared with on-module PHY.
195	GND	Yes	Always Compatible		GND	
197	ETH_2_RGMII_RXC	Yes	Reserved	RGMII2_RXC		
199	ETH_2_RGMII_RX_CTL	Yes	Reserved	RGMII2_RX_CTL		
201	ETH_2_RGMII_RXD_0	Yes	Reserved	RGMII2_RD0		
203	ETH_2_RGMII_RXD_1	Yes	Reserved	RGMII2_RD1		
205	ETH_2_RGMII_RXD_2	Yes	Reserved	RGMII2_RD2		
207	ETH_2_RGMII_RXD_3	Yes	Reserved	RGMII2_RD3		
209	GND	Yes	Always Compatible		GND	
211	ETH_2_RGMII_TX_CTL	Yes	Reserved	RGMII2_TX_CTL		
213	ETH_2_RGMII_TXC	Yes	Reserved	RGMII2_TXC		
215	ETH_2_RGMII_TXD_3	Yes	Reserved	RGMII2_TD3		
217	ETH_2_RGMII_TXD_2	Yes	Reserved	RGMII2_TD2		
219	ETH_2_RGMII_TXD_1	Yes	Reserved	RGMII2_TD1		
221	ETH_2_RGMII_TXD_0	Yes	Reserved	RGMII2_TD0		
223	GND	Yes	Always Compatible		GND	
225	ETH_1_MDI0_P	Yes	Always Compatible		TD_P_A	Ethernet PHY
227	ETH_1_MDI0_N	Yes	Always Compatible		TD_M_A	Ethernet PHY
229	GND	Yes	Always Compatible		GND	

Continued on next page

Table 7: X1 pin assignment - top side - odd pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
231	ETH_1_MDI1_N	Yes	Always Compatible		TD_M_B	Ethernet PHY
233	ETH_1_MDI1_P	Yes	Always Compatible		TD_P_B	Ethernet PHY
235	ETH_1_LED_1	Yes	Always Compatible		Circuit	Ethernet 1 Link
237	ETH_1_LED_2	Yes	Always Compatible		Circuit	Ethernet 1 Active
239	ETH_1_MDI2_P	Yes	Always Compatible		TD_P_C	Ethernet PHY
241	ETH_1_MDI2_N	Yes	Always Compatible		TD_M_C	Ethernet PHY
243	GND	Yes	Always Compatible		GND	
245	ETH_1_MDI3_N	Yes	Always Compatible		TD_M_D	Ethernet PHY
247	ETH_1_MDI3_P	Yes	Always Compatible		TD_P_D	Ethernet PHY
249	VCC_BACKUP	Yes	Always Compatible		RTC Battery	
251	VCC	Yes	Always Compatible		VCC	3.135 to 5.5V input.
253	VCC	Yes	Always Compatible		VCC	3.135 to 5.5V input.
255	VCC	Yes	Always Compatible		VCC	3.135 to 5.5V input.
257	VCC	Yes	Always Compatible		VCC	3.135 to 5.5V input.
259	VCC	Yes	Always Compatible		VCC	3.135 to 5.5V input.

Table 8: X1 pin assignment - bottom side - even pins

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
2	ADC_1	Yes	Reserved		ADC_1	ADC channel 1.
4	ADC_2	Yes	Reserved		ADC_2	ADC channel 2.
6	ADC_3	Yes	Reserved		ADC_3	ADC channel 3.
8	ADC_4	Yes	Reserved		ADC_4	ADC channel 3.
10	GND	Yes	Always Compatible		GND	
12	I2C_1_SDA	Yes	Always Compatible	I2C0_SDA		
14	I2C_1_SCL	Yes	Always Compatible	I2C0_SCL		
16	PWM_2	Yes	Reserved	MMC2_SDCD		
18	GND	Yes	Always Compatible		GND	
20	CAN_1_TX	Yes	Reserved	MCAN0_TX		
22	CAN_1_RX	Yes	Reserved	MCAN0_RX		
24	CAN_2_TX	Yes	Reserved	MCU_MCAN0_TX		Interrupts are available only on R5F core.
26	CAN_2_RX	Yes	Reserved	MCU_MCAN0_RX		Interrupts are available only on R5F core.
28	GND	Yes	Always Compatible		GND	
30	I2S_1_BCLK	Yes	Reserved	MCASP0_ACLKX		
32	I2S_1_SYNC	Yes	Reserved	MCASP0_AFSX		
34	I2S_1_D_OUT	Yes	Reserved	MCASP0_AXR0		
36	I2S_1_D_IN	Yes	Reserved	MCASP0_AXR1		
38	I2S_1_MCLK	Yes	Reserved	VOUT0_DATA3		
40	GND	Yes	Always Compatible		GND	
42	I2S_2_BCLK	Yes	Reserved	GPMC0_BE0n_CLE		
44	I2S_2_SYNC	Yes	Reserved	GPMC0_WAIT0		
46	I2S_2_D_OUT	Yes	Reserved	GPMC0_WEn		

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Table 8: X1 pin assignment - bottom side - even pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
48	I2S_2_D_IN	Yes	Reserved	GPMC0_OEn_REn		
50	GND	Yes	Always Compatible		GND	
52	QSPI_1_CLK	Yes	Reserved	OSPI0_CLK		
54	QSPI_1_CS#	Yes	Reserved	OSPI0_CSn0		
56	QSPI_1_IO0	Yes	Reserved	OSPI0_D0		
58	QSPI_1_IO1	Yes	Reserved	OSPI0_D1		
60	QSPI_1_IO2	Yes	Reserved	OSPI0_D2		
62	QSPI_1_IO3	Yes	Reserved	OSPI0_D3		
64	QSPI_1_CS2#	Yes	Reserved	OSPI0_CSn1		
66	QSPI_1_DQS	Yes	Reserved	OSPI0_DQS		
68	GND	Yes	Always Compatible		GND	
70	SD_1_D2	Yes	Always Compatible	MMC1_DAT2		
72	SD_1_D3	Yes	Always Compatible	MMC1_DAT3		
74	SD_1_CMD	Yes	Always Compatible	MMC1_CMD		
76	SD_1_PWR_EN	Yes	Always Compatible	VOUT0_DATA2		
78	SD_1_CLK	Yes	Always Compatible	MMC1_CLK		
80	SD_1_D0	Yes	Always Compatible	MMC1_DAT0		
82	SD_1_D1	Yes	Always Compatible	MMC1_DAT1		
84	SD_1_CD#	Yes	Always Compatible	MMC1_SDCD		
86	GND	Yes	Always Compatible		GND	
88	MSP_1	-	Module-specific	OLDI0_CLK0N		
90	MSP_2	-	Module-specific	OLDI0_CLK0P		
92	MSP_3	-	Module-specific	GPMC0_CSn3		

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Table 8: X1 pin assignment - bottom side - even pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
94	MSP_4	-	Module-specific	OLDI0_A0N		
96	MSP_5	-	Module-specific	OLDI0_A0P		
98	GND	Yes	Always Compatible		GND	
100	MSP_6	-	Module-specific	OLDI0_A1N		
102	MSP_7	-	Module-specific	OLDI0_A1P		
104	MSP_8	-	Module-specific	GPMC0_CSn2		
106	MSP_9	-	Module-specific	OLDI0_A2N		
108	MSP_10	-	Module-specific	OLDI0_A2P		
110	GND	Yes	Always Compatible		GND	
112	MSP_11	-	Module-specific	OLDI0_A3N		
114	MSP_12	-	Module-specific	OLDI0_A3P		
116	MSP_13	-	Module-specific	MCU_MCAN1_RX		Interrupts are available only on R5F core.
118	MSP_14	-	Module-specific	OLDI0_CLK1N		
120	MSP_15	-	Module-specific	OLDI0_CLK1P		
122	GND	Yes	Always Compatible		GND	
124	MSP_16	-	Module-specific	OLDI0_A4N		
126	MSP_17	-	Module-specific	OLDI0_A4P		
128	MSP_18	-	Module-specific	MCU_MCAN1_TX		Interrupts are available only on R5F core.
130	MSP_19	-	Module-specific	OLDI0_A5N		
132	MSP_20	-	Module-specific	OLDI0_A5P		
134	GND	Yes	Always Compatible		GND	
136	MSP_21	-	Module-specific	OLDI0_A6N		
138	MSP_22	-	Module-specific	OLDI0_A6P		

Continued on next page

Table 8: X1 pin assignment - bottom side - even pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
140	MSP_23	-	Module-specific		RTC_IRQ#	
142	MSP_24	-	Module-specific	OLDI0_A7N		
144	MSP_25	-	Module-specific	OLDI0_A7P		
146	GND	Yes	Always Compatible			
148	MSP_26	-	Module-specific		PCM_CLK / SPI0_CLK	PCM on WiFi Module. SPI assembly option modules w/o Wi-Fi
150	MSP_27	-	Module-specific		PCM_DIN / SPI0_MOSI	PCM on WiFi Module. SPI assembly option modules w/o Wi-Fi
152	MSP_28	-	Module-specific		PCM_DOUT / SPI0_MISO	PCM on WiFi Module. SPI assembly option modules w/o Wi-Fi
154	MSP_29	-	Module-specific		PCM_SYNC / SPI0_CS#	PCM on WiFi Module. SPI assembly option modules w/o Wi-Fi
156	MSP_30	-	Module-specific	MMC2_CLK		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
158	GND	Yes	Always Compatible		GND	
160	MSP_31	-	Module-specific	MMC2_CMD		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
162	MSP_32	-	Module-specific	MMC2_DAT0		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
164	MSP_33	-	Module-specific	MMC2_DAT1		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
166	MSP_34	-	Module-specific	MMC2_DAT2		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
168	MSP_35	-	Module-specific	MMC2_DAT3		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
170	GND	Yes	Always Compatible		GND	
172	MSP_36	-	Module-specific		BT_WAKE_HOST	WiFi/BT module
174	MSP_37	-	Module-specific		WLAN_WAKE_HOST	WiFi/BT module
176	MSP_38	-	Module-specific		PCM_MCLK	WiFi/BT module
178	MSP_39	-	Module-specific		WCI_SIN	WiFi/BT module
180	MSP_40	-	Module-specific		WCI_SOUT	WiFi/BT module
182	GND	Yes	Always Compatible		GND	
184	MSP_41	-	Module-specific	VOUT0_PCLK		UART2_CTSn (Alt Mode)

Continued on next page

Table 8: X1 pin assignment - bottom side - even pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
186	MSP_42	-	Module-specific	VOUT0_VSYNC		UART2_RTSn (Alt Mode)
188	MSP_43	-	Module-specific	MCU_SPI0_CS0		MCU_GPIO0
190	MSP_44	-	Module-specific	VOUT0_DATA1		UART2_TXD (Alt Mode)
192	MSP_45	-	Module-specific	VOUT0_DATA0		UART2_RXD (Alt Mode)
194	GND	Yes	Always Compatible		GND	
196	SPI_1_CLK	Yes	Always Compatible	OSPI0_D5		
198	SPI_1_MISO	Yes	Always Compatible	OSPI0_D7		
200	SPI_1_MOSI	Yes	Always Compatible	OSPI0_D6		
202	SPI_1_CS	Yes	Always Compatible	OSPI0_D4		
204	GND	Yes	Always Compatible		GND	
206	GPIO_1	Yes	Always Compatible	MCU_SPI0_CS1		
208	GPIO_2	Yes	Always Compatible	MCU_SPI0_CLK		
210	GPIO_3	Yes	Always Compatible	MCU_SPI0_D0		
212	GPIO_4	Yes	Always Compatible	MCU_SPI0_D1		
214	PWR_1V8_MOCI	Yes	Always Compatible		1.8V	
216	GPIO_5_CSI	Yes	Always Compatible	VOUT0_DATA4		
218	GPIO_6_CSI	Yes	Always Compatible	VOUT0_DATA5		
220	GPIO_7_CSI	Yes	Always Compatible	VOUT0_DATA6		
222	GPIO_8_CSI	Yes	Always Compatible	VOUT0_DATA7		
224	GND	Yes	Always Compatible		GND	
226	PCIE_1_CLK_N	No	Reserved		NC	Not connected
228	PCIE_1_CLK_P	No	Reserved		NC	Not connected
230	GND	Yes	Always Compatible		GND	

Continued on next page

Table 8: X1 pin assignment - bottom side - even pins (Continued)

X1 Pin	Verdin Specification signal name	Family compatible function	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
232	PCIE_1_L0_RX_N	No	Reserved		NC	Not connected
234	PCIE_1_L0_RX_P	No	Reserved		NC	Not connected
236	GND	Yes	Always Compatible		GND	
238	PCIE_1_L0_TX_N	No	Reserved		NC	Not connected
240	PCIE_1_L0_TX_P	No	Reserved		NC	Not connected
242	GND	Yes	Always Compatible		GND	
244	PCIE_1_RESET#	Yes	Reserved	OSPI0_CSn3		
246	CTRL_RECOVERY_MICO#	Yes	Always Compatible		Recvery Cirucuit	
248	CTRL_PWR_BTN_MICO#	Yes	Always Compatible		EN/BP/VSENSE	PMIC
250	CTRL_FORCE_OFF_MOCI#	Yes	Always Compatible		Circuit	
252	CTRL_WAKE1_MICO#	Yes	Always Compatible	OSPI0_LBCLKO		
254	CTRL_PWR_EN_MOCI	Yes	Always Compatible		Circuit	
256	CTRL_SLEEP_MOCI#	No	Always Compatible		P0	I2C GPIO Expander
258	CTRL_RESET_MOCI#	Yes	Always Compatible		Circuit	
260	CTRL_RESET_MICO#	Yes	Always Compatible	MCU_PORz	PMIC: nRSTOUT	

4 I/O Pins

4.1 Function Multiplexing

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the Table 10 on page 32, there is a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

4.2 SoC Functions List

Table 10 on page 32 contains a list of all the SoC pins that are available on the SODIMM connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT7 function. The alternate functions used to provide the primary interfaces, done to ensure the best compatibility with other Verdin modules, are highlighted in **bold**.

Table 9: Function short forms

Short form	Name
ADC	Analog to Digital Converter input
CAN	Controller Area Network
CSI	Camera Serial Interface
CPTS	Common Platform Time Sync
DDR	Double Data Rate (RAM specification)
DSI	Display Serial Interface
EHRPWM	Enhanced High-Resolution Pulse-Width Modulator
ECAP	Enhanced Capture
ECC	Error-Correcting Code (RAM feature)
EMAC	Ethernet Media Access Control
EMMC	Embedded Multimedia Card
ENET	Ethernet
EQEP	Enhanced Quadrature Encoder Pulse
GPIO	General-Purpose Input Output
GPMC	General Purpose Memory Controller
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
ISP	Image Signal Processor
JTAG	Joint Test Action Group (test/debug interface)
LVDS	FPD-Link/FlatLink Display interface
MCAN	Modular Controller Area Network
MCASP	Multichannel Audio Serial Port
MCU	Micro Conroller Unit
MIPI_CSI	MIPI CSI Subsystem
MIPI_DSI	MIPI DSI Subsystem

Continued on next page

Table 9: Function short forms (Continued)

Short form	Name
MSP	"Module-specific"
NAND	Interface for NAND Flash
NPU	Neural Processing Unit
OLDI	Open LVDS Display Interface
OSPI	Octal Serial Peripheral Interface
PCIE	PCI Express
PDM	Pulse-Density Modulation Microphone Input
PRU	Programmable Real-Time Unit
PRUSS	Programmable Real-Time Unit Subsystem
PWM	Pulse Width Modulation output
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
TRC	Trace (Arm TPIU compliant Trace Port interface)
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WKUP	Wake-Up

4.2.1 Alternate Functions

Table 10: Alternate Functions

Pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
1	TDI	E13	**TDI**									
3	TRSTn	B13	**TRSTn**									
5	TDO	C14	**TDO**									
9	TCK	C13	**TCK**									
13	TMS	E14	**TMS**									
15	MMC2_SDWP	K25	MMC2_SDWP	MCASP1_AFSX		UART4_TXD	**EHRPWM2_B**	EHRPWM_TZn_IN2		GPIO0_72		
17	GPMC0_WAIT1	AD24	GPMC0_WAIT1	VOUT0_EXTPCLKIN	GPMC0_A21	UART6_RXD				**GPIO0_38**	EQEP2_I	
19	SPI0_CS1	E20	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	**EHRPWM0_B**	ECAP0_IN_APWM_OUT		MAIN_ERRORn		GPIO1_16		EHRPWM_TZn_IN5
21	GPMC0_WPn	P24	GPMC0_WPn	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD			TRC_DATA13	**GPIO0_39**		
23	DSI0_TXN3	AE14	**DSI0_TXN3**									
25	DSI0_TXP3	AE15	**DSI0_TXP3**									
29	DSI0_TXN2	AC12	**DSI0_TXN2**									
31	DSI0_TXP2	AC13	**DSI0_TXP2**									
35	DSI0_TXCLKN	AA12	**DSI0_TXCLKN**									
37	DSI0_TXCLKP	AA13	**DSI0_TXCLKP**									
41	DSI0_TXN1	AB13	**DSI0_TXN1**									
43	DSI0_TXP1	AB14	**DSI0_TXP1**									
47	DSI0_TXN0	AD11	**DSI0_TXN0**									
49	DSI0_TXP0	AD12	**DSI0_TXP0**									
53	I2C1_SDA	B24	**I2C1_SDA**	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO			GPIO1_29	EHRPWM2_B	MMC2_SDWP
55	I2C1_SCL	C24	**I2C1_SCL**	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI			GPIO1_28	EHRPWM2_A	MMC2_SDCD
57	MCU_I2C0_SDA	D11	**MCU_I2C0_SDA**							MCU_GPIO0_18		
59	MCU_I2C0_SCL	E11	**MCU_I2C0_SCL**							MCU_GPIO0_17		
61	MCU_UART0_CTSn	B8	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				**MCU_GPIO0_7**		

Continued on next page

Table 10: Alternate Functions (Continued)

Pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
63	MCU_UART0_RTSn	B7	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				**MCU_GPIO0_8**		
91	WKUP_CLKOUT0	F13	**WKUP_CLKOUT0**							MCU_GPIO0_23		
93	UART0_RTSn	C22	UART0_RTSn	SPI0_CS3	**I2C3_SDA**	UART2_TXD	TIMER_IO7	AUDIO_EXT_REFCLK1		GPIO1_23	MCASP2_ACLKX	MMC2_SDWP
95	UART0_CTSn	A23	UART0_CTSn	SPI0_CS2	**I2C3_SCL**	UART2_RXD	TIMER_IO6	AUDIO_EXT_REFCLK0		GPIO1_22	MCASP2_AFSX	MMC2_SDCD
99	CSI0_RXP3	AD8	**CSI0_RXP3**									
101	CSI0_RXN3	AD9	**CSI0_RXN3**									
105	CSI0_RXP2	AA9	**CSI0_RXP2**									
107	CSI0_RXN2	AA10	**CSI0_RXN2**									
111	CSI0_RXCLKP	AE11	**CSI0_RXCLKP**									
113	CSI0_RXCLKN	AE12	**CSI0_RXCLKN**									
117	CSI0_RXP1	AC9	**CSI0_RXP1**									
119	CSI0_RXN1	AC10	**CSI0_RXN1**									
123	CSI0_RXP0	AB10	**CSI0_RXP0**									
125	CSI0_RXN0	AB11	**CSI0_RXN0**									
129	MCASP0_AFSR	G23	MCASP0_AFSR	SPI2_CS0	**UART1_RXD**				EHRPWM0_A	GPIO1_13	EQEP1_S	
131	MCASP0_ACLKR	G20	MCASP0_ACLKR	SPI2_CLK	**UART1_TXD**				EHRPWM0_B	GPIO1_14	EQEP1_I	
133	MCASP0_AXR2	E25	MCASP0_AXR2	SPI2_D1	**UART1_RTSn**	UART6_TXD		ECAP2_IN_APWM_OUT		GPIO1_8	EQEP0_B	
135	MCASP0_AXR3	D25	MCASP0_AXR3	SPI2_D0	**UART1_CTSn**	UART6_RXD		ECAP1_IN_APWM_OUT		GPIO1_7	EQEP0_A	
137	WKUP_UART0_RXD	D8	**WKUP_UART0_RXD**		MCU_SPI0_CS2					MCU_GPIO0_9		
139	WKUP_UART0_TXD	D7	**WKUP_UART0_TXD**		MCU_SPI1_CS2					MCU_GPIO0_10		
141	WKUP_UART0_RTSn	C6	**WKUP_UART0_RTSn**	WKUP_TIMER_IO1		MCU_SPI1_CLK				MCU_GPIO0_12		
143	WKUP_UART0_CTSn	C7	**WKUP_UART0_CTSn**	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11		
147	UART0_RXD	A22	**UART0_RXD**	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A				GPIO1_20		

Continued on next page

Table 10: Alternate Functions (Continued)

Pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
149	UART0_TXD	B22	**UART0_TXD**	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B				GPIO1_21		
151	MCU_UART0_RXD	B6	**MCU_UART0_RXD**							MCU_GPIO0_5		
153	MCU_UART0_TXD	C8	**MCU_UART0_TXD**							MCU_GPIO0_6		
155	USB0_DRVVBUS	G22	**USB0_DRVVBUS**							GPIO1_50		
157	GPMC0_ADVn_ALE	R25	GPMC0_ADVn_ALE		MCASP1_AXR2				TRC_DATA7	**GPIO0_32**		
159	USB0_VBUS	Y7	**USB0_VBUS**									
161	GPMC0_CLK	Y25	**GPMC0_CLK**		MCASP1_AXR3	GPMC0_FCLK_MUX			TRC_DATA6	**GPIO0_31**		
163	USB0_DM	AE8	**USB0_DM**									
165	USB0_DP	AE7	**USB0_DP**									
181	USB1_DM	AE10	**USB1_DM**									
183	USB1_DP	AE9	**USB1_DP**									
185	USB1_DRVVBUS	G21	**USB1_DRVVBUS**							GPIO1_51		
187	GPMC0_CSn0	T23	GPMC0_CSn0			MCASP2_AXR14			TRC_DATA15	**GPIO0_41**		
189	GPMC0_CSn1	U23	GPMC0_CSn1			MCASP2_AXR15			TRC_DATA16	**GPIO0_42**		
191	MDIO0_MDIO	F16	**MDIO0_MDIO**							GPIO0_85		
193	MDIO0_MDC	F17	**MDIO0_MDC**							GPIO0_86		
197	RGMII2_RXC	D19	**RGMII2_RXC**	RMII2_REF_CLK	MCASP2_AXR1					GPIO1_2		
199	RGMII2_RX_CTL	F19	**RGMII2_RX_CTL**	RMII2_RX_ER	MCASP2_AXR3					GPIO1_1		
201	RGMII2_RD0	E19	**RGMII2_RD0**	RMII2_RXD0	MCASP2_AXR2					GPIO1_3		
203	RGMII2_RD1	E16	**RGMII2_RD1**	RMII2_RXD1	MCASP2_AFSR			MCASP2_AXR7		GPIO1_4		
205	RGMII2_RD2	E17	**RGMII2_RD2**		MCASP2_AXR0					GPIO1_5	EQEP2_A	
207	RGMII2_RD3	C19	**RGMII2_RD3**		AUDIO_EXT_REFCLK0					GPIO1_6	EQEP2_B	
211	RGMII2_TX_CTL	A20	**RGMII2_TX_CTL**	RMII2_TX_EN	MCASP2_AXR4					GPIO0_87		

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Table 10: Alternate Functions (Continued)

Pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
213	RGMII2_TXC	D16	**RGMII2_TXC**	RMII2_CRS_DV	MCASP2_AXR5					GPIO0_88		
215	RGMII2_TD3	A19	**RGMII2_TD3**	CLKOUT0	MCASP2_ACLKX					GPIO1_0	EQEP2_S	
217	RGMII2_TD2	D17	**RGMII2_TD2**		MCASP2_AFSX					GPIO0_91	EQEP2_I	
219	RGMII2_TD1	A21	**RGMII2_TD1**	RMII2_TXD1	MCASP2_ACLKR			MCASP2_AXR8		GPIO0_90		
221	RGMII2_TD0	B19	**RGMII2_TD0**	RMII2_TXD0	MCASP2_AXR6					GPIO0_89		
12	I2C0_SDA	A24	**I2C0_SDA**		SPI2_CS2	TIMER_IO5	UART1_DSRn	EQEP2_B	EHRPWM_SOCB	GPIO1_27	ECAP2_IN_APWM_OUT	
14	I2C0_SCL	B25	**I2C0_SCL**		SYNC0_OUT	OBSCLK1	UART1_DCDn	EQEP2_A	EHRPWM_SOCA	GPIO1_26	ECAP1_IN_APWM_OUT	SPI2_CS0
16	MMC2_SDCD	J25	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD	**EHRPWM2_A**	EHRPWM_TZn_IN1		GPIO0_71		
20	MCAN0_TX	B23	**MCAN0_TX**	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I		GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3
22	MCAN0_RX	F20	**MCAN0_RX**	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S		GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4
24	MCU_MCAN0_TX	E8	**MCU_MCAN0_TX**	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13		
26	MCU_MCAN0_RX	D6	**MCU_MCAN0_RX**	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14		
30	MCASP0_ACLKX	F24	**MCASP0_ACLKX**	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A	
32	MCASP0_AFSX	F25	**MCASP0_AFSX**	SPI2_CS3	AUDIO_EXT_REFCLK1					GPIO1_12	EQEP1_B	
34	MCASP0_AXR0	F23	**MCASP0_AXR0**		AUDIO_EXT_REFCLK0				EHRPWM1_B	GPIO1_10	EQEP0_I	
36	MCASP0_AXR1	E24	**MCASP0_AXR1**	SPI2_CS2	ECAP1_IN_APWM_OUT			MAIN_ERRORn	EHRPWM1_A	GPIO1_9	EQEP0_S	
38	VOUT0_DATA3	Y23	VOUT0_DATA3	GPMC0_A3			UART3_TXD	**AUDIO_EXT_REFCLK0**		GPIO0_48		
42	GPMC0_BE0n_CLE	U24	GPMC0_BE0n_CLE		**MCASP1_ACLKX**				TRC_DATA10	GPIO0_35		
44	GPMC0_WAIT0	AA24	GPMC0_WAIT0		**MCASP1_AFSX**				TRC_DATA12	GPIO0_37		
46	GPMC0_WEn	T25	GPMC0_WEn		**MCASP1_AXR0**				TRC_DATA9	GPIO0_34		
48	GPMC0_OEn_REn	R24	GPMC0_OEn_REn		**MCASP1_AXR1**				TRC_DATA8	GPIO0_33		
52	OSPI0_CLK	P23	**OSPI0_CLK**							GPIO0_0		
54	OSPI0_CSn0	M25	**OSPI0_CSn0**							GPIO0_11		

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Table 10: Alternate Functions (Continued)

Pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
56	OSPI0_D0	L25	**OSPI0_D0**							GPIO0_3		
58	OSPI0_D1	N24	**OSPI0_D1**							GPIO0_4		
60	OSPI0_D2	N25	**OSPI0_D2**							GPIO0_5		
62	OSPI0_D3	M24	**OSPI0_D3**							GPIO0_6		
64	OSPI0_CSn1	L24	**OSPI0_CSn1**							GPIO0_12		
66	OSPI0_DQS	P22	**OSPI0_DQS**					UART5_CTSn		GPIO0_2		
70	MMC1_DAT2	H22	**MMC1_DAT2**	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD	MCAN1_RX	SPI1_D1	SPI2_CS3	GPIO1_43		
72	MMC1_DAT3	H25	**MMC1_DAT3**	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD	MCAN1_TX	SPI1_D0	SPI2_CS1	GPIO1_42		
74	MMC1_CMD	H20	**MMC1_CMD**		TIMER_IO5	UART3_TXD		SPI1_CLK	SPI2_CS0	**GPIO1_47**		
76	VOUT0_DATA2	AA23	VOUT0_DATA2	GPMC0_A2			UART3_RXD			GPIO0_47		
78	MMC1_CLK	J24	**MMC1_CLK**		TIMER_IO4	UART3_RXD		SPI1_CS0	SPI2_CS2	GPIO1_46		
80	MMC1_DAT0	H21	**MMC1_DAT0**	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_APWM_OUT		SPI2_D1	GPIO1_45		
82	MMC1_DAT1	H23	**MMC1_DAT1**	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APWM_OUT	SPI1_CS2	SPI2_D0	GPIO1_44		
84	MMC1_SDCD	D23	**MMC1_SDCD**	UART6_RXD	TIMER_IO6	UART3_RTSn	MCAN1_TX	SPI1_CS3	SPI2_CLK	GPIO1_48		
88	OLDI0_CLK0N	AE18	OLDI0_CLK0N									
90	OLDI0_CLK0P	AE17	OLDI0_CLK0P									
92	GPMC0_CSn3	U25	GPMC0_CSn3	I2C2_SDA	GPMC0_A20	UART4_TXD	MCASP1_AXR5	MCAN1_RX	TRC_DATA18	GPIO0_44	MCASP1_ACLKR	
94	OLDI0_A0N	AE20	OLDI0_A0N									
96	OLDI0_A0P	AD20	OLDI0_A0P									
100	OLDI0_A1N	AC19	OLDI0_A1N									
102	OLDI0_A1P	AD19	OLDI0_A1P									
104	GPMC0_CSn2	T22	GPMC0_CSn2	I2C2_SCL	MCASP1_AXR4	UART4_RXD		MCAN1_TX	TRC_DATA17	GPIO0_43	MCASP1_AFSR	
106	OLDI0_A2N	AA19	OLDI0_A2N									

Continued on next page

Table 10: Alternate Functions (Continued)

Pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
108	OLDI0_A2P	AB19	OLDI0_A2P									
112	OLDI0_A3N	AD18	OLDI0_A3N									
114	OLDI0_A3P	AE19	OLDI0_A3P									
116	MCU_MCAN1_RX	E7	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16		
118	OLDI0_CLK1N	AD15	OLDI0_CLK1N									
120	OLDI0_CLK1P	AD14	OLDI0_CLK1P									
124	OLDI0_A4N	AD17	OLDI0_A4N									
126	OLDI0_A4P	AD16	OLDI0_A4P									
128	MCU_MCAN1_TX	F8	MCU_MCAN1_TX	MCU_TIMER_IO2		MCU_SPI1_CS1	MCU_EXT_REFCLK0			MCU_GPIO0_15		
130	OLDI0_A5N	AB17	OLDI0_A5N									
132	OLDI0_A5P	AC17	OLDI0_A5P									
136	OLDI0_A6N	AC16	OLDI0_A6N									
138	OLDI0_A6P	AC15	OLDI0_A6P									
142	OLDI0_A7N	AB16	OLDI0_A7N									
144	OLDI0_A7P	AA16	OLDI0_A7P									
148	SPI0_CLK	B21	SPI0_CLK	CP_GEMAC_CPTS0_TS_SYNC	EHRPWM1_A					GPIO1_17		
150	SPI0_D0	B20	SPI0_D0	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B					GPIO1_18		
152	SPI0_D1	C21	SPI0_D1	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM1_TZn_IN0					GPIO1_19		
154	SPI0_CS0	D20	SPI0_CS0		EHRPWM0_A					GPIO1_15		
156	MMC2_CLK	K21	MMC2_CLK	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD	EHRPWM0_SYNCI		I2C3_SCL	GPIO0_69		
160	MMC2_CMD	K24	MMC2_CMD	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD	EHRPWM0_SYNCO	EHRPWM_TZn_IN0	I2C3_SDA	GPIO0_70		
162	MMC2_DAT0	K23	MMC2_DAT0	MCASP1_AXR0			EHRPWM1_B	I2C2_SCL		GPIO0_68		
164	MMC2_DAT1	K22	MMC2_DAT1	MCASP1_AXR1			EHRPWM1_A	I2C2_SDA		GPIO0_67		

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Table 10: Alternate Functions (Continued)

Pin	SoC ball name	SoC ball ID	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
166	MMC2_DAT2	L20	MMC2_DAT2	MCASP1_AXR2		UART5_TXD	EHRPWM0_B	I2C2_SDA		GPIO0_66		
168	MMC2_DAT3	L21	MMC2_DAT3	MCASP1_AXR3		UART5_RXD	EHRPWM0_A			GPIO0_65		
172	WIFI_BT_WKUP_HOST#	AD21	VOUT0_DATA12	GPMC0_A14			UART4_RTSn			GPIO0_59		
174	WiFi_W_WKUP_HOST#	L22	OSPI0_CSn2	SPI1_CS1	OSPI0_RESET_OUT1	MCASP1_AFSR	MCASP1_AXR2	UART5_RXD		GPIO0_13		
184	VOUT0_PCLK	Y21	VOUT0_PCLK	GPMC0_A19			UART2_CTSn			GPIO0_64		
186	VOUT0_VSYNC	W20	VOUT0_VSYNC	GPMC0_A18			UART2_RTSn			GPIO0_63		
188	MCU_SPI0_CS0	B10	MCU_SPI0_CS0				WKUP_TIMER_IO1			MCU_GPIO0_0		
190	VOUT0_DATA1	W23	VOUT0_DATA1	GPMC0_A1			UART2_TXD			GPIO0_46		
192	VOUT0_DATA0	AE24	VOUT0_DATA0	GPMC0_A0			UART2_RXD			GPIO0_45		
196	OSPI0_D5	N22	OSPI0_D5	**SPI1_CLK**	MCASP1_AXR0	UART6_TXD				GPIO0_8		
198	OSPI0_D7	N20	OSPI0_D7	**SPI1_D1**	MCASP1_AFSX	UART6_CTSn				GPIO0_10		
200	OSPI0_D6	P21	OSPI0_D6	**SPI1_D0**	MCASP1_ACLKX	UART6_RTSn				GPIO0_9		
202	OSPI0_D4	N21	OSPI0_D4	**SPI1_CS0**	MCASP1_AXR1	UART6_RXD				GPIO0_7		
206	MCU_SPI0_CS1	E10	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			**MCU_GPIO0_1**		
208	MCU_SPI0_CLK	C10	MCU_SPI0_CLK							**MCU_GPIO0_2**		
210	MCU_SPI0_D0	B11	MCU_SPI0_D0							**MCU_GPIO0_3**		
212	MCU_SPI0_D1	D10	MCU_SPI0_D1							**MCU_GPIO0_4**		
216	VOUT0_DATA4	AB23	VOUT0_DATA4	GPMC0_A4			UART4_RXD	EQEP2_I		**GPIO0_49**		
218	VOUT0_DATA5	AD23	VOUT0_DATA5	GPMC0_A5			UART4_TXD	EQEP2_S		**GPIO0_50**		
220	VOUT0_DATA6	AC23	VOUT0_DATA6	GPMC0_A6			UART5_RXD	EQEP2_A		**GPIO0_51**		
222	VOUT0_DATA7	AE23	VOUT0_DATA7	GPMC0_A7			UART5_TXD	EQEP2_B		**GPIO0_52**		
244	OSPI0_CSn3	L23	OSPI0_CSn3	OSPI0_RESET_OUT0	OSPI0_ECC_FAIL	MCASP1_ACLKR	MCASP1_AXR3	UART5_TXD		**GPIO0_14**		
252	OSPI0_LBCLKO	N23	OSPI0_LBCLKO					UART5_RTSn		**GPIO0_1**		

***Bold** text*: Alternate function which provides maximum compatibility between modules of the same family.
Rows in ■: "Module-specific" interface.
Rows in ■: "Boot source selection pin at startup (also "Module-specific").

5 Interface Description

5.1 ADC – Analog to Digital Converter

The Verdin AM62P has four analog inputs, with 0 to 3.3V input range, 12-bit resolution, and a sampling rate of up to 3300 samples per second. The analog inputs can be used in single-ended mode, or in differential mode with either ADC_1 or ADC_3 as inverted input.

The analog-to-digital conversion is handled by the TLA2024 ADC from Texas Instruments, as the AM62P SoC does not feature an analog-to-digital converter. The TLA2024 is a low-power delta-sigma ADC with integrated voltage reference and oscillator. See the TLA2024 Datasheet[1] for more information on the ADC functional modes, specifications, and register maps.

The AM62P SoC communicates with the TLA2024 ADC through the SoC's I2C0 I²C interface, with the ADC on address `0x49`. The I2C0 port is also shared with other peripherals such as the on-module PMIC, RTC, TPM, and EEPROM.

The ADC features a programmable gain amplifier, allowing input ranges from 256mV (0.125mV/LSB) to 3.3V (2mV/LSB). To use the 3.3V range, the Full-Scale Range (FSR) of the amplifier should be set to 4.096V, although the full 4.096V range is not achievable due to the amplifier's supply voltage of 3.3V.

Table 11: ADC voltage ranges

ADC FSR mode	Input voltage range	ADC resolution	Remark
±0.256 V	0 to 256 mV	0.125 mV/LSB	
±0.512 V	0 to 512 mV	0.25 mV/LSB	
±1.024 V	0 to 1.024 V	0.5 mV/LSB	
±2.048 V	0 to 2.048 V	1 mV/LSB	
±4.096 V	0 to 3.3 V	2 mV/LSB	Input voltage range is limited by ADC's supply voltage (3.3V)
±6.144 V	0 to 3.3 V	3 mV/LSB	Input voltage range is limited by ADC's supply voltage (3.3V)

To maintain compatibility with other Verdin modules, it is recommended to keep the analog signal voltages in the 0 to 1.8V range as per Verdin family specification. The differential input mode is not part of the Verdin standard and potentially not compatible with other modules.

The analog input pins are part of a reserved Verdin interface, with guaranteed electrical compatibility within modules of the Verdin family.

Table 12: ADC pins even pins (bottom)

X1 pin	Verdin spec. signal name	TLA2024 pin name	I/O *SoM perspective*	Description
2	ADC_1	AIN3	I	Analog input 1, may be also used as inverted input in differential mode with ADC_2, ADC_3, and ADC_4
4	ADC_2	AIN2	I	Analog input 2
6	ADC_3	AIN1	I	Analog input 3, may be also used as inverted input in differential mode with ADC_4
8	ADC_4	AIN0	I	Analog input 4

[1] https://www.ti.com/lit/ds/symlink/tla2024.pdf

5.2 Display

The Verdin AM62P supports up to two displays while providing independent video pipelines, overlay managers, and video port output processors. The LVDS interface is available as a “module-specific” interface, while the DSI interface is a “reserved” interface bridge.

The TI AM62P SoC display subsystem offloads some of the GPU work by leveraging features such as multi-layer blending with transparency to enable on-the-fly composition, various pixel processing capabilities such as color space conversion and scaling, and the display subsystem DMA engine allows direct access to the frame buffer in the device system memory.

5.2.1 DSI

The Verdin AM62P module supports MIPI-DSI interface directly from the AM62P SoC, offering up-to 4 data lanes, each capable of up-to 2.5Gbps. Details can be found in TI AM62P SoC Technical Reference Manual.

Table 13: DSI Interface Signals

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
35	DSI_1_CLK_N	DSI0_TXCLKN	DSI0_TXCLKN	O	Positive differential DSI Interface clock
37	DSI_1_CLK_P	DSI0_TXCLKP	DSI0_TXCLKP	O	Negative differential DSI Interface clock
47	DSI_1_D0_N	DSI0_TXN0	DSI0_TXN0	O	Positive differential DSI Interface data lane 0
49	DSI_1_D0_P	DSI0_TXP0	DSI0_TXP0	O	Negative differential DSI Interface data lane 0
41	DSI_1_D1_N	DSI0_TXN1	DSI0_TXN1	O	Positive differential DSI Interface data lane 1
43	DSI_1_D1_P	DSI0_TXP1	DSI0_TXP1	O	Negative differential DSI Interface data lane 1
29	DSI_1_D2_N	DSI0_TXN2	DSI0_TXN2	O	Positive differential DSI Interface data lane 2
31	DSI_1_D2_P	DSI0_TXP2	DSI0_TXP2	O	Negative differential DSI Interface data lane 2
23	DSI_1_D3_N	DSI0_TXN3	DSI0_TXN3	O	Positive differential DSI Interface data lane 3
25	DSI_1_D3_P	DSI0_TXP3	DSI0_TXP3	O	Negative differential DSI Interface data lane 3
55	I2C_2_DSI_SCL	I2C1_SCL	I2C1_SCL	I/O	I2C interface, intended to be used as DDC or for controlling DSI bridges on carrier board.
53	I2C_2_DSI_SDA	I2C1_SDA	I2C1_SDA	I/O	
19	PWM_3_DSI	SPI0_CS1	EHRPWM0_B \verify	O	Display backlight brightness control
17	GPIO_9_DSI	GPMC0_WAIT1	GPIO0_38	O	DSI_1_INT#; Interrupt input, intended to be used as hotplug detect or for interrupt messages from DSI bridges on carrier board.
21	GPIO_10_DSI	GPMC0_Wpn	GPIO0_39	I/O	DSI_1_BKL_EN; Display backlight enable

5.2.2 LVDS

The native LVDS signals are located on module-specific pins.
Using module-specific interfaces may prevent compatibility with other Verdin modules. If a LVDS display is used and compatibility with other modules from Verdin Family is required, a MIPI DSI to LVDS bridge on the carrier board should be considered.

The Verdin AM62P supports native LVDS video output at up-to 24-bit color depth through the Open LVDS Display Interface (OLDI) on the SoC (OLDITX0), providing 8 data lanes (pairs) split into 2 channels. The SoC OLDITX1 interface is not available on the X1 connector.

A single channel LVDS interface can support resolutions up to 1920×1080p at 60 frames per second (165MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual-channel configuration, the odd bits are transmitted in the first channel, and the even bits are sent in the second channel.

The LVDS interface is classified as "module-specific", meaning it may not be present on other modules or even when present it may not share the same pins, although we try to keep module-specific interfaces on the same pins to improve module compatibility.

The amount of active data lanes depend on the selected data format. A list with the correlation between active lanes and selected mode can be found on Table 15 on the next page. Detailed information about color mappings and signal timings can be found on the TI AM62P SoC Technical Reference Manual[2].

Table 14: LVDS signals – X1

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
Channel 0					
90	MSP_2	OLDI0_CLK0P	OLDI0_CLK0P	O	
88	MSP_1	OLDI0_CLK0N	OLDI0_CLK0N	O	
96	MSP_5	OLDI0_A0P	OLDI0_A0P	O	
94	MSP_4	OLDI0_A0N	OLDI0_A0N	O	
102	MSP_7	OLDI0_A1P	OLDI0_A1P	O	
100	MSP_6	OLDI0_A1N	OLDI0_A1N	O	
108	MSP_10	OLDI0_A2P	OLDI0_A2P	O	
106	MSP_9	OLDI0_A2N	OLDI0_A2N	O	
114	MSP_12	OLDI0_A3P	OLDI0_A3P	O	
112	MSP_11	OLDI0_A3N	OLDI0_A3N	O	
Channel 1					
120	MSP_15	OLDI0_CLK1P	OLDI0_CLK1P	O	
118	MSP_14	OLDI0_CLK1N	OLDI0_CLK1N	O	
126	MSP_17	OLDI0_A4P	OLDI0_A4P	O	
124	MSP_16	OLDI0_A4N	OLDI0_A4N	O	
132	MSP_20	OLDI0_A5P	OLDI0_A5P	O	
130	MSP_19	OLDI0_A5N	OLDI0_A5N	O	
138	MSP_22	OLDI0_A6P	OLDI0_A6P	O	
136	MSP_21	OLDI0_A6N	OLDI0_A6N	O	

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[2] https://www.ti.com/product/AM62P?keyMatch=am62p&tisearch=universal_search

Table 14: LVDS signals – X1 (Continued)

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
144	MSP_25	OLDI0_A7P	OLDI0_A7P	O	
142	MSP_24	OLDI0_A7N	OLDI0_A7N	O	

Table 15: LVDS modes × Active lanes

Signal pair	Single channel 16-bit	Single channel 16-bit	Single channel 16-bit	Single channel 16-bit
Channel 0				
Ch. 0 Clock	Yes	Yes	Yes	Yes
Ch. 0 Data 0	Yes	Yes	Yes	Yes
Ch. 0 Data 1	Yes	Yes	Yes	Yes
Ch. 0 Data 2	Yes	Yes	Yes	Yes
Ch. 0 Data 3	No	Yes	No	Yes
Channel 1				
Ch. 1 Clock	No	No	Yes	Yes
Ch. 1 Data 0	No	No	Yes	Yes
Ch. 1 Data 1	No	No	Yes	Yes
Ch. 1 Data 2	No	No	Yes	Yes
Ch. 1 Data 3	No	No	No	Yes

5.3 MIPI Camera Serial Interface (MIPI CSI)

The MIPI CSI interface is compatible with single, dual, and quad lane CSI cameras. The interface uses MIPI D-PHY as the physical layer. The interface supports RGB, YUV, and RAW color space definitions. The MIPI CSI interface is in the Reserved class of the Verdin specifications, and is compatible with other Verdin modules.

Table 16: MIPI CSI Interface Signals

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
111	CSI_1_CLK_P	CSI0_RXCLKP	CSI0_RXCLKP	I	Positive differential CSI interface clock signal
113	CSI_1_CLK_N	CSI0_RXCLKN	CSI0_RXCLKN	I	Negative differential CSI interface clock signal
123	CSI_1_D0_P	CSI0_RXN0	CSI0_RXN0	I	Positive differential CSI interface data signal, lane 0
125	CSI_1_D0_N	CSI0_RXP0	CSI0_RXP0	I	Negative differential CSI interface data signal, lane 0
117	CSI_1_D1_P	CSI0_RXN1	CSI0_RXN1	I	Positive differential CSI interface data signal, lane 1
119	CSI_1_D1_N	CSI0_RXP1	CSI0_RXP1	I	Negative differential CSI interface data signal, lane 1
105	CSI_1_D2_P	CSI0_RXN2	CSI0_RXN2	I	Positive differential CSI interface data signal, lane 2
107	CSI_1_D2_N	CSI0_RXP2	CSI0_RXP2	I	Negative differential CSI interface data signal, lane 2

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Table 16: MIPI CSI Interface Signals (Continued)

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
99	CSI_1_D3_P	CSI0_RXN3	CSI0_RXN3	I	Positive differential CSI interface data signal, lane 3
101	CSI_1_D3_N	CSI0_RXP3	CSI0_RXP3	I	Negative differential CSI interface data signal, lane 3

In addition to the MIPI CSI interface pins, the Verdin offers a dedicated I²C interface and a master clock output for the camera.

Table 17: Additional Camera Interface Signals

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
95	I2C_4_CSI_SCL	UART0_CTSn	I2C3_SCL	I/O	Camera control I2C
93	I2C_4_CSI_SDA	UART0_RTSn	I2C3_SDA	I/O	
91	CSI_1_MCLK	WKUP_CLKOUT0	WKUP_CLKOUT0	O	Camera master clock
216	GPIO_5_CSI	VOUT0_DATA4	GPIO0_49	I/O	Dedicated camera GPIO signals
218	GPIO_6_CSI	VOUT0_DATA5	GPIO0_50	I/O	
220	GPIO_7_CSI	VOUT0_DATA6	GPIO0_51	I/O	
222	GPIO_8_CSI	VOUT0_DATA7	GPIO0_52	I/O	

5.4 UART

The AM62P SoC features a total of nine UARTs, of which six are used in the Verdin AM62P SoM and five are exposed. In the Verdin module specifications, there are four standard UARTs available. UART_1 and UART_2 are general-purpose interfaces. Only the RX and TX signals of these interfaces are in the Always Compatible section. In contrast, the additional TS/CTS signals for hardware flow control are located in the Reserved section.

UART_3 is in the Always Compatible section and is intended to be used for the main OS terminal (A53 cores) as a debug port. It could be used for general-purpose, but we recommend making this interface available for debugging purposes. UART_4 is in the Reserved class. This interface is intended to be used for the real-time operating system (R5F core). The interface may be used as a general-purpose UART.

The UARTs of the AM62P SoC can be configured either in the DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) mode. Changing the mode will change the direction of all UART pins (data and all control signals). To ensure compatibility with the entire Verdin family, the SoCs need to be configured in DCE mode, even though the data direction is defined in DTE mode in the Verdin standard.

Particular attention should be paid to the names of the AM62P data signals. In the correct DTE mode, TX and RTS signals are outputs while the RX and CTS signals are inputs. In DCE mode, all signals change their direction. Unfortunately, the data directions of the AM62P SoC are mixed up. In DCE mode, TX and CTS signals are outputs while RX and RTS are inputs. In DTE mode, RX and RTS are outputs, and TX and CTS are inputs. Therefore, the SoC must be set to DCE mode with the RTS and CTS signals swapped on the module. This means the SoC signal UARTx_CTS_B is connected to the UART_x_RTS edge connector pin and vice versa.

Table 18: Always Compatible UART Signal Pins

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
129	UART_1_RXD	MCASP0_AFSR	UART1_RXD	I	Received Data of general-purpose UART_1
131	UART_1_TXD	MCASP0_ACLKR	UART1_TXD	O	Transmitted Data of general-purpose UART_1
133	UART_1_RTS	MCASP0_AXR2	UART1_RTSn / UART6_TXD	O	Request to Send of general-purpose UART_1
135	UART_1_CTS	MCASP0_AXR3	UART1_CTSn / UART6_RXD	I	Clear to Send of general-purpose UART_1
137	UART_2_RXD	WKUP_UART0_RXD	WKUP_UART0_RXD	I	Received Data of general-purpose UART_2
139	UART_2_TXD	WKUP_UART0_TXD	WKUP_UART0_TXD	O	Transmitted Data of general-purpose UART_2
141	UART_2_RTS	WKUP_UART0_RTSn	WKUP_UART0_RTSn	O	Request to Send of general-purpose UART_2
143	UART_2_CTS	WKUP_UART0_CTSn	WKUP_UART0_CTSn	I	Clear to Send of general-purpose UART_2
147	UART_3_RXD	UART0_RXD	UART0_RXD	I	Received Data of A53 debug UART_3
149	UART_3_TXD	UART0_TXD	UART0_TXD	O	Transmitted Data of A53 debug UART_3

Table 19: Reserved UART Signal Pins

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
151	UART_4_RXD	MCU_UART0_RXD	MCU_UART0_RXD	I	Received Data of R5F debug UART_4
153	UART_4_TXD	MCU_UART0_TXD	MCU_UART0_TXD	O	Transmitted Data of R5F debug UART_4

In addition to the UART signals in the Always Compatible and Reserved class, there are UART signals available as alternate functions of other pins. These pins are not compatible with other Verdin modules. Therefore, they should be used very carefully.

Table 20: Alternate Function UART Signal Pins

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
61	HDMI_1_HPD	MCU_UART0_CTSn	MCU_UART0_CTSn	I	Clear to Send of R5F debug UART_4
63	HDMI_1_CEC	MCU_UART0_RTSn	MCU_UART0_RTSn	O	Request to Send of R5F debug UART_4
93	I2C_4_CSI_SDA	UART0_RTSn	UART0_RTSn	O	Request to Send of A53 debug UART_3
95	I2C_4_CSI_SCL	UART0_CTSn	UART0_CTSn	I	Clear to Send of A53 debug UART_3
55	I2C_2_DSI_SCL	I2C1_SCL	UART1_RXD	I	Received Data of general-purpose UART_1
12	I2C_1_SDA	I2C0_SDA	UART1_DSRn	O	Data Set Ready of general-purpose UART_1
14	I2C_1_SCL	I2C0_SCL	UART1_DCDn	I	Data Carrier Detect of general-purpose UART_1
20	CAN_1_TX	MCAN0_TX	UART1_DTRn	O	Data Terminal Ready of general-purpose UART_1
22	CAN_1_RX	MCAN0_RX	UART1_Rin	I	Ring Indicator of general purpose UART_1
190	MSP_44	VOUT0_DATA1	UART2_TXD	O	Transmitted Data of general-purpose UART_6 (default)
70	SD_1_D2	MMC1_DAT2	UART2_TXD	O	Transmitted Data of general-purpose UART_6
93	I2C_4_CSI_SDA	UART0_RTSn	UART2_TXD	O	
190	MSP_44	VOUT0_DATA1	UART2_TXD	O	
192	MSP_45	VOUT0_DATA0	UART2_RXD	I	Received Data of general-purpose UART_6 (default)

Continued on next page

Table 20: Alternate Function UART Signal Pins (Continued)

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
72	SD_1_D3	MMC1_DAT3	UART2_RXD	I	Received Data of general-purpose UART_6
95	I2C_4_CSI_SCL	UART0_CTSn	UART2_RXD	I	
192	MSP_45	VOUT0_DATA0	UART2_RXD	I	
184	MSP_41	VOUT0_PCLK	UART2_CTSn	I	Clear to Send of general-purpose UART_6 (default)
80	SD_1_D0	MMC1_DAT0	UART2_CTSn	I	Clear to Send of general-purpose UART_6
186	MSP_42	VOUT0_VSYNC	UART2_RTSn	O	Request to Send of general-purpose UART_6 (default)
82	SD_1_D1	MMC1_DAT1	UART2_RTSn	O	Request to Send of general-purpose UART_6
38	I2S_1_MCLK	VOUT0_DATA3	UART3_TXD	O	Transmitted Data of general-purpose SoC UART3
74	SD_1_CMD	MMC1_CMD	UART3_TXD	O	
76	SD_1_PWR_EN	VOUT0_DATA2	UART3_RXD	I	Received Data of general-purpose SoC UART3
78	SD_1_CLK	MMC1_CLK	UART3_RXD	I	
84	SD_1_CD#	MMC1_SDCD	UART3_RTSn	O	Request to Send of general-purpose SoC UART3
15	PWM_1	MMC2_SDWP	UART4_TXD	O	Transmitted Data of general-purpose SoC UART4
92	MSP_3	GPMC0_CSn3	UART4_TXD	O	
218	GPIO_6	VOUT0_DATA5	UART4_TXD	O	
16	PWM_2	MMC2_SDCD	UART4_RXD	I	Received Data of general-purpose SoC UART4
104	MSP_8	GPMC0_CSn2	UART4_RXD	I	
216	GPIO_5	VOUT0_DATA4	UART4_RXD	I	
22	CAN_1_RX	MCAN0_RXD	UART5_TXD	O	Transmitted Data of general-purpose SoC UART5
166	MSP_34	MMC2_DAT2	UART5_TXD	O	
222	GPIO_8	VOUT0_DATA7	UART5_TXD	O	
244	PCIE_1_RESET#	OSPI0_CSn3	UART5_TXD	O	
20	CAN_1_TX	MCAN0_TXD	UART5_RXD	I	Received Data of general-purpose SoC UART5
168	MSP_35	MMC2_DAT3	UART5_RXD	I	
220	GPIO_7	VOUT0_DATA6	UART5_RXD	I	
66	QSPI_1_DQS	OSPI0_DQS	UART5_CTSn	I	Clear to Send of general-purpose SoC UART5
252	CTRL_WAKE1_MICO#	OSPI0_LBCLKO	UART5_RTSn	O	Request to Send of general-purpose SoC UART5
160	MSP_31	MMC2_CMD	UART6_TXD	O	Transmitted Data of general-purpose SoC UART6 (Connected to Wi-Fi module)
196	SPI_1_CLK	OSPI0_D5	UART6_TXD	O	
17	DSI_1_INT#	GPMC0_WAIT1	UART6_RXD	I	Received Data of general-purpose SoC UART6 (Connected to Wi-Fi module)
156	MSP_30	MMC2_CLK	UART6_RXD	I	
84	SD_1_CD#	MMC1_SDCD	UART6_RXD	I	
202	SPI_1_CS	OSPI0_D4	UART6_RXD	I	
198	SPI_1_MISO	OSPI0_D7	UART6_CTSn	I	Clear to Send of general-purpose SoC UART6 (Connected to Wi-Fi module)
200	SPI_1_MOSI	OSPI0_D6	UART6_RTSn	O	Request to Send of general-purpose SoC UART6 (Connected to Wi-Fi module)

5.5 PWM

The AM62P features three general-purpose Pulse Width Modulator (PWM) modules, and two of these are used as PWM pin outputs on the Verdin AM62P. The PWM modules feature 16-bit counters and a 6-bit pre-scaler available for dividing the clock.

There are 3 PWM signals on the Verdin standard specification. PWM_1 is the only one in the Always Compatible class. Both PWM_1 and PWM_2 are general-purpose pulse with modulation outputs. The third interface is dedicated to the DSI output for the display backlight inverter control. Other PWM outputs of the AM62P SoC are available as alternate functions, but they are not guaranteed to be compatible with other modules.

Table 21: Standard PWM Interface Signals

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
15	PWM_1	MMC2_SDWP	EHRPWM2_B	O	General-purpose Always Compatible PWM
16	PWM_2	MMC2_SDCD	EHRPWM2_A	O	General-purpose Reserved PWM
19	PWM_3_DSI	SPI0_CS1	EHRPWM0_B	O	Reserved PWM dedicated for display backlight

Table 22: Additional PWM Interface Signals

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
53	I2C_2_DSI_SDA	I2C1_SDA	EHRPWM2_B	O	Alternate pins for general-purpose PWM_1
149	UART_3_TXD	UART0_TXD	EHRPWM2_B	O	
55	I2C_2_DSI_SCL	I2C1_SCL	EHRPWM2_A	O	Alternate pins for general-purpose PWM_2
147	UART_3_RXD	UART0_RXD	EHRPWM2_A	O	
131	UART_1_TXD	MCASP0_ACLKR	EHRPWM0_B	O	Alternate pins for PWM_3_DSI
166	MSP_34	MMC2_DAT2	EHRPWM0_B	O	Alternate pins for PWM_3_DSI, but unavailable for the Verdin AM62P (only available for SoMs without the WiFi module)
129	UART_1_RXD	MCASP0_AFSR	EHRPWM0_A	O	Additional general-purpose EHRPWM0_A SoC PWM
168	MSP_35	MMC2_DAT3	EHRPWM0_A	O	Additional general-purpose EHRPWM0_A SoC PWM, but unavailable for the Verdin AM62P (only available for SoMs without the WiFi module)
34	I2S_1_D_OUT	MCASP0_AXR0	EHRPWM1_B	O	Additional general-purpose EHRPWM1_B SoC PWM
162	MSP_32	MMC2_DAT0	EHRPWM1_B	O	Additional general-purpose EHRPWM1_B SoC PWM, but unavailable for the Verdin AM62P (only available for SoMs without the WiFi module)
36	I2S_1_D_IN	MCASP0_AXR1	EHRPWM1_A	O	Additional general-purpose EHRPWM1_A SoC PWM
164	MSP_33	MMC2_DAT1	EHRPWM1_A	O	Additional general-purpose EHRPWM1_A SoC PWM, but unavailable for the Verdin AM62P (only available for SoMs without the WiFi module)

5.6 SD/MMC

The AM62P SoC provides two SDIO interfaces, capable of interfacing with SD Memory Cards, SDIO, MMC, and eMMC devices. One is available on the module edge connector pins as the Always Compatible Verdin SD® Memory Card Interface. The second interface is used for the Wi-Fi and Bluetooth module.

Table 23: SDIO Interfaces

AM62P SDIO Interface	Max Bus Width	Description
MMC1	4-bit	Always Compatible Verdin SD interface
MMC2	4-bit	Used for the on-module Wi-Fi and Bluetooth interface. Not available at the module edge connector

Table 24: Always Compatible SD Card Interface Signal Pins

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Voltage	Description
74	SD_1_CMD	MMC1_CMD	MMC1_CMD	I/O	3.3/1.8 V	Command, enable SoC pull-up resistor
80	SD_1_D0	MMC1_DAT0	MMC1_DAT0	I/O	3.3/1.8 V	Serial Data 0, enable SoC pull-up resistor
82	SD_1_D1	MMC1_DAT1	MMC1_DAT1	I/O	3.3/1.8 V	Serial Data 1, enable SoC pull-up resistor
70	SD_1_D2	MMC1_DAT2	MMC1_DAT2	I/O	3.3/1.8 V	Serial Data 2, enable SoC pull-up resistor
72	SD_1_D3	MMC1_DAT3	MMC1_DAT3	I/O	3.3/1.8 V	Serial Data 3, enable SoC pull-up resistor
78	SD_1_CLK	MMC1_CLK	MMC1_CLK	O	3.3/1.8 V	Serial Clock
84	SD_1_CD#	MMC1_SDCD	MMC1_SDCD	I	3.3/1.8 V	Card Detect, enable SoC pull-up resistor. Can be an I/O pin when used as GPIO
76	SD_1_PWR_EN	GPMC0_AD14	GPIO0_29	O	1.8 V	Enable pin for SD card power rail. Regular GPIO pin which is 1.8V only, and does not change the IO voltage level with the rest of the SD card signal pins. Can be an I/O pin when used as GPIO

5.7 Controller Area Network (CAN)

The AM62P SoC features four Controller Area Network (MCAN) interfaces, and two of them are available as Verdin Reserved interfaces and therefore are compatible with other Verdin modules.

Table 25: CAN Signal Pins*

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
20	CAN_1_TX	MCAN0_TX	MCAN0_TX	O	CAN port 1 transmit pin
22	CAN_1_RX	MCAN0_RX	MCAN0_RX	I	CAN port 1 receive pin
24	CAN_2_TX	MCU_MCAN0_TX	MCU_MCAN0_TX	O	CAN port 2 transmit pin
26	CAN_2_RX	MCU_MCAN0_RX	MCU_MCAN0_RX	I	CAN port 2 receive pin

* Compatible with other Verdin modules.

The CAN signals are also available on other module edge connector pins as alternate functions. However, the location of these signals is not compatible with other Verdin modules. Therefore, it is highly recommended to use the compatible pins in Table 25.

Table 26: Additional Camera Interface Signals

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
95	I2C_4_CSI_SCL	UART0_CTSn	I2C3_SCL	I/O	Camera control I2C
93	I2C_4_CSI_SDA	UART0_RTSn	I2C3_SDA	I/O	

Continued on next page

Table 26: Additional Camera Interface Signals (Continued)

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
91	CSI_1_MCLK	WKUP_CLKOUT0	WKUP_CLKOUT0	O	Camera master clock
216	GPIO_5_CSI	VOUT0_DATA4	GPIO0_49	I/O	Dedicated camera GPIO signals
218	GPIO_6_CSI	VOUT0_DATA5	GPIO0_50	I/O	
220	GPIO_7_CSI	VOUT0_DATA6	GPIO0_51	I/O	
222	GPIO_8_CSI	VOUT0_DATA7	GPIO0_52	I/O	

5.8 JTAG

The JTAG interface usually is not required for programming the Verdin. However, it can be helpful for debugging the Cortex-R5F Core or very advanced debugging of the Arm® Cortex® -A Cores.

Instead of using the JTAG port, it is possible to reprogram the module using the Recovery Mode over USB. To flash the module in recovery mode (and for debugging), it is strongly recommended that the USB_1 interface is accessible even if not needed in the production system. Additionally, UART_3 for the console of the main CPUs (A53) and UART_4 for debugging the R5F core should be accessible as well.

Table 27: JTAG Signal Pins

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
1	JTAG_1_TDI	TDI	TDI	I	Test Data In
5	JTAG_1_TDO	TDO	TDO	O	Test Data Out
9	JTAG_1_TCK	TCK	TCK	I	Test Clock
13	JTAG_1_TMS	TMS	TMS	I	Test Mode Select
3	JTAG_1_TRST#	TRSTn	TRSTn	I	Test reset
7	JTAG_1_VREF			O	1.8V reference output for JTAG adapter

5.9 eFuse

eFuse programing requires specific power-up sequence and software.
The eFuse programming on the Verdin AM62P requires the SoC VPP to be driven at 1.8V ±5% after the SoC is powered up, and may consume up to 400mA.
The eFuse programming software is provided by TI.

The TI AM62P One-Time Programmable eFuses may be used to configure the MAC address, security keys, or provide reset values to some registers.

If you are not planning to use eFuses, the X1 pin 104 may be left unconnected. Otherwise, it should be driven to 0V when not programming the eFuses. More information on eFuse programming can be found on the TI AM62P SoC Datasheet.

5.10 Ethernet

5.10.1 ETH_1

Table 28: ETH1

X1 Pin	Verdin Signal Name	DP83867IR Signal Name	I/O	Description	Remarks
225	ETH_1_MDI0_P	TD_P_A	I/O	Positive differential Media Dependent Interface signal, lane 0	
227	ETH_1_MDI0_N	TD_M_A	I/O	Negative differential Media Dependent Interface signal, lane 0	
233	ETH_1_MDI1_P	TD_P_B	I/O	Positive differential Media Dependent Interface signal, lane 1	
231	ETH_1_MDI1_N	TD_M_B	I/O	Negative differential Media Dependent Interface signal, lane 1	
239	ETH_1_MDI2_P	TD_P_C	I/O	Positive differential Media Dependent Interface signal, lane 2	
241	ETH_1_MDI2_N	TD_M_C	I/O	Negative differential Media Dependent Interface signal, lane 2	
247	ETH_1_MDI3_P	TD_P_D	I/O	Positive differential Media Dependent Interface signal, lane 3	
245	ETH_1_MDI3_N	TD_M_D	I/O	Negative differential Media Dependent Interface signal, lane 3	
237	ETH_1_LED_2	LED2	O	LED indication output	
235	ETH_1_LED_1	LED1	O	LED indication output	

5.10.2 ETH_2 - RGMII Signals

Table 29: ETH2

X1 Pin	Verdin specification signal name	SoC ball name	SoC alternate function name	I/O	Description
199	ETH_2_RGMII_RX_CTL	RGMII2_RX_CTL	RGMII2_RX_CTL	I	
197	ETH_2_RGMII_RXC	RGMII2_RXC	RGMII2_RXC	I	
201	ETH_2_RGMII_RXD_0	RGMII2_RD0	RGMII2_RD0	I	
203	ETH_2_RGMII_RXD_1	RGMII2_RD1	RGMII2_RD1	I	
205	ETH_2_RGMII_RXD_2	RGMII2_RD2	RGMII2_RD2	I	
207	ETH_2_RGMII_RXD_3	RGMII2_RD3	RGMII2_RD3	I	
211	ETH_2_RGMII_TX_CTL	RGMII2_TX_CTL	RGMII2_TX_CTL	O	
213	ETH_2_RGMII_TXC	RGMII2_TXC	RGMII2_TXC	O	
221	ETH_2_RGMII_TXD_0	RGMII2_TD0	RGMII2_TD0	O	
219	ETH_2_RGMII_TXD_1	RGMII2_TD1	RGMII2_TD1	O	
217	ETH_2_RGMII_TXD_2	RGMII2_TD2	RGMII2_TD2	O	
215	ETH_2_RGMII_TXD_3	RGMII2_TD3	RGMII2_TD3	O	
193	ETH_2_RGMII_MDC	MDIO0_MDC	MDIO0_MDC	O	
191	ETH_2_RGMII_MDIO	MDIO0_MDIO	MDIO0_MDIO	I/O	
189	ETH_2_RGMII_INT#	GPMC0_Csn1	GPIO0_42	I	

5.11 GPIOs

Table 30: GPIO Interfaces

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
188	MCU_GPIO0	MCU_SPI0CS0	MCU_GPIO0	I/O	
206	GPIO_1	MCU_SPI0_CS1	MCU_GPIO0_1	I/O	
208	GPIO_2	MCU_SPI0_CLK	MCU_GPIO0_2	I/O	
210	GPIO_3	MCU_SPI0_D0	MCU_GPIO0_3	I/O	
212	GPIO_4	MCU_SPI0_D1	MCU_GPIO0_4	I/O	
216	GPIO_5_CSI	VOUT_DATA4	GPIO_049	I/O	
218	GPIO_6_CSI	VOUT_DATA5	GPIO_050	I/O	
220	GPIO_7_CSI	VOUT_DATA6	GPIO_051	I/O	
222	GPIO_8_CSI	VOUT_DATA7	GPIO_052	I/O	

5.12 USB

5.12.1 USB_1

Table 31: USB1

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
155	USB_1_EN	USB0_DRVVBUS	USB0_DRVVBUS	O	
157	USB_1_OC#	GPMC0_ADVn_ALE	GPIO0_32	I	
159	USB_1_VBUS	USB0_VBUS	USB0_VBUS	I	
161	USB_1_ID	GPMC0_CLK	GPIO0_31	I	
163	USB_1_D_N	USB0_DM	USB0_DM	I/O	
165	USB_1_D_P	USB0_DP	USB0_DP	I/O	

5.12.2 USB_2

Table 32: USB2

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
185	USB_2_EN	USB1_DRVVBUS	USB1_DRVVBUS	O	
187	USB_2_OC#	GPMC0_CSn1	GPIO0_41	I	
181	USB_2_D_N	USB1_DM	USB1_DM	I/O	
183	USB_2_D_P	USB1_DP	USB1_DP	I/O	

5.13 Power

5.13.1 Digital Supply

The carrier board should supply the power to the SoM, through the X1 connector. The SoM uses a TPS65219 PMIC and a mix of switched and linear converters to feed the power rails.

Table 33: Power Supply pins

X1 pin	Verdin signal name	I/O	Description	Remarks
251, 253, 255, 257, 259	VCC	I	3.135V to 5.5V	Use decoupling capacitors on the carrier board
10, 11, 18, 27, 28, 33, 39, 40, 45, 50, 51, 65, 68, 71, 77, 83, 86, 89, 97, 98, 103, 109, 110, 115, 121, 122, 127, 134, 145, 146, 158, 167, 170, 173, 179, 182, 194, 195, 204, 209, 223, 224, 229, 230, 236, 242, 243	GND	I	Digital ground	
214	PWR_1V8_MOCI	O	1.8V output	Max. 250mA
249	VCC_BACKUP	I	RTC power supply backup battery	May be left unconnected

5.13.2 Analog Supply

The analog power rail is supplied by an LDO on the SoM, drawing power from the VCC rail. No external analog supplies are required.

5.13.3 Power Management Signals

Power sequence and timings are available in another document.
The power sequence to start up the module or to switch between power states, as well as the required timings, can be found on the Verdin Carrier Board Design Guide.

The power management signals allow the carrier board to power on/off, reset, and wake-up the module, and may force the module into recovery mode. The signals also indicate to the carrier board when to power off the main power rail and peripherals.

Table 34: Power Management pins

X1 pin	Verdin signal name	I/O	Description	Remarks
246	CTRL_RECOVERY_MICO#	I	1.8V OD	Shorting to the ground during power-up is setting the module into recovery mode. There is a 10k pull-up on the module. It can be left floating on the carrier board.
248	CTRL_PWR_BTN_MICO#	I	1.8V OD	Long[1] pulling down is shutting down the module. Short pulling down is turning on module from off state. Open-drain input with on-module 10k pull-up resistor to the 1.8V_STBY rail. It can be left floating on the carrier board.
250	CTRL_FORCE_OFF_MOCI#	O	5V OD	Output for forcing the turning-off of the main power rail. This signal needs to be ignored for the first 400ms during the power-up sequence. The signal is 5V tolerant. The carrier board can pull the signal up to 1.8V, 3.3V, or 5V. It can be left floating on the carrier board.
252	CTRL_WAKE1_MICO#	I	1.8V	Wake-capable pin, which allows you to resume from sleep mode. There are no pull resistors on the module. It can be left floating on the carrier board if the wake feature is disabled in the software. It is a regular SoC GPIO.
254	CTRL_PWR_EN_MOCI	O	1.8V	Enable signal for the power rails of the carrier board peripherals. This output remains high during sleep modes.
256	CTRL_SLEEP_MOCI#	O	1.8V	Enable signal for the power rails on the carrier board peripherals, which need to be turned off during sleep mode. It is only high during the running mode. The signal is standard GPIO with an on-module 10k pull-down resistor. The signal is defined during the power-up sequence. The signal can be left floating on the carrier board.
258	CTRL_RESET_MOCI#	O	3.3V OD	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# does not get asserted. The output is an open-drain type without a pull-up resistor on the module. The signal is 3.3V tolerant. The carrier board can pull the signal up to 1.8V or 3.3V. It can be left floating on the carrier board.
260	CTRL_RESET_MICO#	I	1.8V OD	Open-drain input, which resets the module if shorted to ground on carrier board. There is a 10k on-module pull-up to the 1.8V rail. This means it can be left floating on the carrier board.

[1] More than 5s.

5.14 Wi-Fi and Bluetooth

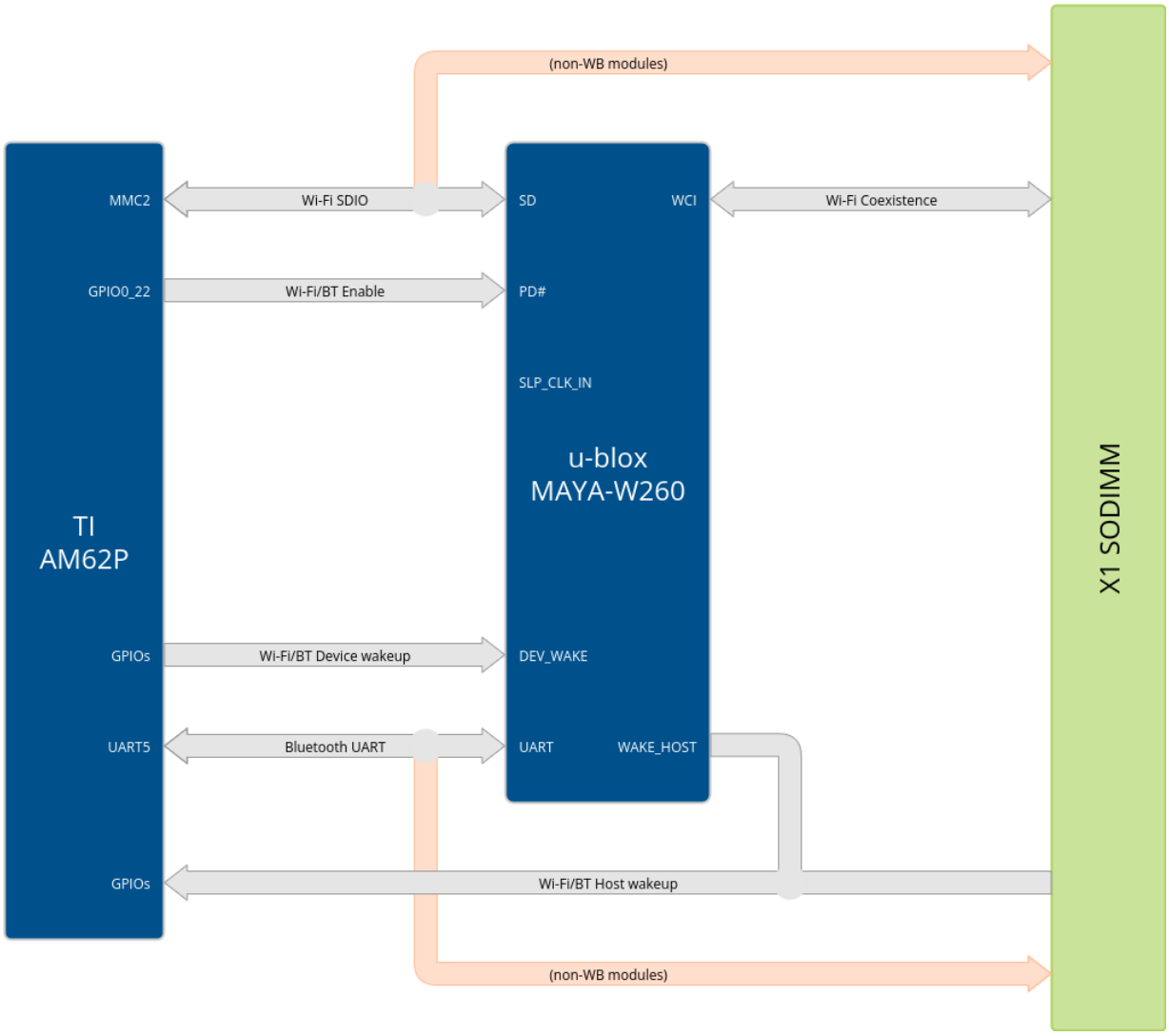
"WB" indicates Wi-Fi/Bluetooth.
The addition of "WB" in the product name indicates that a version features Wi-Fi and Bluetooth.

The Verdin AM62P is available with optional on-module Wi-Fi and Bluetooth interfaces. These Verdin module versions make use of the u-blox MAYA-W260-00B Host-based multiradio module based on the NXP IW611 SoC, capable of up to 150 Mbps (MCS7) data rate.

The Wi-Fi/BT module features:

- Wi-Fi 6 802.11a/b/g/n/ac/ax dual-band
- IEEE 802.15.4-2020 compliant
- Bluetooth classic and full-featured Bluetooth Low Energy 5.3
- Support for long range Bluetooth Low Energy
- Access-point up to eight stations
- Wi-Fi direct
- Two separate U.FL connectors for Wi-Fi and Bluetooth

Figure 4: Wi-Fi/BT Block Diagram



The Wi-Fi/BT module requires external antennas.
The u-blox MAYA-W260-00B needs two U.FL external antennas for Wi-Fi and Bluetooth. The MHF-4 antennas used by some modules are not compatible with the U.FL connectors.

The Wi-Fi module is connected over a 4-bit SDIO interface with the TI AM62P SoC. It uses the MMC2 instance of the SoC. The sleep clock input (SLP_CLK_IN) is provided by the RTC (32.768kHz).

Table 35: Wi-Fi/BT module signals – SoC

MAYA W260 pin name	SoC Ball Name	SoC alternate function name	I/O SoC Perspective	Description
PCM_SYNC	MMC1_SDWP	GPIO1_49	O	
SD_CLK	MMC2_CLK	MMC2_CLK	O	
SD_CMD	MMC2_CMD	MMC2_CMD	I/O	
SD_DAT0	MMC2_DAT0	MMC2_DAT0	I/O	
SD_DAT1	MMC2_DAT1	MMC2_DAT1	I/O	
SD_DAT2	MMC2_DAT2	MMC2_DAT2	I/O	
SD_DAT3	MMC2_DAT3	MMC2_DAT3	I/O	
SD_INT	VOUT0_DATA14	GPIO0_59	I	
UART_RX	VOUT0_DATA8	UART6_RXD	I	
UART_TX	VOUT0_DATA9	UART6_TXD	O	
UART_RTSn	VOUT0_DATA10	UART6_RTSn	I	
UART_CTSn	VOUT0_DATA11	UART6_CTSn	O	
SPI_CLK	SPI0_CLK	SPI0_CLK	O	
SPI_RXD	SPI0_D0	SPI0_D0	I/O	
SPI_TXD	SPI0_D1	SPI0_D1	I/O	
SPI_FRM	VOUT0_DATA15	GPIO0_60	I	
WLAN_WAKE_HOST[1]	OSPI0_CSn2	GPIO0_13	I	
BT_WAKE_HOST[1]	OSPI0_CSn3	GPIO0_14	I	

[1] This signal is also available on X1 connector, see Table 36.

Table 36: Wi-Fi/BT module signals – X1 alternate functions

MAYA W160 pin name	X1 pin name	I/O *SoM perspective*	Description
BT_WAKE_HOST	MSP_36	I[1]/O	Bluetooth transceiver to SoC wake-up
WLAN_WAKE_HOST	MSP_37	I[1]/O	Wi-Fi transceiver to SoC wake-up
WCI_SIN	MSP_39	I	WCI-2 serial interface
WCI_SOUT	MSP_40	O	WCI-2 serial interface

[1] On modules without Wi-Fi/BT.

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. More information can be found on our developer website[3].

[3] https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products

5.15 I²C

Table 37: I2C

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I2C Port	Description
14	I2C_1_SCL	I2C0_SCL	I2C0_SCL	I2C1	Generic
12	I2C_1_SDA	I2C0_SDA	I2C0_SDA	I2C1	Generic
55	I2C_2_DSI_SCL	I2C1_SCL	I2C1_SCL	I2C2	DSI
53	I2C_2_DSI_SDA	I2C1_SDA	I2C1_SDA	I2C2	DSI
59	I2C_3_HDMI_SCL	MCU_I2C0_SCL	I2C2_SCL	I2C3	MCU
57	I2C_3_HDMI_SDA	MCU_I2C0_SC	I2C2_SDA	I2C3	MCU
95	I2C_4_CSI_SCL	UART0_CTSn	I2C3_SCL	I2C4	Camera
93	I2C_4_CSI_SDA	UART0_RTSn	I2C3_SDA	I2C4	Camera

There is also a PMIC_I2C used for controling internal peripherals, check the table 38 for more info.

5.15.1 I²C Peripherals

Table 38: I2C Peripherals

Interface	I2C Address
PMIC	0x30
HCPS	0x40 / 0x41
ADC	0x49
Digital Temperature Sensor	0x48
TPM	0x08 to 0x77
EEPROM	0x50
RTC	0x32
GPIO Expander	0x21

5.16 SPI

Table 39: SPI

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
196	SPI_1_CLK	OSIP0_D5	SPI1_CLK	I/O	Serial Clock
198	SPI_1_MISO	OSIP0_D7	SPI_D1	I	Master Input, Slave Output
200	SPI_1_MOSI	OSIP0_D6	SPI_D0	O	Master Output, Slave Input
202	SPI_1_CS	OSIP0_D4	SPI1_CS0	I/O	Slave Select

5.16.1 QSPI

Table 40: QSPI

X1 Pin	Verdin Standard Function	AM62P Ball Name	AM62P Function	I/O	Description
52	QSPI_1_CLK	OSPI0_CLK	OSPI0_CLK	O	Serial Clock
54	QSPI_1_CS#	OSPI0_CSn0	OSPI0_CSn0	O	Chip Select 0
64	QSPI_1_CS2#	OSPI0_CSn1	OSPI0_CSn1	O	Chip Select 1, used to select second instance of Quad-SPI device (dual die flash require CS0 and CS1)
56	QSPI_1_IO0	OSPI0_D0	OSPI0_D0	I/O	Serial I/O for command, address, and data
58	QSPI_1_IO1	OSPI0_D1	OSPI0_D1	I/O	Serial I/O for command, address, and data
60	QSPI_1_IO2	OSPI0_D2	OSPI0_D2	I/O	Serial I/O for command, address, and data
62	QSPI_1_IO3	OSPI0_D3	OSPI0_D3	I/O	Serial I/O for command, address, and data
66	QSPI_1_DQS	OSPI0_LBCLKO	GPIO0_1	I	Data Strobe signal, required on some high-speed DDR devices

6 Technical Specifcations

6.1 Absolute Maximum Ratings

Table 41: Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
VCC	Main power supply	-0.3	6	V
VCC_BACKUP	RTC power supply	-0.3	6	V
IO_1.8V	SoC IO pins with 1.8V logic level	-0.3	2.1	V
IO_3.3V	SoC IO pins with 3.3V logic level (SDIO)	-0.3	3.6	V
ADC	ADC analog input	-0.3	3.6	V
USB_1_VBUS	Input voltage at USB_1_VBUS	-0.3	5.5	V

6.2 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website[4].

R 022-220054

[4] https://www.toradex.com/support/product-compliance

6.3 Recommended Operation Conditions

Table 42: Recommended operation conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Main power supply	3.135	3.3 or 5	5.5	V
VCC_BACKUP	RTC power supply	1.1	3.0	5.5	V

6.4 Mechanical Characteristics

6.4.1 Sockets for Verdin Modules

The Verdin module uses the SODIMM DDR4 memory module edge connector. This connector has 260 pins and is available from different manufacturers in various stacking heights from 4mm to 9.2mm. Toradex recommends using the TE Connectivity 2309409-2 with a stacking height of 5.2mm, which provides a board-to-board distance of 2.62mm.

A list of other SODIMM DDR4 connector manufacturers is given below:

Amphenol:
https://www.amphenol-icc.com/product-series/ddr4-so-dimm.html

TE Connectivity:
https://www.te.com/usa-en/products/connectors/card-socket-connectors/memory-sockets.html

6.5 Thermal Specification

The Verdin AM62P incorporates dynamic frequency scaling on the Cortex-A53 cores, enabling the system to continuously adjust the operating frequency in response to the changes in workload and temperature.

The Verdin AM62P modules come with embedded temperature sensors. The sensors measure the die (junction) temperature and determine whether the cores need to be throttled to prevent overheating. If the SoC reaches the maximum permitted temperature, the system will automatically shut down.

Temperature affects power consumption.
A lower die temperature will also lower the power consumption due to the smaller leakage currents while idle.

Table 43: Thermal specification – Verdin AM62P

Description	Min.	Typ.	Max.	Unit
Operating temperature range	0		+70	°C
Storage temperature	−40		+85	°C
SoC junction temperature	−40		+95	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		TBD		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		TBD		°C/W

7 Device and Documentation Support

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