Toradex
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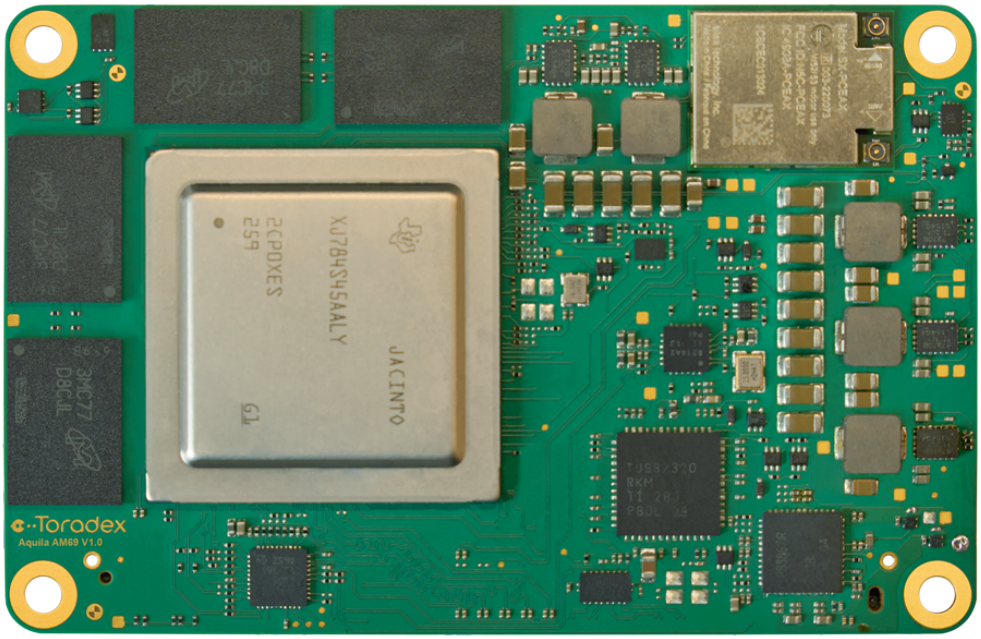
Aquila Carrier Board

Design Guide

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
19-Jan-2025	Rev. 0.1	N/A	Initial documentation
24-Feb-2025	Rev. 0.2	N/A	Section 2.10.2: Rename section from SPI Reference Schematics to UART Reference Schematics.

Contents

1 Introduction

1.1 Overview

This document guides users through the development of a customized carrier board for the Aquila System-on-Module (SoM) family. It describes the different interfaces of those modules and provides reference schematics as well. The document highlights standardized features of Aquila SoMs (compatible between different modules). "Module-specific" interfaces, features, and alternate functions are not detailed in this document. These interfaces are detailed in the respective datasheets of Aquila SoMs. Some Aquila modules may not feature the complete set of the "Reserved" interfaces. It is strongly recommended always to read the datasheet of the module that is intended to be used with an off-the-shelf or a custom carrier board.

Aquila modules feature high-speed interfaces such as PCI Express, DisplayPort, MIPI CSI, and MIPI DSI, requiring special layout considerations regarding trace impedance and length matching. Please read the Toradex Layout Design Guide carefully for additional information on the routing of these interfaces.

1.1.1 Layout design guide

This document contains layout requirement specifications for high-speed signals and helps to avoid layout-related issues.

https://developer.toradex.com/carrier-board-design

1.1.2 Aquila module datasheets

For every Aquila Module, there is a datasheet available. Among other things, the datasheet describes the "Module-specific" interfaces and secondary functionalities of pins. Before starting the development of a customized carrier board, please check these documents to verify if the required interfaces are available on the selected modules.

https://www.toradex.com/computer-on-modules/aquila-arm-family

1.1.3 Aquila family specification

This document describes the Aquila Module standard. It provides information on the mechanical and electrical properties of Aquila modules, in addition to functionalities and interfaces provided by those modules.

https://developer.toradex.com/hardware/aquila-som-family/aquila-family-specification/

1.1.4 Toradex developer Center

You can find a lot of additional information in the Toradex Developer Center, which is updated with the latest product support information regularly.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information is valid or relevant to the Aquila modules.

https://developer.toradex.com/

1.1.5 Aquila reference designs

Schematic files, assembly drawings, bills of material, and the complete Altium project files for the Aquila3 reference carrier boards are available for download for free. There is also an online viewer available, convenient for customers without a license for Altium.

https://developer.toradex.com/carrier-board-design/reference-designs

1.1.6 Pinout designer

The Toradex Pinout Designer is a powerful tool for evaluating different pin multiplexing options for Toradex SoMs.

The tool allows comparing interfaces across different modules as well.

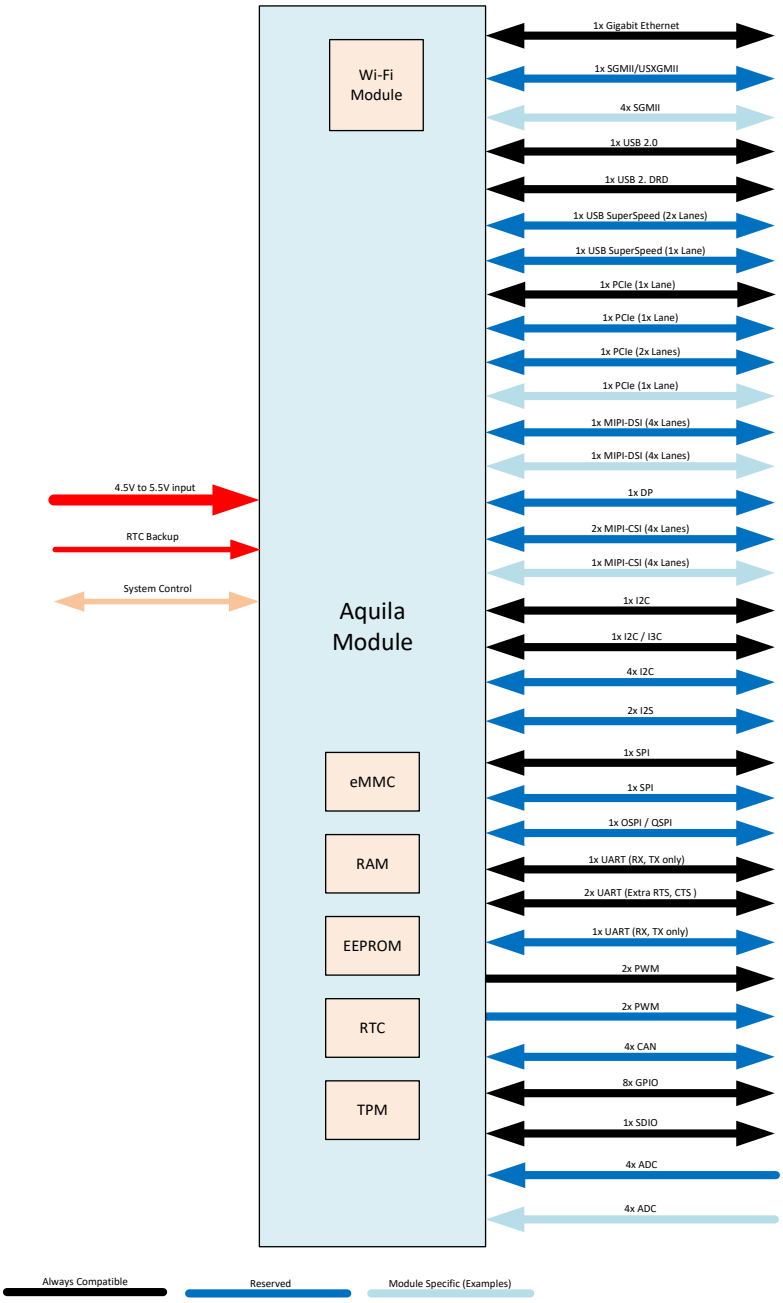
https://developer.toradex.com/carrier-board-design/pinout-designer/

2 Interfaces

2.1 Architecture

The block diagram in Figure 1 shows the basic architecture of the Aquila module, depicting the “Always Compatible” interfaces, “Reserved” interfaces, and some examples of “Module-specific” interfaces.

Figure 1: Aquila SoM block diagram



Features of Aquila modules are split into three distinct groups: “Always Compatible”, “Reserved”, and “Module-specific”.

“Always Compatible” interfaces are features that shall be present on each SoM in the Aquila Family. Customers can expect upgradeability and maximum scalability.

“Reserved” interfaces are features that are defined and reserved but possibly missing on some Aquila SoMs. The reason for that could be that a certain SoC does not feature an interface, or there is an assembly option that omits certain interfaces for cost optimization purposes. Replacement pins must be electrically compatible with the functionality specified. This means that any Aquila SoM can be inserted into any Aquila carrier board without risking damage to the module or the carrier board (caused by electrically not-compatible pins).

A “Module-specific” feature is a feature that is not guaranteed to be functionally or electrically compatible across Aquila modules. Suppose a carrier board design uses such features. In that case, it is possible that other modules in the Aquila module family do not provide these features and instead provide other features on the associated pins. In this case, Aquila modules that are suitable for being used together with the carrier board design may need to be restricted. An incompatible SoM/carrier board combination may disable any/all functionalities or even damage the SoM or the carrier board. Using or relying on functionalities provided on “Module-specific” pins or interfaces in the context of a carrier board could make upgrades to other Aquila modules impossible.

See the Aquila family specification[1] for more information about interface groups.

[1] https://developer.toradex.com/hardware/aquila-som-family/aquila-family-specification/

2.2 PCI Express

Aquila module form factor features one PCIe x1 lane as “Always Compatible” interface. It can be complemented with second lane, which belongs to “Reserved” class (which means it’s not available in all Aquila modules). Additionally there is one PCIe x2 lanes interface in “Reserved” class. Depending on the module, there may be additional lanes available in the “Module-specific” area.

Table 1: PCIe pins

Aquila pin	Aquila specification signal name	I/O *SoM POV*	Type	Power rail	Description
D36	PCIE_1_CLK_P	O	PCIe		PCIe 100MHz reference clock output positive
D37	PCIE_1_CLK_N	O	PCIe		PCIe 100MHz reference clock output positive
C40	PCIE_1_L0_RX_P	I	PCIe		PCIe L0 receive data positive
C41	PCIE_1_L0_RX_N	I	PCIe		PCIe L0 receive data negative
D39	PCIE_1_L0_TX_P	O	PCIe		PCIe L0 transmit data positive
D40	PCIE_1_L0_TX_N	O	PCIe		PCIe L0 transmit data negative
C43	PCIE_1_L1_RX_P	I	PCIe		PCIe L1 receive data positive
C44	PCIE_1_L1_RX_N	I	PCIe		PCIe L1 receive data negative
D42	PCIE_1_L1_TX_P	O	PCIe		PCIe L1 transmit data positive
D43	PCIE_1_L1_TX_N	O	PCIe		PCIe L1 transmit data negative
C36	PCIE_WAKE#	I	CMOS	1.8V	PCIe wake signal
C37	PCIE_1_CLKREQ#	I	CMOS	1.8V	PCIe Clock Request signal
C38	PCIE_1_RESET#	O	CMOS	1.8V	Dedicated PCIe reset output

Reference schematics

The PCIe schematic differs depending on whether the PCIe device is soldered directly to the carrier board (device-down) or is located on a PCIe card. Special care needs to be taken to determine whether AC coupling capacitors are required. The maximum trace length of the lanes depends on whether the design is for an external card or a device-down.

Every PCIe lane consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as the host transmitter needs to be connected to the receiver of the device and vice versa. Usually, the signals are named from the host’s perspective until they reach the pins of the PCIe device. Therefore, the Aquila modules’ transmitting pins should be called TX at the carrier board, while the module’s receiving pins should be called RX. Please carefully read the datasheet of the PCIe device to make sure that RX and TX are not inadvertently swapped.

PCIe reference clock

PCIe devices need a 100MHz reference clock. It is not permitted to connect a reference clock to two device loads. The Aquila module provides one reference clock output as a “Always Compatible” and one as “Reserved” interface.

There may be additional PCIe reference clock outputs in the “Module-specific” area. If there are not enough PCIe reference clocks available (e.g., if a PCIe switch is used or the PCIe interfaces in the “Module-specific” area do not provide additional clock outputs), a zero-delay PCIe clock buffer is required on the carrier board. Some PCIe switches feature an internal PCIe clock buffer, eliminating the need for a dedicated clock buffer.

2.2.1 PCIe x1/x4 connector schematic example

For a regular PCIe slot connector, no additional decoupling capacitors are permitted to be placed on the carrier board in the RX, TX, and reference clock lines. The decoupling capacitors are located on the module and the PCIe card.

Figure 2: PCIe x1 connector example

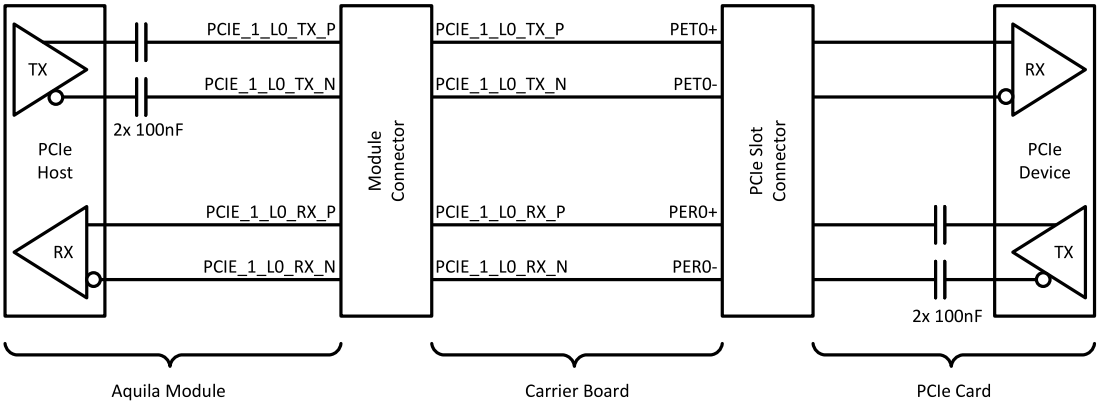
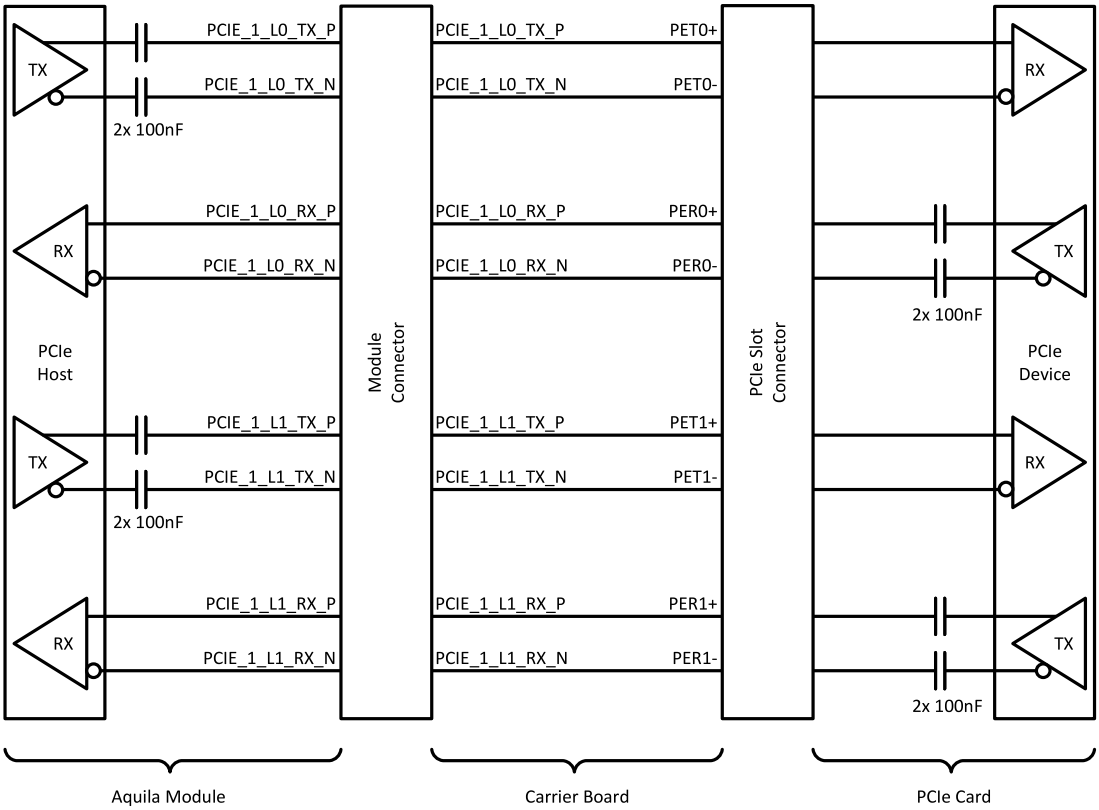


Figure 3: PCIe x4 connector example



The Aquila module standard features a dedicated PCIe reset. This reset (PCIE_1_RESET#) should be used to guarantee the power ramp-up timing requirements of PCI Express. Since the PCIe slot connector has a 3.3V logic level and the PCIE_1_RESET# output of the module is only 1.8V, a level shifter is required. Please note that the Aquila module standard does not support PCIe hot-plug functionality.

The PCIe x1 slot connector has two card present signals (PRSNT1# pin A1 and PRSNT2# pin B18) that are shorted to ground by the card (if it is inserted). Since the Aquila standard does not feature the

PCIe hot-plug feature, these pins can be left unconnected or connected to any free module GPIOs if the presence detection of the card needs to be emulated.

The wake output of the PCIe slot (WAKE#, pin B11) can be connected to the general wake input of the Aquila module (CTRL_WAKE1_MICO#). Wake-up-capable PCIe cards such as Ethernet cards can use this signal to wake up the module from the suspend state. The WAKE# signal of the PCIe card slot is an open drain type. Therefore, no level shifter is required if the signal is pulled up to 1.8V on the carrier board and not to 3.3V.

The JTAG interface on the PCIe slot can be left unconnected. This interface is only used for debugging purposes. No termination on the carrier board is needed.

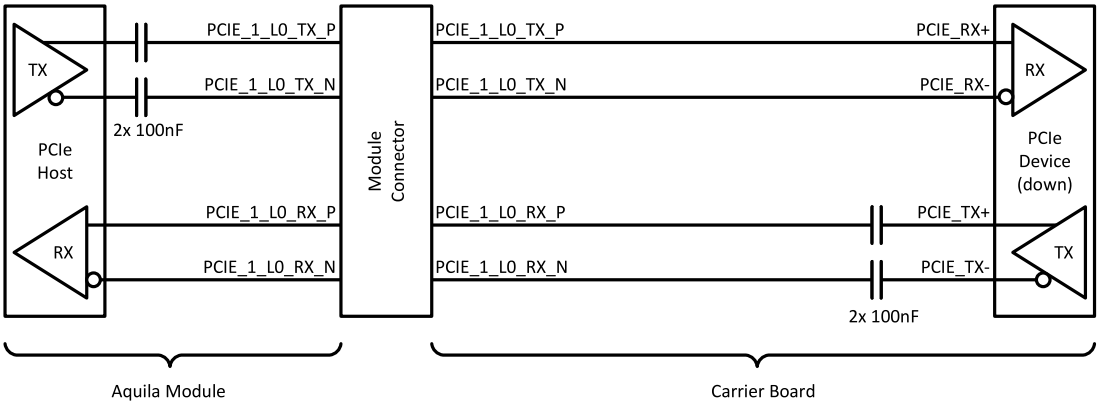
The PCIe slot pin-out features an SMB interface for additional power management control. As the SMB and I2C buses are compatible from a hardware perspective, it is recommended that the general-purpose I2C_2 interface of the Aquila module is used if the SMB interface is needed. Most PCIe cards do not make use of the SMB interface. Therefore, these pins can be left unconnected for most applications. Please note that the SMB interface has a logic level of 3.3V while the I2C_2 has 1.8V. Therefore, a bidirectional level shifter is required.

According to the PCIe specifications, the regular +3.3V supply rail (pin A9, A10, and B8) and the +12V (pin A2, A3, B1, and B2) are required to be provided. The +3.3Vaux is optional. However, the +3.3Vaux must be supplied to the PCIe add-in card slot if the platform supports the wake features (WAKE#).

Not all PCIe cards need a +12V supply. It might be challenging for a battery-powered system or a carrier board with a wide voltage input range to generate a regulated 12V rail. In this case, we recommend checking with the PCIe card(s) manufacturer to determine if the +12V supply is required. Please note that omitting the +12V violates the PCI Express specifications and makes the design incompatible with some add-in cards.

2.2.2 PCIe x1/x2 device-down schematic example

Figure 4: PCIe device down example



2.3 Ethernet

The Aquila module standard features up to six Ethernet interfaces. There is a media-dependent Gigabit Ethernet port on the “Always Compatible” interfaces with the Ethernet PHY on the module. A second Ethernet interface is available as Serial Gigabit Media-Independent Interface (SGMII) as a “Reserved” interface, and up to four “Module-Specific” SGMII interfaces are available on some modules. Maximum speed of this interface depends on the module. The SGMII requires a PHY to be placed on the carrier board and uses multiple media types for the physical link layer.

2.3.1 Media-dependent port

2.3.1.1 Media-dependent ethernet signals

Table 2: Media-dependent ethernet signals

Aquila pin	Aquila specification signal name	I/O *SoM POV*	Type	Power rail	Description
A88	ETH_1_MDI0_P	I/O	Analog		1000Base-T: DA+ 10/100Base-TX: Transmit +
A89	ETH_1_MDI0_N	I/O	Analog		1000Base-T: DA- 10/100Base -TX: Transmit -
A91	ETH_1_MDI1_P	I/O	Analog		1000Base-T: DB+ 10/100Base -TX: Receive +
A92	ETH_1_MDI1_N	I/O	Analog		1000Base-T: DB- 10/100Base -TX: Receive -
A94	ETH_1_MDI2_P	I/O	Analog		1000Base-T: DC+ 10/100Base -TX: Unused
A95	ETH_1_MDI2_N	I/O	Analog		1000Base-T: DC- 10/100Base -TX: Unused
A97	ETH_1_MDI3_P	I/O	Analog		1000Base-T: DD+ 10/100Base -TX: Unused
A98	ETH_1_MDI3_N	I/O	Analog		1000Base-T: DD- 10/100Base -TX: Unused
A99	ETH_1_LED_1	O	OD	3.3V tolerant	LED indication output for activity on the Ethernet port
A100	ETH_1_LED_2	O	OD	3.3V tolerant	LED indication output for established Ethernet link

2.3.1.2 Media-dependent ethernet reference schematics

Figure 5: Gigabit Ethernet schematic example – integrated magnetics

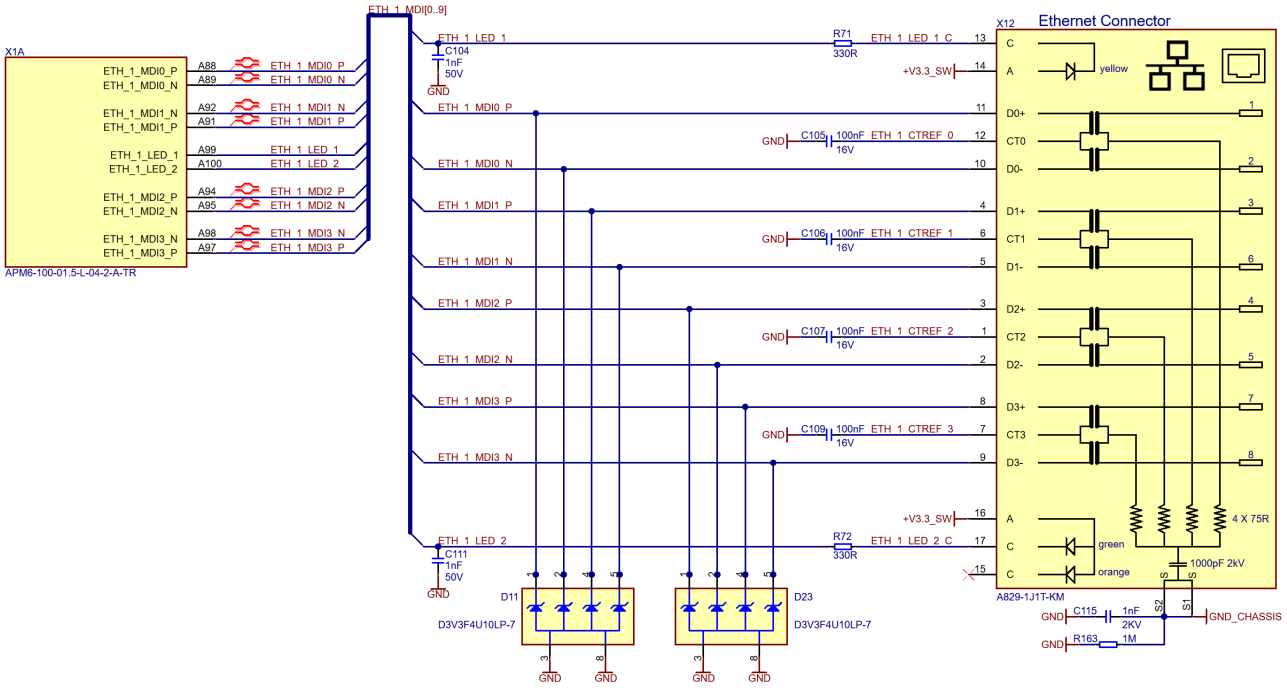


Figure 6: Gigabit Ethernet schematic example – discrete magnetics

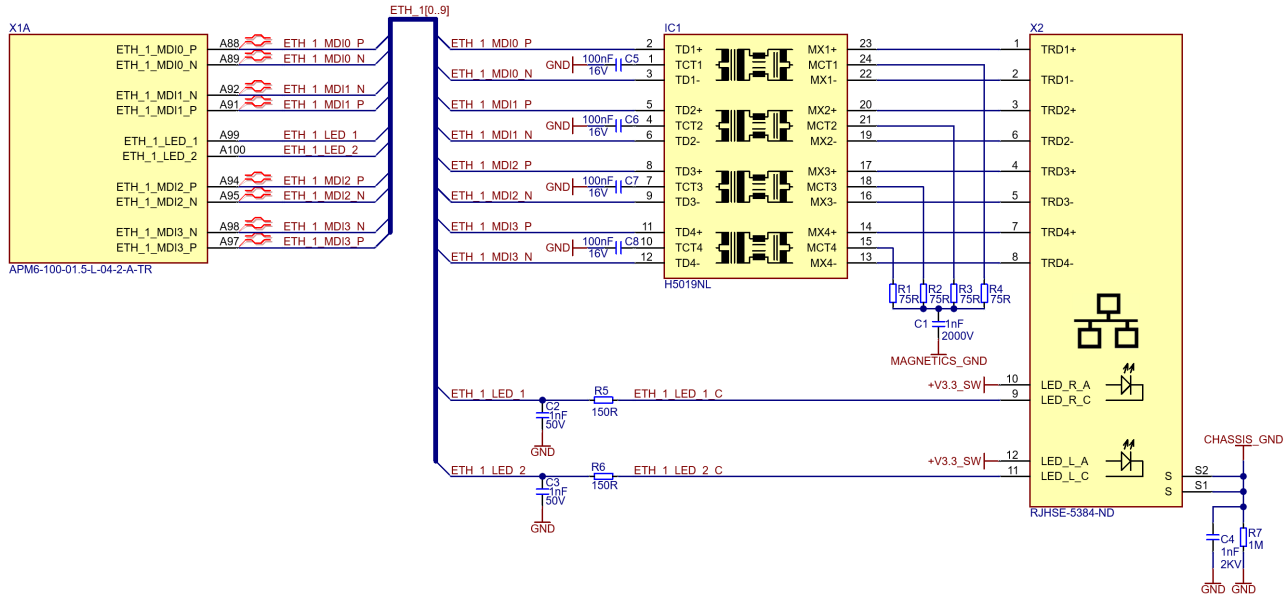
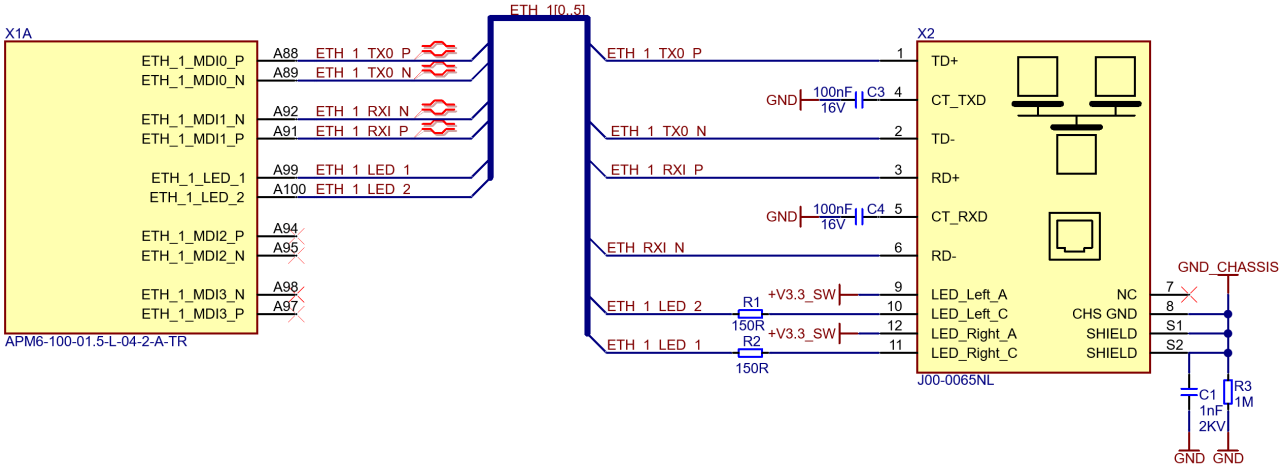
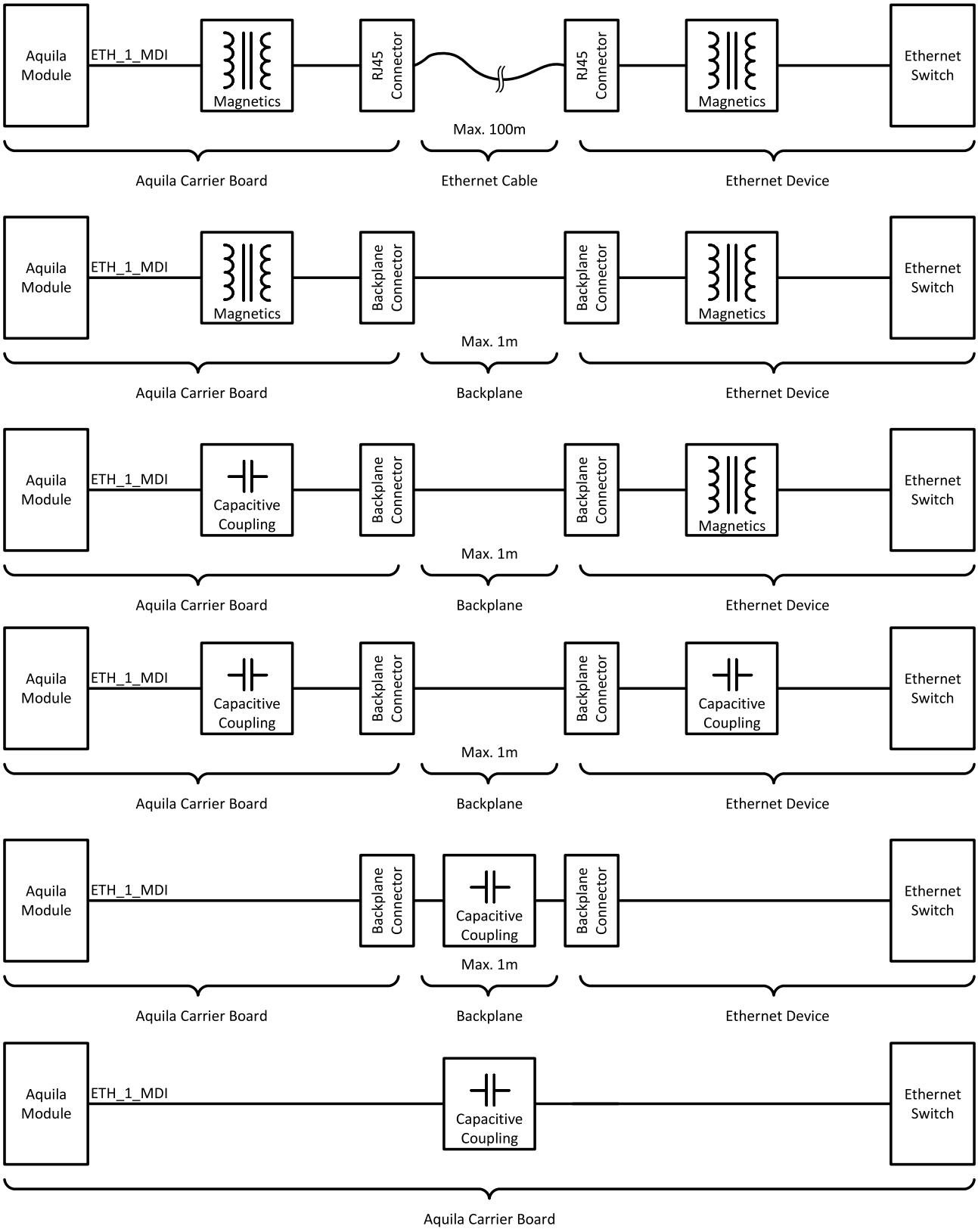


Figure 7: Fast Ethernet schematic example – integrated magnetics



2.3.1.3 Capacitive coupling of media-dependent interfaces

Figure 8: Capacitive coupling of media-dependent interfaces



2.3.1.4 Ethernet schematic examples

Figure 9: Aquila-Aquila Ethernet connection

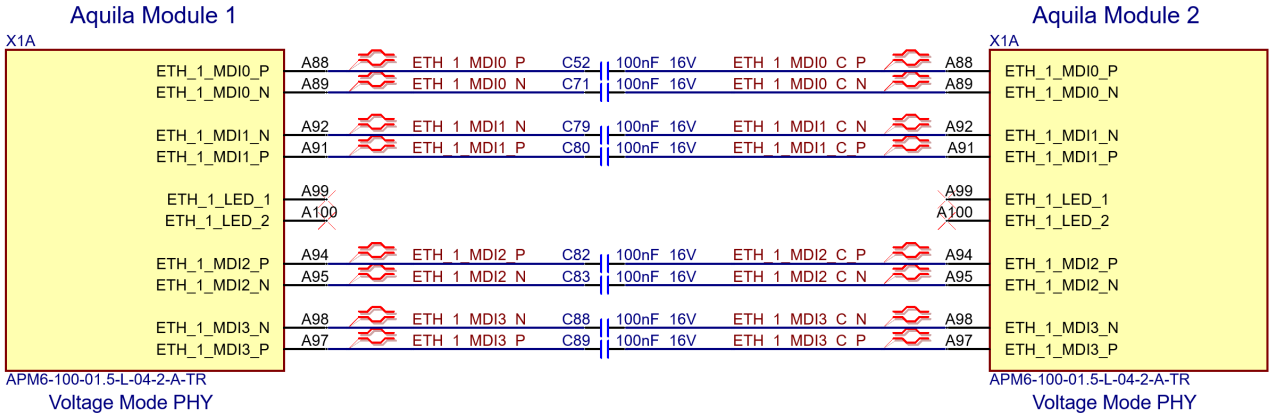


Figure 10: Aquila-Verdin Ethernet connection

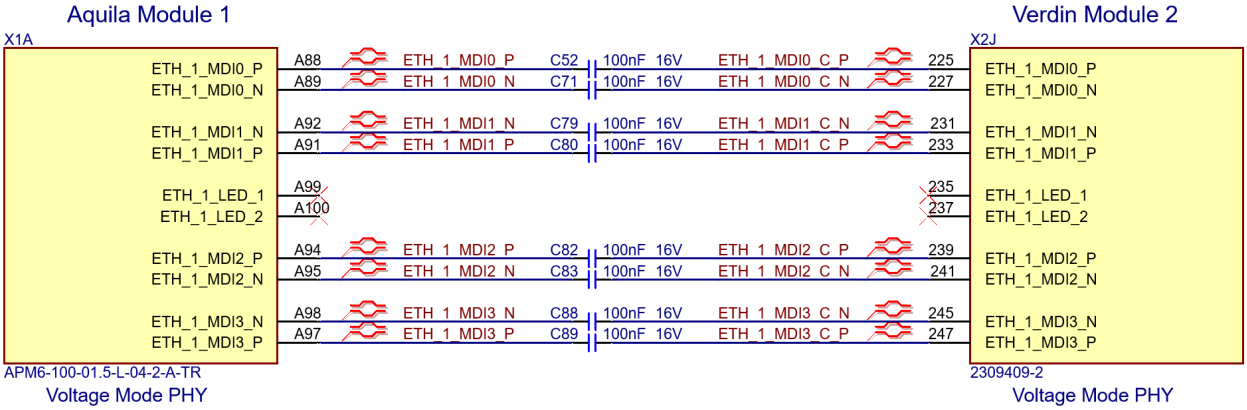
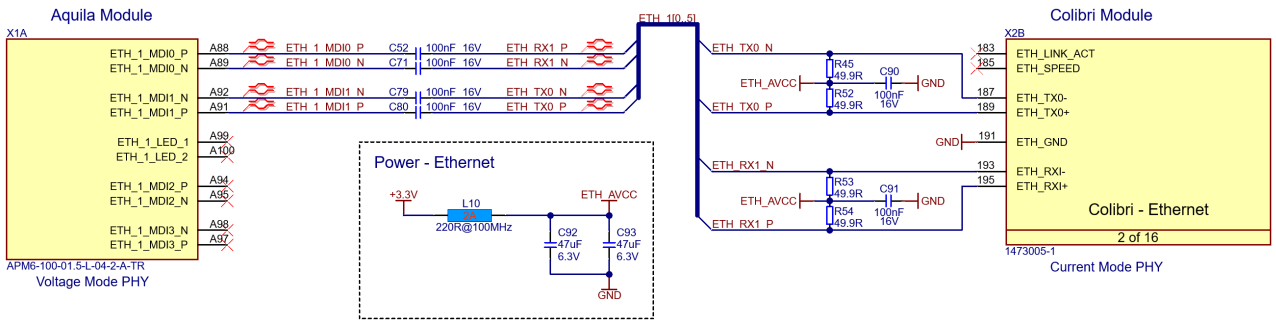


Figure 11: Aquila-Colibri Ethernet connection



2.3.2 Serial Gigabit Media-Independent Interface Ethernet Port

In addition to the Media Dependent Ethernet port, the Aquila family provides a second Ethernet port in the "Reserved" category. However, this secondary port is provided as a Serial Gigabit Media-Independent Interface (SGMII). This means only the Ethernet MAC (Medium Access Control) is on the module. The PHY (physical layer) needs to be on the carrier board. This allows for additional flexibility in choosing the suitable transport medium (e.g., fiber-optical cable).

The Serial Media-Independent interface may support different speed standards. Please check the module datasheet for details.

Besides the SGMII, there is a Management Data Input/Output interface (MDIO) for managing the PHY on the carrier board. Some Aquila modules maybe share the interface with the on-module Ethernet PHY. In these cases, special care must be taken to address the carrier board PHY does not conflict with the on-module PHY address.

2.3.2.1 xSGMII Signals

Table 3: xSGMII signals

Aquila pin	Aquila specification signal name	I/O *SoM POV*	Type	Power rail	Description
B87	ETH_2_SGMII_TX_P	O	Analog		Serial Gigabit Media-Independent Transmit pair - Positive
B86	ETH_2_SGMII_TX_N	O	Analog		Serial Gigabit Media-Independent Transmit pair - Negative
B84	ETH_2_SGMII_RX_P	I	Analog		Serial Gigabit Media-Independent Receive pair - Positive
B83	ETH_2_SGMII_RX_N	I	Analog		Serial Gigabit Media-Independent Receive pair - Negative
B90	ETH_2_SGMII_MDC	O	CMOS	1.8V	Management interface clock (output from MAC)
B89	ETH_2_SGMII_MDIO	I/O	OD	1.8V	Management interface data (bidirectional, needs pull-up on carrier board)
B81	ETH_2_SGMII_INT#	I	OD	1.8V	Optional interrupt, requires a pull-up on the carrier board

2.4 USB

The Aquila specifications contain two USB ports. One port is a Dual Role Port that can be configured as a host or client. This port is usually used in the recovery mode for loading new software onto the module. The second port supports host mode only. Both ports can support the low, full, and high-speed modes of the USB 2.0 specifications.

There are two USB-SS interfaces available in the “Reserved” class. USB_1 is 2-lane interface with USB mux integrated on the module or directly into the SoC. It requires additional USB-C controller on the carrier board for providing cable orientation data or link capabilities. I2C_1 interface is reserved for communicating with this controller.

USB_2 is 1-lane USB-SS interface that can be used for USB 3.0 port or to connect external hub. Please check availability in the module documentation.

Table 4: USB availability

Aquila USB port	1.5 Mbit/s Low Speed (1.1)	12 Mbit/s Full Speed (1.1)	480 Mbit/s High Speed (2.0)	5 Gbit/s SuperSpeed (3.x)	10 Gbit/s SuperSpeed (3.x)	DRP
USB_1	yes	yes	yes	yes	yes	yes
USB_2	yes	yes	yes	yes	no	no

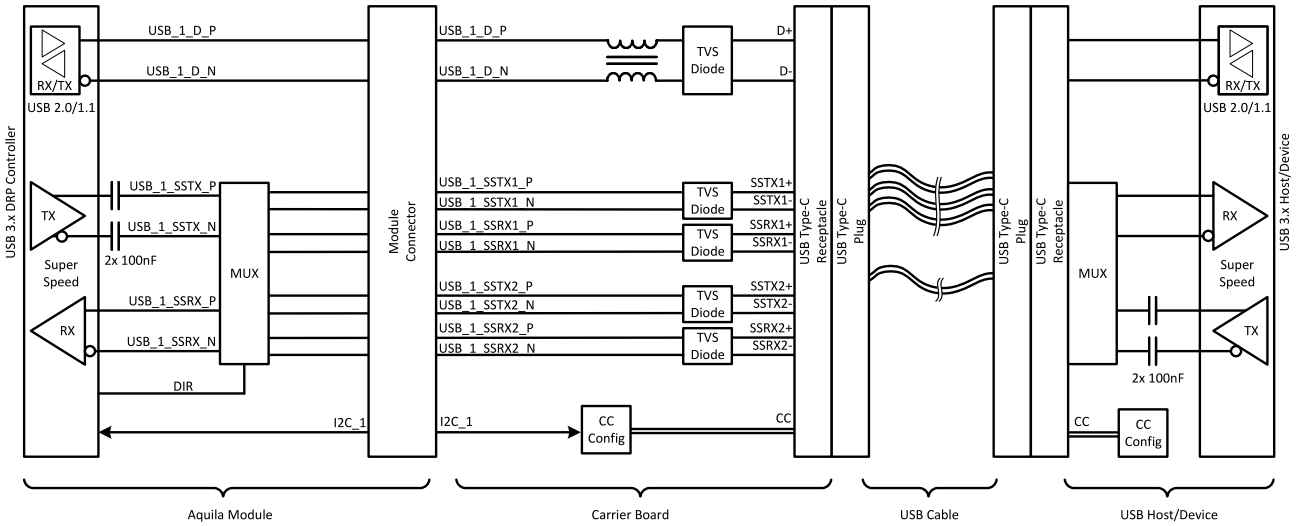
2.4.1 USB signals

Table 5: USB signals

Aquila pin	Aquila specification signal name	I/O *SoM POV*	Type	Power rail	Description
A70	USB_1_D_P	I/O	USB		Positive differential USB signal, DRP capable
A71	USB_1_D_N	I/O	USB		Negative differential USB signal, DRP capable
A62	USB_1_SSRX1_P	I	USB		USB-SS Receive 1 positive signal
A61	USB_1_SSRX1_N	I	USB		USB-SS Receive 1 negative signal
A74	USB_1_SSRX2_P	I	USB		USB-SS Receive 2 positive signal
A73	USB_1_SSRX2_N	I	USB		USB-SS Receive 2 negative signal
A64	USB_1_SSTX1_P	O	USB		USB-SS Transmit 1 positive signal
A65	USB_1_SSTX1_N	O	USB		USB-SS Transmit 1 negative signal
A76	USB_1_SSTX2_P	O	USB		USB-SS Transmit 2 positive signal
A77	USB_1_SSTX2_N	O	USB		USB-SS Transmit 2 negative signal
B76	USB_1_VBUS	I	CMOS	5V tolerant	Bus voltage detection in the DRP client mode
B77	USB_1_EN	O	CMOS	1.8V	Enable signal for the bus voltage output in host mode
B75	USB_1_OC#	I	OD	1.8V	Overcurrent input signal
B74	USB_1_INT#	I	OD	1.8V	Interrupt input (from CC controller)

2.4.2 USB-C DRP – Dual Role Port

Figure 12: USB-C SuperSpeed DRP



2.4.3 USB-C DFP – Downstream Facing Port

Figure 13: USB-C High Speed downstream-facing

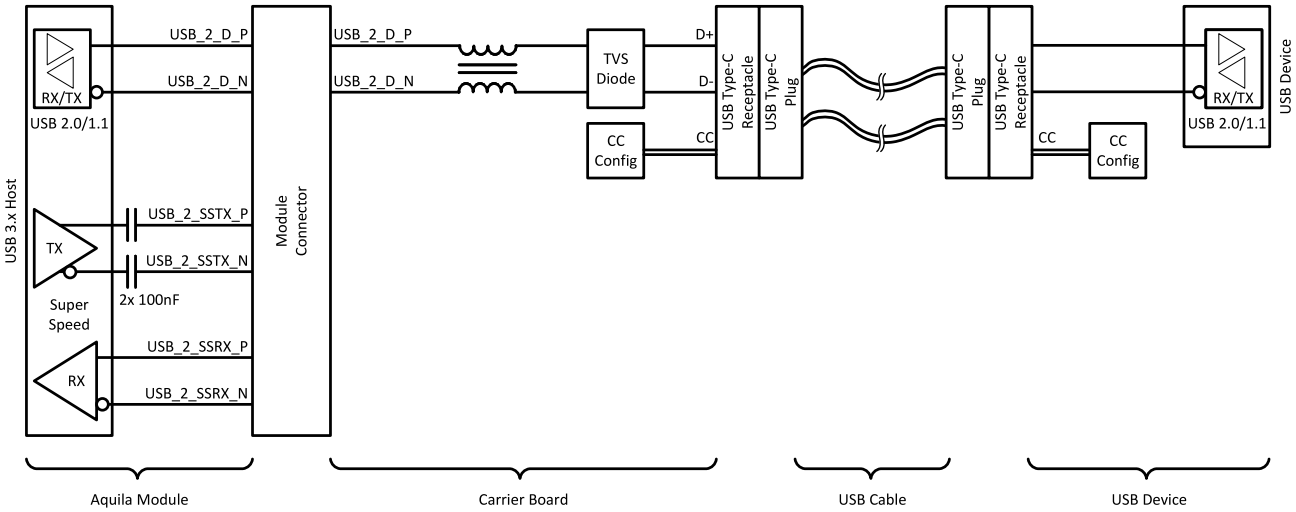
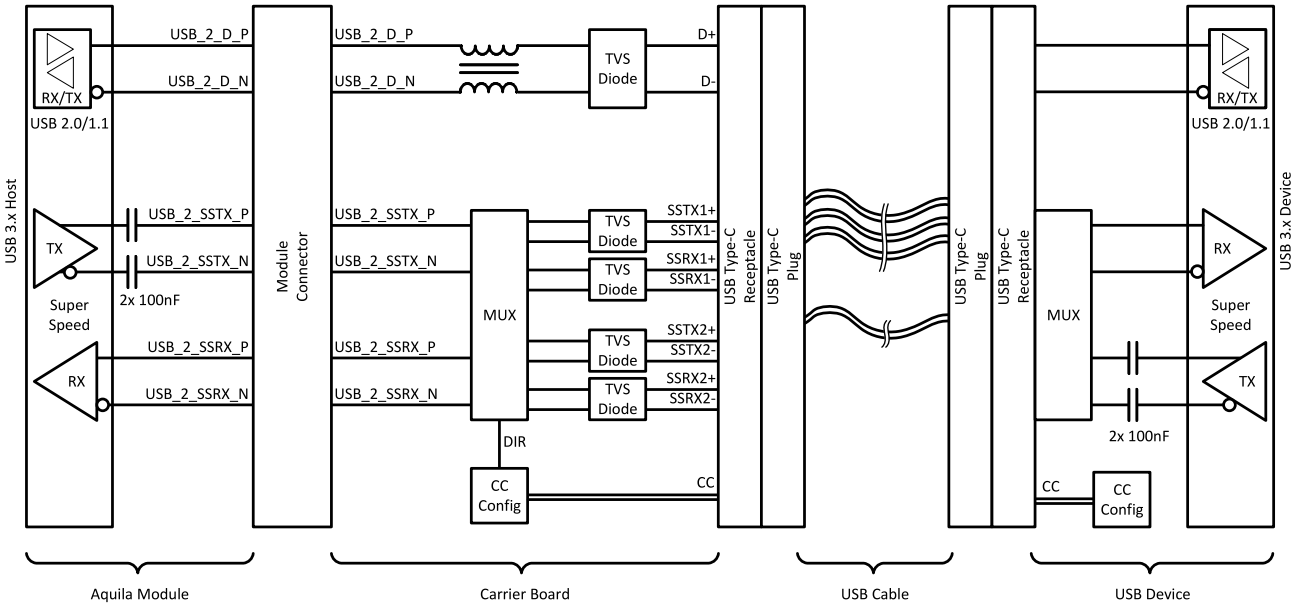
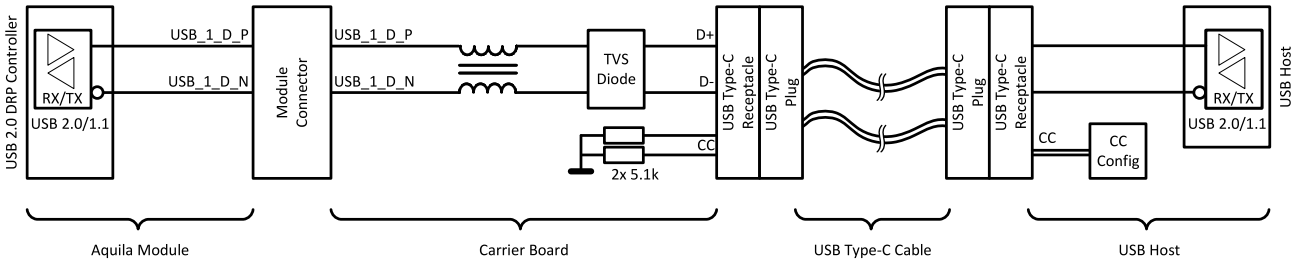


Figure 14: USB-C SuperSpeed downstream-facing



2.4.4 USB-C UFP – Upstream Facing Port

Figure 15: USB-C High Speed upstream-facing



2.4.5 USB-A Host

Figure 16: USB-A High Speed Host

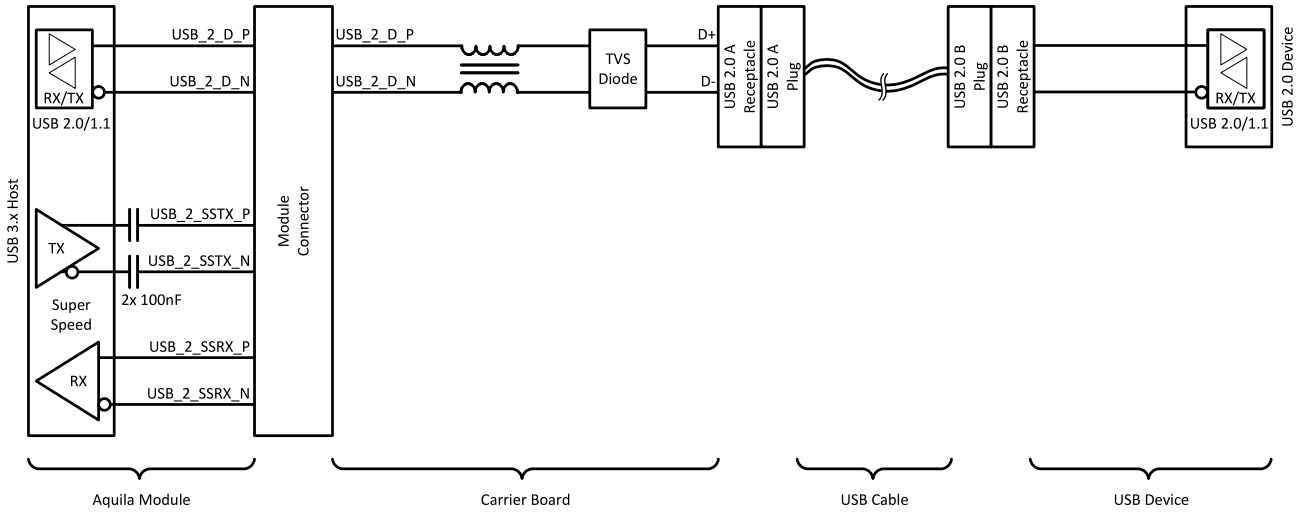
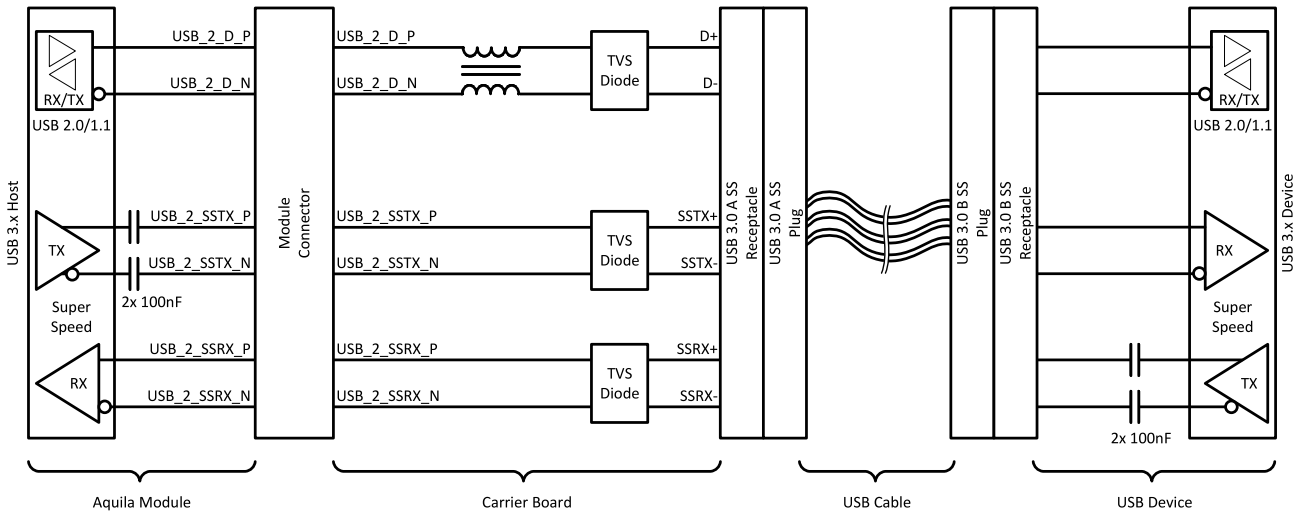
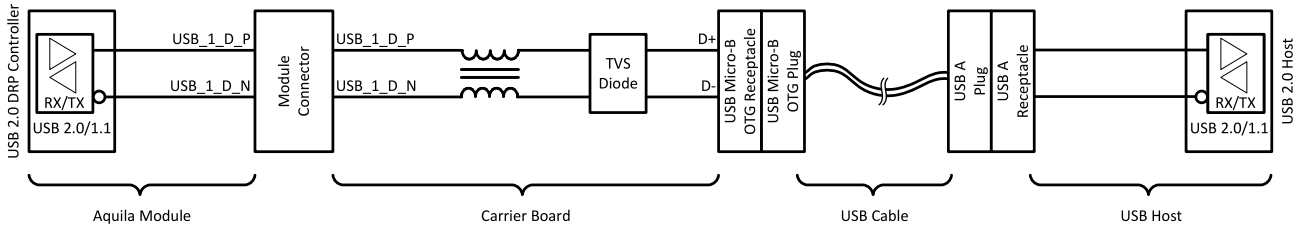


Figure 17: USB-A SuperSpeed Host



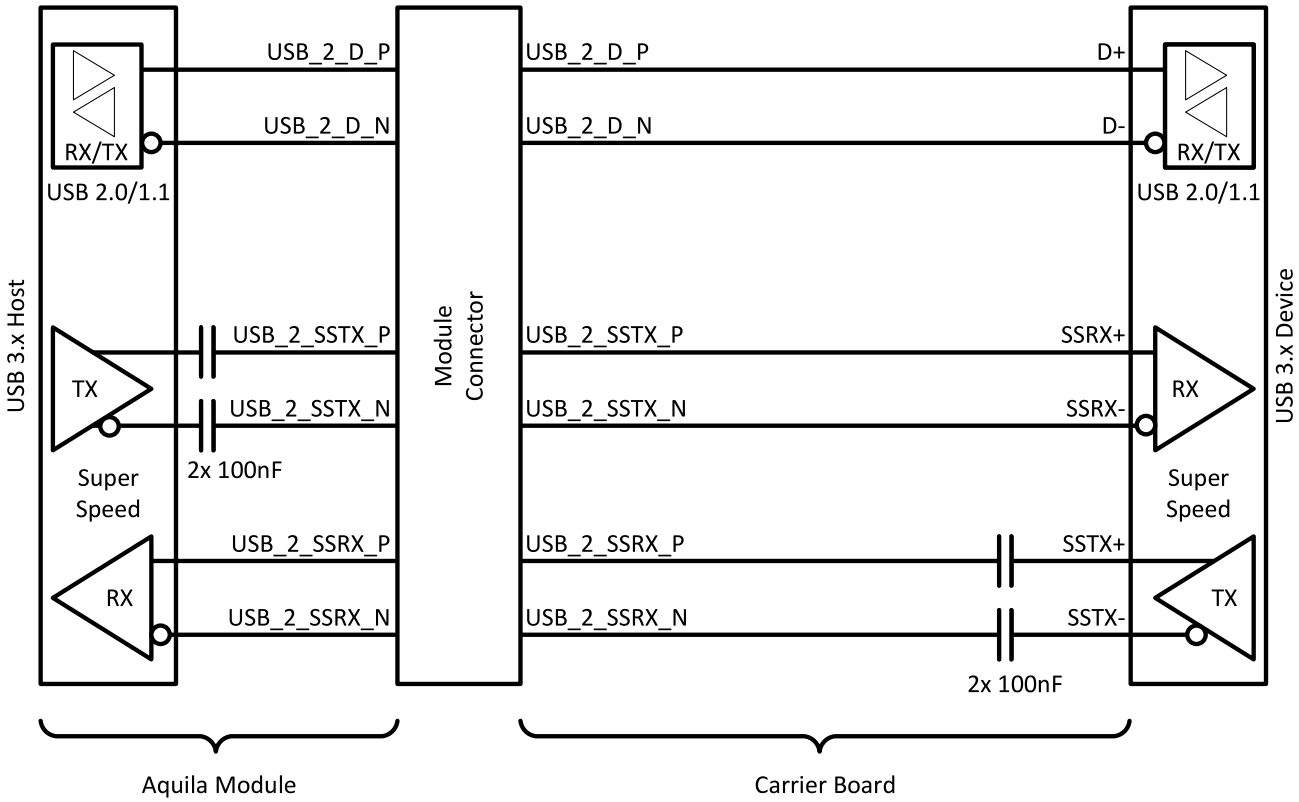
2.4.6 USB Micro-B Client

Figure 18: USB Micro-B High Speed Host



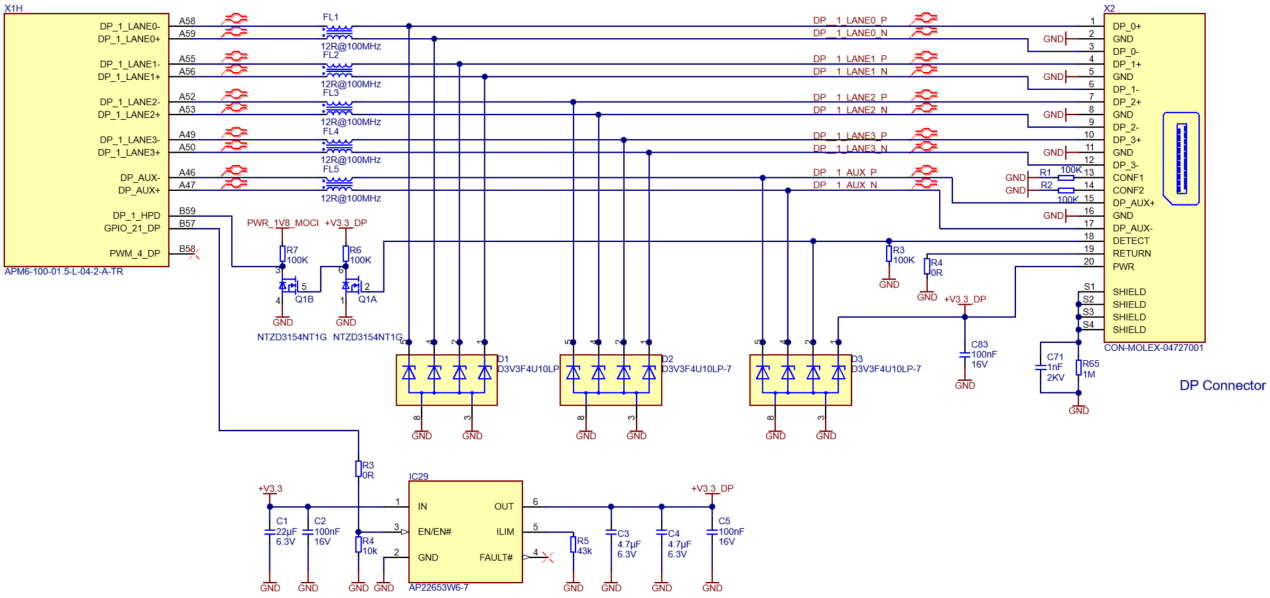
2.4.7 USB device down (without connector)

Figure 19: USB High Speed device down client



2.5 DisplayPort

Figure 20: DisplayPort reference schematic



2.6 MIPI DSI – Display Serial Interface

The Digital Serial Interface (DSI) is specified by the Mobile Industry Processor Interface Alliance (MIPI) and is available as a "Reserved" interface on the Aquila module specifications. The interface targets to connect high-resolution displays with low energy consumption. The interface is intended to be used for internal displays with shorter cable lengths.

The interface consists of a differential pair bit clock and between one and four differential data signal lanes. While the data lanes 1 to 3 are traveling from the module to the display, the lane 0 is bidirectional. This lane is capable of a bus turnaround (BTA) for commands. In the low power mode, the separate clock signal is disabled. The clock is then embedded into the data lanes. However, image data can only be sent in the high-speed mode, which also uses the external clock signal.

2.6.1 MIPI DSI signals

Table 6: MIPI DSI signals

Aquila pin	Aquila specification signal name
A38	DSI_1_CLK_P
A37	DSI_1_CLK_N
A44	DSI_1_D0_P
A43	DSI_1_D0_N
A41	DSI_1_D1_P
A40	DSI_1_D1_N
A35	DSI_1_D2_P
A34	DSI_1_D2_N
A32	DSI_1_D3_P
A31	DSI_1_D3_N
B41	I2C_3_DSI1_SCL
B40	I2C_3_DSI1_SDA
B46	PWM_3_DSI
B42	GPIO_17_DSI_1
B43	GPIO_18_DSI_1
B44	GPIO_19_DSI_1
B45	GPIO_20_DSI_1

2.6.2 MIPI DSI reference schematics

Figure 21: MIPI DSI to HDMI reference schematic

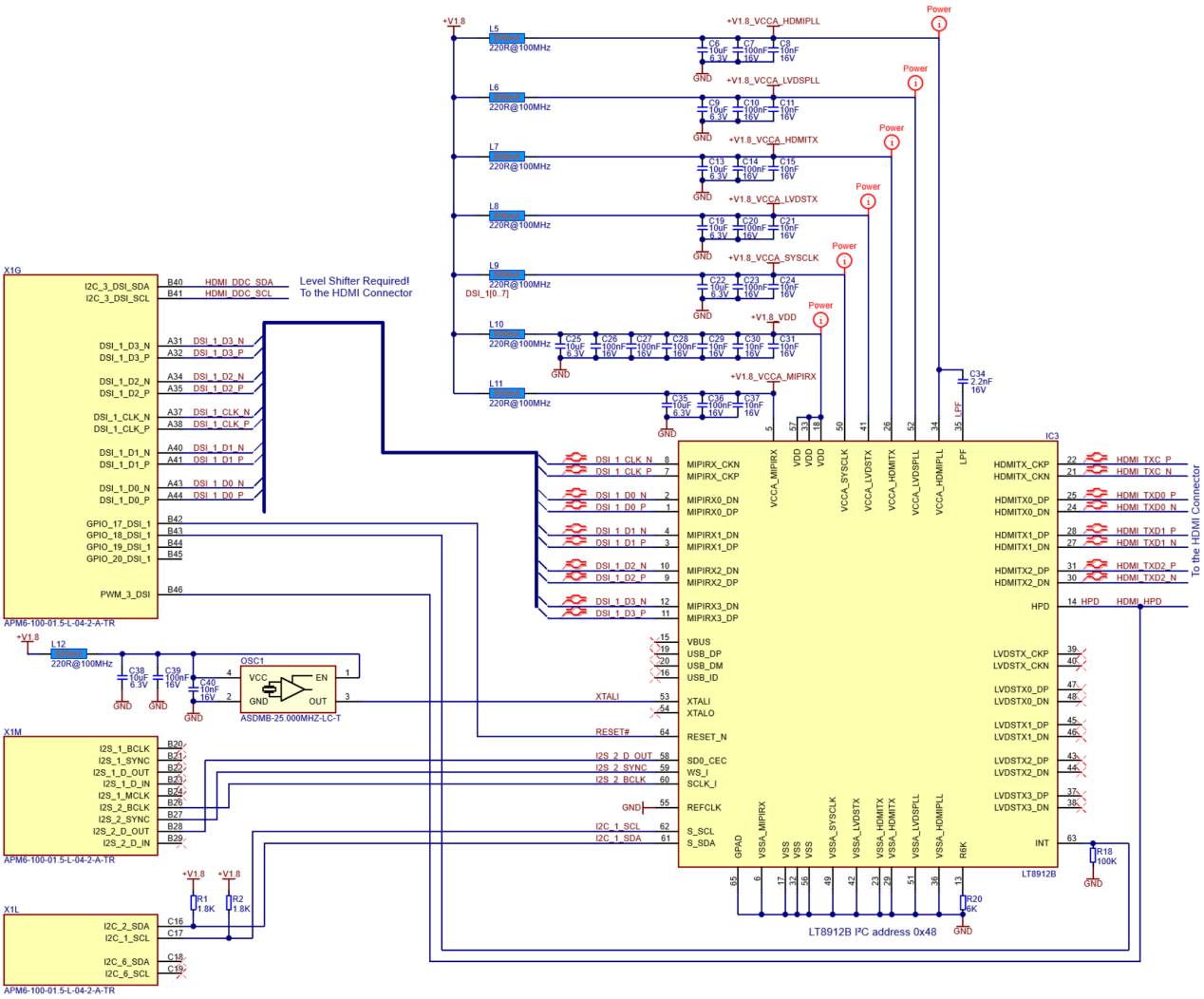


Figure 22: MIPI DSI to LVDS reference schematic

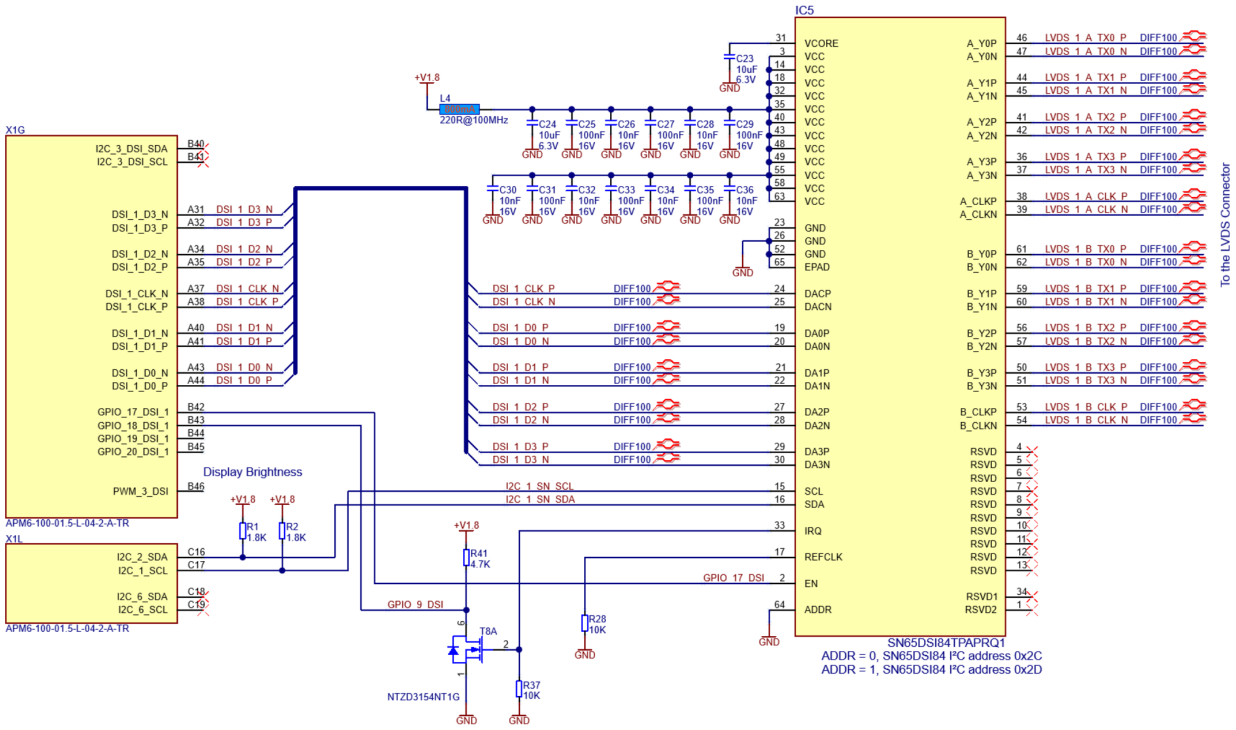
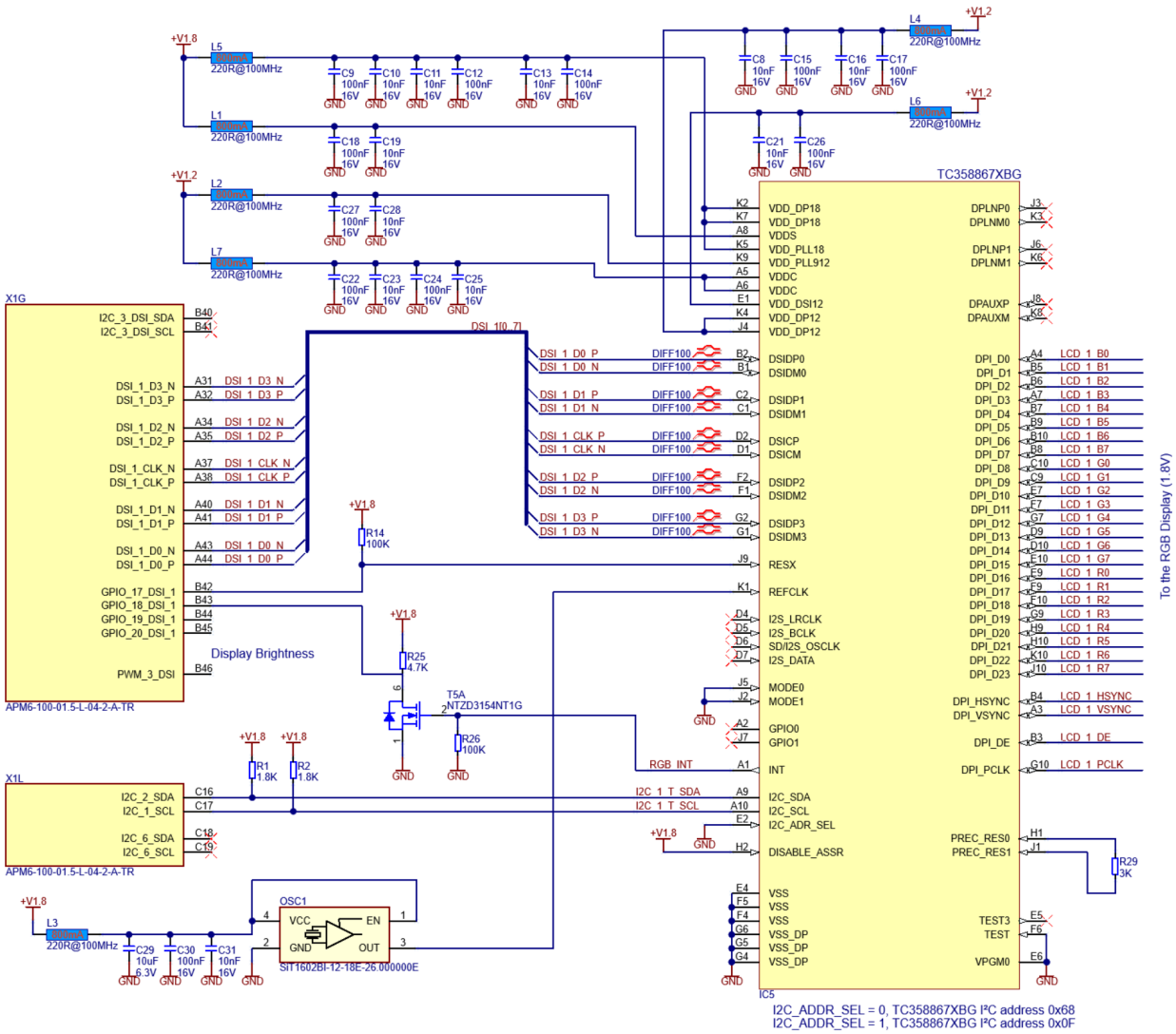


Figure 23: MIPI DSI to parallelRGB reference schematic



2.7 MIPI CSI – Camera Serial Interface

The Camera Serial Interface (CSI) from the Mobile Industry Processor Interface Alliance (MIPI) is related to the MIPI DSI, intended to be used for displays. The Aquila standard reserves up to four lanes for CSI_1 and CSI_2 interfaces. This interface version uses the MIPI D-PHY as a physical layer which is also used for the MIPI DSI interface on the Aquila module. As with the MIPI DSI, the first data lane is bidirectional.

The MIPI CSI-2 supports different camera formats (e.g., RGB, YUV, YCbCr, RAW Bayer, and others.). Please carefully check the datasheet of the Aquila module whether it supports the format of the camera. Also, the maximum interface speed and supported camera resolution depend on the module.

2.7.1 CSI_1 signals

Table 7: CSI_1 signals

Aquila pin	Aquila specification signal name
A22	CSI_1_CLK_P
A23	CSI_1_CLK_N
A28	CSI_1_D0_P
A29	CSI_1_D0_N
A25	CSI_1_D1_P
A26	CSI_1_D1_N
A19	CSI_1_D2_P
A20	CSI_1_D2_N
A16	CSI_1_D3_P
A17	CSI_1_D3_N
A13	I2C_4_CSI1_SCL
A12	I2C_4_CSI1_SDA
B17	GPIO_09_CSI_1
B18	GPIO_10_CSI_1
A11	GPIO_11_CSI_1
B19	GPIO_12_CSI_1
A14	CTRL_MCLK_MOCI

2.7.2 CSI_2 signals

Table 8: CSI_2 signals

Aquila pin	Aquila specification signal name
B8	CSI_2_CLK_P
B9	CSI_2_CLK_N
B14	CSI_2_D0_P
B15	CSI_2_D0_N
B11	CSI_2_D1_P
B12	CSI_2_D1_N

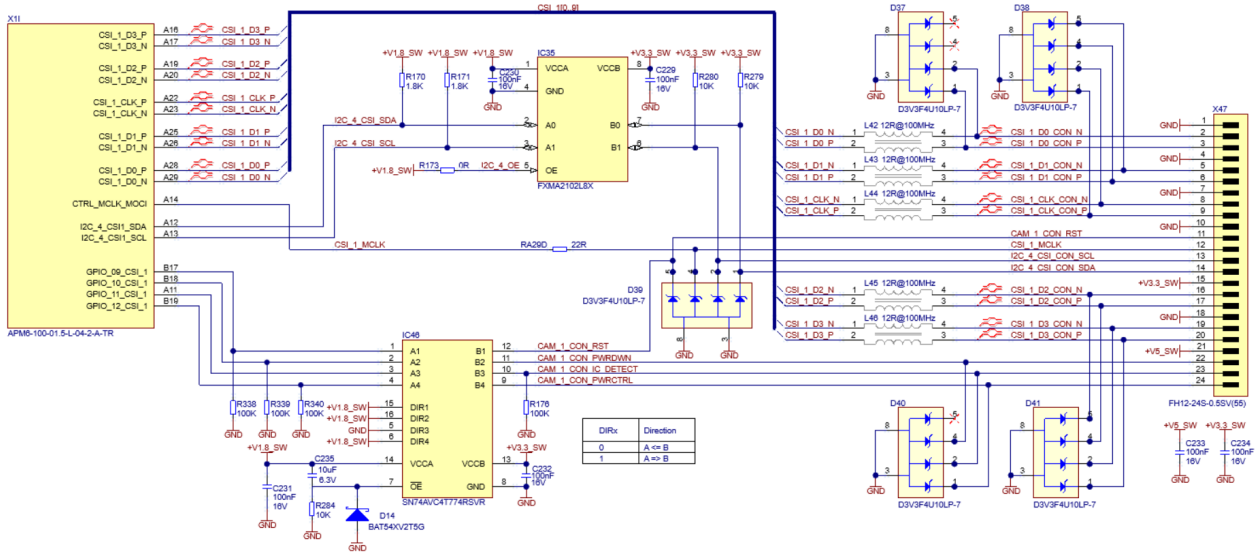
Continued on next page

Table 8: CSI_2 signals (Continued)

Aquila pin	Aquila specification signal name
B5	CSI_2_D2_P
B6	CSI_2_D2_N
B2	CSI_2_D3_P
B3	CSI_2_D3_N
C6	I2C_5_CSI2_SCL
C5	I2C_5_CSI2_SDA
C1	GPIO_13_CSI_2
C2	GPIO_14_CSI_2
C3	GPIO_15_CSI_2
C4	GPIO_16_CSI_2

2.7.3 CSI reference schematic

Figure 24: MIPI CSI reference schematic



2.7.4 Unused MIPI CSI-2 signal termination

All unused MIPI CSI-2 signals can be left unconnected.

2.8 SD/MMC/SDIO

The Aquila module form factor features one SDIO interface as “Always Compatible”. The interface provides 4 data bit which can be used for interfacing SD, SDIO, MMC and eMMC devices.

The SD cards support different bus speed modes. The required signal voltage depends on the bus speed mode. In UHS-I (Ultra High Speed), the signaling voltage must be changed from 3.3V to 1.8V. In the Aquila module definition, all GPIO capable interfaces are defined for 1.8V only. The SDIO interface pins are an exception here. To be compliant with older SD cards, IO pins need to start the communication at a 3.3V voltage level. Therefore, the IO voltage rail of the SD card signals is switchable between 1.8V and 3.3V voltage levels.

Some Aquila modules may feature additional SD interfaces as alternate functions of other interfaces or on the “Module-specific” pins. Some of these additional SD interfaces may support only 1.8V IO voltage levels. Since a detachable SD card needs to start the negotiation at a 3.3V voltage level, these ports can only be used for permanently attached devices like an eMMC memory or an SDIO peripheral device.

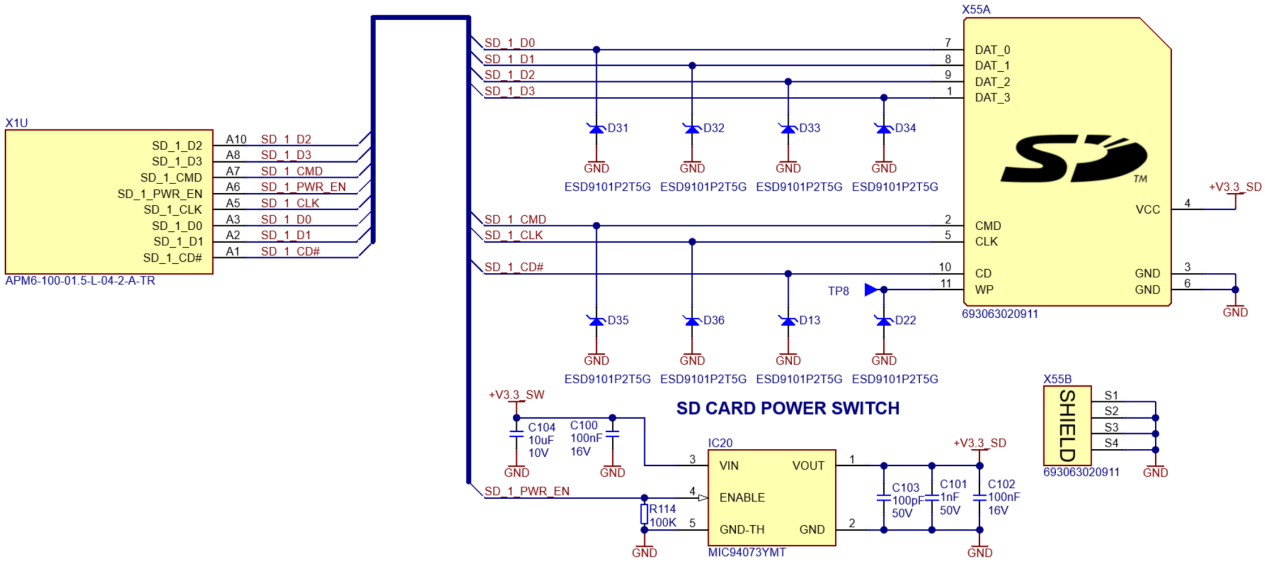
2.8.1 SD/MMC/SDIO signals

Table 9: SD/MMC/SDIO pins

Aquila pin	Aquila specification signal name
A1	SD_1_CD#
A5	SD_1_CLK
A7	SD_1_CMD
A3	SD_1_D0
A2	SD_1_D1
A10	SD_1_D2
A8	SD_1_D3
A6	SD_1_PWR_EN

2.8.2 SD/MMC/SDIO reference schematics

Figure 25: SD card reference schematic



2.8.3 Unused SD/MMC/SDIO signal termination

Unused SD/MMC/SDIO Interface Signal Termination All unused SD interface signals can be left unconnected. If the SD/MMC/SDIO port is unused, the signal could be used as GPIO. Check the datasheet of the Aquila module whether there are any restrictions for using the signals as GPIOs.

2.9 I²C

The Aquila module standard features six I2C interfaces. The interface I2C_1 and I2C_2 are a general-purpose I2C and is in the "Always Compatible" interface group. Additionally I2C_1 may be used to connect USB-CC controller. The additional four I2C ports are in the "Reserved" group and are dedicated to other interfaces. I2C_3_DSI1 is dedicated to the MIPI DSI port, I2C_4_CSI1 and I2C_5_CSI2 are dedicated to the MIPI CSI port, and I2C_6 is a general-purpose I2C port. Check the Aquila datasheet whether these I2C ports can be used as general-purpose interfaces. Some modules do not provide all six I2C ports. Whether a port is available or not depends on whether the interface they are dedicated to is existing.

The I2C interfaces do not feature any pull-up resistors on the module. It is required to add pull-up resistors for the data and clock lines on the carrier board. The pull-up resistor value is typically between 1Ω and 10kΩ. A small pull-up resistor increases power consumption, while a large resistor could lead to signal quality problems. The optimum size of the resistor depends on the capacitive load on the I2C lines and the required bus speed.

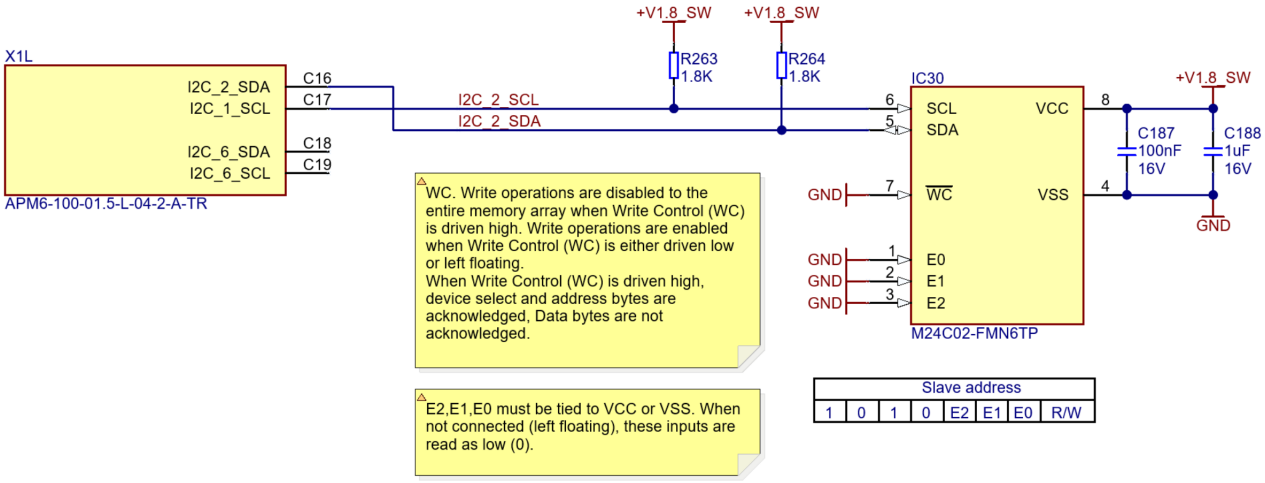
2.9.1 I²C signals

Table 10: I²C signals

Aquila pin	Aquila specification signal name
D8	I2C_1_SCL
D7	I2C_1_SDA
C17	I2C_2_SCL
C16	I2C_2_SDA
B41	I2C_3_DSI1_SCL
B40	I2C_3_DSI1_SDA
A13	I2C_4_CSI1_SCL
A12	I2C_4_CSI1_SDA
C6	I2C_5_CSI2_SCL
C5	I2C_5_CSI2_SDA
C19	I2C_6_SCL
C18	I2C_6_SDA

2.9.2 I²C reference schematics

Figure 26: I²C reference schematic



2.9.3 Unused I²C signal termination

All unused I²C signals can be left unconnected if the I²C port is switched off in software. Otherwise, it is recommended to keep the pull-up resistors available. Unused I²C signals can be configured as GPIO.

2.10 UART

There are four UART ports available in the Aquila module standard. UART_1 and UART_2 are general-purpose interfaces. The RX and TX signals of these interfaces are in the “Always Compatible” section, while the additional RTS/CTS signals for hardware flow control are in the “Reserved” group.

UART_3 is in the “Always Compatible” section and is intended to be used for main OS debug log output. It could be used for general purposes, but we recommend making this interface available for debugging purposes. UART_4 is in the “Reserved” class. On modules with a real-time core, this instance is intended to be used as the debug log output of the real-time operating system. The interface may be used as a general-purpose UART.

Do not re-assign the debug UARTs
Please note that changing the default UART interface instances being used for debug log output or serial console purposes is not supported in software. It is highly recommended to use the default UART interface instances specified for these purposes.

2.10.1 UART signals

Table 11: ”Always-compatible” UART signals

Aquila pin	Aquila specification signal name
B35	UART_1_RXD
B37	UART_1_TXD
B31	UART_2_RXD
B33	UART_2_TXD
D19	UART_3_RXD
D20	UART_3_TXD

Table 12: ”Reserved” UART signals

Aquila pin	Aquila specification signal name
B38	UART_1_RTS
B36	UART_1_CTS
B34	UART_2_RTS
B32	UART_2_CTS
D21	UART_4_RXD
D22	UART_4_TXD

2.10.2 UART reference schematics

Figure 27: RS232 reference schematic

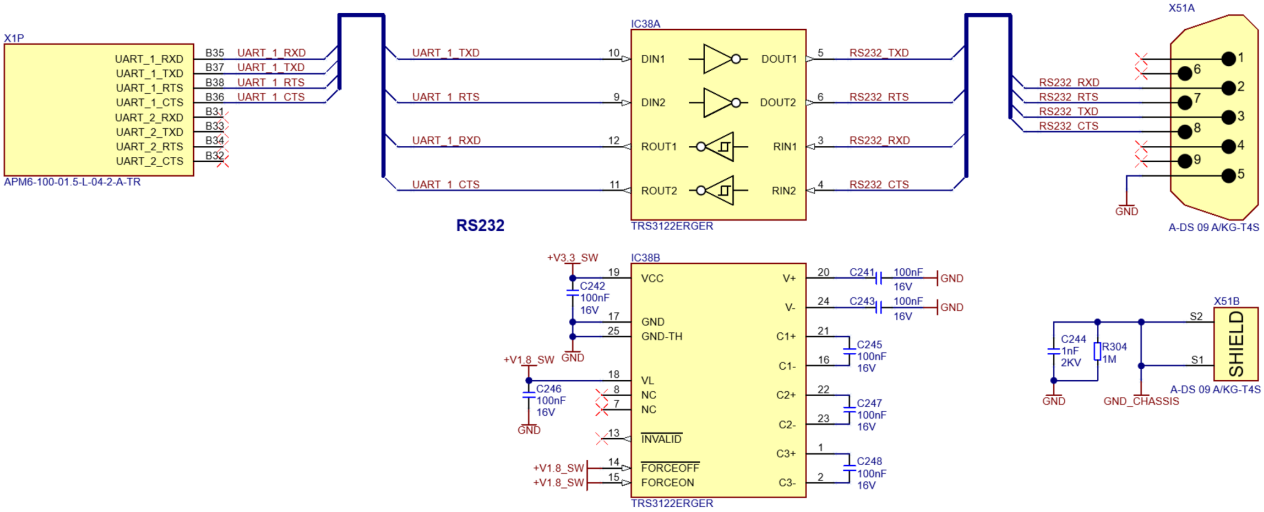


Figure 28: RS422 reference schematic

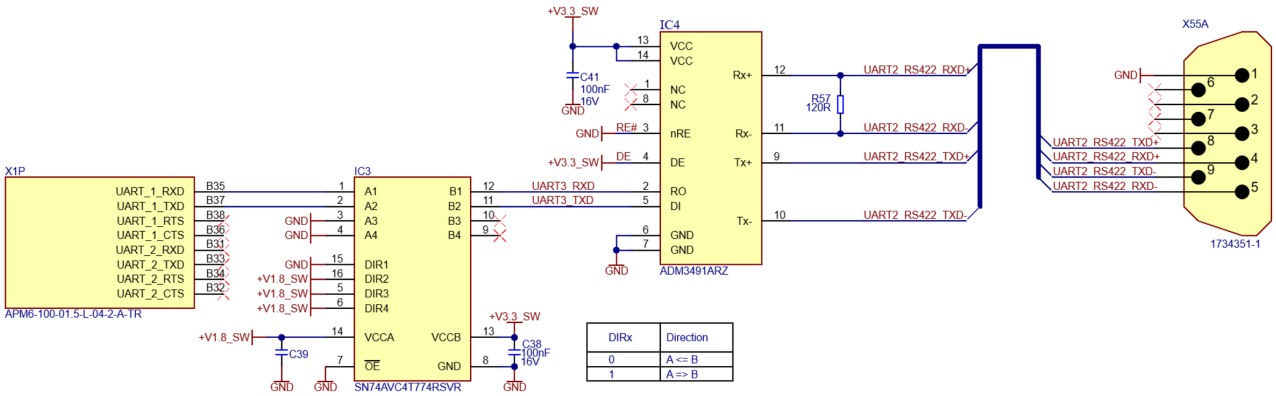
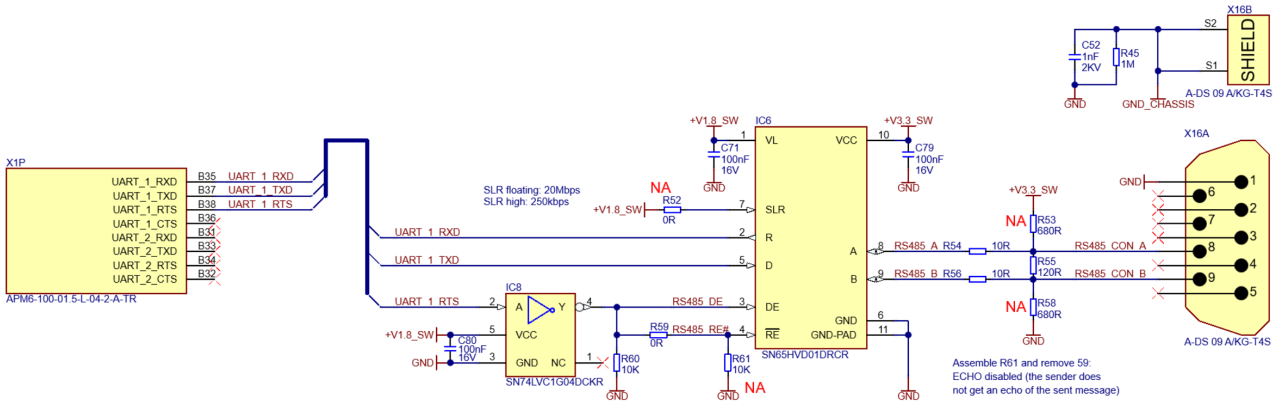


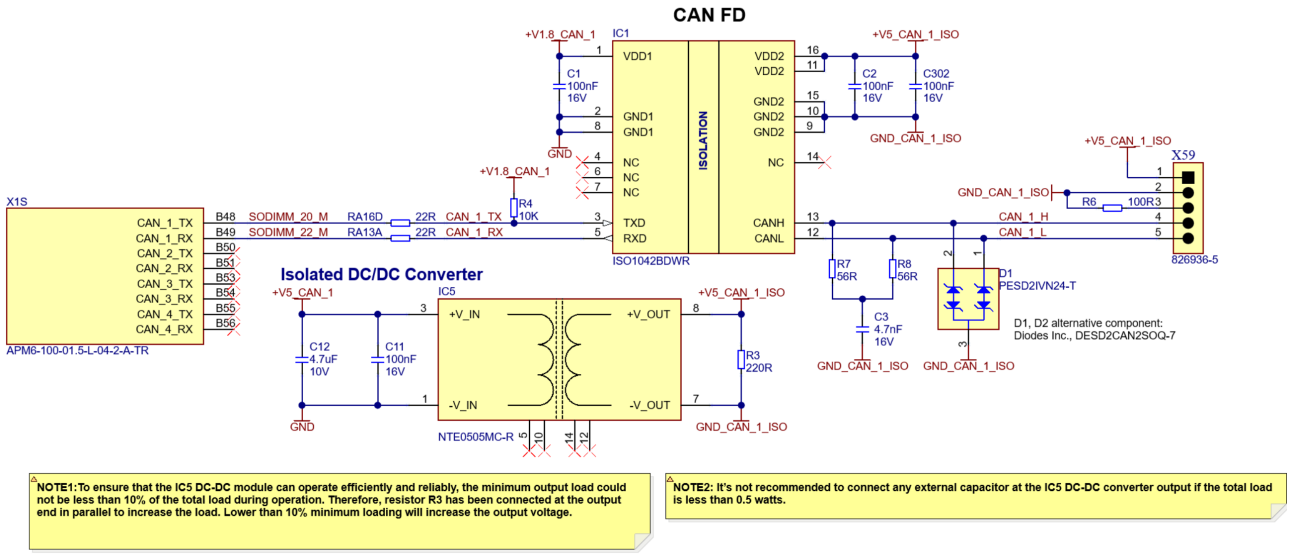
Figure 29: RS485 reference schematic



2.11 CAN

2.11.1 CAN reference schematics

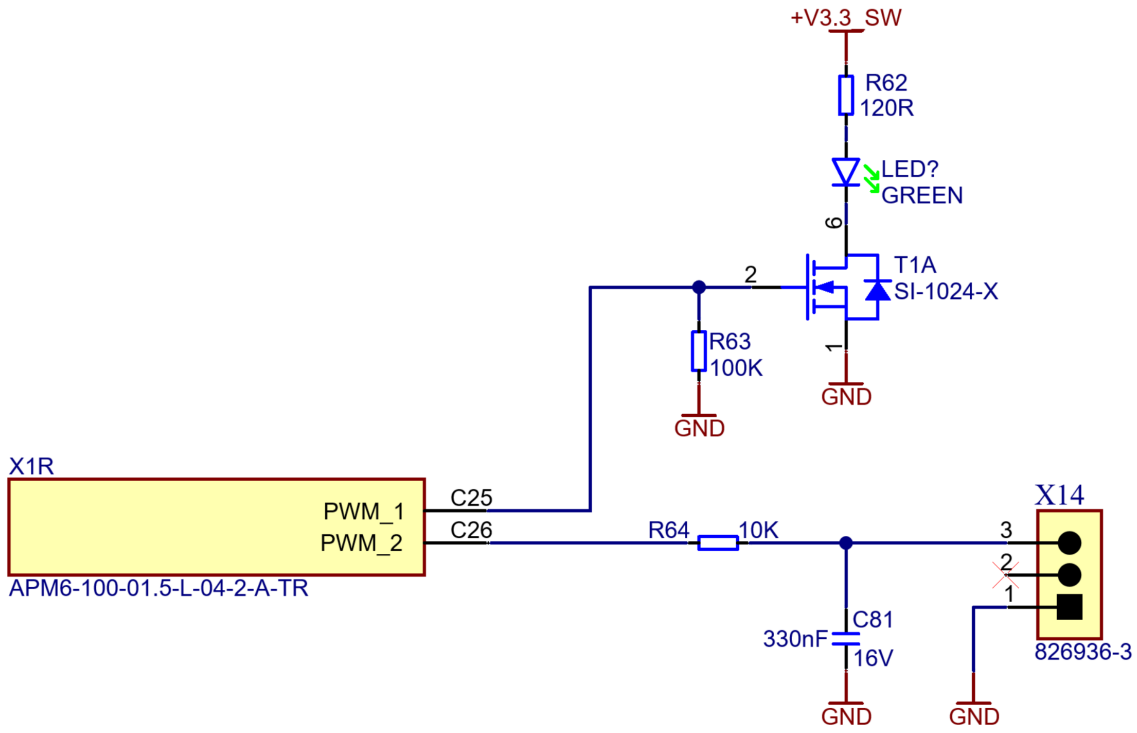
Figure 30: CAN reference schematic



2.12 PWM

2.12.1 PWM reference schematic

Figure 31: PWM reference schematic



2.13 I²S – Inter-IC Sound

2.13.1 I²S reference schematics

Figure 32: I²S W8904 refence schematic

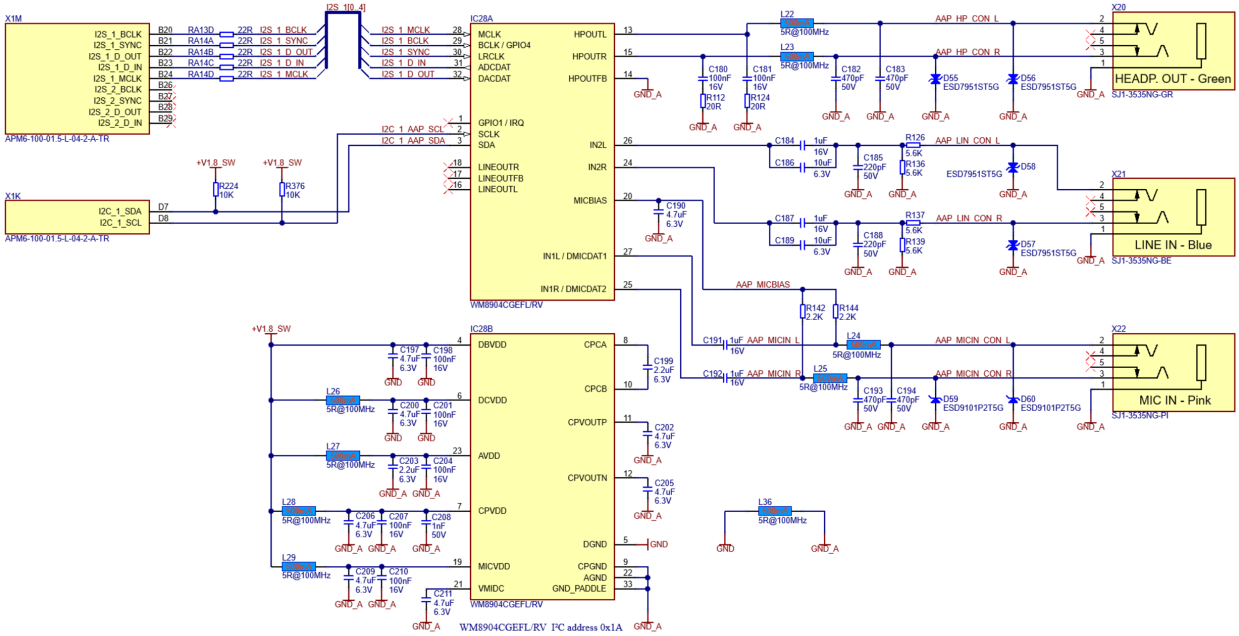
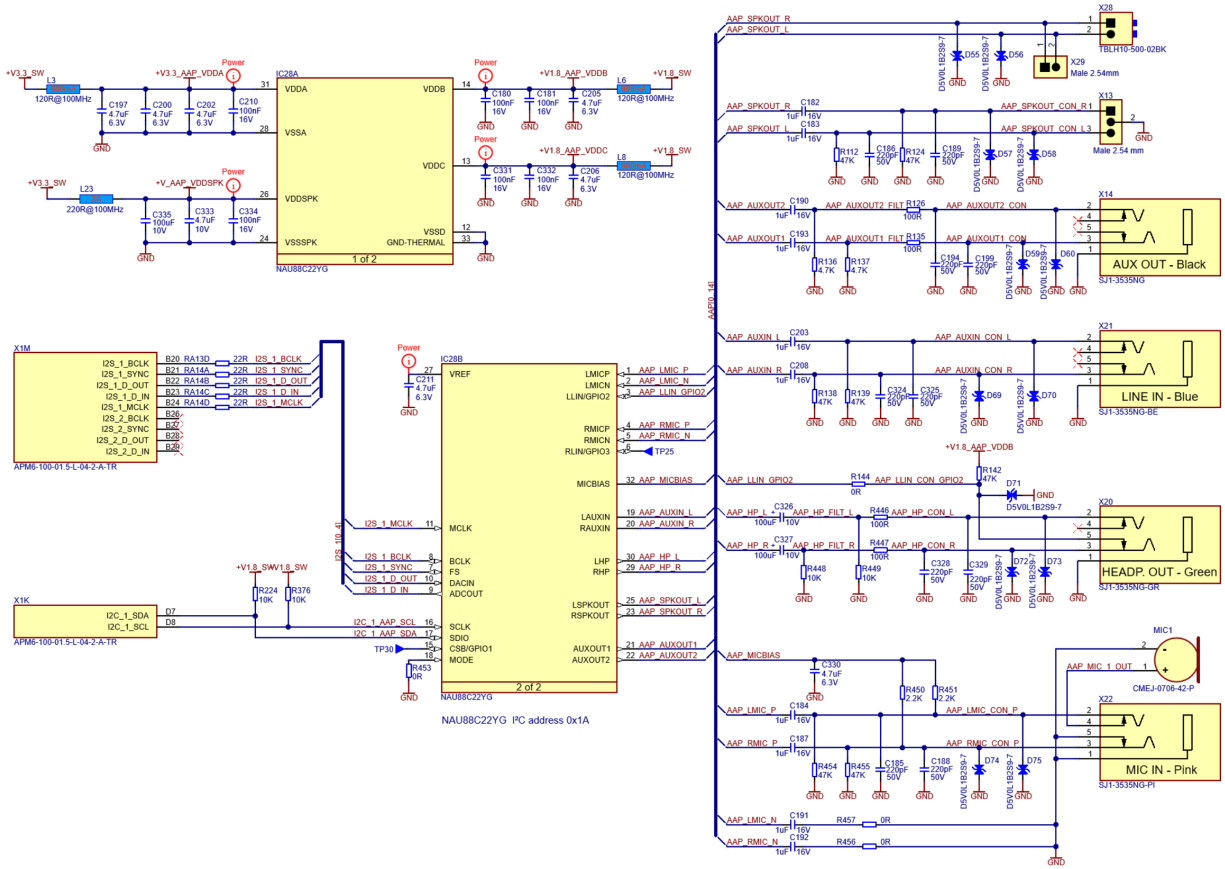


Figure 33: I²S NAU88C22 refence schematic



2.13.2 Unused I²S signal termination

Unused digital audio interface signals can be left unconnected.

2.14 Analog inputs

2.14.1 Unused analog input signal termination

The unused analog input signals can be left unconnected or tied to the ground. It is recommended to disable the corresponding inputs in the driver or disable the whole ADC block if unused.

2.15 General purpose clock outputs

The Aquila module standard reserves two module connector pins as general-purpose clock outputs. One output is intended to be used for the digital audio interface, while the other one is reserved for the camera interface. The clock outputs could also be used for other purposes if not required by the dedicated function. Please note that on some modules, the possible output frequencies are limited. There might also be limitations due to the other clock sources used in the module, or the interface they are dedicated to needs to be enabled to enable the clock output. Read the relevant datasheets carefully.

2.15.1 Clock output signals

Table 13: General purpose clock output signals

Aquila pin	Aquila specification signal name	I/O *SoM POV*	Type	Power rail	Description
B24	I2S_1_MCLK	O	CMOS	1.8V	Clock output for the digital audio interface
A14	CTRL_MCLK_MOCI	O	CMOS	1.8V	Clock output for the MIPI CSI-2 camera interface / General-Purpose Clock Output

2.15.2 Schematic and layout considerations

The clock output signals can have a pretty high frequency, especially for single-ended clock signals. This could lead to significant problems due to electromagnetic interferences (EMI). The clock signals should be kept as short as possible. High slew rates of the signal can increase the EMI problems. Therefore, it is desirable to reduce the slew rate as much as the signal quality allows it. Therefore, series resistors should be placed close to the clock output of the module. Start with a value of 22Ω. Try to increase this value until the corresponding interface fails due to the signal quality of the clock signal. Decrease the serial resistor again to have a reasonable margin.

Instead of using the clock output signals, some of the interfaces also allow using a different asynchronous clock reference. For example, suppose the audio codec or the camera needs to be located far away from the Aquila computer module. In that case, it might be a better solution to use an oscillator instead of the reference clock output of the module. This oscillator can be placed close to the audio codec or camera.

2.15.3 Unused clock output signal termination

Unused clock output signals can be left unconnected. The output should be disabled to reduce power consumption and EMI problems.

2.16 GPIO

The Aquila form factor features eight dedicated general-purpose input-output pins (GPIO) plus additional four GPIOs reserved for the MIPI DSI interface. Additional four GPIOs are reserved for the MIPI CSI_1 interface and four for MIPI CSI_2 interface and one GPIO pin is reserved for DP interface. Besides these 21x GPIOs, several pins can be used as GPIO if their primary function is not used. Table 2 and Table 3 show an overview of the interfaces.

For carrier boards intended to provide the highest compatibility with all different Aquila modules, it is recommended to use the 21x GPIO signals first. If additional GPIO signals are required, unused signal pins of the interfaces stated as “GPIO Capable” could be used.

2.16.1 GPIO Signals

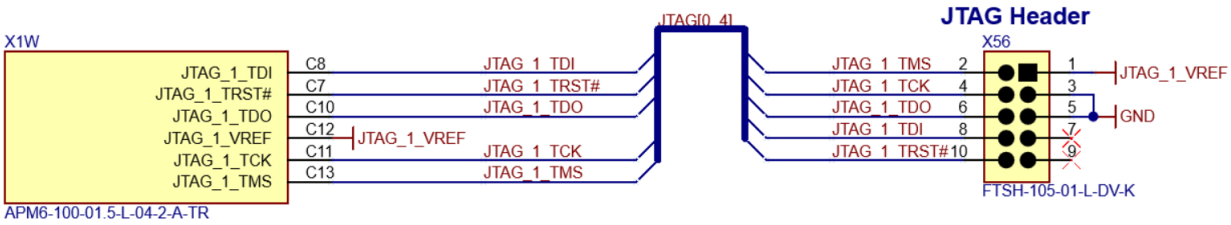
The following table contains the 21x GPIO pins available on Aquila modules. Consult the relevant datasheet of the modules for information on the other module edge connector pins that can be used as GPIO interface.

Table 14: GPIO signals

Aquila pin	Aquila specification signal name	I/O *SoM POV*	Type	Power rail	Description
D23	GPIO_1	I/O	CMOS	1.8V	General-purpose GPIO
D24	GPIO_2	I/O	CMOS	1.8V	General-purpose GPIO
D25	GPIO_3	I/O	CMOS	1.8V	General-purpose GPIO
C20	GPIO_4	I/O	CMOS	1.8V	General-purpose GPIO
C21	GPIO_5	I/O	CMOS	1.8V	General-purpose GPIO
C22	GPIO_6	I/O	CMOS	1.8V	General-purpose GPIO
C23	GPIO_7	I/O	CMOS	1.8V	General-purpose GPIO
C24	GPIO_8	I/O	CMOS	1.8V	General-purpose GPIO
B17	GPIO_9_CSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_1 interface
B18	GPIO_10_CSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_1 interface
A11	GPIO_11_CSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_1 interface
B19	GPIO_12_CSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_1 interface
C1	GPIO_13_CSI_2	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_2 interface
C2	GPIO_14_CSI_2	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_2 interface
C3	GPIO_15_CSI_2	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_2 interface
C4	GPIO_16_CSI_2	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI_2 interface
B42	GPIO_17_DSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI DSI interface
B43	GPIO_18_DSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI DSI interface
B44	GPIO_19_DSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI DSI interface
B45	GPIO_20_DSI_1	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI DSI interface
B57	GPIO_21_DP	I/O	CMOS	1.8V	Reserved general-purpose IO for DP interface

2.17 JTAG

Figure 34: JTAG refence schematic



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