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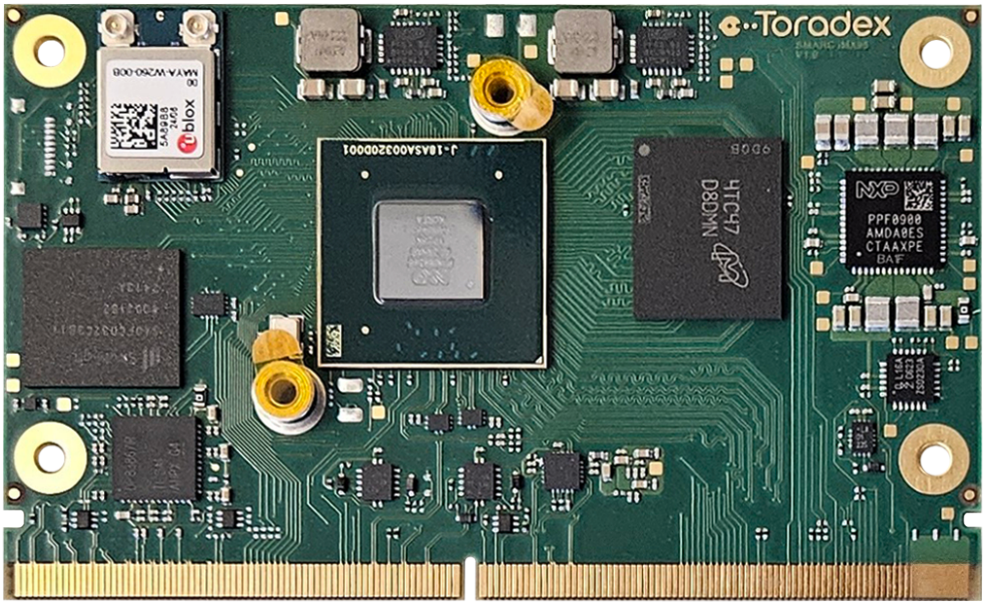
SMARC i.MX95

HW Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
07-Apr-2025	Rev. 0.1	V1.0	Initial documentation
06-May-2025	Rev. 0.2	V1.0	Section 5.1: Update title and diagram Figure 2. Minor changes.
21-May-2025	Rev. 0.3	V1.0	Section 1.6: Updated information about GPIOs, USB, SERDES and Display interfaces Section 3.2: Updated SPI Signal Group naming on Pin Assignment Tables (Table 9 and Table 10). Section 3.2: Updated Signal Group from USB4_EN_OC# Signal on Table 9. Section 5.1: Update Display Solution Block diagram on Figure 2. Section 5.3: Update USB Solution Block diagram on Figure 3. Minor changes.
27-May-2025	Rev. 0.4	V1.0	Section 1.5: Updated module variants for all section tables Section 1.5: Updated A55 core information on Table 1 Section 1.5: Updated USB and Gigabit Ethernet Information on Table 3 Section 1.5: Added Display Serial Interface Information on Table 3 Section 1.5: Updated LVDS Information on Table 3 Section 1.5: Updated Camera Information on Table 3 Section 1.5: Updated RAM and Flash Memory Information on Table 4 Section 1.5: Updated Temperature information on Table 5 Section 1.6: Updated information about Display Port++. Added comment about SERDES Section 1.10: Update DSI information for Option 3

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1 Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the SMARC i.MX95. For information on the actual features supported by software, please refer to the relevant SoM product page on the Toradex Website:

https://www.toradex.com/computer-on-modules/smarc-arm-family/nxp-imx95

1.2 SMARC SoM Family

The Toradex SMARC Family brings the trusted, well-known Toradex quality, reliability, and ease-of-use to the SMARC (Smart Mobility Architecture) standard. The Toradex SMARC Module is built according to the latest SMARC 2.2 and is compatible with most SMARC 2.1/2.0 carrier boards.

As a standard designed to accommodate a wide range of ARM and x86 Systems-on-Chip, SMARC made trade-offs to prioritize broad compatibility over cost, size, and performance.

1.3 NXP i.MX95 SoC

The i.MX 95 applications processor family delivers safe, secure, power-efficient edge computing for use in aerospace, automotive edge, commercial IoT, industrial, medical, and network platforms. It combines powerful AI-accelerated vision processing and immersive graphics abilities with functional safety, advanced security, and high-performance connectivity.

The NXP i.MX 95 SoC, featuring a rich set of high-speed interfaces with Ethernet Port up to 10 Gbps, and offering a high-performance computer with 6 Arm Cortex-A55. It also provides an expansive machine vision capability, advanced security, and support for several types of displays and multimedia.

1.4 SMARC i.MX95 SoM

The SMARC i.MX95 is a versatile System-on-Module (SoM) designed to cater to a diverse array of applications, including but not limited to Industrial Automation, Medical, Transportation, Smart Cities, Test and Measurement, and more.

Equipped with an optional Wi-Fi 6 and Bluetooth 5.2 interface, this SoM ensures cutting-edge connectivity. Its extensive range of interfaces spans from fundamental GPIOs to industry-standard I2C, I3C, SPI, USB, CAN FD, and UART buses. Furthermore, it accommodates advanced features like MIPI CSI camera interfaces, DisplayPort, LVDS, and 2x PCIe Gen3 x1 ports.

Notably, the SMARC i.MX95 module incorporates up to 2 Gigabit Ethernet PHY with IEEE1588 support directly on the module. A third Ethernet MAC with a SGMII/USXGMII interface is available for incorporating a 2.5 or 10-Gigabit Ethernet PHY on the carrier board.

In essence, the SMARC i.MX95 stands as a comprehensive solution, seamlessly blending robust connectivity, advanced interfaces, and adaptability for diverse applications.

1.5 Main Features

1.5.1 CPU

Table 1: CPU Features

Parameter	SMARC iMX95 Hexa 2GB ET	SMARC iMX95 Hexa 2GB WB IT	SMARC iMX95 Hexa 4GB ET	SMARC iMX95 Hexa 4GB WB IT	SMARC iMX95 Hexa 8GB IT	SMARC iMX95 Hexa 8GB WB IT
General						
SoC	i.MX95 *MIMX9596*	i.MX95 *MIMX9596*	i.MX95 *MIMX9596*	i.MX95 *MIMX9596*	i.MX95 *MIMX9596*	i.MX95 *MIMX9596*
Crypto	Yes	Yes	Yes	Yes	Yes	Yes
eFuse key storage	Yes	Yes	Yes	Yes	Yes	Yes
Secure boot	Yes	Yes	Yes	Yes	Yes	Yes
Secure clock	Yes	Yes	Yes	Yes	Yes	Yes
Tamper detection	Yes	Yes	Yes	Yes	Yes	Yes
Arm® Cortex®-A55 – Main CPU						
A55 Cores	6	6	6	6	6	6
A55 Clock	1.8GHz	1.8GHz	1.8GHz	1.8GHz	1.8GHz	1.8GHz
L1 Instruction Cache *per core*	32kB	32kB	32kB	32kB	32kB	32kB
L1 Data Cache *per core*	32kB	32kB	32kB	32kB	32kB	32kB
L2 Cache *per core*	64kB	64kB	64kB	64kB	64kB	64kB
L3 Cache *shared*	512kB	512kB	512kB	512kB	512kB	512kB
Neon SIMD	Yes	Yes	Yes	Yes	Yes	Yes
Arm® Cortex®-M7 – Real-time CPU						
M7 Cores	1	1	1	1	1	1
M7 Clock	400MHz	400MHz	400MHz	400MHz	400MHz	400MHz
Tightly Coupled Memory	512kB *with ECC*	512kB *with ECC*	512kB *with ECC*	512kB *with ECC*	512kB *with ECC*	512kB *with ECC*
Arm® Cortex®-M33 – Low power/Safety CPU						
M33 Cores	1	1	1	1	1	1
M33 Clock	333MHz	333MHz	333MHz	333MHz	333MHz	333MHz
OCRAM	256kB *with ECC*	256kB *with ECC*	256kB *with ECC*	256kB *with ECC*	256kB *with ECC*	256kB *with ECC*

1.5.2 GPU

Table 2: GPU features

Parameter	SMARC iMX95 Hexa 2GB ET	SMARC iMX95 Hexa 2GB WB IT	SMARC iMX95 Hexa 4GB ET	SMARC iMX95 Hexa 4GB WB IT	SMARC iMX95 Hexa 8GB IT	SMARC iMX95 Hexa 8GB WB IT
GPU Model	Arm Mali-G310 GPU					
2D Acceleration	Yes					
3D Acceleration	Yes					

Continued on next page

Table 2: GPU features (Continued)

Parameter	SMARC iMX95 Hexa 2GB ET	SMARC iMX95 Hexa 2GB WB IT	SMARC iMX95 Hexa 4GB ET	SMARC iMX95 Hexa 4GB WB IT	SMARC iMX95 Hexa 8GB IT	SMARC iMX95 Hexa 8GB WB IT
OpenGL ES				3.2		
Vulkan				1.3		

1.5.3 Interfaces

Table 3: Interfaces Features

Parameter	SMARC iMX95 Hexa 2GB ET	SMARC iMX95 Hexa 2GB WB IT	SMARC iMX95 Hexa 4GB ET	SMARC iMX95 Hexa 4GB WB IT	SMARC iMX95 Hexa 8GB IT	SMARC iMX95 Hexa 8GB WB IT
Audio						
Digital Audio	2x I^2S	2x I^2S	2x I^2S	2x I^2S	2x I^2S	2x I^2S
Camera						
MIPI® CSI-2	1x Quad Lane	1x Quad Lane	1x Quad Lane + 1x Dual Lane	1x Quad Lane + 1x Dual Lane	1x Quad Lane	1x Quad Lane
Display						
Display Controllers	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)	Single (Dual Engine)
DisplayPort *2.0a*	-	-	-	-	1x (up to 4K)	1x (up to 4K)
Display Serial Interface (DSI)	1x Quad-Lane DSI (up to 4k)	1x Quad-Lane DSI (up to 4k)	-	-	-	-
LVDS *dual-channel*	1x Single Channel (up to 1920x1080)	1x Single Channel (up to 1920x1080)	1x Dual Channel (up to 1920x1080)	1x Dual Channel (up to 1920x1080)	1x Dual Channel (up to 1920x1080)	1x Dual Channel (up to 1920x1080)
Low Speed						
CAN-FD	2x	2x	2x	2x	2x	2x
I^2C	5x	5x	5x	5x	5x	5x
PWM	3x	3x	3x	3x	3x	3x
SPI	2x	2x	2x	2x	2x	2x
UART	4x	4x	4x	4x	4x	4x
Network						
Bluetooth	-	BT 5.2	-	BT 5.2	-	BT 5.2
Gigabit	1x	1x	2x	2x	2x	2x
10-Gigabit Ethernet	1x	1x	1x	1x	1x	1x
Wi-Fi	-	2.4/5 GHz Dual Band 1x1 Wi-Fi 6 (802.11ax)	-	2.4/5 GHz Dual Band 1x1 Wi-Fi 6 (802.11ax)	-	2.4/5 GHz Dual Band 1x1 Wi-Fi 6 (802.11ax)
Other						
PCIe *Gen 3*	2x	2x	2x	2x	2x	2x
Storage						
SD/SDIO/MMC	1x	1x	1x	1x	1x	1x
USB						
USB 2.0 OTG	1x	1x	1x	1x	1x	1x

Continued on next page

Table 3: Interfaces Features (Continued)

Parameter	SMARC iMX95 Hexa 2GB ET	SMARC iMX95 Hexa 2GB WB IT	SMARC iMX95 Hexa 4GB ET	SMARC iMX95 Hexa 4GB WB IT	SMARC iMX95 Hexa 8GB IT	SMARC iMX95 Hexa 8GB WB IT
USB 2.0 Host (SS Signals for USB 2.0 OTG)	-	-	2x	2x	2x	2x
USB 3.2 (Gen 1)	1x	1x	2x	2x	2x	2x

1.5.4 Memory

Table 4: Memory

Parameter	SMARC iMX95 Hexa 2GB ET	SMARC iMX95 Hexa 2GB WB IT	SMARC iMX95 Hexa 4GB ET	SMARC iMX95 Hexa 4GB WB IT	SMARC iMX95 Hexa 8GB IT	SMARC iMX95 Hexa 8GB WB IT
eMMC						
eMMC Configuration	3D TLC	2D MLC	2D MLC	2D MLC	2D MLC	2D MLC
eMMC Capacity	16GB	16GB	32GB	32GB	32GB	32GB
I²C EEPROM						
I²C EEPROM Capacity	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits
RAM						
RAM Capacity	2GB	2GB	4GB	4GB	8GB	8GB
RAM Configuration *ctrl. × ch. × bits*[1]	32-bit Dual Channel 1 × 2 × 16	32-bit Dual Channel 1 × 2 × 16	32-bit Dual Channel 1 × 2 × 16	32-bit Dual Channel 1 × 2 × 16	32-bit Dual Channel 1 × 2 × 16	32-bit Dual Channel 1 × 2 × 16
RAM Type	LPDDR5	LPDDR5	LPDDR5	LPDDR5	LPDDR5	LPDDR5
RAM Speed	6400MT/s	6400MT/s	6400MT/s	6400MT/s	6400MT/s	6400MT/s
Inline ECC	Yes	Yes	Yes	Yes	Yes	Yes

[1] Controllers × channels per controller × bits per channel.

1.5.5 Physical

Table 5: Physical Features

Parameter	SMARC iMX95 Hexa 2GB ET	SMARC iMX95 Hexa 2GB WB IT	SMARC iMX95 Hexa 4GB ET	SMARC iMX95 Hexa 4GB WB IT	SMARC iMX95 Hexa 8GB IT	SMARC iMX95 Hexa 8GB WB IT
Size	82.0 x 50.0 mm					
Temperature	-25°C to 85°C	-40°C to 85°C	-25°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
Shock / Vibration	EN 60068-2-6/50g 20ms					
Power Dissipation	TBD					

1.6 Interface Overview

The table below shows the interfaces that are supported on the SMARC i.MX95 module. The following convention is used for the features:

- “Shall” indicates a mandatory requirement

- "Should" indicates a recommended but not mandatory requirement
- "May" indicates a lesser used optional interface

Table 6: Interfaces Overview

Feature	Sub Feature	SMARC Spec	Toradex SMARC i.MX95	Comments
Wireless Module	It is optional, shows if option is available	May	Yes	Build-to-Order (BTO) options without Wi-fi
Size	82 x 50 mm	Shall	Yes	
	82 x 80 mm	May	Not Available	Unavailable
LVDS LCD	LVDS0 18/24 bit single channel	Should	Yes	
	LVDS1 24 bit single channel	May	Yes	Assembly Option
eDP on LVDS Pins	eDP0 on LVDS0 - 4 diff pairs	May	Not Available	eDP only available on regular Display Port
	eDP1 on LVDS1 - 4 diff pairs	May	Not Available	eDP only available on regular Display Port
DSI on LVDS Pins	DSI0-2 lane implementation	May	Not Available	
	DSI0-4 lane implementation	May	Not Available	
	DSI1-2 lane implementation	May	Yes	Shared with LVDS1. Assembly Option
	DSI1-4 lane implementation	May	Yes	Shared with LVDS1. Assembly Option
HDMI	HDMI Display interface	Should	Not Available	HDMI not available
DP on HDMI Pins		May	Not Available	HDMI not available
DP++	DisplayPort++	May	Yes	HDMI not available. Regular DP available on DP0. There is a DSI to DP converter on the SoM (Assembly Option)
CSI	CSI0 - 2 lane implementation	May	Yes	Assembly Option
	CSI1 - 2 lane implementation	Should	Yes	
	CSI1 - 4 lane implementation	Should	Yes	
	CSI2 - 2 lane implementation	May	Not Available	
	CSI2 - 4 lane implementation	May	Not Available	
	CSI3 - 2 lane implementation	May	Not Available	
	CSI3 - 4 lane implementation	May	Not Available	
SDIO	SDIO (4 bit, for SD cards)	Should	Yes	
SPI	SPI0	Should	Yes	
	SPI1	Should	Yes	
	QuadSPI	Should	Not Available	
	eSPI	Should	Not Available	
Audio	I2S0	Should	Yes	
	HDA or I2S2	Should	Yes (I2S2)	
I2C	Power Management	Shall	Yes	
	General Purpose	Shall	Yes	
	Camera 0/1	Should	Yes	
	LCD Display I/D	Should	Yes	
	HDMI	Should	Not Available	
Serial Ports	SER0 (4 wire)	Shall	Yes	

Continued on next page

Table 6: Interfaces Overview (Continued)

Feature	Sub Feature	SMARC Spec	Toradex SMARC i.MX95	Comments
	SER1 (2 wire)	Shall	Yes	
	SER2 (4 wire)	Should	Yes	
	SER3 (2 wire)	Should	Yes	
CAN	CAN0	May	Yes	
CAN	CAN1	May	Yes	
USB	USB0 (2.0)	Shall	Yes	
	USB1 (2.0)	Should	Yes	Assembly option: USB Hub
	USB2 (2.0)	May	Yes	
	USB2 (3.2)	Should	Yes	Assembly option: USB Hub
	USB3 (2.0)	May	Yes	Assembly option: USB Hub
	USB3 (3.2)(OTG)	May	Yes	Assembly option: USB Hub
	USB4 (2.0)	May	Yes	Assembly option: USB Hub
	USB5 (2.0)	May	Not Available	
PCIe	PCIE_A (x1 Gen 1 Root)	Should	Yes	Gen 3
	PCIE_B (x1 Gen 1 Root)	May	Yes	Gen 3
	PCIE_C (x1 Gen 1 Root)	May	Not Available	
	PCIE_D (x1 Gen 1 Root)	May	Not Available	
SERDES	Alternative use of PCIE_C and/or PCIE_D	May	Yes	SERDES 0 implemented on PCIE_D
SATA	SATA Gen 1	Should	Not Available	
	SATA Gen 2 operation	May	Not Available	
	SATA Gen 3 operation	May	Not Available	
GbE	GBE0	Should	Yes	
	GBE1	May	Yes	
	IEEE1588 Triggers(GBE[0:1]_SDP)	May	Yes	
Watchdog	WDT Out	Should	Yes	
GPIO	GPIO[0:11]	Shall	Yes	
	GPIO[12:13]	Should	Yes	
	GPIO[0:11] interrupt capability	Shall	Yes	
	GPIO[12:13] interrupt capability	Should	Yes	
	GPIO Camera Support	Shall	Yes	
	GPIO5 PWM capability	Should	Yes	
	GPIO6 Tachin capability	Should	Not Available	
Management	System and power management features	Shall	Yes	Implemented according to SMARC V2.2 spec.
	BATLOW#	Shall	Yes	
	CARRIER_PWR_ON	Shall	Yes	
	CARRIER_STBY#	Should	Yes	
	CHARGER_PRSNT#	Should	Yes	

Continued on next page

Table 6: Interfaces Overview (Continued)

Feature	Sub Feature	SMARC Spec	Toradex SMARC i.MX95	Comments
	CHARGING#	Should	Yes	
	VIN_PWR_BAD#	Should	Yes	
	SLEEP#	Should	Yes	
	LID#	Should	Yes	
Management	POWER_BTN#	Should	Yes	
	RESET_OUT#	Should	Yes	
	RESET_IN#	Should	Yes	
	SMB_ALERT#	Should	Yes	
	TEST#	Should	Yes	
Boot Select	BOOT_SEL0# nBOOT_SEL1# nBOOT_SEL2#	Shall	Yes	Implemented according to SMARC V2.2 spec.
Force Recovery	FORCE_RECOV	Shall	Yes	Implemented according to SMARC V2.2 spec.
JTAG	JTAG Connector on Module	May	Yes	The on-module JTAG connector is not assembled on samples
RTC		Should	Yes	

Note: Data provided is based on the latest available specifications.

1.7 Reference Documents

1.7.1 NXP i.MX95

You will find additional details about the i.MX95 SoC on the Datasheet and the Reference Manual provided by NXP:

https://www.nxp.com/products/iMX95

1.7.2 Carrier Board Design Guide

Missing Content
More information about the carrier board design guide will be available on the next release of the datasheet.

1.7.3 SMARC Specification

The SMARC i.MX95 follows the SMARC 2.2 spefication.

- SMARC Hardware Specification 2.2
- SMARC Design Guide 2.1.1

1.7.4 Layout Design Guide

This document contains information about high-speed layout design and additional factors that help get the carrier board layout right the first time.

https://docs.toradex.com/102492-layout-design-guide.pdf

1.7.5 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information on a regular basis. You can find an abundance of additional information there. Please note that the Developer Center is common to all Toradex products. You should always check to ensure if the information provided is valid or relevant for the SMARC i.MX95.

https://developer.toradex.com

1.7.6 SMARC Carrier Board Schematics

Missing Content
More information about the SMARC Carrier Board Schematics will be available on the next release of the datasheet.

1.7.7 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin, Apalis,Colibri and SMARC Modules. The tool allows comparing the interfaces across different modules.

https://developer.toradex.com/knowledge-base/pinout-designer

1.7.8 EEPROM

The SMARC i.MX95 has an on-module I²C EEPROM, the M24C02 from STMicroelectronics.

https://www.st.com/en/memories/m24c02-r.html

1.7.9 Ethernet Transceiver

SMARC i.MX95 utilizes a DP83867IR Gigabit Ethernet Transceiver with RGMII from Texas Instruments. https://www.ti.com/product/DP83867IR

1.7.10 PCB Temperature Sensor

The SMARC i.MX95 can be assembled with a PCB temperature sensor, the TI TMP1075DSGR. https://www.ti.com/product/TMP1075

1.7.11 RTC

The SMARC i.MX95 has a low-power RX8130CE real-time clock from Epson.

https://www5.epsondevice.com/en/products/rtc/rx8130ce.html

1.7.12 TPM 2.0 Module

The SMARC i.MX95 can be assembled with a Trusted Platform Module (TPM 2.0), the ST33KTPM2I from STMicroelectronics. The complete documentation is only available under a STMicroelectronics NDA.

1.7.13 Wi-Fi and Bluetooth Module

The SMARC i.MX95 has a MAYA-W260 host-based multiradio module with Wi-Fi 6 and BT 5.4.

https://www.u-blox.com/en/product/maya-w2-series

1.8 Naming Conventions

In this document, a consistent naming convention is used. It is essential to notice the punctuation and spaces in the names. Do not confuse:

- The NXP i.MX95 SoC with the Toradex SMARC i.MX95 SoM.
- The SMARC i.MX95 SoM with the Verdin i.MX95 SoM. Each one belongs to different SoM families, having different features.

Table 7: Naming conventions

Name	Description
i.MX 9 Series	An i.MX 9 series of applications processors that bring together higher performance applications cores. It's composed by i.MX 91, i.MX 93 and i.MX 95 SoCs. For information on the i.MX 9-based chips, please visit the NXP website.
i.MX 95	An i.MX 95 applications processor family. Whenever this document uses the term i.MX 95, all versions of the i.MX 95 SoC family are meant.
SMARC i.MX 95	Short Name for the SMARC module based on the i.MX 95 family SoC.
Verdin i.MX 95	Short name for the Verdin module based on the i.MX 95 family SoC. This document only contains information on the SMARC module. For information on other i.MX95 Series based modules, please visit the Toradex website.

1.9 Abbreviations

Table 8: Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground

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Table 8: Abbreviations (Continued)

Abbreviation	Explanation
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface

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Table 8: Abbreviations (Continued)

Abbreviation	Explanation
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.10 Build-To-Order (BTO) Options

The SMARC i.MX95 module is available in different variants. In addition to these configurations, it is possible to order customized versions of the module. These versions are Build-To-Order (BTO). More information can be found on our Developer Website.

The following customization options are technically possible for the SMARC i.MX95:

SoC variant:

- As defined by NXP SoC Datasheet

Capacity options:

- RAM capacity (2 - 16GB)
- Flash capacity (4 - 128GB)

Connectivity options:

- Addition or removal of Wi-Fi/Bluetooth module
- Addition or removal of 2nd Ethernet PHY

Display and CSI Interface assembly options:

- Option 1 (Default option):

  LVDS0 and LVDS1 Implemented (Dual Channel LVDS)

  DP (DSI to DP conversion)

  CSI0 not available

- Option 2

  LVDS0 and LVDS1 Implemented (Dual Channel LVDS)

  No DP (No DSI)

  CSI0 (2-Lane) implemented

- Option 3

  DSI1 (Quad-lane DSI) on LVDS1 pins

  LVDS 0 Implemented (Single Channel LVDS)

  No DP

  CSI0 not available

Other interface and peripheral options:

- Addition or removal of PCB temperature sensor
- Addition or removal of TPM 2.0 (on SPI interface)

- Addition or removal of USB Hub

Other options:

- Temperature Range:

  Commercial : 0°C - 70°C

  Wide Temp : -25°C - 85°C

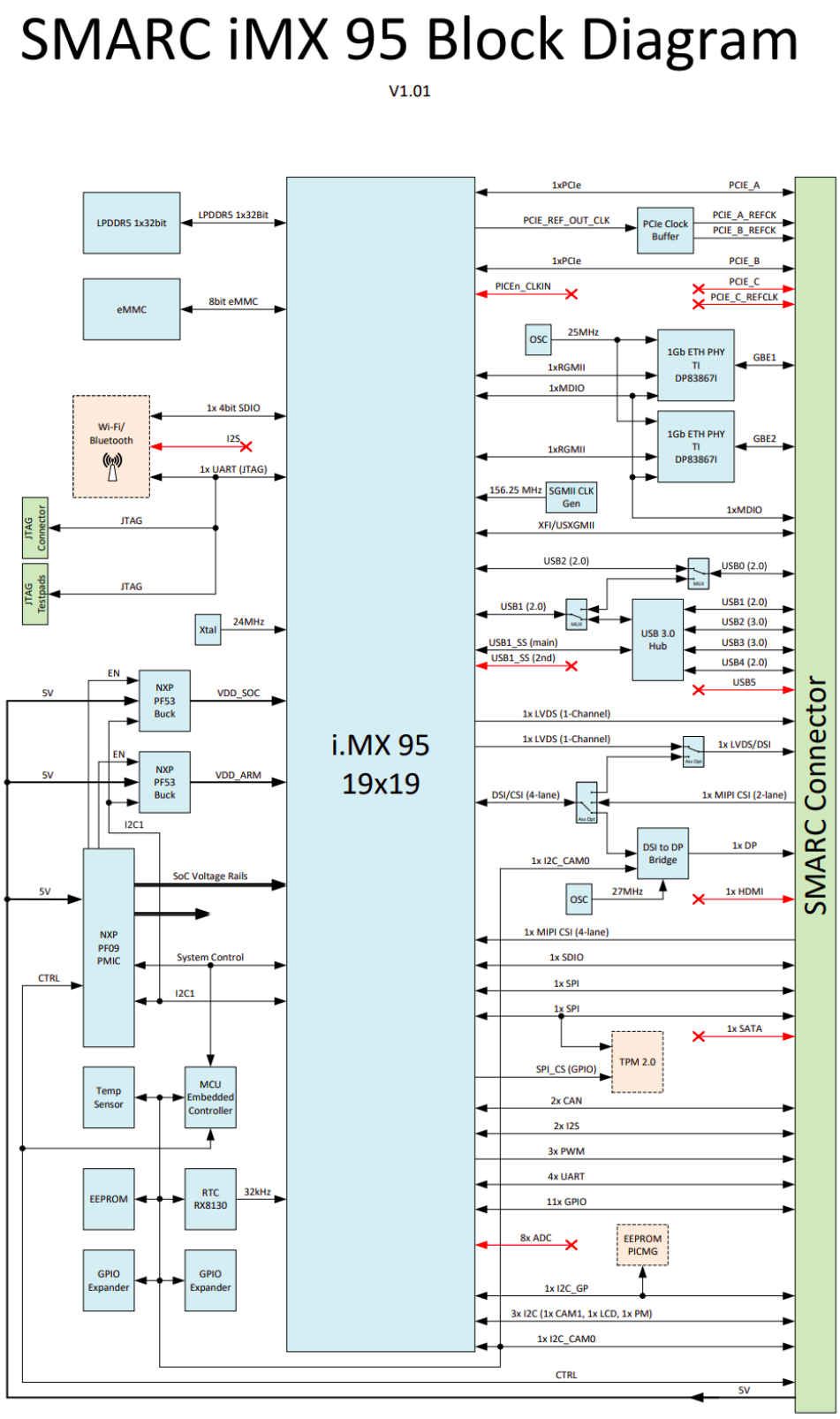
  Industrial : -40°C - 85°C

- FuSa PMICs (PF53 FuSa PNs from NXP)

2 Architecture Overview

2.1 Block Diagram

Figure 1: SMARC iMX95 Block Diagram



3 Connector

3.1 Pin Numbering

The SMARC i.MX95 module follows the standard proposed by the SMARC standard (Section 1.7.3). Pins on the top side of the module are numbered from P1 to P156, while the pins on the bottom side are numbered from S1 to S158. Key pins are not numbered.

3.2 Pin Assignment

Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
P1	CTRL	SMB_ALERT#		CCM_CLKO3	AK20	NVCC_CCM_DAP	
P2	CTRL	GND	_GND				
P3	CSI	CSI1_CK+	MIPI_CSI1_CLK_P		E15	VDD_MIPI_1P8	
P4	CSI	CSI1_CK-	MIPI_CSI1_CLK_N		F16	VDD_MIPI_1P8	
P5	Ethernet	GBE1_SDP	CCM_CLKO4		AJ21	NVCC_CCM_DAP	3.3V Level Shifter
P6	Ethernet	GBE0_SDP	CCM_CLKO2		AF20	NVCC_CCM_DAP	3.3V Level Shifter
P7	CSI	CSI1_RX0+	MIPI_CSI1_D0_P		E19	VDD_MIPI_1P8	
P8	CSI	CSI1_RX0-	MIPI_CSI1_D0_N		F20	VDD_MIPI_1P8	
P9	CSI	GND	_GND				
P10	CSI	CSI1_RX1+	MIPI_CSI1_D1_P		E17	VDD_MIPI_1P8	
P11	CSI	CSI1_RX1-	MIPI_CSI1_D1_N		D18	VDD_MIPI_1P8	
P12	CSI	GND	_GND				
P13	CSI	CSI1_RX2+	MIPI_CSI1_D2_P		E13	VDD_MIPI_1P8	
P14	CSI	CSI1_RX2-	MIPI_CSI1_D2_N		D14	VDD_MIPI_1P8	
P15	CSI	GND	_GND				
P16	CSI	CSI1_RX3+	MIPI_CSI1_D3_P		E11	VDD_MIPI_1P8	
P17	CSI	CSI1_RX3-	MIPI_CSI1_D3_N		F12	VDD_MIPI_1P8	
P18	CSI	GND	_GND				
P19	Ethernet	GBE0_MDI3-	Ethernet PHY				
P20	Ethernet	GBE0_MDI3+	Ethernet PHY				
P21	Ethernet	GBE0_LINK_100#	Ethernet PHY				3.3V IO
P22	Ethernet	GBE0_LINK_1000#	Ethernet PHY				3.3V IO
P23	Ethernet	GBE0_MDI2-	Ethernet PHY				

Continued on next page

Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
P24	Ethernet	GBE0_MDI2+	Ethernet PHY				
P25	Ethernet	GBE0_LINK_ACT#	Ethernet PHY				3.3V IO
P26	Ethernet	GBE0_MDI1-	Ethernet PHY				
P27	Ethernet	GBE0_MDI1+	Ethernet PHY				
P28	Ethernet	GBE0_CTREF	Ethernet PHY				
P29	Ethernet	GBE0_MDI0-	Ethernet PHY				
P30	Ethernet	GBE0_MDI0+	Ethernet PHY				
P31	SPI	SPI0_CS1#	GPIO_IO24		T48	NVCC_GPIO	
P32	SPI	GND	_GND				
P33	SDIO	SDIO_WP		IO_EXP18_P1_7			Connected to IO Expander
P34	SDIO	SDIO_CMD	SD2_CMD		AB52	NVCC_SD2	
P35	SDIO	SDIO_CD#	SD2_CD_B		AD48	NVCC_SD2	
P36	SDIO	SDIO_CK	SD2_CLK		AB48	NVCC_SD2	
P37	SDIO	SDIO_PWR_EN	SD2_RESET_B		AD52	NVCC_SD2	3.3V Level Shifter
P38	SDIO	GND	_GND				
P39	SDIO	SDIO_D0	SD2_DATA0		AC51	NVCC_SD2	
P40	SDIO	SDIO_D1	SD2_DATA1		AC49	NVCC_SD2	
P41	SDIO	SDIO_D2	SD2_DATA2		AA51	NVCC_SD2	
P42	SDIO	SDIO_D3	SD2_DATA3		AA49	NVCC_SD2	
P43	SPI	SPI0_CS0#	GPIO_IO00		J49	NVCC_GPIO	
P44	SPI	SPI0_CK	GPIO_IO03		K52	NVCC_GPIO	
P45	SPI	SPI0_DIN	GPIO_IO01		J51	NVCC_GPIO	
P46	SPI	SPI0_DO	GPIO_IO02		K48	NVCC_GPIO	

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
P47	SPI	GND	_GND				
P48	SATA	SATA_TX+			Not Connected		
P49	SATA	SATA_TX-			Not Connected		
P50	SATA	GND	_GND				
P51	SATA	SATA_RX+			Not Connected		
P52	SATA	SATA_RX-			Not Connected		
P53	SATA	GND	_GND				
P54	SPI	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	GPIO_IO18		P52	NVCC_GPIO	
P55	SPI	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#		XSPI1_SS1_B	AH42		
P56	SPI	ESPI_CK / SPI1_CK / QSPI_CK	GPIO_IO37		Y52	NVCC_GPIO	
P57	SPI	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	GPIO_IO19		R45	NVCC_GPIO	
P58	SPI	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	GPIO_IO36		Y48	NVCC_GPIO	
P59	SPI	GND	_GND				
P60	USB	USB0+	USB2_D_P	USB1_D_P		VDD_USB_3P3	
P61	USB	USB0-	USB2_D_N	USB1_D_N		VDD_USB_3P3	
P62	USB	USB0_EN_OC#	IO_EXP33_P4	IO_EXP33_P5			3.3V IO / Connected to IO Expander
P63	USB	USB0_VBUS_DET	USB2_VBUS	USB1_VBUS		VDD_USB_3P3	5V IO
P64	USB	USB0_OTG_ID		IO_EXP33_P3			3.3V IO / Connected to IO Expander
P65	USB	USB1+	USB_Hub				
P66	USB	USB1-	USB_Hub				
P67	USB	USB1_EN_OC#	USB_Hub				3.3V IO
P68	USB	GND	_GND				
P69	USB	USB2+	USB_Hub				

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
P70	USB	USB2-	USB_Hub				
P71	USB	USB2_EN_OC#	USB_Hub				3.3V IO
P72	USB	RSVD			Not Connected		
P73	USB	RSVD			Not Connected		
P74	USB	USB3_EN_OC#	USB_Hub				3.3V IO
key							
key							
key							
key							
P75	PCIe	PCIE_A_RST#		IO_EXP33_P2			Connected to IO Expander
P76	USB	USB4_EN_OC#	USB_Hub				
P77	PCIe	PCIE_B_CKREQ#	GPIO_IO35		W51		FET bidirectional level shifter
P78	PCIe	PCIE_A_CKREQ#	GPIO_IO32		V52		FET bidirectional level shifter
P79	PCIe	GND	_GND				
P80	PCIe	PCIE_C_REFCK+					
P81	PCIe	PCIE_C_REFCK-					
P82	PCIe	GND	_GND				
P83	PCIe	PCIE_A_REFCK+	CLK Buffer				
P84	PCIe	PCIE_A_REFCK-	CLK Buffer				
P85	PCIe	GND	_GND				
P86	PCIe	PCIE_A_RX+	PCIE1_RX0_P		B28	VDD_PCI_1P8	
P87	PCIe	PCIE_A_RX-	PCIE1_RX0_N		A29	VDD_PCI_1P8	
P88	PCIe	GND	_GND				

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Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
P89	PCIe	PCIE_A_TX+	PCIE1_TX0_P		E29	VDD_PCI_1P8	
P90	PCIe	PCIE_A_TX-	PCIE1_TX0_N		D30	VDD_PCI_1P8	
P91	HDMI/DP	GND	_GND				
P92	HDMI/DP	HDMI_D2+ / DP1_LANE0+			Not Connected		
P93	HDMI/DP	HDMI_D2- / DP1_LANE0-			Not Connected		
P94	HDMI/DP	GND	_GND				
P95	HDMI/DP	HDMI_D1+ / DP1_LANE1+			Not Connected		
P96	HDMI/DP	HDMI_D1- / DP1_LANE1-			Not Connected		
P97	HDMI/DP	GND	_GND				
P98	HDMI/DP	HDMI_D0+ / DP1_LANE2+			Not Connected		
P99	HDMI/DP	HDMI_D0- / DP1_LANE2-			Not Connected		
P100	HDMI/DP	GND	_GND				
P101	HDMI/DP	HDMI_CK+ / DP1_LANE3+			Not Connected		
P102	HDMI/DP	HDMI_CK- / DP1_LANE3-			Not Connected		
P103	HDMI/DP	GND	_GND				
P104	HDMI/DP	HDMI_HPD / DP1_HPD			Not Connected		
P105	HDMI/DP	HDMI_CTRL_CK / DP1_AUX+			Not Connected		
P106	HDMI/DP	HDMI_CTRL_DAT / DP1_AUX-			Not Connected		
P107	HDMI/DP	DP1_AUX_SEL			Not Connected		
P108	GPIO	GPIO0 / CAM0_PWR#		IO_EXP18_P0_0			Connected to IO Expander
P109	GPIO	GPIO1 / CAM1_PWR#		IO_EXP18_P0_1			Connected to IO Expander
P110	GPIO	GPIO2 / CAM0_RST#		XSPI1_DATA0	AJ45		
P111	GPIO	GPIO3 / CAM1_RST#		XSPI1_DATA1	AH46		

Continued on next page

Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
P112	GPIO	GPIO4 / HDA_RST#		XSPI1_DATA2	AJ47		
P113	GPIO	GPIO5 / PWM_OUT	GPIO1_IO6		L49		
P114	GPIO	GPIO6 / TACHIN		XSPI1_DATA3	AK48		Alternate Function: GPT1_CLK
P115	GPIO	GPIO7		XSPI1_SCLK	AJ43		
P116	GPIO	GPIO8		XSPI1_SS0_B	AJ41		
P117	GPIO	GPIO9		XSPI1_DQS	AK44		
P118	GPIO	GPIO10		ENET2_MDIO	AJ31		
P119	GPIO	GPIO11		ENET2_MDC	AK32		
P120	I2C	GND	_GND				
P121	I2C	I2C_PM_CK	GPIO_IO29		V44	NVCC_GPIO	
P122	I2C	I2C_PM_DAT	GPIO_IO28		U51	NVCC_GPIO	
P123	CTRL	BOOT_SEL0#	MCU	MCU_PA27			
P124	CTRL	BOOT_SEL1#	MCU	MCU_PA26			
P125	CTRL	BOOT_SEL2#	MCU	MCU_PA25			
P126	CTRL	RESET_OUT#	MCU	MCU_PA24			
P127	CTRL	RESET_IN#	MCU	MCU_PA21			
P128	CTRL	POWER_BTN#	MCU+SoC	MCU_PA6			
P129	UART	SER0_TX	UART2_TXD		F48	NVCC_AON	
P130	UART	SER0_RX	UART2_RXD		E51	NVCC_AON	
P131	UART	SER0_RTS#	SAI1_TXD0		H48	NVCC_AON	
P132	UART	SER0_CTS#	SAI1_TXC		G51	NVCC_AON	
P133	UART	GND	_GND				
P134	UART	SER1_TX	UART1_TXD		E52	NVCC_AON	

Continued on next page

Table 9: X1 pin assignment – top side – Primary pins Secondary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
P135	UART	SER1_RX	UART1_RXD		E49	NVCC_AON	
P136	UART	SER2_TX	GPIO_IO04		K46	NVCC_GPIO	
P137	UART	SER2_RX	GPIO_IO05		L45	NVCC_GPIO	
P138	UART	SER2_RTS#	GPIO_IO07		L51	NVCC_GPIO	
P139	UART	SER2_CTS#	GPIO_IO34		W49	NVCC_GPIO	
P140	UART	SER3_TX	GPIO_IO14		N51	NVCC_GPIO	
P141	UART	SER3_RX	GPIO_IO14		P44	NVCC_GPIO	
P142	UART	GND	_GND				
P143	CAN	CAN0_TX	PDM_CLK		F46	NVCC_AON	
P144	CAN	CAN0_RX	PDM_BIT_STREAM0		G45	NVCC_AON	
P145	CAN	CAN1_TX	GPIO_IO25		T52	NVCC_GPIO	
P146	CAN	CAN1_RX	GPIO_IO27		U49	NVCC_GPIO	
P147	PWR	VDD_IN	_VCC				
P148	PWR	VDD_IN	_VCC				
P149	PWR	VDD_IN	_VCC				
P150	PWR	VDD_IN	_VCC				
P151	PWR	VDD_IN	_VCC				
P152	PWR	VDD_IN	_VCC				
P153	PWR	VDD_IN	_VCC				
P154	PWR	VDD_IN	_VCC				
P155	PWR	VDD_IN	_VCC				
P156	PWR	VDD_IN	_VCC				

Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
S1	CSI	CSI1_TX+ / I2C_CAM1_CK	GPIO_IO09		M46	NVCC_GPIO	
S2	CSI	CSI1_TX- / I2C_CAM1_DAT	GPIO_IO08		M44	NVCC_GPIO	
S3	CSI	GND	_GND				
S4	CSI	RSVD			Not Connected		
S5	CSI	CSI0_TX+ / I2C_CAM0_CK	GPIO_IO31		V48	NVCC_GPIO	
S6	CSI	CAM_MCK	CCM_CLKO1		AH20	NVCC_CCM_DAP	
S7	CSI	CSI0_TX- / I2C_CAM0_DAT	GPIO_IO30		V46	NVCC_GPIO	
S8	CSI	CSI0_CK+	MIPI_DSICSI1_CLK_P		B10	VDD_MIPI_1P8	
S9	CSI	CSI0_CK-	MIPI_DSICSI1_CLK_N		C11	VDD_MIPI_1P8	
S10	CSI	GND	_GND				
S11	CSI	CSI0_RX0+	MIPI_DSICSI1_D0_P		B14	VDD_MIPI_1P8	
S12	CSI	CSI0_RX0-	MIPI_DSICSI1_D0_N		C15	VDD_MIPI_1P8	
S13	CSI	GND	_GND				
S14	CSI	CSI0_RX1+	MIPI_DSICSI1_D1_P		B12	VDD_MIPI_1P8	
S15	CSI	CSI0_RX1-	MIPI_DSICSI1_D1_N		A13	VDD_MIPI_1P8	
S16	CSI	GND	_GND				
S17	Ethernet	GBE1_MDI0+	Ethernet PHY				
S18	Ethernet	GBE1_MDI0-	Ethernet PHY				
S19	Ethernet	GBE1_LINK100#	Ethernet PHY				3.3V IO
S20	Ethernet	GBE1_MDI1+	Ethernet PHY				
S21	Ethernet	GBE1_MDI1-	Ethernet PHY				
S22	Ethernet	GBE1_LINK1000#	Ethernet PHY				3.3V IO
S23	Ethernet	GBE1_MDI2+	Ethernet PHY				

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
S24	Ethernet	GBE1_MDI2-	Ethernet PHY				
S25	Ethernet	GND	_GND				
S26	Ethernet	GBE1_MDI3+	Ethernet PHY				
S27	Ethernet	GBE1_MDI3-	Ethernet PHY				
S28	Ethernet	GBE1_CTREF	Ethernet PHY				
S29	PCIe / ETH SERDES	PCIE_D_TX+ / SERDES_0_TX+	ETH_TX0_P		AJ17	VDD_ETH_0P8	
S30	PCIe / ETH SERDES	PCIE_D_TX- / SERDES_0_TX-	ETH_TX0_N		AK16	VDD_ETH_0P8	
S31	PCIe / ETH SERDES	GBE1_LINK_ACT#	Ethernet PHY				3.3V IO
S32	PCIe / ETH SERDES	PCIE_D_RX+ / SERDES_0_RX+	ETH_RX0_P		AJ13	VDD_ETH_0P8	
S33	PCIe / ETH SERDES	PCIE_D_RX- / SERDES_0_RX-	ETH_RX0_N		AK12	VDD_ETH_0P8	
S34	USB	GND	_GND				
S35	USB	USB4+	USB Hub				
S36	USB	USB4-	USB Hub				
S37	USB	USB3_VBUS_DET		USB1_VBUS			5V IO
S38	I2S	AUDIO_MCK	GPIO_IO17		P48	NVCC_GPIO	
S39	I2S	I2S0_LRCK	GPIO_IO26		U45	NVCC_GPIO	
S40	I2S	I2S0_SDOUT	GPIO_IO21		R51	NVCC_GPIO	
S41	I2S	I2S0_SDIN	GPIO_IO20		R49	NVCC_GPIO	
S42	I2S	I2S0_CK	GPIO_IO16		P46	NVCC_GPIO	
S43	SPI	ESPI_ALERT0#			Not Connected		
S44	SPI	ESPI_ALERT1#			Not Connected		
S45	ETH	MDIO_CLK	ENET1_MDC		AK40	NVCC_ENET	
S46	ETH	MDIO_DAT	ENET1_MDIO		AJ39	NVCC_ENET	

Continued on next page

Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
S47	I2C	GND	_GND				
S48	I2C	I2C_GP_CK	I2C2_SCL		E43	NVCC_AON	
S49	I2C	I2C_GP_DAT	I2C2_SDA		E45	NVCC_AON	
S50	HDA	HDA_SYNC / I2S2_LRCK	XSPI1_DATA5		AK50	NVCC_WAKEUP	
S51	HDA	HDA_SDO / I2S2_SDOUT	XSPI1_DATA4		AJ49	NVCC_WAKEUP	
S52	HDA	HDA_SDI / I2S2_SDIN	XSPI1_DATA7		AH50	NVCC_WAKEUP	
S53	HDA	HDA_CK / I2S2_CK	XSPI1_DATA6		AJ51	NVCC_WAKEUP	
S54	CTRL	SATA_ACT#			Not Connected		3.3V IO
S55	CTRL	USB5_EN_OC#			Not Connected		3.3V IO
S56	SPI	ESPI_IO_2 / QSPI_IO_2			Not Connected		
S57	SPI	ESPI_IO_3 / QSPI_IO_3			Not Connected		
S58	SPI	ESPI_RESET#			Not Connected		
S59	USB	USB5+			Not Connected		
S60	USB	USB5-			Not Connected		
S61	USB	GND	_GND				
S62	USB	USB3_SSTX+	USB Hub	USB1_TX1_P			
S63	USB	USB3_SSTX-	USB Hub	USB1_TX1_N			
S64	USB	GND	_GND				
S65	USB	USB3_SSRX+	USB Hub	USB1_RX1_P			
S66	USB	USB3_SSRX-	USB Hub	USB1_RX1_N			
S67	USB	GND	_GND				
S68	USB	USB3+	USB Hub				
S69	USB	USB3-	USB Hub				

Continued on next page

Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
S70	USB	GND	_GND				
S71	USB	USB2_SSTX+	USB Hub	USB1_TX0_P			
S72	USB	USB2_SSTX-	USB Hub	USB1_TX0_N			
S73	USB	GND	_GND				
S74	USB	USB2_SSRX+	USB Hub	USB1_RX0_P			
key							
key							
key							
S75	USB	USB2_SSRX-	USB Hub	USB1_RX0_N			
S76	PCIe	PCIE_B_RST#		IO_EXP33_P1			3.3V IO / Connected to IO Expander
S77	PCIe	PCIE_C_RST#/SERDES_RST#		IO_EXP33_P7			3.3V IO / Connected to IO Expander
S78	PCIe	PCIE_C_RX+ / SERDES_1_RX+			Not Connected		
S79	PCIe	PCIE_C_RX- / SERDES_1_RX-			Not Connected		
S80	PCIe	GND	_GND				
S81	PCIe	PCIE_C_TX+ / SERDES_1_TX+					
S82	PCIe	PCIE_C_TX- / SERDES_1_TX-			Not Connected		
S83	PCIe	GND	_GND		Not Connected		
S84	PCIe	PCIE_B_REFCK+	CLK Buffer				
S85	PCIe	PCIE_B_REFCK-	CLK Buffer				
S86	PCIe	GND	_GND				
S87	PCIe	PCIE_B_RX+	PCIE2_RX0_P		B34	VDD_PCI_1P8	
S88	PCIe	PCIE_B_RX-	PCIE2_RX0_N		C35	VDD_PCI_1P8	
S89	PCIe	GND	_GND				

Continued on next page

Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
S90	PCIe	PCIE_B_TX+	PCIE2_TX0_P		E31	VDD_PCI_1P8	
S91	PCIe	PCIE_B_TX-	PCIE2_TX0_N		F32	VDD_PCI_1P8	
S92	PCIe	GND	_GND				
S93	Display Port	DP0_LANE0+	DSI Bridge				
S94	Display Port	DP0_LANE0-	DSI Bridge				
S95	Display Port	DP0_AUX_SEL			Not Connected		
S96	Display Port	DP0_LANE1+	DSI Bridge				
S97	Display Port	DP0_LANE1-	DSI Bridge				
S98	Display Port	DP0_HPD	DSI Bridge				
S99	Display Port	DP0_LANE2+	DSI Bridge				
S100	Display Port	DP0_LANE2-	DSI Bridge				
S101	Display Port	GND	_GND				
S102	Display Port	DP0_LANE3+	DSI Bridge				
S103	Display Port	DP0_LANE3-	DSI Bridge				
S104	Display Port	USB3_OTG_ID			Not Connected		3.3V IO
S105	Display Port	DP0_AUX+	DSI Bridge				
S106	Display Port	DP0_AUX-	DSI Bridge				
S107	LVDS	LCD1_BKLT_EN		IO_EXP18_P0_5			Connected to IO Expander
S108	LVDS	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	MIPI_DSICSI1_CLK_P	D2	VDD_LVDS_1P8	
S109	LVDS	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	MIPI_DSICSI1_CLK_N	D4	VDD_LVDS_1P8	
S110	LVDS	GND	_GND				
S111	LVDS	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_D0_P	MIPI_DSICSI1_D0_P	B2	VDD_LVDS_1P8	
S112	LVDS	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_D0_N	MIPI_DSICSI1_D0_N	A3	VDD_LVDS_1P8	

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
S113	LVDS	eDP1_HPD / DSI1_TE			Not Connected		
S114	LVDS	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_D1_P	MIPI_DSICSI1_D1_P	C1	VDD_LVDS_1P8	
S115	LVDS	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_D1_N	MIPI_DSICSI1_D1_N	C3	VDD_LVDS_1P8	
S116	LVDS	LCD1_VDD_EN		IO_EXP18_P0_4			Connected to IO Expander
S117	LVDS	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_D2_P	MIPI_DSICSI1_D2_P	E1	VDD_LVDS_1P8	
S118	LVDS	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_D2_N	MIPI_DSICSI1_D2_N	E3	VDD_LVDS_1P8	
S119	LVDS	GND	_GND				
S120	LVDS	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_D3_P	MIPI_DSICSI1_D3_P	F2	VDD_LVDS_1P8	
S121	LVDS	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_D3_N	MIPI_DSICSI1_D3_N	F4	VDD_LVDS_1P8	
S122	LVDS	LCD1_BKLT_PWM	GPIO_IO13		N49	NVCC_GPIO	
S123	LVDS	GPIO13		GPIO_IO11	M52		
S124	LVDS	GND	_GND				
S125	LVDS	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_D0_P		G7	VDD_LVDS_1P8	
S126	LVDS	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_D0_N		G9	VDD_LVDS_1P8	
S127	LVDS	LCD0_BKLT_EN		IO_EXP18_P0_3			Connected to IO Expander
S128	LVDS	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_D1_P		F6	VDD_LVDS_1P8	
S129	LVDS	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_D1_N		F8	VDD_LVDS_1P8	
S130	LVDS	GND	_GND				
S131	LVDS	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_D2_P		D6	VDD_LVDS_1P8	
S132	LVDS	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_D2_N		E7	VDD_LVDS_1P8	
S133	LVDS	LCD0_VDD_EN		IO_EXP18_P0_2			Connected to IO Expander
S134	LVDS	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0_CLK_P		B4	VDD_LVDS_1P8	
S135	LVDS	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0_CLK_N		A5	VDD_LVDS_1P8	

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Table 10: X1 pin assignment – bottom side – Secondary pins Primary pins – Alternate functions (Continued)

MXM3 Pins	Signal Group	SMARC Signal	Soc Signal	SoC Multiplexed Pin	Soc Ball Name	Power Group	Note
S136	LVDS	GND	_GND				
S137	LVDS	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0_D3_P		D8	VDD_LVDS_1P8	
S138	LVDS	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0_D3_N		E9	VDD_LVDS_1P8	
S139	LVDS	I2C_LCD_CK	GPIO_IO23		T46	NVCC_GPIO	
S140	LVDS	I2C_LCD_DAT	GPIO_IO22		T44	NVCC_GPIO	
S141	CTRL	LCD0_BKLT_PWM	GPIO_IO12		N45	NVCC_GPIO	
S142	CTRL	GPIO12		GPIO_IO10	M48		
S143	CTRL	GND	_GND				
S144	CTRL	eDP0_HPD / DSI0_TE			Not Connected		
S145	CTRL	WDT_TIME_OUT#		MCU_PA17			
S146	CTRL	PCIE_WAKE#		IO_EXP33_P0			3.3V IO / Connected to IO Expander
S147	CTRL	VDD_RTC	_VCC_RTC				
S148	CTRL	LID#	MCU_PA22				
S149	CTRL	SLEEP#	MCU_PA1				
S150	CTRL	VIN_PWR_BAD#	MCU_PA0				5V IO
S151	CTRL	CHARGING#	MCU_PA20				
S152	CTRL	CHARGER_PRSNT#	MCU_PA19				
S153	CTRL	CARRIER_STBY#		MCU_PA2			
S154	CTRL	CARRIER_PWR_ON		MCU_PA16			
S155	CTRL	FORCE_RECOV#		MCU_PA15			
S156	CTRL	BATLOW#	MCU_PA23				
S157	CTRL	TEST#	MCU_PA18				
S158	CTRL	GND	_GND				

4 I/O Pins

4.1 Function Multiplexing

4.1.1 Alternate Functions

Table 11: X1 pin Alternate Functions Primary pins – Secondary pins

MXM3 Pin	SMARC Signal	Soc Signal	Soc Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
P5	GBE1_SDP	CCM_CLKO4	AJ21	ccmsrcgpcmix .CLKO4	netc .TMR_1588_PP2	can3.RX		flexio2.FLEXIO[29]	gpio4.IO[29]		
P6	GBE0_SDP	CCM_CLKO2	AF20	ccmsrcgpcmix .CLKO2	netc .TMR_1588_PP1			flexio1.FLEXIO[27]	gpio3.IO[27]		
P31	SPI0_CS1#	GPIO_IO24	T48	gpio2.IO[24]	usdhc3.DATA0			tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]
P34	SDIO_CMD	SD2_CMD	AB52	usdhc2.CMD	netc .TMR_1588_TRIG2	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]		
P35	SDIO_CD#	SD2_CD_B	AD48	usdhc2.CD_B	netc .TMR_1588_TRIG1	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]		
P36	SDIO_CK	SD2_CLK	AB48	usdhc2.CLK	netc .TMR_1588_PP1	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]		
P37	SDIO_PWR_EN	SD2_RESET_B	AD52	usdhc2 .RESET_B	lptmr2.ALT2		netc .TMR_1588_GCLK	flexio1.FLEXIO[7]	gpio3.IO[7]		
P39	SDIO_D0	SD2_DATA0	AC51	usdhc2 .DATA0	netc .TMR_1588_PP2	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]		
P40	SDIO_D1	SD2_DATA1	AC49	usdhc2 .DATA1	netc .TMR_1588_CLK	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]		
P41	SDIO_D2	SD2_DATA2	AA51	usdhc2 .DATA2	netc .TMR_1588_PP3	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]		
P42	SDIO_D3	SD2_DATA3	AA49	usdhc2 .DATA3	lptmr2.ALT1	mqs2.LEFT	netc .TMR_1588_ALARM1	flexio1.FLEXIO[6]	gpio3.IO[6]		
P43	SPI0_CS0#	GPIO_IO00	J49	gpio2.IO[0]	i2c3.SDA			spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]
P44	SPI0_CK	GPIO_IO03	K52	gpio2.IO[3]	i2c4.SCL			spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]
P45	SPI0_DIN	GPIO_IO01	J51	gpio2.IO[1]	i2c3.SCL			spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]
P46	SPI0_DO	GPIO_IO02	K48	gpio2.IO[2]	i2c4.SDA			spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]
P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	GPIO_IO18	P52	gpio2.IO[18]	sai3.RX_BCLK			spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]

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Table 11: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

MXM3 Pin	SMARC Signal	Soc Signal	Soc Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#		AH42	gpio5.IO[13]		uart6.RX		spi4.PCS1			
P56	ESPI_CK / SPI1_CK / QSPI_CK	GPIO_IO37	Y52	gpio5.IO[17]		uart7.RX		spi4.SCK			
P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	GPIO_IO19	R45	gpio2.IO[19]	sai3.RX_SYNC	pdm .BIT_STREAM[3]	flexio1.FLEXIO[19]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]
P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	GPIO_IO36	Y48	gpio5.IO[16]		uart7.TX		spi4.SOUT			
P77	PCIE_B_CKREQ#	GPIO_IO35	W51	gpio5.IO[15]	pcie2.CLKREQ_B	uart6.RTS_B		spi4.SIN			
P78	PCIE_A_CKREQ#	GPIO_IO32	V52	gpio5.IO[12]	pcie1.CLKREQ_B	uart6.TX		spi4.PCS2			
P105	HDMI_CTRL_CK / DP1_AUX+	Not Connected		gpio2.IO[31]	i2c4.SCL	can5.RX					flexio1.FLEXIO[31]
P106	HDMI_CTRL_DAT / DP1_AUX-	Not Connected		gpio2.IO[30]	i2c4.SDA	can5.TX					flexio1.FLEXIO[30]
P113	GPIO5 / PWM_OUT	GPIO_IO06	L49	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]		spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]
P121	I2C_PM_CK	GPIO_IO29	V44	gpio2.IO[29]	i2c3.SCL	can3.RX					flexio1.FLEXIO[29]
P122	I2C_PM_DAT	GPIO_IO28	U51	gpio2.IO[28]	i2c3.SDA	can3.TX					flexio1.FLEXIO[28]
P129	SER0_TX	UART2_TXD	E48	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7] / ccmsrcgpcmix .BOOT_MODE[1]		
P130	SER0_RX	UART2_RXD	E51	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]		
P131	SER0_RTS#	SAI1_TXD0	H48	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ ccmsrcgpcmix .BOOT_MODE[3]		
P132	SER0_CTS#	SAI1_TXC	G51	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]		

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Table 11: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

MXM3 Pin	SMARC Signal	Soc Signal	Soc Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
P134	SER1_TX	UART1_TXD	F52	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1	vpu.UART_TX	gpio1.IO[5]/ ccmsrcgpcmix .BOOT_MODE[0]		
P135	SER1_RX	UART1_RXD	E49	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0	vpu.UART_RX	gpio1.IO[4]		
P136	SER2_TX	GPIO_IO04	K46	gpio2.IO[4]	tpm3.CH0	pdm.CLK	can4.TX	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]
P137	SER2_RX	GPIO_IO05	L45	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	can4.RX	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]
P138	SER2_RTS#	GPIO_IO07	L51	gpio2.IO[7]	spi3.PCS1			spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]
P139	SER2_CTS#	GPIO_IO34	W49	gpio5.IO[14]		uart6.CTS_B		spi4.PCS0			
P140	SER3_TX	GPIO_IO14	N51	gpio2.IO[14]	uart3.TX			spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]
P141	SER3_RX	GPIO_IO15	P44	gpio2.IO[15]	uart3.RX			spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]
P143	CAN0_TX	PDM_CLK	F46	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX	
P144	CAN0_RX	PDM_BIT_STREAM0	G45	pdm .BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX	
P145	CAN1_TX	GPIO_IO25	T52	gpio2.IO[25]	usdhc3.DATA1	can2.TX		tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]
P146	CAN1_RX	GPIO_IO27	U49	gpio2.IO[27]	usdhc3.DATA3	can2.RX		tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]
S2	CSI1_TX- / I2C_CAM1_DAT	GPIO_IO08	M44	gpio2.IO[8]	spi3.PCS0			tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]
S5	CSI0_TX+ / I2C_CAM0_CK	GPIO_IO31		gpio2.IO[31]	i2c4.SCL	can5.RX					flexio1.FLEXIO[31]
S6	CAM_MCK	CCM_CLKO1	AH20	ccmsrcgpcmix .CLKO1	netc TMR_1588_TRIG1			flexio1.FLEXIO[26]	gpio3.IO[26]		
S7	CSI0_TX- / I2C_CAM0_DAT	GPIO_IO30		gpio2.IO[30]	i2c4.SDA	can5.TX					flexio1.FLEXIO[30]
S38	AUDIO_MCK	GPIO_IO17	P48	gpio2.IO[17]	sai3.MCLK			uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]
S39	I2S0_LRCK	GPIO_IO26	U45	gpio2.IO[26]	usdhc3.DATA2	pdm .BIT_STREAM[1]	flexio1.FLEXIO[26]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC
S40	I2S0_SDOUT	GPIO_IO21	R51	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	flexio1.FLEXIO[21]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK

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Table 11: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

MXM3 Pin	SMARC Signal	Soc Signal	Soc Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
S41	I2S0_SDIN	GPIO_IO20	R49	gpio2.IO[20]	sai3.RX_DATA[0]	pdm .BIT_STREAM[0]		spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]
S42	I2S0_CK	GPIO_IO16	P46	gpio2.IO[16]	sai3.TX_BCLK	pdm .BIT_STREAM[2]		uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]
S45	MDIO_CLK	ENET1_MDC		netc.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]		
S46	MDIO_DAT	ENET1_MDIO		netc.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]		
S48	I2C_GP_CK	I2C2_SCL	E43	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B	
S49	I2C_GP_DAT	I2C2_SDA	E45	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]		
S50	HDA_SYNC / I2S2_LRCK	XSPI1_DATA5	AK50	flexspi .A_DATA[5]	sai5.TX_SYNC	sai5 .RX_DATA[2]	sai2.RX_DATA[6]	xspi_slv.DATA[5]	gpio5.IO[5]		
S51	HDA_SDO / I2S2_SDOUT	XSPI1_DATA4	AJ49	flexspi .A_DATA[4]	sai5.TX_DATA[0]	sai5 .RX_DATA[1]		xspi_slv.DATA[4]	gpio5.IO[4]		
S52	HDA_SDI / I2S2_SDIN	XSPI1_DATA7	AH50	flexspi .A_DATA[7]	sai5.RX_DATA[0]	sai5 .TX_DATA[1]		xspi_slv.DATA[7]	gpio5.IO[7]		
S53	HDA_CK / I2S2_CK	XSPI1_DATA6	AJ51	flexspi .A_DATA[6]	sai5.TX_BCLK	sai5 .RX_DATA[3]	sai2.RX_DATA[7]	xspi_slv.DATA[6]	gpio5.IO[6]		
S56	ESPI_IO_2 / QSPI_IO_2	Not Connected		flexspi .A_DATA[2]	sai2.TX_DATA[6]	sai4.TX_DATA[0]		xspi_slv.DATA[2]	gpio5.IO[2]		
S57	ESPI_IO_3 / QSPI_IO_3	Not Connected	N49	flexspi .A_DATA[3]	sai2.TX_DATA[7]	sai4.RX_DATA[0]		xspi_slv.DATA[3]	gpio5.IO[3]		
S122	LCD1_BKLT_PWM	GPIO_IO13	M52	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]		spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]
S139	I2C_LCD_CK	GPIO_IO23	T46	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	can5.RX	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]
S140	I2C_LCD_DAT	GPIO_IO22	T44	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	can5.TX	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]
S141	LCD0_BKLT_PWM	GPIO_IO12	N45	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	flexio1.FLEXIO[12]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
S148	LID#	MCU_PA22	M48	A4 / GPAMP_OUT / OPA0_OUT	UART0_RX	TIMG2_C1	UART0_RTS	CLK_OUT	UART1_RX	Default BSL UART_RX	
S149	SLEEP#	MCU_PA1			UART1_RX	I2C0_SCL	TIMG1_C1			Default BSL I2C_SCL	

Continued on next page

Table 11: X1 pin Alternate Functions Primary pins – Secondary pins (Continued)

MXM3 Pin	SMARC Signal	Soc Signal	Soc Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
S150	VIN_PWR_BAD#	MCU_PA0			UART1_TX	I2C0_SDA	TIMG1_C0	SPI0_CS1		Default BSL I2C_SDA	
S151	CHARGING#	MCU_PA20		A6 / COMP0_IN1+	SWCLK	I2C1_SCL	TIMG4_C0				
S152	CHARGER_PRSNT#	MCU_PA19			SWDIO	I2C1_SDA	SPI0_POCI				
S153	CARRIER_STBY#			ROSC	TIMG1_C1	SPI0_CS0					
S156	BATLOW#	MCU_PA23		VREF+ / COMP0_IN1-	UART0_TX	SPI0_CS3	TIMG0_C0	UART0_CTS	UART1_TX	Default BSL UART_TX	
S157	TEST#	MCU_PA18		A7 / OPA1_IN0+ / GPAMP_IN-	UART0_RX	SPI0_PICO	I2C1_SDA	TIMG4_C1		BSL Invoke	
S158	GND	_GND									

4.1.2 Alternate Functions for Multiplexed Pins

Table 12: X1 pin Alternate Functions for Multiplexed Pins Primary pins – Secondary pins

MXM3 Pin	SMARC Signal	i.MX95 Multiplexed Pin	Soc Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
P1	SMB_ALERT#	CCM_CLKO3	AK20	ccmsrcgpcmix.CLKO3	netc.TMR_1588_TRIG2	can3.TX		flexio2.FLEXIO[28]	gpio4.IO[28]		
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	XSPI1_SS1_B	P56	flexspi.A_SS1_B	sai5.RX_BCLK	sai5.TX_DATA[3]	sai2.RX_DATA[7]		gpio5.IO[11]		
P110	GPIO2 / CAM0_RST#	XSPI1_DATA0	AJ45	flexspi.A_DATA[0]	sai2.TX_DATA[4]	sai4.TX_BCLK	sai4.RX_DATA[1]	xspi_slv.DATA[0]	gpio5.IO[0]		
P111	GPIO3 / CAM1_RST#	XSPI1_DATA1	AH46	flexspi.A_DATA[1]	sai2.TX_DATA[5]	sai4.TX_SYNC	sai4.TX_DATA[1]	xspi_slv.DATA[1]	gpio5.IO[1]		
P112	GPIO4 / HDA_RST#	XSPI1_DATA2	AJ47	flexspi.A_DATA[2]	sai2.TX_DATA[6]	sai4.TX_DATA[0]		xspi_slv.DATA[2]	gpio5.IO[2]		
P114	GPIO6 / TACHIN	XSPI1_DATA3	AK48	flexspi.A_DATA[3]	sai2.TX_DATA[7]	sai4.RX_DATA[0]		xspi_slv.DATA[3]	gpio5.IO[3]		
P115	GPIO7	XSPI1_SCLK	AJ43	flexspi.A_SCLK	sai2.RX_DATA[4]	sai4.RX_SYNC	earc.hpd	xspi_slv.CLK	gpio5.IO[9]		
P116	GPIO8	XSPI1_SS0_B	AJ41	flexspi.A_SS0_B	sai2.RX_DATA[5]	sai4.RX_BCLK	earc.cec	xspi_slv.CS	gpio5.IO[10]		
P117	GPIO9	XSPI1_DQS	AK44	flexspi.A_DQS	sai5.RX_SYNC	sai5.TX_DATA[2]	sai2.RX_DATA[6]	xspi_slv.DQS	gpio5.IO[8]		
P118	GPIO10	ENET2_MDIO	AJ31	netc.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]		
P119	GPIO11	ENET2_MDC	AK32	netc.MDC	uart4.DCB_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]		
P123	BOOT_SEL0#	MCU_PA27		A0 / COMP0_IN0-	TIMG1_C1	SPI0_CS3					
P124	BOOT_SEL1#	MCU_PA26		A1 / GPAMP_IN+ / COMP0_IN0+	TIMG1_C0	UART0_RX	SPI0_POCI				
P125	BOOT_SEL2#	MCU_PA25		A2 / OPA0_IN0+	TIMG4_C1	UART0_TX	SPI0_PICO				
P126	RESET_OUT#	MCU_PA24		A3 / OPA0_IN1- / OPA0_IN0-	SPI0_CS2	TIMG0_C1	UART0_RTS				
P127	RESET_IN#	MCU_PA21		A5 / VREF-	TIMG2_C0	UART0_CTS	UART0_TX				
P128	POWER_BTN#	MCU_PA6			TIMG0_C1	SPI0_SCK					
S58	ESPI_RESET#		Not Connected	flexspi.A_DQS	sai5.RX_SYNC	sai5.TX_DATA[2]	sai2.RX_DATA[6]	xspi_slv.DQS	gpio5.IO[8]		

Continued on next page

Table 12: X1 pin Alternate Functions for Multiplexed Pins Primary pins – Secondary pins (Continued)

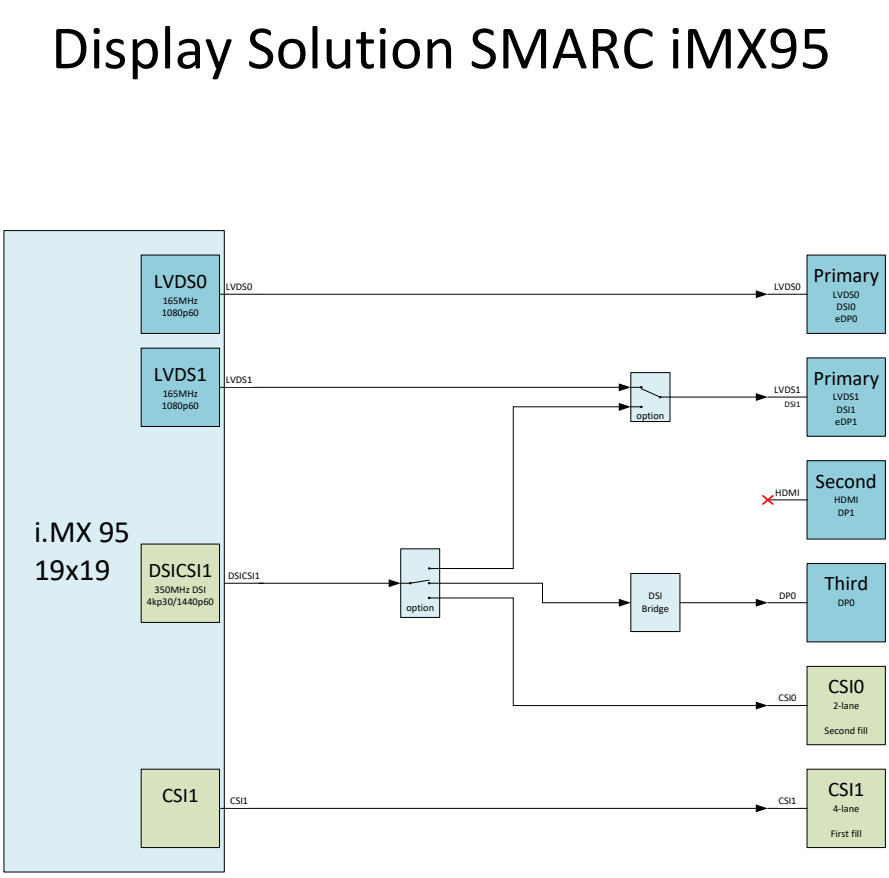
MXM3 Pin	SMARC Signal	i.MX95 Multiplexed Pin	Soc Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
S123	GPIO13	GPIO_IO11	M52	gpio2.IO[11]	spi3.SCK			tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]
S142	GPIO12	GPIO_IO10	M48	gpio2.IO[10]	spi3.SOUT			tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]
S145	WDT_TIME_OUT#	MCU_PA17		OPA1_IN1-	UART0_TX	I2C1_SCL	SPI0_SCK	TIMG4_C0	SPI0_CS1		
S153	CARRIER_STBY#	MCU_PA2		ROSC	TIMG1_C1	SPI0_CS0					
S154	CARRIER_PWR_ON	MCU_PA16		A8 / OPA1_OUT	COMP0_OUT	I2C1_SDA	SPI0_POCI	TIMG0_C0	FCC_IN		
S155	FORCE_RECOV#	MCU_PA15		A9	UART1_RTS	I2C1_SCL	SPI0_CS2	TIMG4_C1			

5 Interface Description

5.1 Display

The SMARC i.MX95 has two display interfaces with LVDS and MIPI DSI, able to support up to 4K displays. The following Figure show the block diagram for the Display solution. The 'option' boxes represent the assembly options available.

Figure 2: Display Solution Block Diagram



5.2 GPIOs

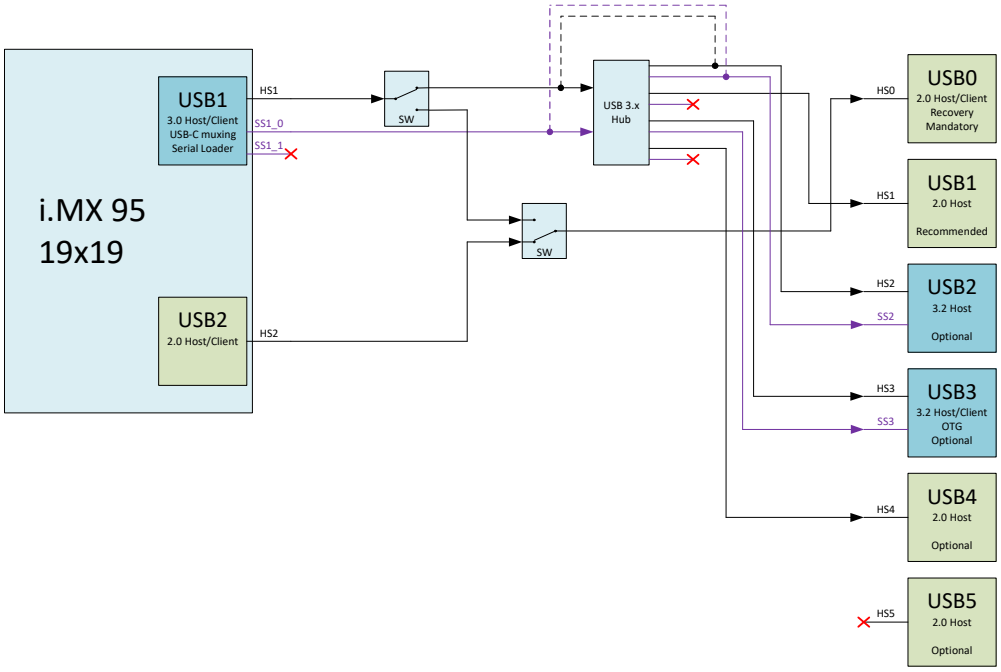
As described in Table 6, the SMARC i.MX95 implements 14 dedicated general-purpose input-output (GPIO). Besides these 14 GPIOs, several pins can be used as GPIO if their primary function is not used. For compatibility reasons, it is recommended to use the dedicated GPIOs first. The GPIOs were implemented following the SMARC specification document (Section 1.7.3).

Table 13: Dedicated GPIOs

MXM3 Pin	SMARC Signal	SoC Signal	Non SoC Ball Name	SoC Ball Name	SoC Alternate Function	Alternate Function Name
P108	GPIO0 / CAM0_PWR#		GPIO_Expander P0_0			
P109	GPIO1 / CAM1_PWR#		GPIO_Expander P0_1			
P110	GPIO2 / CAM0_RST#	XSPI1_DATA0		AJ45	ALT5	gpio5.IO[0]
P111	GPIO3 / CAM1_RST#	XSPI1_DATA1		AH46	ALT5	gpio5.IO[1]
P112	GPIO4 / HDA_RST#	XSPI1_DATA2		AJ47	ALT5	gpio5.IO[2]
P113	GPIO5 / PWM_OUT	GPIO_IO6		L49	ALT0	gpio2.IO[6]
P114	GPIO6 / TACHIN	XSPI1_DATA3		AK48	ALT5	gpio5.IO[3]
P115	GPIO7	XSPI1_CLK		AJ43	ALT5	gpio5.IO[9]
P116	GPIO8	XSPI1_SS0_B		AJ41	ALT5	gpio5.IO[10]
P117	GPIO9	XSPI1_DQS		AK44	ALT5	gpio5.IO[8]
P118	GPIO10	ENET2_MDIO		AJ31	ALT5	gpio5.IO[15]
P119	GPIO11	ENET2_MDC		AK32	ALT5	gpio5.IO[14]
S123	GPIO13	GPIO_IO11		M52	ALT0	gpio2.IO[11]
S142	GPIO12	GPIO_IO10		M48	ALT0	gpio2.IO[10]

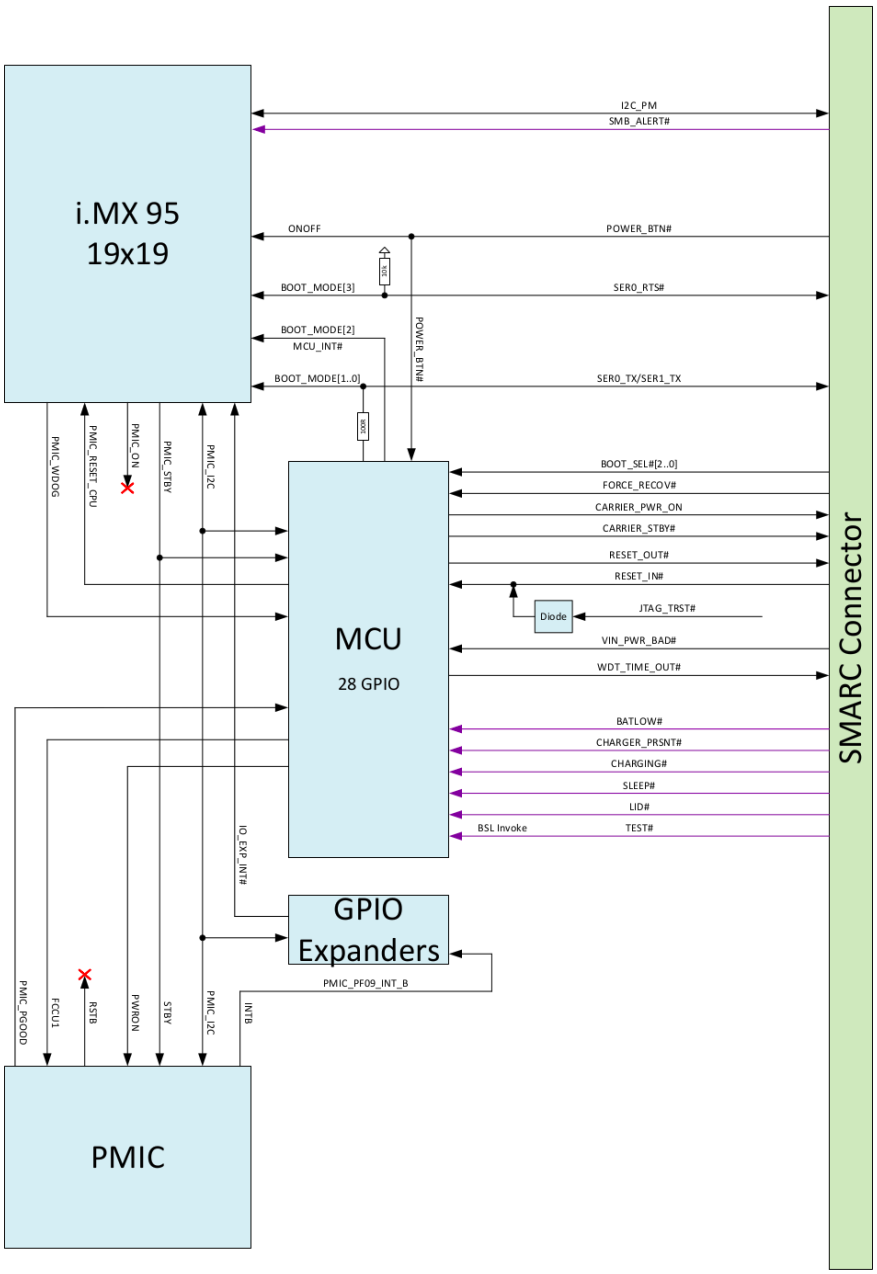
5.3 USB

Figure 3: USB Solution Block Diagram



5.4 Power Management Signals

Figure 4: Power Management Solution Block Diagram



5.5 Wi-Fi and Bluetooth

"WB" indicates Wi-Fi/Bluetooth.
The addition of "WB" in the product name indicates that a version features Wi-Fi and Bluetooth.

The SMARC i.MX95 is available with optional on-module Wi-Fi and Bluetooth interfaces. These module versions make use of the u-blox MAYA-W260-00B Host-based multiradio module based on the NXP IW611 chip, up to 480 Mbit/s throughput (600Mbit/s maximum data rate)

The Wi-Fi/BT module features:

- Wi-Fi 6 802.11 dual-band
- Bluetooth classic and full-featured Bluetooth Low Energy 5.4, includeing LE Audio
- Support for long range Bluetooth Low Energy
- Wi-Fi direct
- Two separate U.FL connectors for Wi-Fi and Bluetooth

The Wi-Fi/BT module requires external antennas.
The u-blox MAYA-260-00B needs two U.FL external antennas for Wi-Fi and Bluetooth.
The MHF-4 antennas used by some modules are not compatible with the U.FL connectors.

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. More information can be found on our developer website[1].

5.6 Recovery Mode

Missing Content
More information about the recovery mode will be available on the next release of the datasheet.

5.7 Known Issues

Up-to-date information about all known hardware issues can be found in the errata document, which can be downloaded from Toradex Developer Website.

https://developer.toradex.com/hardware/smarc-som-family/modules/smarc-imx95#erratakown-issues.

[1] https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products

6 Technical Specifications

6.1 Absolute Maximum Ratings

Missing Content
More information about the absolute maximum ranges will be available on the next release of the datasheet.

6.2 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at: https://www.toradex.com/support/product-compliance.

6.3 Power Consumption

Missing Content
More information about power consumption will be available on the next release of the datasheet.

6.4 Recommended Operation Conditions

Missing Content
More information about power consumption will be available on the next release of the datasheet.

6.5 Mechanical Characteristics

The SMARC modules are available in the 82 x 50 mm size, as described on the Section 1.6. Check the “Module Outline - 82×50mm Module” section of the SMARC specification Section 1.7.3 on page 12.

6.5.1 Sockets for SMARC Modules

The SMARC i.MX95 modules use the MXM3 graphics cards edge connector with 314 pins. Check the “Carrier Connector” section of the SMARC specification Section 1.7.3.

6.5.2 Thermal Specification

Missing Content
More information about the thermal specification will be available on the next release of the datasheet.

7 Device and Documentation Support

7.1 Trademarks

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