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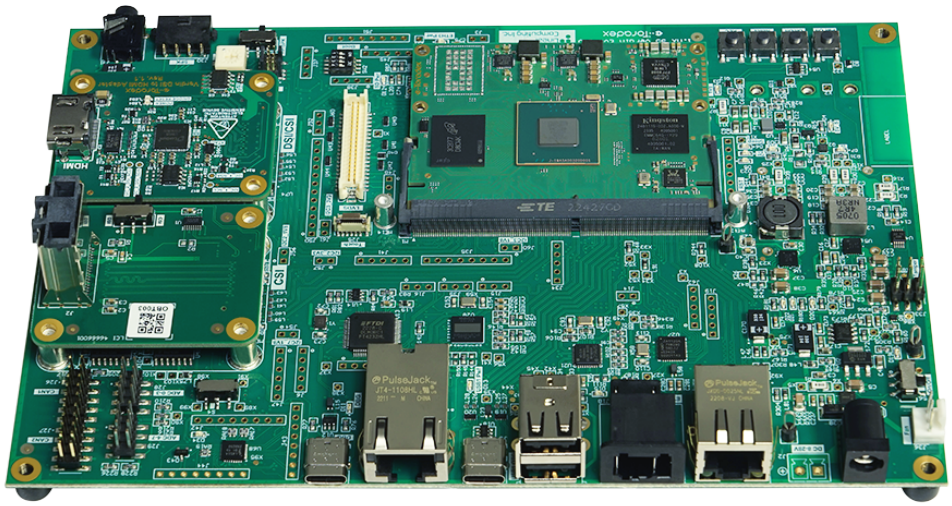
NXP i.MX 95 Verdin EVK

HW Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
14-Mar-2024	Rev. 0.1	V1.0	Initial documentation
08-May-2024	Rev. 0.2	V1.0	Section 1.1: Add Purpose of the Datahseet section. Section 1.2: Add SoC description section. Section 1.3: Add EVK description section. Section 1.4: Add main features section. Section 1.5: Add reference documents section. Section 2: Rename and reorder subsections. Section 2: Add description and pin tables to subsections. Section 4.1: Add Product Compliance section. Section 4.2: Add Sockets for Verdin modules section. Minor changes.

Contents

1 Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the i.MX 95 Verdin EVK. For information on the actual features supported by software, please refer to the i.MX 95 Verdin EVK product page[1] on the Toradex Developer website.

1.2 NXP i.MX 95 SoC

The i.MX 95 Verdin Evaluation Kit is based on the NXP i.MX 95 SoC, featuring a rich set of high-speed interfaces with Ethernet Port up to 10 Gbps, and offering a high-performance computer with 6 Arm Cortex-A55. It also provides an expansive machine vision capability, advanced security, and support for several types of displays and multimedia.

1.3 i.MX 95 Verdin EVK

i.MX 95 Verdin Evaluation Kit provides a product for the next generation of Edge AI, Automotive, Industrial and Medical Applications.

CAE data for the board, including schematics and layout will be available on NXP i.MX 95 Early Access Sharepoint.

To ensure optimal compatibility and user experience, the i.MX 95 Verdin Evaluation Kit comes with one Verdin DSI to HDMI Adapter[2]. This adapter uses a MIPI DSI interface to provide an HDMI output that seamlessly integrates with all Verdin System on Modules, guaranteeing an enhanced and comprehensive user experience.

To ensure the best accessory eco-system compatibility and an easy out-of-the-box user experience, the i.MX 95 Verdin Evaluation Kit includes:

Table 1: i.MX 95 EVK contents

Qty.	Item	Description	Reference
1	Power adapter	12V/30W AC/DC power supply (Barrel plug, 2.1mm I.D. and 5.5mm O.D.)	Section 2.14.6
1	Heatsink	Verdin industrial heatsink	
1	DSI to HDMI adapter	Verdin DSI to HDMI adapter providing out-of-the-box support for HDMI displays	Section 2.6.1
1	DSI/CSI to mini SAS adapter	Verdin DSI/CSI to mini SAS adapter allowing easy integration with NXP accessory ecosystem	
1	Wi-Fi/Bluetooth module	u-blox Maya-W2 Wi-Fi 6 module with M.2 (Key E) connector	Section 2.18.1
2	Wi-Fi/Bluetooth antennas	Antennas for the Maya-W2 Wi-Fi/Bluetooth module	Section 2.18.1

1.4 Main Features

1.4.1 CPU

[1] https://www.toradex.com/computer-on-modules/verdin-arm-family/nxp-imx95-evaluation-kit
[2] https://developer.toradex.com/hardware/verdin-som-family/add-ons/verdin-dsi-to-hdmi-adapter/

Table 2: CPU Features

Parameter	i.MX 95 Verdin Evaluation Kit
General	
SoC	i.MX 95 *MIMX9596C VYXNAC*
Crypto	Yes
eFuse key storage	Yes
Secute boot	Yes
Secure clock	Yes
Tamper detection	Yes
Cortex A55 – Main CPU	
A55 Cores	6
A55 Clock	1.8GHz
L1 Instruction Cache *per core*	32kB
L1 Data Cache *per core*	32kB
L2 Cache *per core*	64kB
L3 Cache *shared*	512kB
Neon SIMD	Yes
Cortex M7 – Real-time MCU	
M7 Cores	1
M7 Clock	400MHz
Tightly Coupled Memory	512kB *with ECC*
Cortex M33 – Low power/Safety MCU	
M33 Cores	1
M33 Clock	333MHz
OCRAM	256kB *with ECC*

1.4.2 Memory

Table 3: Memory

Parameter	i.MX 95 Verdin Evaluation Kit
eMMC	
eMMC Capacity	64GB
I²C EEPROM	
I²C EEPROM Capacity	2kbit 256 × 8bits
I²C EEPROM Bus Speed	Fast: 400kHz Std.: 100kHz

Continued on next page

Table 3: Memory (Continued)

Parameter	i.MX 95 Verdin Evaluation Kit
RAM	
RAM Capacity	128GB
RAM Type	LPDDR5
RAM Speed	6400MT/s
Inline ECC	Yes

[1] Controllers × channels per controller × bits per channel.

1.4.3 Physical

Table 4: Physical Features

Parameter	i.MX 95 Verdin Evaluation Kit
EVK dimensions	200 × 136 × 18 mm
Temperature range	–25 °C to + 85 °C

1.5 Reference Documents

1.5.1 1 Gigabit Automotive Ethernet Transceiver datasheet

https://www.nxp.com/docs/en/fact-sheet/TJA1120FS.pdf

1.5.2 Audio Codec datasheet

https://www.mouser.com/datasheet/2/76/WM8904_v3.5-1075382.pdf

1.5.3 CAN Transceiver datasheet

https://www.nxp.com/docs/en/data-sheet/TJA1463.pdf

1.5.4 EEPROM datasheet

M24:

https://www.st.com/resource/en/datasheet/m24c01-w.pdf

NV24:

https://www.onsemi.com/pdf/datasheet/nv24c64lv-d.pdf

1.5.5 GPIO Expander datasheet

https://www.nxp.com/docs/en/data-sheet/PCAL6408A.pdf

1.5.6 Power Monitor datasheet

https://www.ti.com/lit/ds/symlink/ina226.pdf

1.5.7 RTC Module datasheet

https://www.mouser.com/datasheet/2/137/RX8130CE_en-1825324.pdf

1.5.8 Temperature sensor datasheet

https://www.nxp.com/docs/en/data-sheet/PCT2075.pdf

1.5.9 USB HUB datasheet

https://ww1.microchip.com/downloads/en/devicedoc/00001692c.pdf

1.5.10 USB-C Logic Detector datasheet

https://www.nxp.com/docs/en/data-sheet/PTN5110.pdf

1.5.11 USB-UART FTDI datasheet

https://ftdichip.com/wp-content/uploads/2020/08/DS_FT4232H.pdf

1.5.12 Verdin DSI to HDMI Adapter

https://developer.toradex.com/hardware/verdin-som-family/add-ons/verdin-dsi-to-hdmi-adapter/

1.5.13 Wi-Fi/Bluetooth Module MAYA-W2

https://www.u-blox.com/en/product/m2-maya-w2-card

1.6 Naming Conventions

Table 5: Naming conventions

Name	Description
i.MX 9 Series	An i.MX 9 series of applications processors that bring together higher performance applications cores. It's composed by i.MX 91, i.MX 93 and i.MX 95 SoCs. For information on the i.MX 9-based chips, please visit the NXP website.
i.MX 95	An i.MX 95 applications processor family. Whenever this document uses the term i.MX 95, all versions of the i.MX 95 SoC family are meant.
i.MX 95 Verdin EVK	Refers to the i.MX 95 Verdin Evaluation Kit.

1.7 Abbreviations

Table 6: Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display

Continued on next page

Table 6: Abbreviations (Continued)

Abbreviation	Explanation
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes

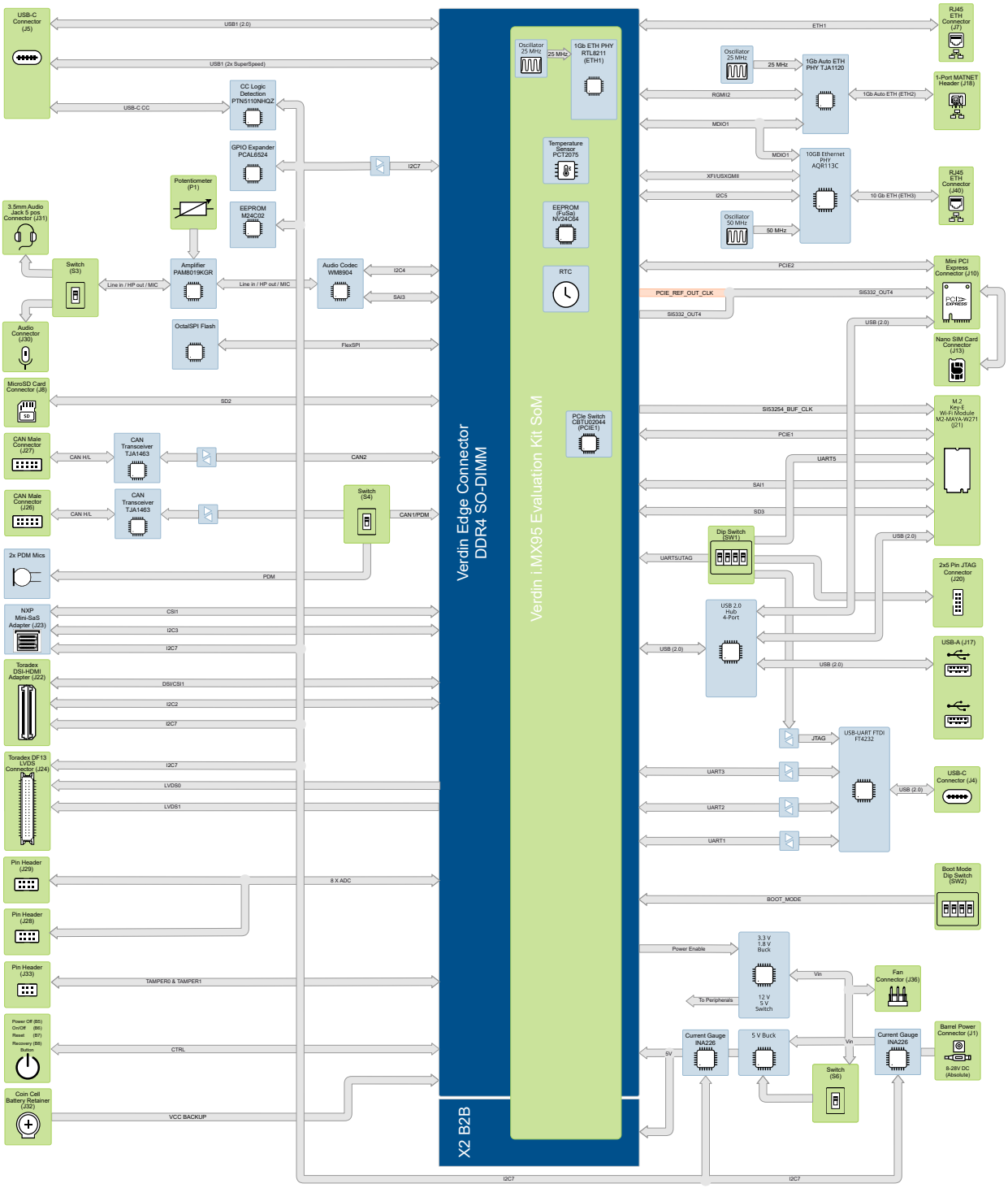
Continued on next page

Table 6: Abbreviations (Continued)

Abbreviation	Explanation
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.8 Architecture Block Diagram

Figure 1: i.MX 95 Verdin Evaluation Kit Hardware Architecture



1.9 Physical Drawings

1.9.1 Top Side Connectors

Figure 2: i.MX 95 Verdin Evaluation Kit top side connectors

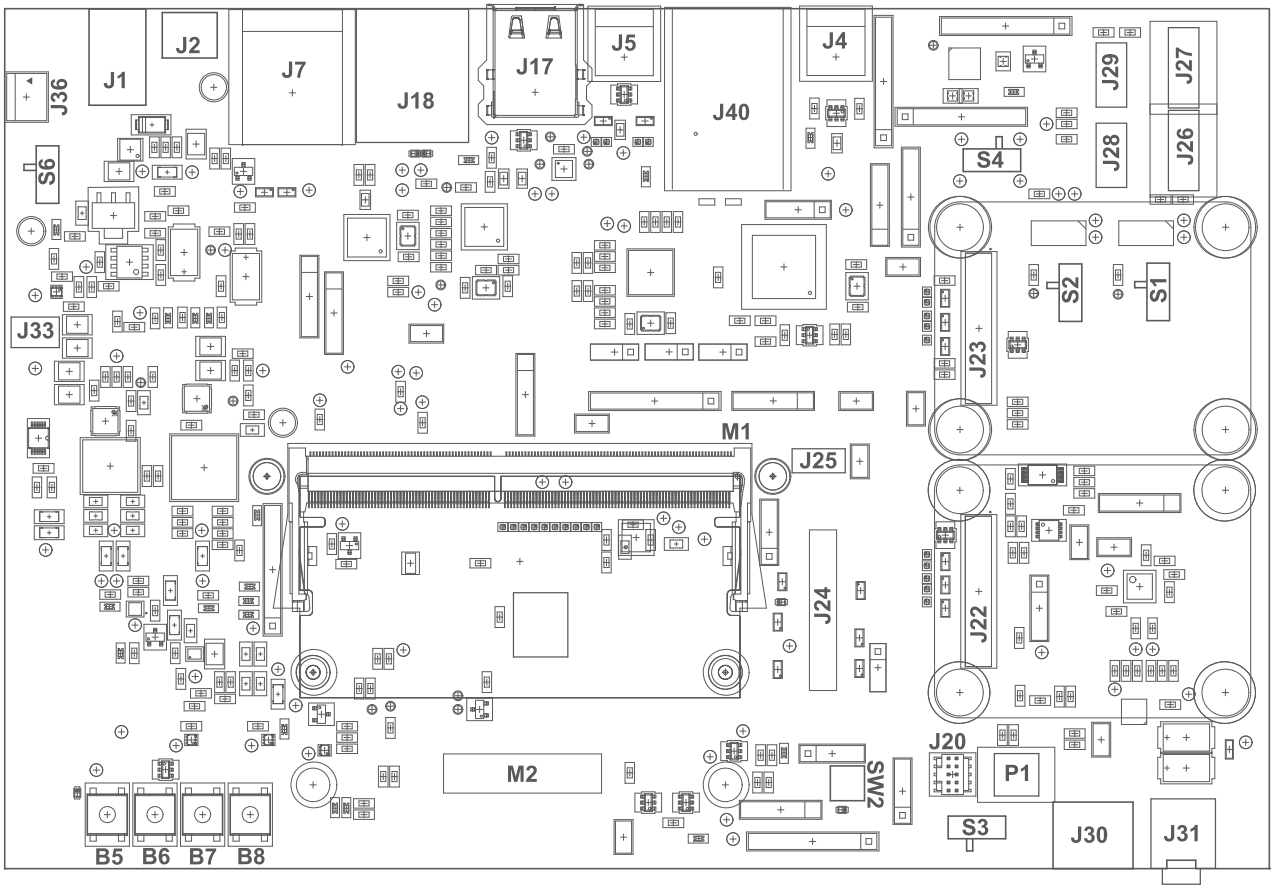


Table 7: Top Side Connectors

Identifier	Function	Description	Reference
M1, M2	Verdin SoM Connector		
J1	Power	Input power connection	Section 2.14.6
J2	Power	Not assembled	
J4	USB-C Debug Connection	For debug console	Section 2.17.1
J5	USB-C OTG	For UUU Boot mode	Section 2.17.2
J7	ETH1	1 Gbit Ethernet connection	Section 2.7.1
J17	2x USB 2.0 Host Connector	Upper: USBA1 Lower: USBA2	Section 2.17.3
J18	ETH2	1000 Base-T1 Ethernet connection	Section 2.7.2
J20	JTAG		Section 2.11
J22	MIPI DSI/CSI		Section 2.6.1
J23	MIPI CSI		Section 2.4.1

Continued on next page

Table 7: Top Side Connectors (Continued)

Identifier	Function	Description	Reference
J24	LVDS		Section 2.6.2
J25	Capacitive Touch Connector		Section 2.6.3
J26	CAN1	CAN1 pin header	Section 2.5.1
J27	CAN2	CAN2 pin header	Section 2.5.3
J28	ADC 0-3	ADC pin header	Section 2.1
J29	ADC 4-7	ADC pin header	Section 2.1
J30	Speaker		Section 2.2.1
J31	Audio Jack		Section 2.2.2
J33	Tamper		Section 2.16
J36	Fan		Section 2.8
J40	ETH3	10 Gbit Ethernet connection	Section 2.7.3
J42	IO Expander		Section 2.10.1
J43	IO Expander		Section 2.10.2
J44	IO Expander		Section 2.10.3

1.9.2 Bottom Side Connectors

Figure 3: i.MX 95 Verdin Evaluation Kit bottom side connectors

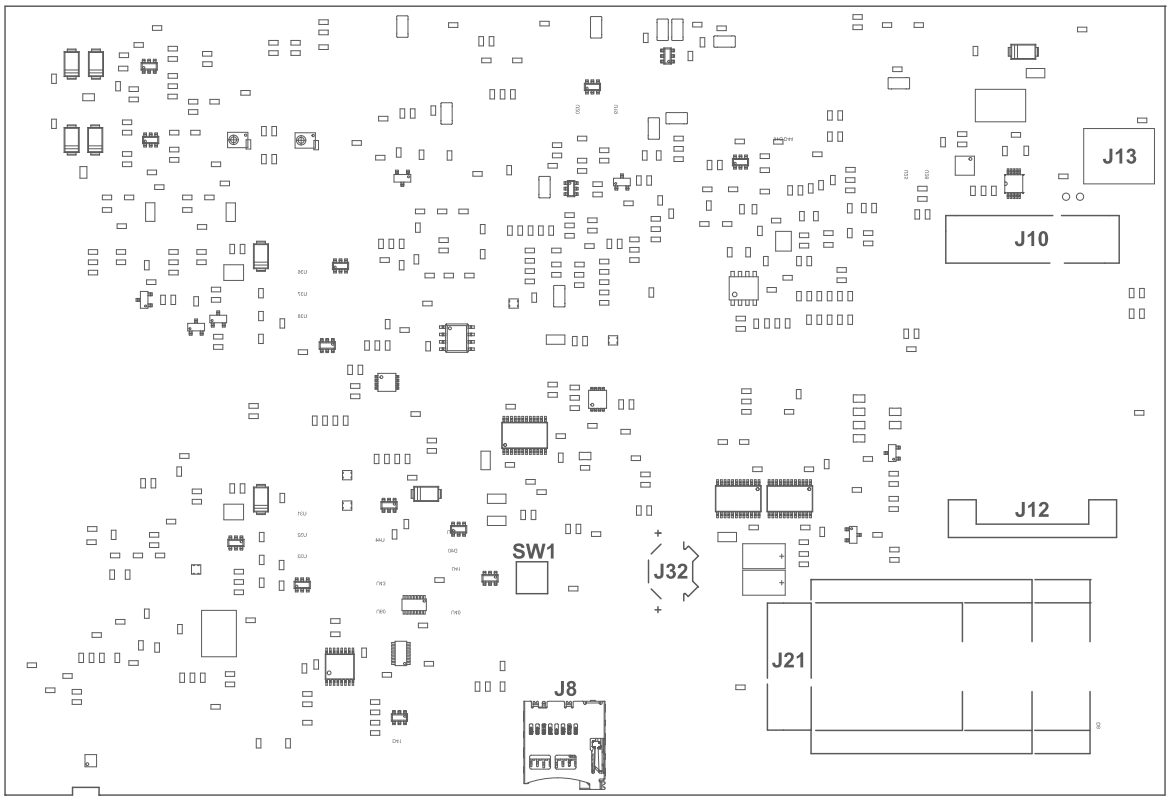


Table 8: Bottom Side Connectors

Identifier	Function	Description	Reference
J8	Micro SD		Section 2.15
J10, J12	Mini PCIe		Section 2.12
J13	Nano SIM		Section 2.12
J21	M2 Key E		Section 2.18.1
J32	Battery Holder		Section 2.14.7

2 Interface Description

2.1 ADC – Analog to Digital Converter (J28 and J29)

The i.MX 95 EVK comes with two ADC connectors, J28 and J29, which are pre-assembled. The even pins connect to the ADC in the i.MX 95 SoC, while the odd pins provide reference voltages.

The analog signals are filtered by a 1.3MHz RC low pass filter, then routed to the SoC through the M1 conector. Negative voltages are shorted to ground.

Figure 4: ADC Connector (J28 and J29)

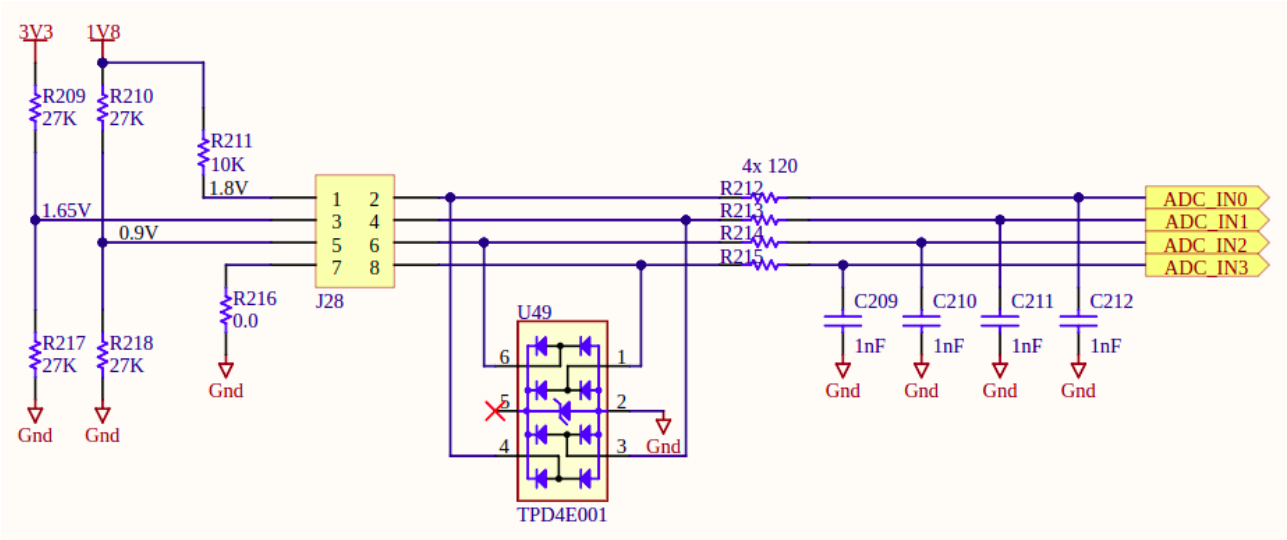


Table 9: J28 pins

Pin *J28*	SoC ball name	Non-SoC ball name	I/O *EVK perspective*	Reset state	Description
Odd pins					
1		1.8V reference	O	O	1.8V through 10k resistor
3		1.65V reference	O	O	1.65V through resistive divider
5		0.9V reference	O	O	0.9V through resistive divider
7		GND	O	O	GND without resistor
Even pins					
2	ADC_IN0		I	I	Connected to SoC ADC_IN0 ball
4	ADC_IN1		I	I	Connected to SoC ADC_IN1 ball
6	ADC_IN2		I	I	Connected to SoC ADC_IN2 ball
8	ADC_IN3		I	I	Connected to SoC ADC_IN3 ball

Table 10: J29 pins

Pin *J29*	SoC ball name	Non-SoC ball name	I/O *EVK perspective*	Reset state	Description
Odd pins					
1		1.8V reference	O	O	1.8V through 10k resistor
3		1.65V reference	O	O	1.65V through resistive divider
5		0.9V reference	O	O	0.9V through resistive divider
7		GND	O	O	GND without resistor
Even pins					
2	ADC_IN4		I	I	Connected to SoC ADC_IN4 ball
4	ADC_IN5		I	I	Connected to SoC ADC_IN5 ball
6	ADC_IN6		I	I	Connected to SoC ADC_IN6 ball
8	ADC_IN7		I	I	Connected to SoC ADC_IN7 ball

2.2 Audio

The i.MX 95 EVK audio subsystem uses the WM8904 codec connected to the SAI3 pins (also available in J49 Section 2.2.5), with the power output delivered by the PAM8019 audio amplifier.

The WM8904 codec can be accessed through the I2C4 interface, with the GIPO1/IRQ pin connected to the SoC GPIO_IO11 ball.

Table 11: WM8904 codec signals

Signal name *WM8904*	SoC ball name	Non-SoC ball name	I/O *WM8904 perspective*	Remark
ADCDAT	SAI3_RXD0			
BCLK/GPIO4	SAI3_TXC			
DACDAT	SAI3_TXD0			
GPIO1/IRQ	GPIO_IO11		I/O	
HPOUTFB		Pin 4 *J31*		Can be shorted to ground through jumper JP1
HPOUTL		LIN *PAM8019*		
HPOUTR		RIN *PAM8019*		
IN2L		Pin 1 *J31*		
LINEOUTFB		GND		
LRCLK	SAI3_TXFS			
MCLK	SAI3_MCLK			
MICBIAS		Pin 1 *J31*		
SCLK	I2C4_SCL		I	
SDA	I2C4_SDA		I/O	

Table 12: PAM8019 amplifier signals

Signal name *PAM8019*	SoC ball name	Non-SoC ball name	I/O *PAM8019 perspective*	Remark
Bypass		C229	I	1uF to GND
GND		GND	I/O *power*	
HP/SPK		Pin 2 *S3*	I	
HPL_OUT		Pin 2 *J31*	O *power*	
HPR_OUT		Pin 3 *J31*	O *power*	
L_OUTN		Pin 2 *J30*	O *power*	
L_OUTP		Pin 1 *J30*	O *power*	
LIN		HPOUTL *WM8904*	I	

Continued on next page

Table 12: PAM8019 amplifier signals (Continued)

Signal name *PAM8019*	SoC ball name	Non-SoC ball name	I/O *PAM8019 perspective*	Remark
Mute		GND	I	
PAD		GND		
PL				NC
R_OUTN		Pin 4 *J30*	O *power*	
R_OUTP		Pin 3 *J30*	O *power*	
RIN		HPOUTR *WM8904*	I	
SD		AUD_5V	I	
UVP				NC
VDD		AUD_5V	I *power*	
Volume		Pin 2 *P1*	I	Connected to volume potentiometer, see Section 2.2.3 on the next page

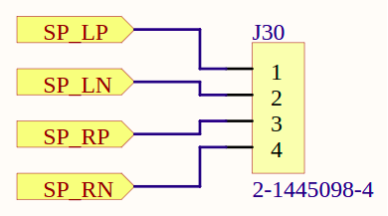
2.2.1 Speaker Connector (J30)

The speaker connector – J30 – connects to the PAM8019 3W Class D audio amplifier present in the EVK.

Table 13: Speaker connector (J30) signals

Pin *J30*	PAM8019 signal	I/O *EVK perspective*	Description
1	L_OUTP	O	Left speaker audio output – positive terminal
2	L_OUTN	O	Left speaker audio output – negative terminal
3	R_OUTP	O	Right speaker audio output – positive terminal
4	R_OUTN	O	Right speaker audio output – negative terminal

Figure 5: Speaker Connector (J30)

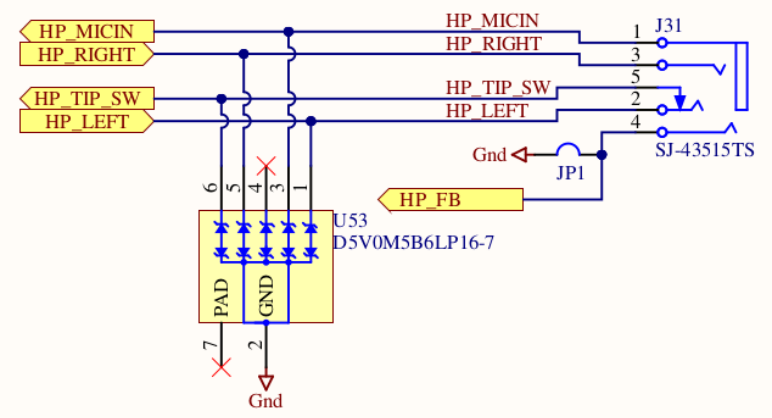


2.2.2 Audio Connector (J31)

Table 14: Audio connector (J31) signals

Pin *J31*	WM8904 signal	PAM8019 signal	I/O *EVK perspective*	Description
1	IN2L MICBIAS		I	Microphone input – mono
2		HPL_OUT	O	Headphone out – left
3		HPR_OUT	O	Headphone out – right
4	HPOUTFB		I	
5			I	NC

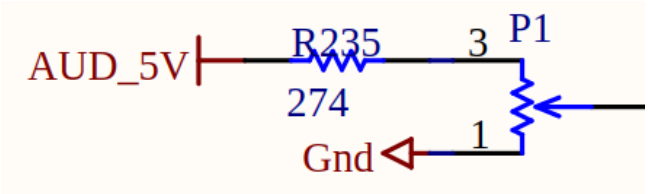
Figure 6: Audio Connector (J31)



2.2.3 Audio volume potentiometer (P1)

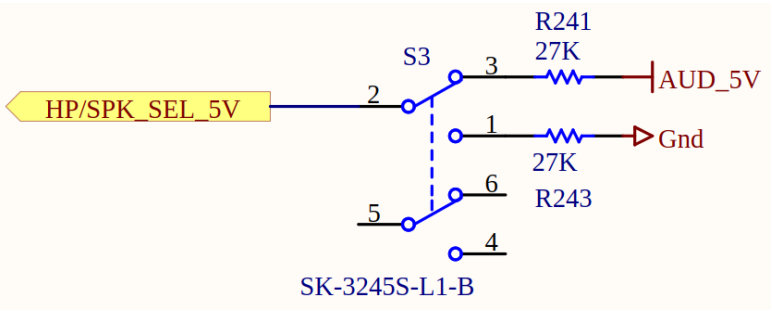
The audio volume potentiometer control the gain of the PAM8019 audio amplifier through the amplifiers' Volume pin (pin 8), providing an analog voltage signal derived from the 5V audio supply. Turning the potentiometer knob clockwise increases the voltage at the Volume pin.

Figure 7: Potentiometer for adjusting audio volume (P1)



2.2.4 Headphone/Speaker Selector (S3)

Figure 8: Switch select for Headphone/Speaker (S3)

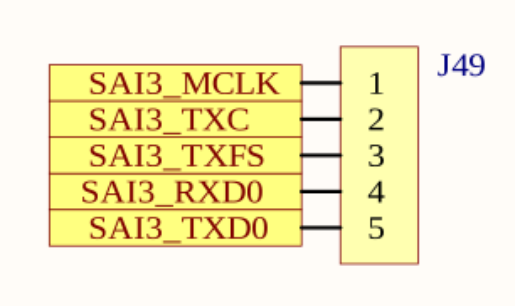


2.2.5 SAI – Serial Audio Interface Connector (J49)

Table 15: Serial Audio Interface (SAI3) connector (J49) signals

Pin *J45*	SAI3 signal	I/O *EVK perspective*	Description
1	SAI3_MCLK	O	
2	SAI3_TXC	O	
3	SAI3_TXFS	O	
4	SAI3_RXD0	I	
5	SAI3_TXD0	O	

Figure 9: Serial Audio Interface Connector (J49)



2.3 Boot Configuration

The i.MX 95 SoC boot mode can be selected through the switches in SW2 (Figure 11 on the following page). The boot modes are mapped in Table 16.

Table 16: SW2 Boot Modes

SW2 switch 1 BOOT_MODE [3]	SW2 switch 2 BOOT_MODE [2]	SW2 switch 3 BOOT_MODE [1]	SW2 switch 4 BOOT_MODE [0]	Core	Boot source
0	0	0	0	–	Reserved
0	0	0	1	–	Reserved
0	0	1	0	–	Reserved
0	0	1	1	–	Reserved
0	1	0	0	–	Reserved
0	1	0	1	–	Reserved
0	1	1	0	–	Reserved
1	0	0	0	M33	Defined by internal fuses
1	0	0	1	M33	Serial downloader USB1/2
1	0	1	0	M33	8-bit eMMC 5.1
1	0	1	1	M33	4-bit SD 3.0
1	1	0	0	M33	FlexSPI Serial NOR
1	1	0	1	M33	FlexSPI Serial NAND
1	1	1	0	–	Reserved

Switch position: 1 = ON; 0 = OFF

2.3.1 Boot Mode DIP Switch (SW2)

Figure 10: Boot Mode DIP Switch (SW2) shcematic

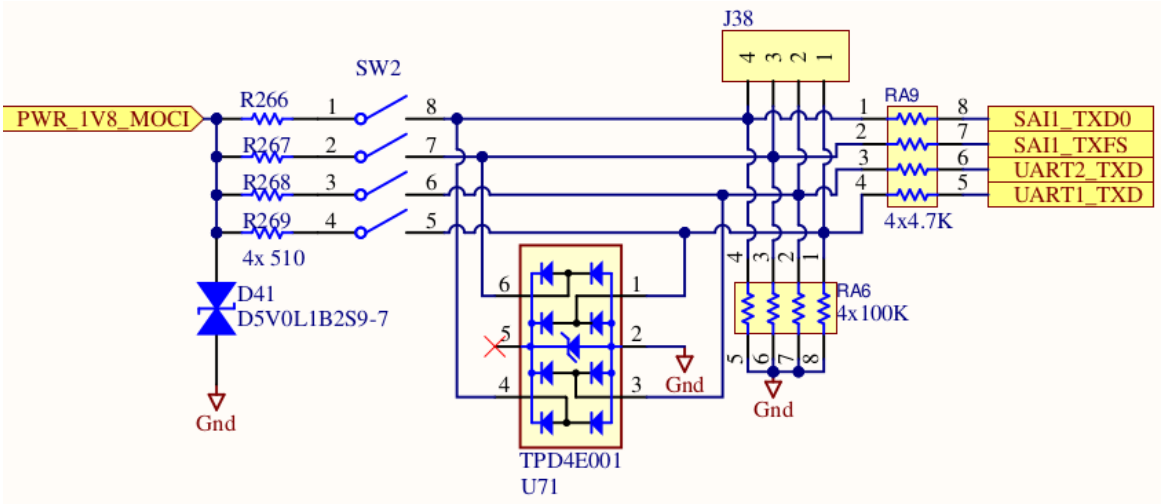


Figure 11: Boot Mode DIP Switch (SW2)

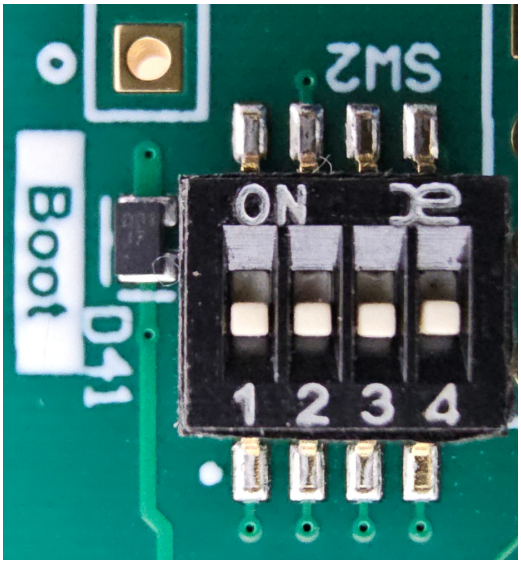
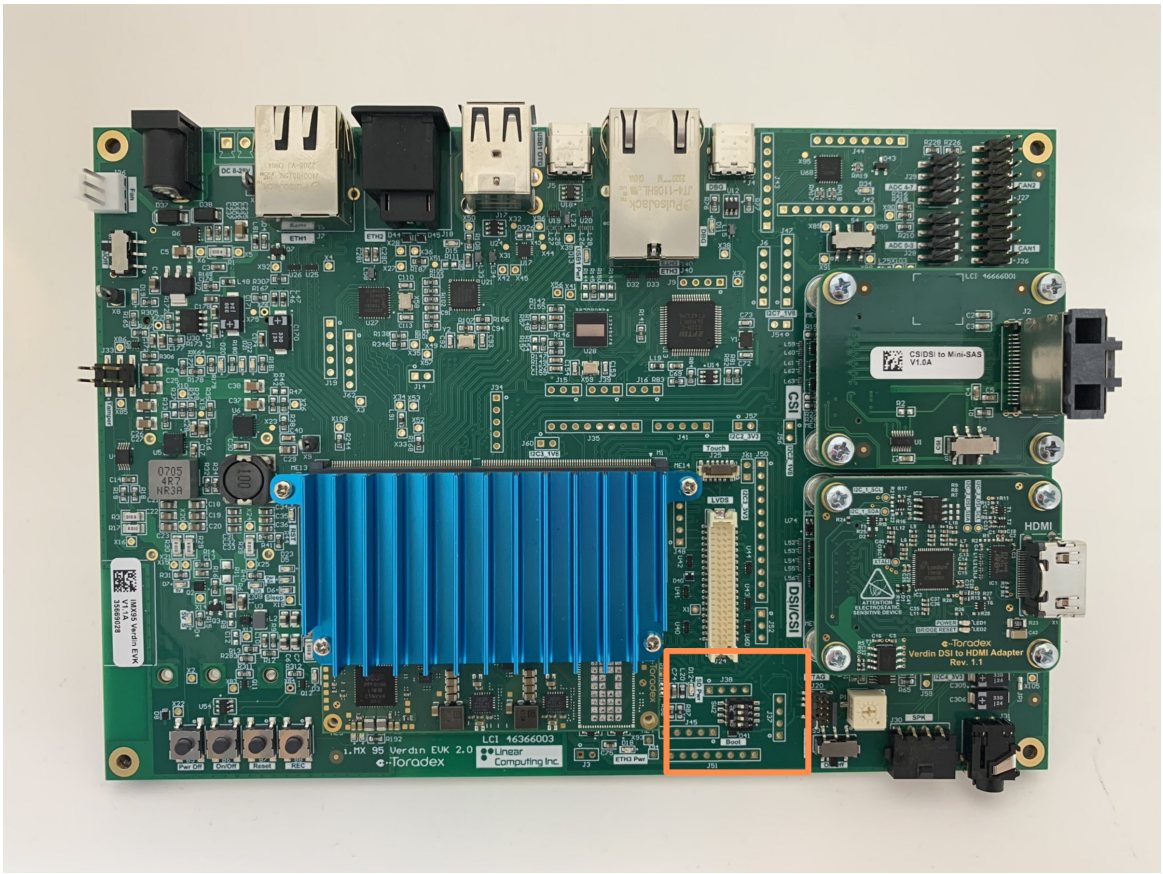


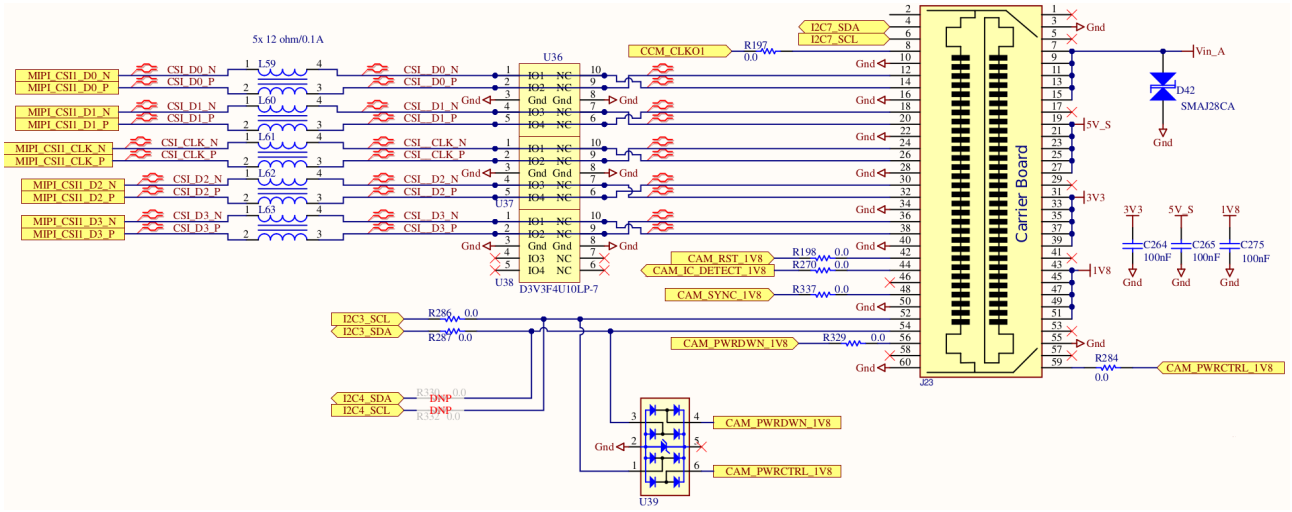
Figure 12: Boot Mode Dip Switch (SW2) location



2.4 Camera

2.4.1 MIPI CSI – Camera Serial Interface (J23)

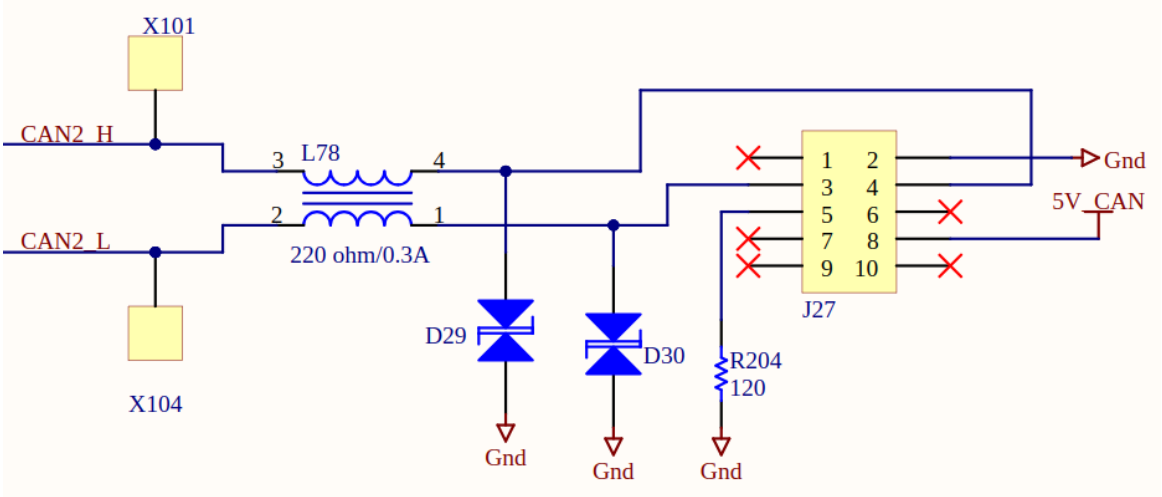
Figure 13: MIPI CSI Camera Connector (J23)



2.5 CAN – Control Area Network

The i.MX 95 EVK comes with two pre-assembled CAN headers, J26 and J27, each connected to a TJA1463 CAN transceiver.

Figure 14: CAN Connector (J26 and J27)



2.5.1 CAN1 (J26)

Enable CAN1 in the DMIC/CAN1 switch (S4).
The S4 switch (Section 2.13.1 on page 39) routes either CAN1 signals or Digital Microphone Interface (DMIC) signals to the SoC. The CAN1_TX and CAN1_RX signals are not accessible to the SoC when the S4 switch is in DMIC position.

The CAN1 header (J26) connects to a TJA1463 CAN transceiver attached to the CAN1 interface in the SoC.

The CAN1 bus termination impedance can be selected from the S1 switch, which is described in Section 2.5.2 on the next page.

Table 17: CAN1 header (J26) signals

Pin *J26*	Signal name	I/O *EVK perspective*	Description
Odd pins			
1			NC
3	CAN_L *TJA1463 (U47)*	I/O	CAN1 L terminal
5	GND	I/O	120Ω GND
7			NC
9			NC
Even pins			
2	GND	I/O *power*	Power GND
4	CAN_H *TJA1463 (U47)*	I/O	CAN1 H terminal

Continued on next page

Table 17: CAN1 header (J26) signals (Continued)

Pin *J26*	Signal name	I/O *EVK perspective*	Description
6			NC
8	5V_CAN	O *power*	Can 5V supply
10			NC

Table 18: CAN1 TJA1463 signals

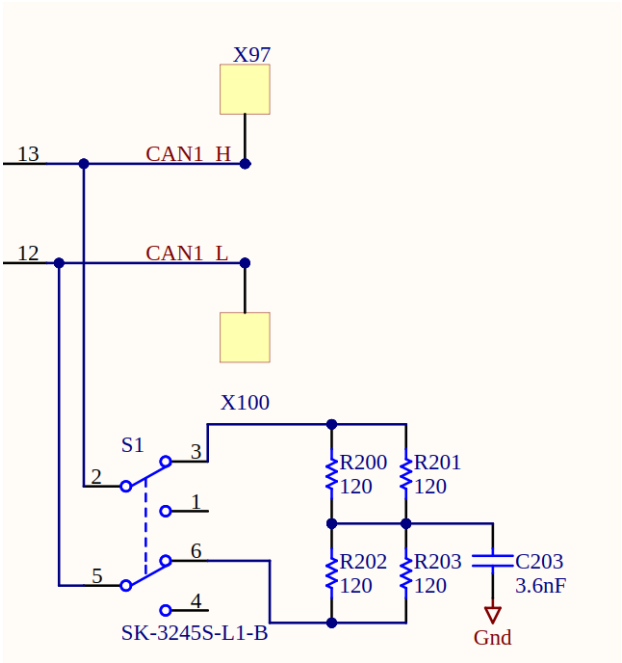
Signal name *TJA1463*	SoC ball name	Non-SoC ball name	I/O *TJA1463 perspective*	Remark
CAN-H		Pin 4 *J26*		More information about J26 on Table 17 on the previous page
CAN-L		Pin 3 *J26*		More information about J26 on Table 17 on the preceding page
EN		P0_2 *IO expander (U68)*	I *PU 4k7*	
GND		GND		
INH				NC
NC				NC
nERR	SPI7_SCK		O OD *PU 4k7*	
nSTB		P0_0 *IO expander (U68)*	I *PU 4k7*	
RXD	PDM_BIT_STREAM0[1]			
TXD	PDM_CLK[1]			
VBAT		Vin		Connected to main supply
VCC		5V_CAN		
Vio		3V3_CAN		
WAKE		P0_1 *IO expander (U68)*		Inverted by circuit

[1] Only when CAN functionality is selected at switch S4, see Section 2.13.1 on page 39.

2.5.2 CAN1 Termination Selector (S1)

The i.MX 95 EVK CAN1 bus comes with a pre-built termination (shown in Figure 15 on the next page), which can be enabled/disabled through the S1 switch.

Figure 15: CAN1 termination selector (S1)



2.5.3 CAN2 (J27)

The CAN2 header (J27) connects to a TJA1463 CAN transceiver attached to the CAN2 interface in the SoC.

The CAN2 bus termination impedance can be selected from the S2 switch, which is described in Section 2.5.4 on the following page.

Table 19: CAN2 header (J27) signals

Pin *J27*	Signal name	I/O *EVK perspective*	Description
Odd pins			
1			NC
3	CAN_L *TJA1463 (U48)*	I/O	CAN2 L terminal
5	GND	I/O	120Ω GND
7			NC
9			NC
Even pins			
2	GND	I/O *power*	Power GND
4	CAN_H *TJA1463 (U48)*	I/O	CAN2 H terminal
6			NC
8	5V_CAN	O *power*	Can 5V supply
10			NC

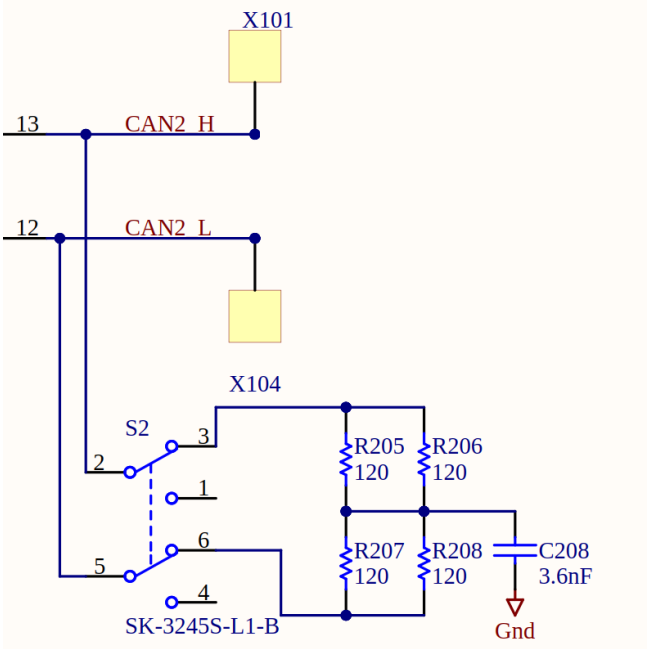
Table 20: CAN2 TJA1463 signals

Signal name *TJA1463*	SoC ball name	Non-SoC ball name	I/O *TJA1463 perspective*	Remark
CAN-H		Pin 4 *J27*		More information about J27 on Table 19 on the previous page
CAN-L		Pin 3 *J27*		More information about J27 on Table 19 on the preceding page
EN		P0_5 *IO expander (U68)*	I *PU 4k7*	
GND		GND		
INH				NC
NC				NC
nERR	SPI7_SOUT		O OD *PU 4k7*	
nSTB		P0_3 *IO expander (U68)*	I *PU 4k7*	
RXD	CAN2_RX			
TXD	CAN2_TD			
VBAT		Vin		Connected to main supply
VCC		5V_CAN		
Vio		3V3_CAN		
WAKE		P0_4 *IO expander (U68)*		Inverted by circuit

2.5.4 CAN2 Termination Selector (S2)

The i.MX 95 EVK CAN2 bus comes with a pre-built termination (shown in Figure 16), which can be enabled/disabled through the S2 switch.

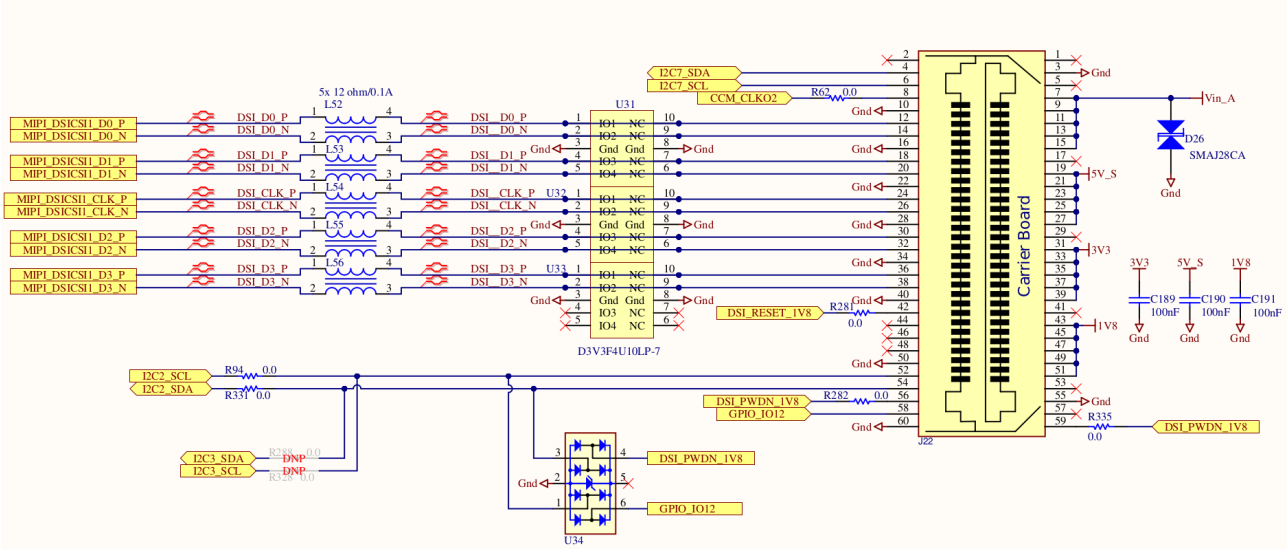
Figure 16: CAN2 termination selector (S2)



2.6 Display

2.6.1 MIPI DSI – Display Serial Interface (J22)

Figure 17: MIPI DSI Display Connector (J22)



2.6.2 LVDS – Low-Voltage Differential Signaling (J24)

Ensure the EVK supply voltage is suitable to the display.
The display's operational voltage range must cover the voltage supplied to the EVK through the power input barrel jack (J1, Section 2.14.6 on page 44), as this voltage is supplied to the pins 39 and 40 of the LVDS connector (J24).

The LVDS connector (J24) routes directly to the LVDS interfaces in the SoC, with the LVDS_A pins mapping to the LVDS0 interface, and the LVDS_B pins mapping to the LVDS1 interface. Data and clock lanes are protected by TVS diodes and common-mode chokes.

The touch screen I2C pins (36 and 38) are routed to the SoC's I2C7 interface.

Table 21: LVDS connector (J24) signals

Pin *J24*	SoC ball name	Non-SoC ball name	I/O *EVK perspective*	Remark
Odd pins				
1	LVDS0_D3_P		O	LVDS channel 0, data lane 3, polarity P
3	LVDS0_D3_N		O	LVDS channel 0, data lane 3, polarity N
5		GND	GND *power*	
7	LVDS0_D2_P		O	LVDS channel 0, data lane 2, polarity P
9	LVDS0_D2_N		O	LVDS channel 0, data lane 2, polarity N
11		GND	GND *power*	
13	LVDS0_D1_P		O	LVDS channel 0, data lane 1, polarity P

Continued on next page

Table 21: LVDS connector (J24) signals (Continued)

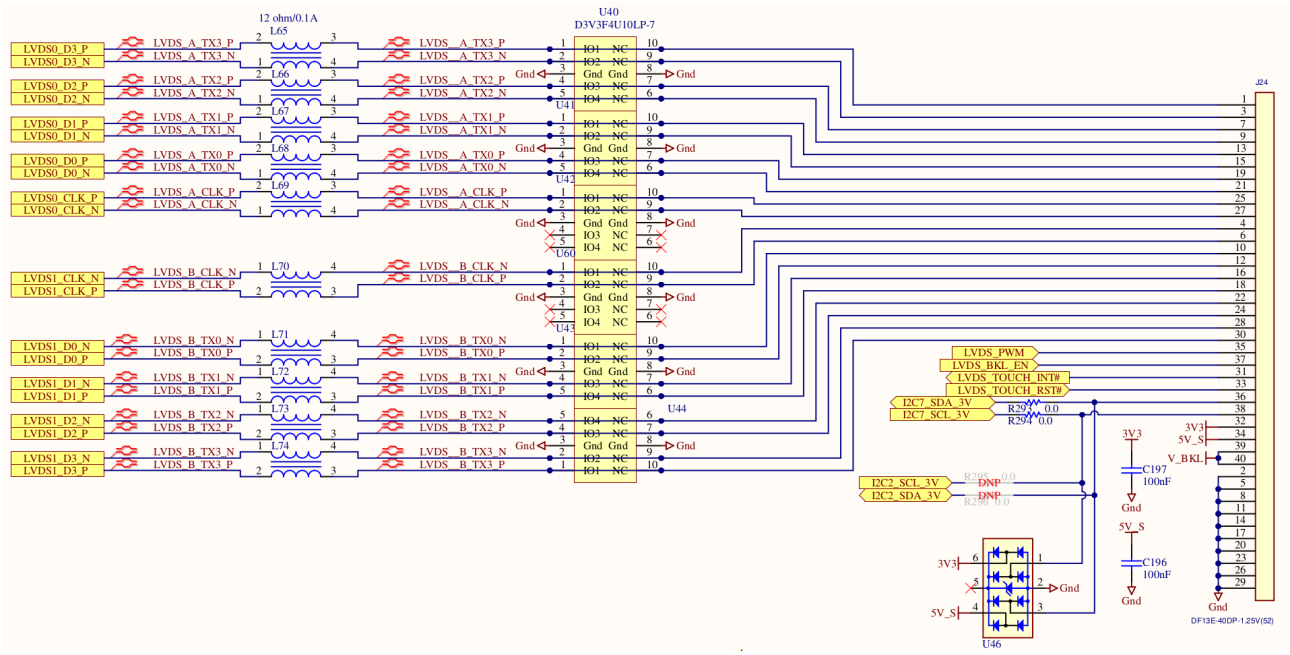
Pin *J24*	SoC ball name	Non-SoC ball name	I/O *EVK perspective*	Remark
15	LVDS0_D1_N		O	LVDS channel 0, data lane 1, polarity N
17		GND	GND *power*	
19	LVDS0_D0_P		O	LVDS channel 0, data lane 0, polarity P
21	LVDS0_D0_N		O	LVDS channel 0, data lane 0, polarity N
23		GND	GND *power*	
25	LVDS0_CLK_P		O	LVDS channel 0, clock lane, polarity P
27	LVDS0_CLK_N		O	LVDS channel 0, clock lane, polarity N
29		GND	GND *power*	
31			I	Display touch interrupt
33			O	Display touch reset
35	GPIO_IO19		O	Display backlight PWM
37			O	Diaplay backlight enable
39		Vin	O *power*	Connected to main power supply
Even pins				
2		GND	GND *power*	
4	LVDS1_CLK_N		O	LVDS channel 1, clock lane, polarity N
6	LVDS1_CLK_P		O	LVDS channel 1, clock lane, polarity P
8		GND	GND *power*	
10	LVDS1_D0_N		O	LVDS channel 1, data lane 0, polarity N
12	LVDS1_D0_P		O	LVDS channel 1, data lane 0, polarity P
14		GND	GND *power*	
16	LVDS1_D1_N		O	LVDS channel 1, data lane 1, polarity N
18	LVDS1_D1_P		O	LVDS channel 1, data lane 1, polarity P
20		GND	GND *power*	
22	LVDS1_D2_N		O	LVDS channel 1, data lane 2, polarity N
24	LVDS1_D2_P		O	LVDS channel 1, data lane 2, polarity P
26		GND	GND *power*	
28	LVDS1_D3_N		O	LVDS channel 1, data lane 3, polarity N
30	LVDS1_D3_P		O	LVDS channel 1, data lane 3, polarity P
32		3V3	O *power*	3.3V supply
34		5V_S	O *power*	5V supply
36	GPIO_IO08		I/O	Display touch I2C SDA
38	GPIO_IO09		O	Display touch I2C SCL

Continued on next page

Table 21: LVDS connector (J24) signals (Continued)

Pin *J24*	SoC ball name	Non-SoC ball name	I/O *EVK perspective*	Remark
40		Vin	O *power*	Connected to main power supply

Figure 18: LVDS Connector (J24)



2.6.3 Capacitive Touchscreen Connector (J25)

The Capacitive Touch Connector allows the connection of I2C touch control interfaces. The connector expects a 10 pin, 0.5mm pitch flat cable.

Connector type: Receptacle FPC/FFC connector, Hirose FH12-10S-0.5SVA(54)

Table 22: Capacitive Touch Connector (J25) signals

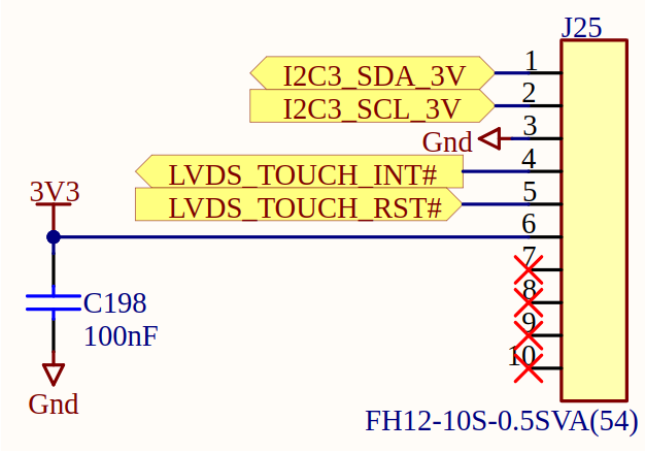
Pin *J25*	SoC ball name	Non-SoC ball name	I/O *EVK perspective*	Remark
1	GPIO_IO00		I/O OD *5.1k PU*	I2C3_SDA
2	GPIO_IO01		O OD *5.1k PU*	I2C3_SCL
3		GND	GND *power*	
4	GPIO_IO28		I	Touch interrupt
5		P0_6 *IO expander (U68)*	O	Touch reset
6		3V3	O *power*	3.3V supply

Continued on next page

Table 22: Capacitive Touch Connector (J25) signals (Continued)

Pin *J25*	SoC ball name	Non-SoC ball name	I/O *EVK perspective*	Remark
7				NC
8				NC
9				NC
10				NC

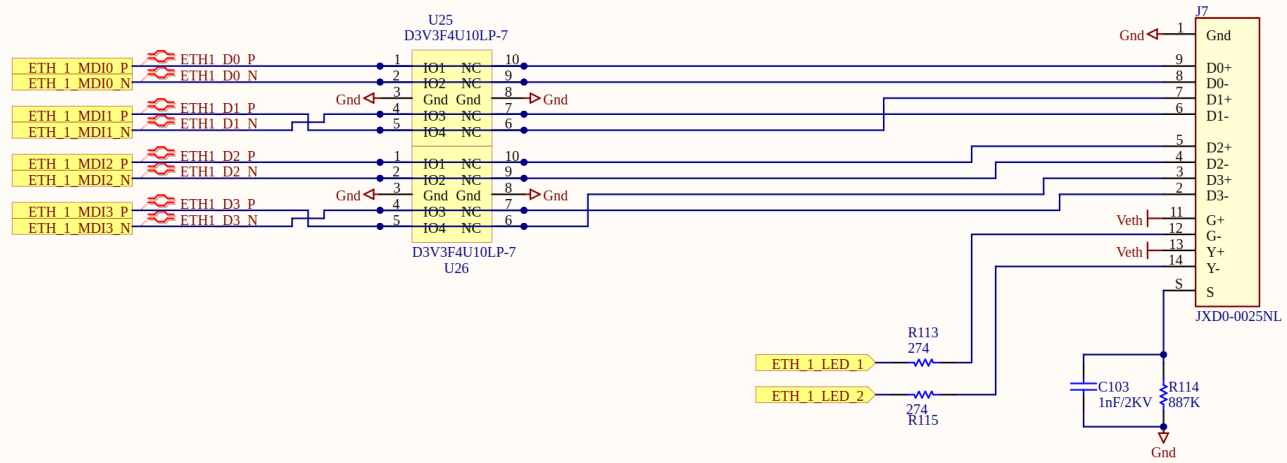
Figure 19: Capacitive Touchscreen Connector (J25)



2.7 Ethernet

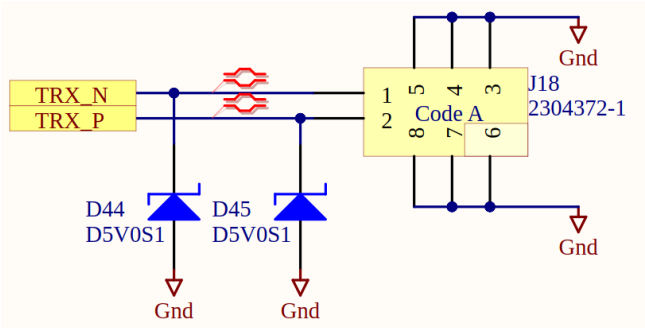
2.7.1 1 Gbps Ethernet Connector (J7)

Figure 20: 1 Gbps Ethernet Connector (J7)



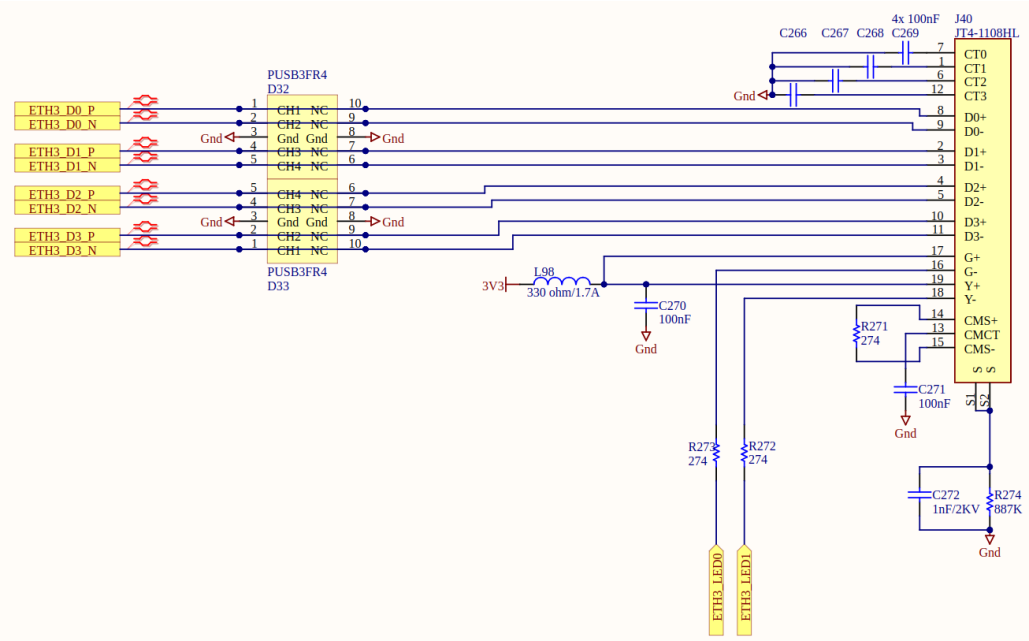
2.7.2 1 Gbps Automotive Ethernet (J18)

Figure 21: 1 Gbps Automotive Ethernet Connector (J18)



2.7.3 10 Gbps Ethernet (J40)

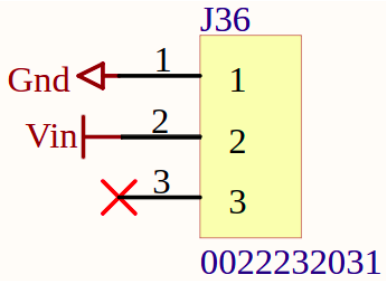
Figure 22: 10 Gbps Ethernet Connector (J40)



2.8 Fan Connector (J36)

Ensure the EVK supply voltage is suitable to the fan.
The fan's operational voltage range must cover the voltage supplied to the EVK through the power input barrel jack (J1, Section 2.14.6 on page 44), as this voltage is supplied to the pin 2 of the fan connector (J36).

Figure 23: Fan Connector (J36)



2.9 FTDI

The FTDI interface allows for debugging and programming on the USB-C connectivity. The circuit utilizes an FTDI chip to convert USB signals to UART or JTAG interfaces, enabling communication with the different core (A55, M7 and M33).

See Section 2.13.2 on page 39 for information on the FTDI/JTAG configuration switch.

Figure 24: FTDI

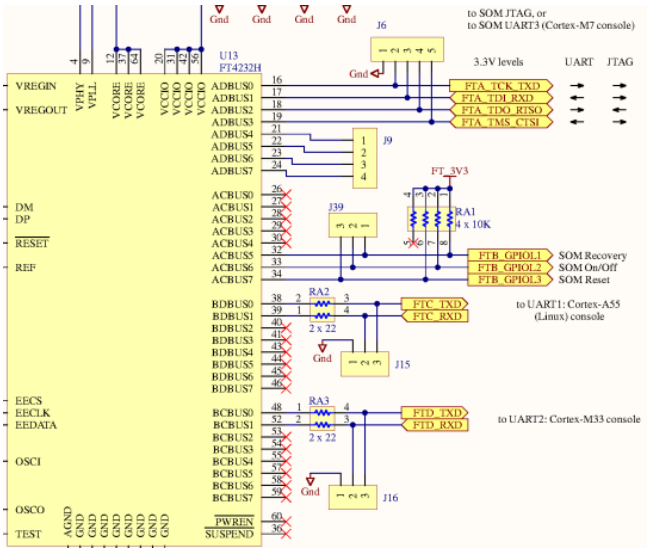


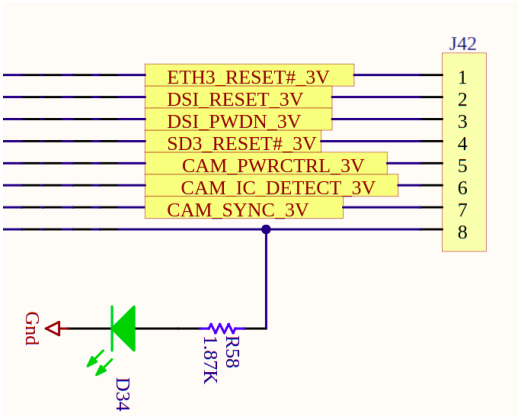
Table 23: FTDI Connectors and Signals

Connector	Pin	Signal	I/O FTDI perspective	Description
J6	1	GND		
	2	FTC_TCK_TXD	O	JTAG clock signal Transmit data to UART3: Cortex-M7 (Linux) console
	3	FTC_TDI_RXD	I O	JTAG Test Data In Receive data from UART3: Cortex-M7 (Linux) console
	4	FTC_TDO_RTSO	I	JTAG Test Data Out
	5	FTC_TMS_CTSI	O	JTAG Test Mode Select
J15	1	GND		
	3	FTC_TXD	O	Transmit data to UART1: Cortex-A55 (Linux) console
	2	FTC_RXD	I	Receive data from UART1: Cortex-A55 (Linux) console
J16	1	GND		
	3	FTC_TXD	O	Transmit data to UART2: Cortex-M33 console
	2	FTC_RXD	I	Receive data from UART2: Cortex-M33 console

2.10 IO Expanders

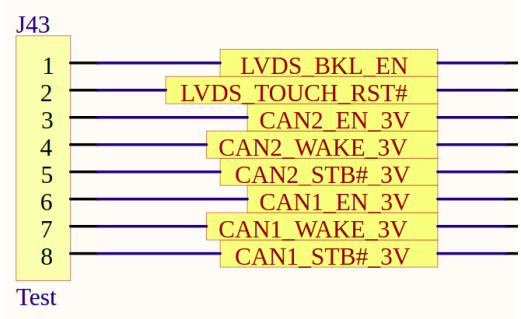
2.10.1 IO Expander 1 (J42)

Figure 25: IO Expander (J42)



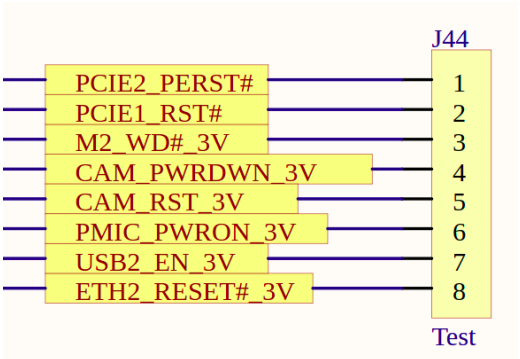
2.10.2 IO Expander 2 (J43)

Figure 26: IO Expander (J43)



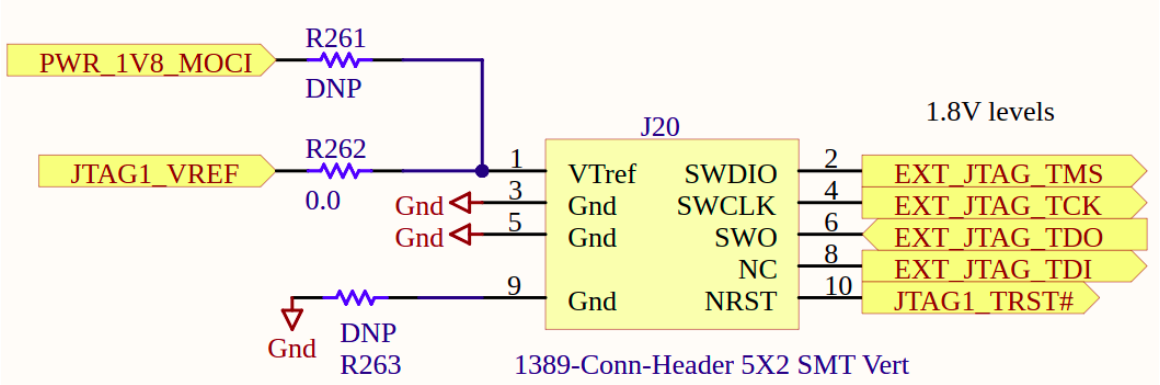
2.10.3 IO Expander 3 (J44)

Figure 27: IO Expander (J44)



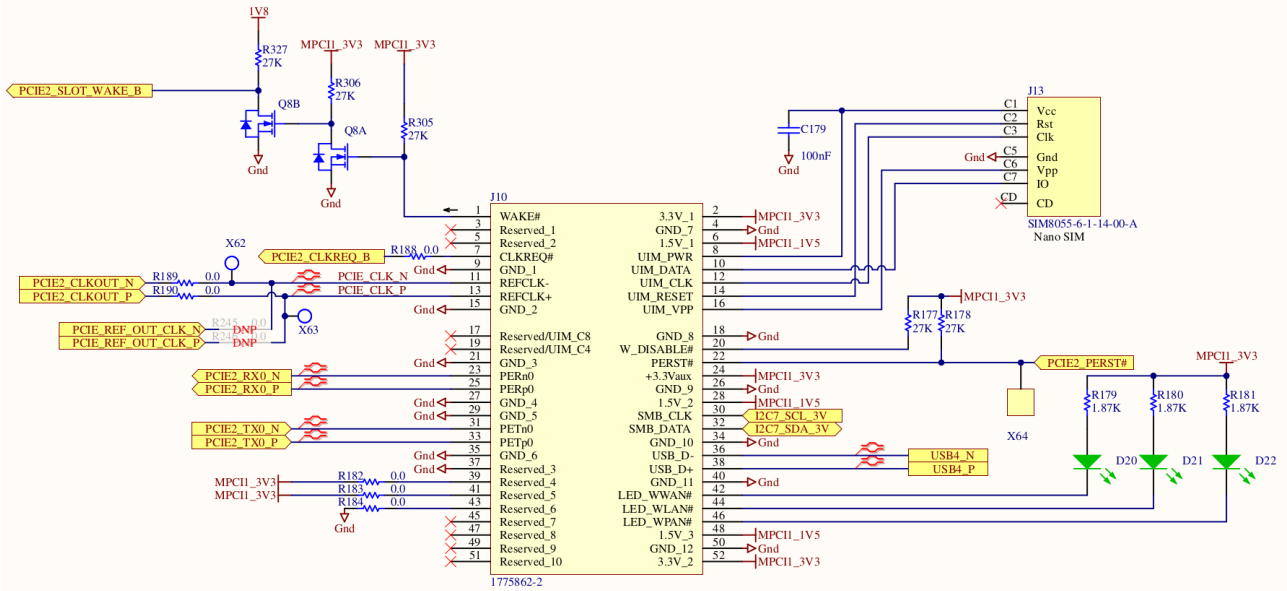
2.11 JTAG (J20)

Figure 28: JTAG Connector (J20)



2.12 PCIe (J10) and Nano-SIM Card Holder (J13)

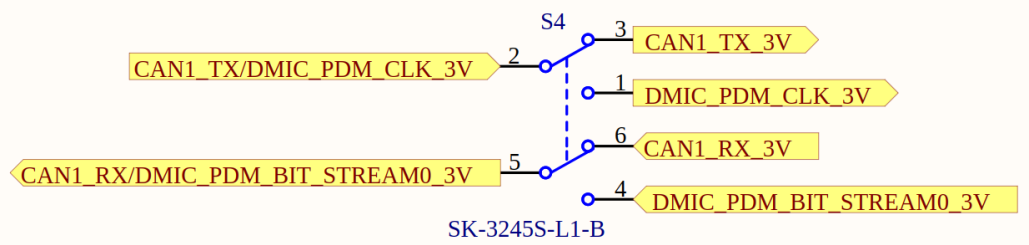
Figure 29: PCIe (J10) and Nano-SIM Card Holder (J13)



2.13 Peripheral Configuration

2.13.1 DMIC/CAN1 Selector (S4)

Figure 30: Switch select for for DMIC/CAN1 (S4)



2.13.2 FTDI/JTAG Configuration DIP Switch (SW1)

The FTDI/JTAG Configuration DIP Switch (SW1) allows selecting the SoC JTAG destination, the FTDI port A mode, and enable/disable FTDI control signals.

Table 24: SW1 switches

Switch	Description
SW1 switch 1	Selects SoC signal path: JTAG/"Bluetooth UART"
SW1 switch 2	Enables FTDI port A to JTAG[1]
SW1 switch 3	Selects FTDI port A signal: JTAG/UART3
SW1 switch 4	Enables FTDI control signals

[1] Requires SW1 switch 3 in JTAG (ON) position

Table 25: SoC JTAG routes (SW1)

SW1 switch 1 state	SW1 switch 2 state	SW1 switch 3 state	Description
On	Any	Any	SoC JTAG pins used for M.2 Bluetooth UART
Off	Off	Any	SoC JTAG connected to external JTAG connector
Off	On	On	SoC JTAG connected to FTDI JTAG port A
Off	On	Off	Invalid configuration

Table 26: JTAG port A routes

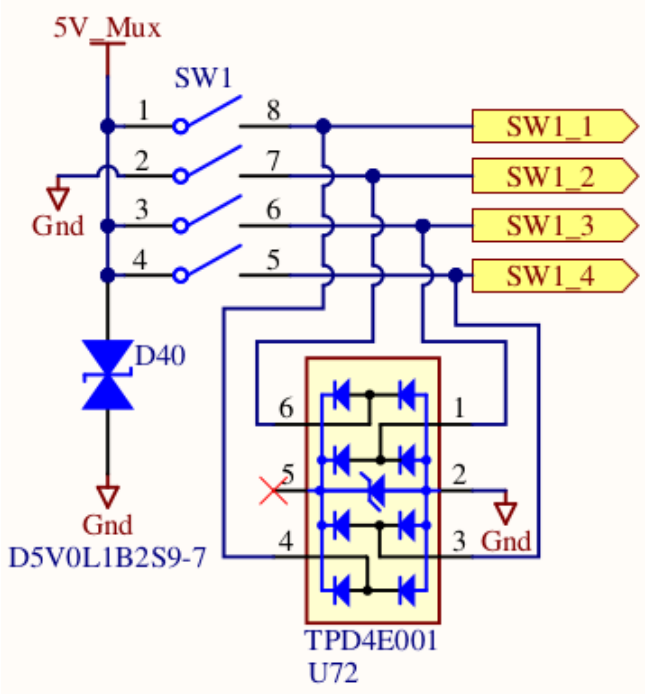
SW1 switch 3 state	Description
Off	FTDI port A connected to SoC UART3 (Cortex-M7 console)
On	FTDI port A connected to SoC JTAG[1]

[1] Requires SW1 switch 1 in JTAG mode, and SW1 switch 2 enabling FTDI port A JTAG. See Table 25.

Table 27: FTDI control signals selector

SW1 switch 4 state	Description
Off	FTDI control signals disabled
On	FTDI control signals enabled

Figure 31: FTDI Configuration DIP Switch (SW1)



2.14 Power

2.14.1 On/Off Switch (S6)

The S6 switch controls the power from the main supply to the system. When S6 is off, the On/Off Button (Section 2.14.3 on page 43) cannot power on the module.

Figure 32: On/Off Switch (S6) shcematic

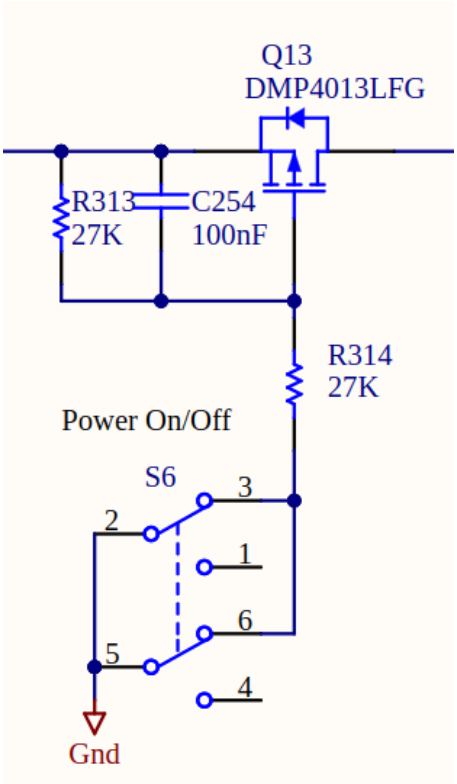
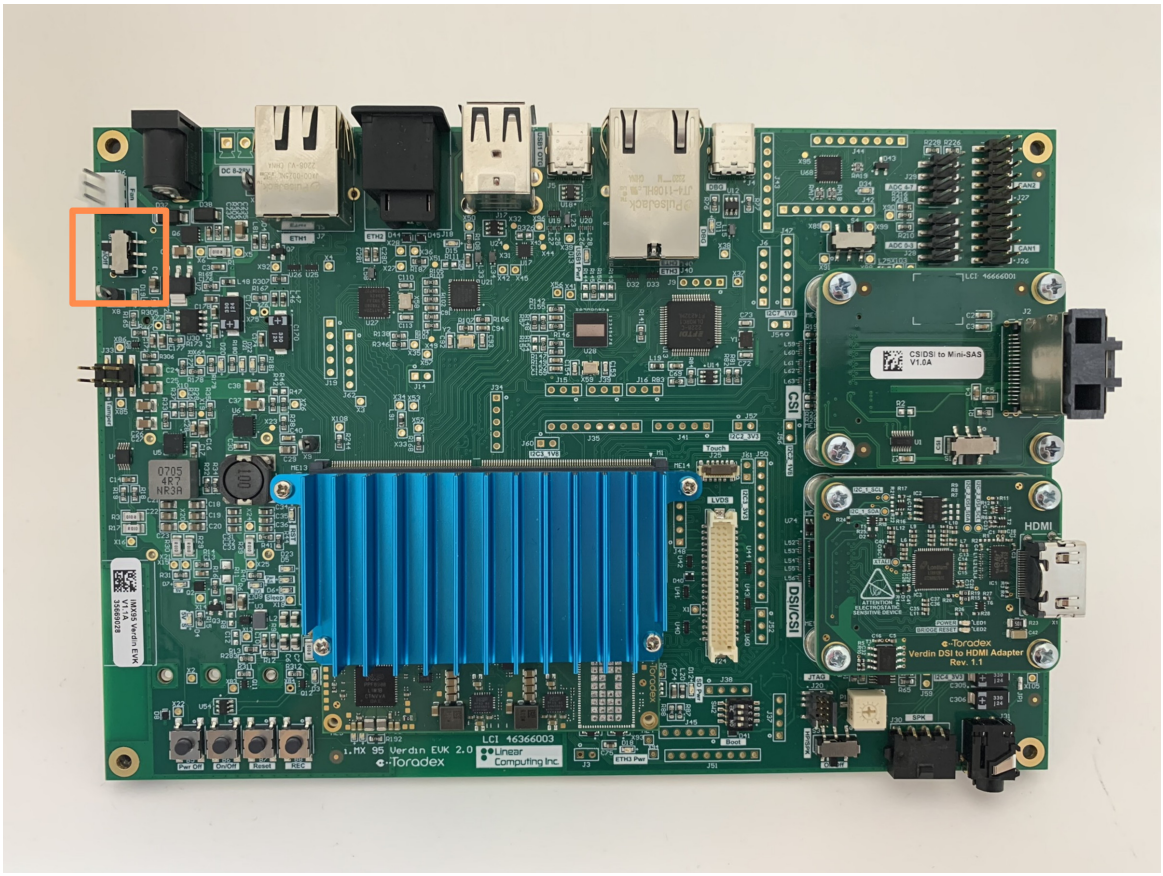


Figure 33: On/Off Switch (S6)

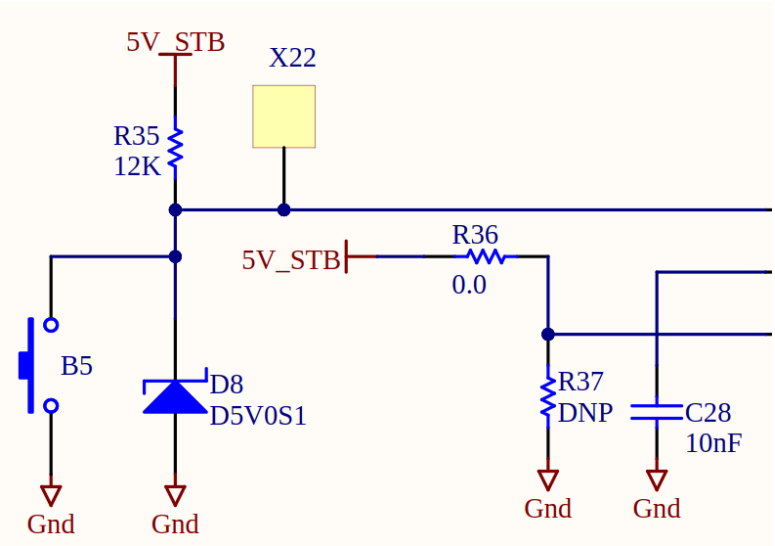
Figure 34: On/Off Switch (S6) location



2.14.2 Power Off Button (B5)

The power off button shuts down the main power supply for the entire EVK. To power off only the SoM, refer to the On/Off Button in Section 2.14.3 on the next page.

Figure 35: Power Off Button (B5)

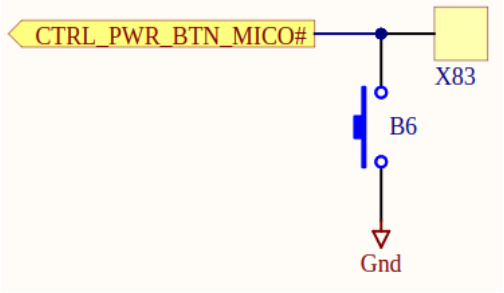


2.14.3 On/Off Button (B6)

Enable power in the On/Off switch (S6).
The On/Off Button cannot turn on the module when the power switch (S6, see Section 2.14.1 on page 41) is off, as the power switch cuts the main supply from the system.

The On/Off button controls the SoC power through the ONOFF ball (SoC F40), without interfering with the supplies in the EVK. To power off the main power supply for the entire EVK, please refer to Section 2.14.2 on the previous page.

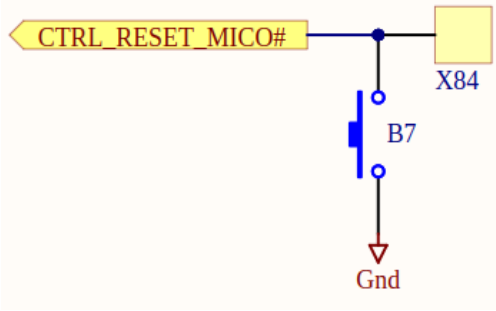
Figure 36: On/Off Button (B6)



2.14.4 Reset Button (B7)

The reset button disables the SoM's PMIC through the FCCU1 pin, without interfering with the supplies in the EVK.

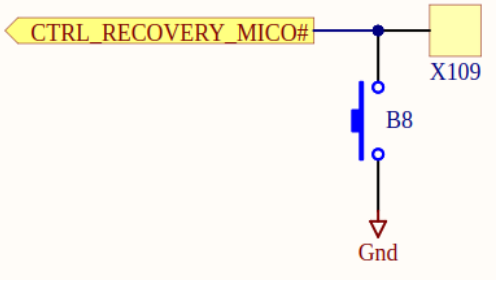
Figure 37: Reset Button (B7)



2.14.5 Recovery Button (B8)

When pressed during boot, the recovery button sets the boot mode to "USB Serial Downloader" by forcing the BOOT_MODE[3:0] signals to 0b0001. Booting via USB Serial Downloader allows a recovery software to be loaded on RAM.

Figure 38: Recovery Button (B8)



2.14.6 Power Input Barrel Jack (J1)

The power to the EVK should be provided through the Power Input Barrel Jack (J1), and may range from 8V to 28V DC, with 12V nominal.

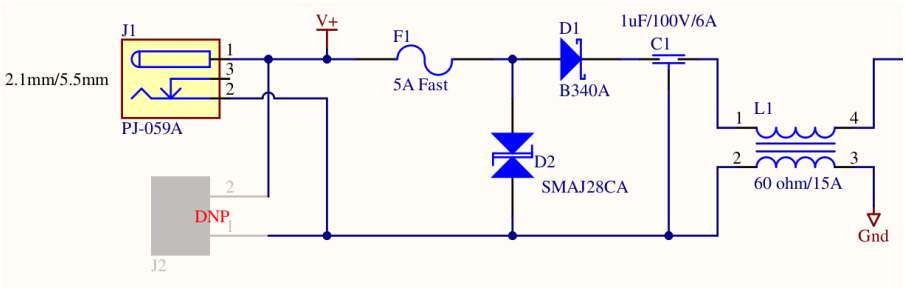
The Vin power rail is connected to the Power Input Barrel Jack, providing power to internal regulators (U5 to provide 5V, U6 to provide 3.3V, and U2 to provide standby 5V) and some interfaces (described in Table 28).

Some interfaces provide unregulated power from J1.
Check if your supply voltage is compatible with the devices connected to the interfaces listed in Table 28, as these interfaces provide unregulated power from the Power Input Barrel Jack (J1) in some of their power pins.

Table 28: Vin-connected interfaces

Connector	Pins	Description	Reference
CSI *J23*	9, 11, 13, 15	Optional power source	Section 2.4.1
DSI *J22*	9, 11, 13, 15	Optional power source	Section 2.6.1
FAN *J36*	2	Fan VCC on pin 2	Section 2.8
LVDS *J24*	39, 40	Vin is provided to the display backlight	Section 2.6.2

Figure 39: Barrel Jack Power Input Connector (J1)



2.14.7 Backup Battery

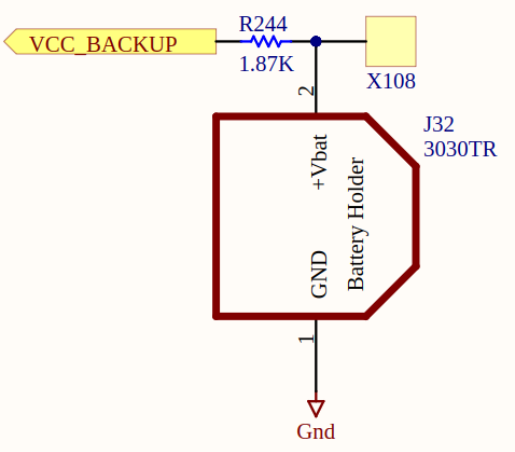
A backup battery holder (J32) is available on the EVK to provide backup power to the Real Time Clock through the VCC_BACKUP power rail. The battery charge is only used when the main system supply is off.

2.14.7.1 Backup Battery Holder (J32) The coin cell battery holder (J32) can house a single 10mm (diameter) battery, compatible with the CR927 and the CR1025 battery series.

Thick batteries expand the battery holder's contact spring.
The battery holder will not hold firmly a thin battery (CR1025, 2.5mm thickness) after the insertion of a thick battery (CR927, 2.7mm thickness) due to the expansion of the contact springs on the top side of the battery holder (J32) to house the thicker battery.

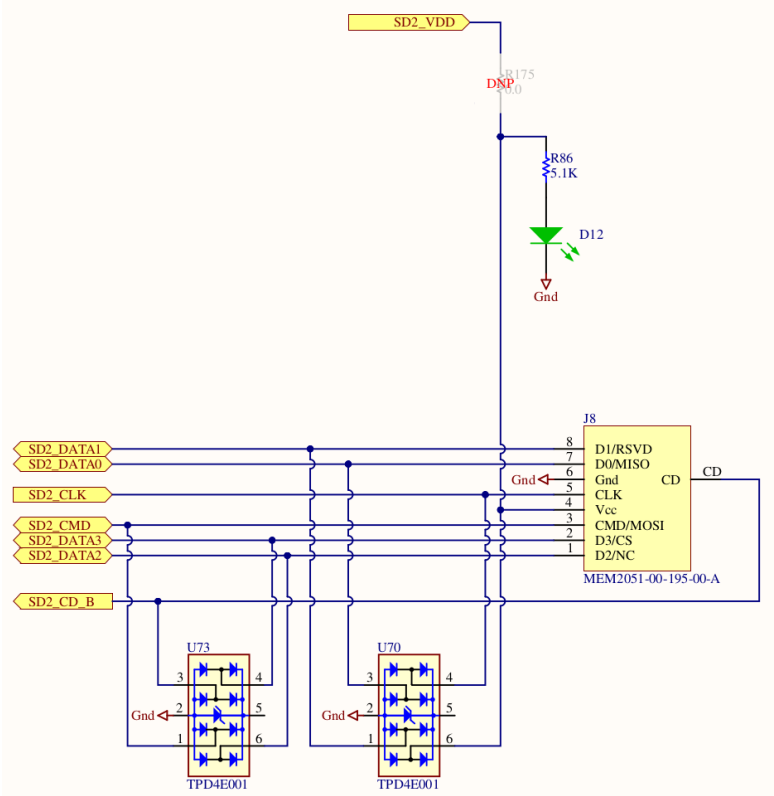
Connector type: KEYSTONE-3030

Figure 40: Backup battery holder (J32)



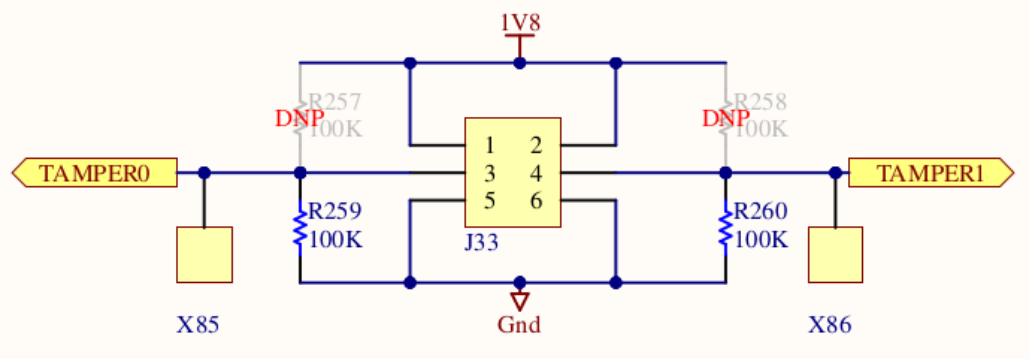
2.15 SD Card (J8)

Figure 41: SD Card Connector (J8)



2.16 Tamper Detection (J33)

Figure 42: Tamper (J33)

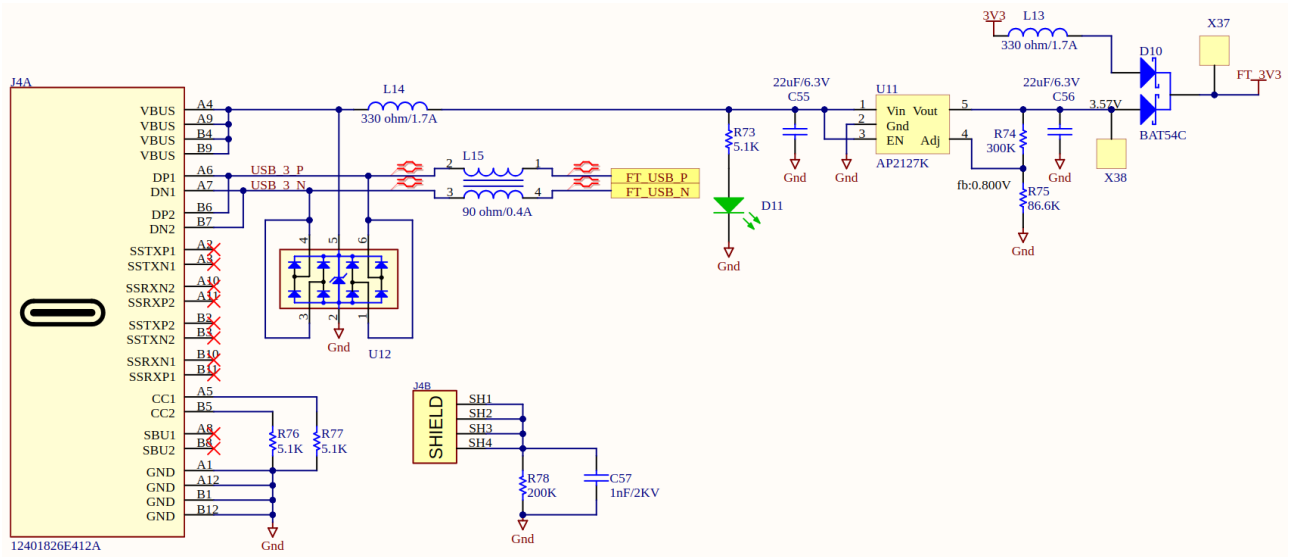


2.17 USB

2.17.1 Debug USB-C 2.0 (J4)

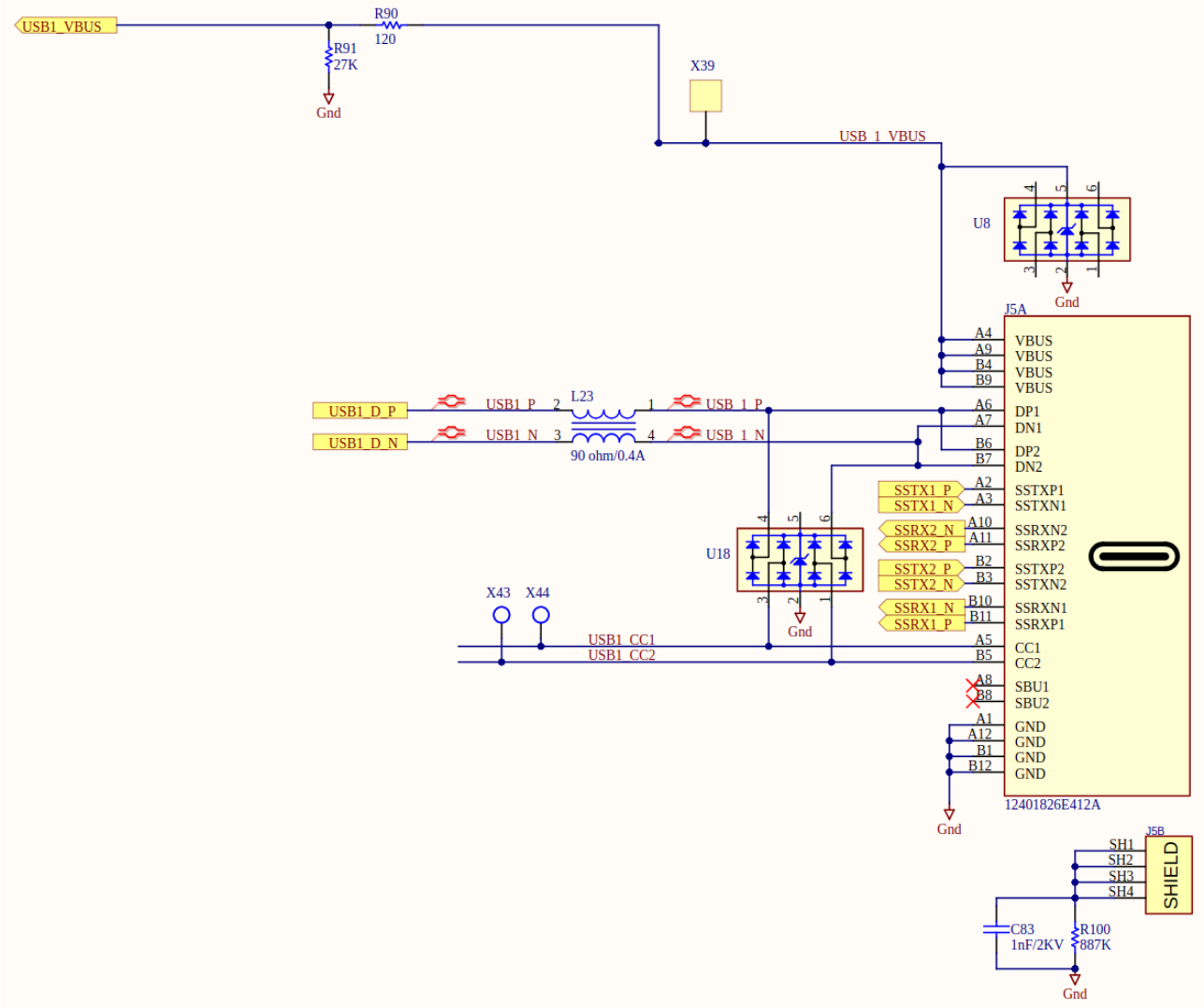
USB-C (optionally connected to UART1, UART2, and UART3 or JTAG) for connecting the multipurpose USB to serial converter based on the FT4232HL IC.

Figure 43: 2.0 Debug USB-C Connector (J4)



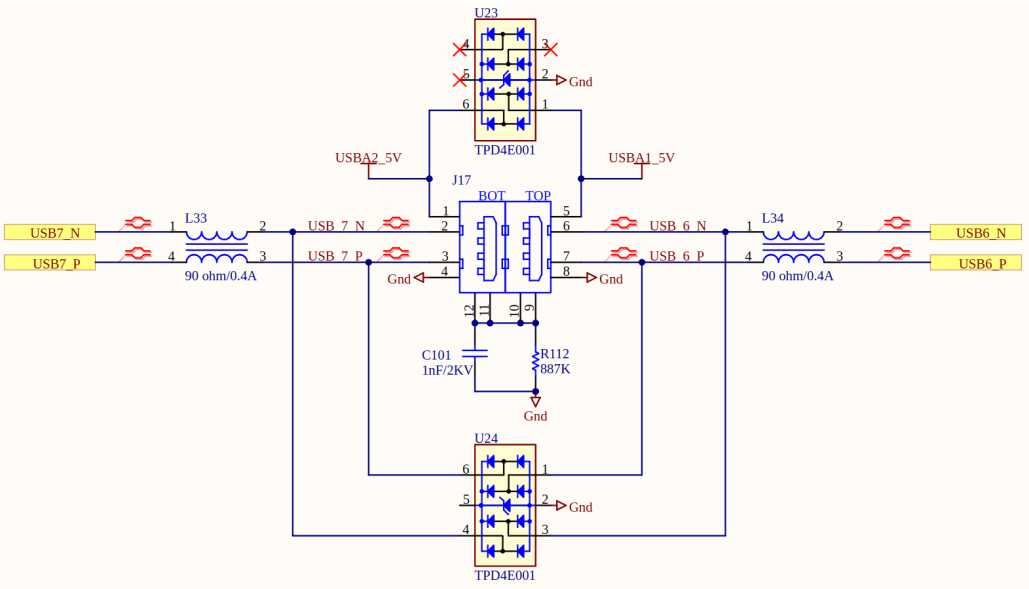
2.17.2 Dual-Role-Port USB-C 2.0 (J5)

Figure 44: 2.0 Dual-Role-Port USB-C Connector (J5)



2.17.3 USB 2.0 Type-A Hub (J17)

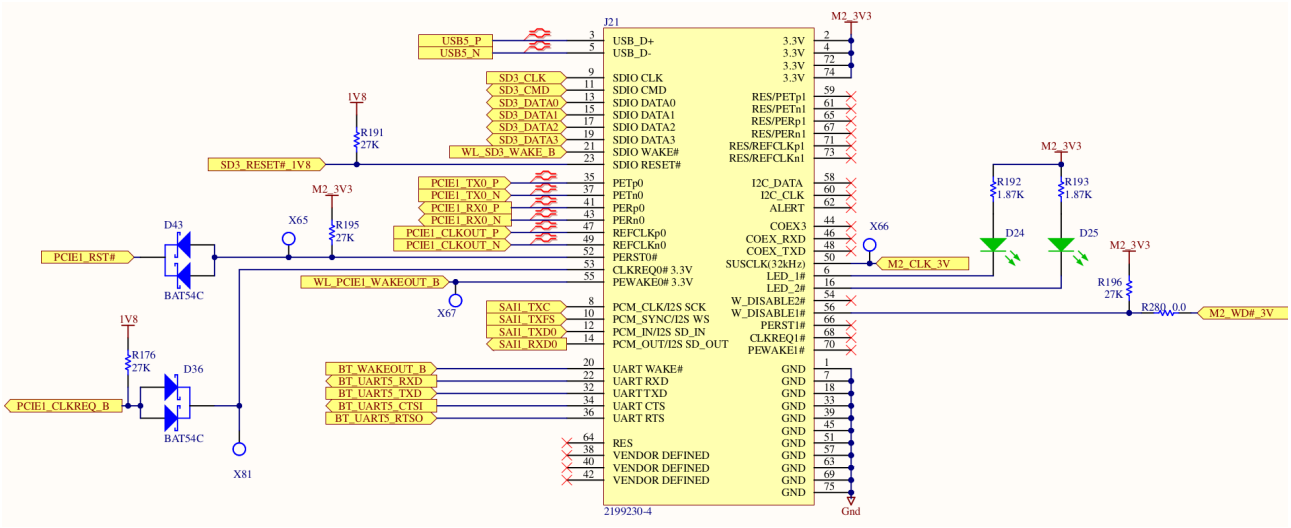
Figure 45: 2x USB Type-A 2.0 Host ports Hub (J17)



2.18 Wi-Fi and Bluetooth

2.18.1 M.2 Connector – Maya-W2 (J21)

Figure 46: M.2 Connector – Maya-W2 (J21)



3 Device Status

3.1 LEDs

Figure 47: Indicators LEDs

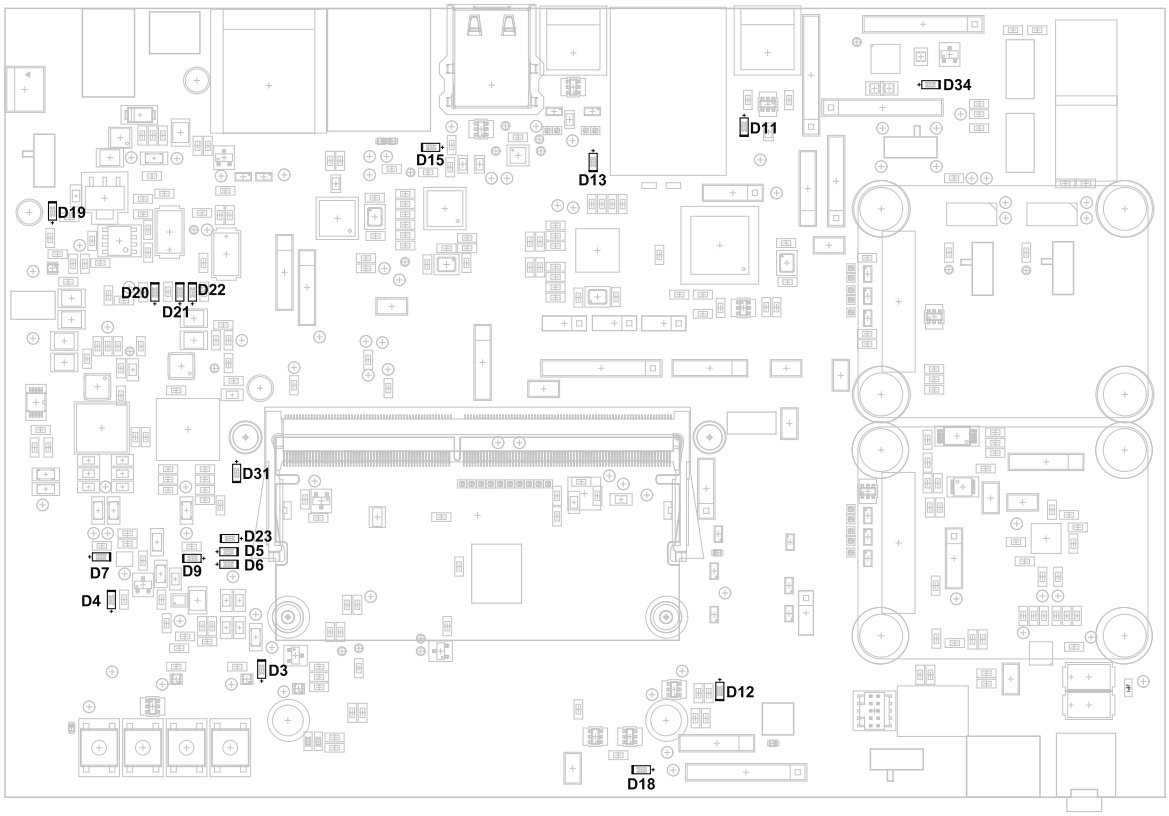


Table 29: Indicators LEDs

Designator	Color	Description
D3	Green	LED is lit when the board is powered on with SoM
D4	Green	LED is lit when the board is powered on with SoM
D5	Green	LED is lit when peripherals power is enabled
D6	Red	LED is lit when sleep mode is active and peripherals power is disabled
D7	Green	LED is lit when the board is powered on with SoM
D9	Green	LED is lit when the board is powered on with SoM
D11	Green	LED is lit when USB Debugger connected to the PC
D12	Green	LED is lit when MicroSD Card power is ON
D13	Green	LED is lit when USB1-OTG port power is ON (Connector J5)
D15	Green	LED is lit when USB 2.0 Host port power is ON (Connector J17)
D18	Green	LED is lit when 10 Gbit Ethernet PMIC is ON

Continued on next page

Table 29: Indicators LEDs (Continued)

Designator	Color	Description
D19	Green	LED is lit when Mini PCIe connector power is ON
D20	Green	Mini PCIe status indicator: WWAN. (Indication depend on the installed card)
D21	Green	Mini PCIe status indicator: WLAN. (Indication depend on the installed card)
D22	Green	Mini PCIe status indicator: WPAN. (Indication depend on the installed card)
D23	Green	LED is lit when M.2 Maya-W2 Wifi Connector power is ON
D31	Red	LED is lit when module is in reset state
D34	Green	LED is lit when using IO Expander (Connector J42)

4 Technical Specifications

4.1 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website[3].

4.2 Sockets for Verdin Modules

The Verdin module uses the SODIMM DDR4 memory module edge connector. This connector has 260 pins and is available from different manufacturers in various stacking heights from 4mm to 9.2mm. Toradex recommends using the TE Connectivity 2309409-2 with a stacking height of 5.2mm, which provides a board-to-board distance of 2.62mm.

A list of other SODIMM DDR4 connector manufacturers is given below:

Amphenol:
https://www.amphenol-icc.com/product-series/ddr4-so-dimm.html

TE Connectivity:
https://www.te.com/usa-en/products/connectors/card-socket-connectors/memory-sockets.html

[3] https://www.toradex.com/support/product-compliance

5 Device and Documentation Support

5.1 Trademarks

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