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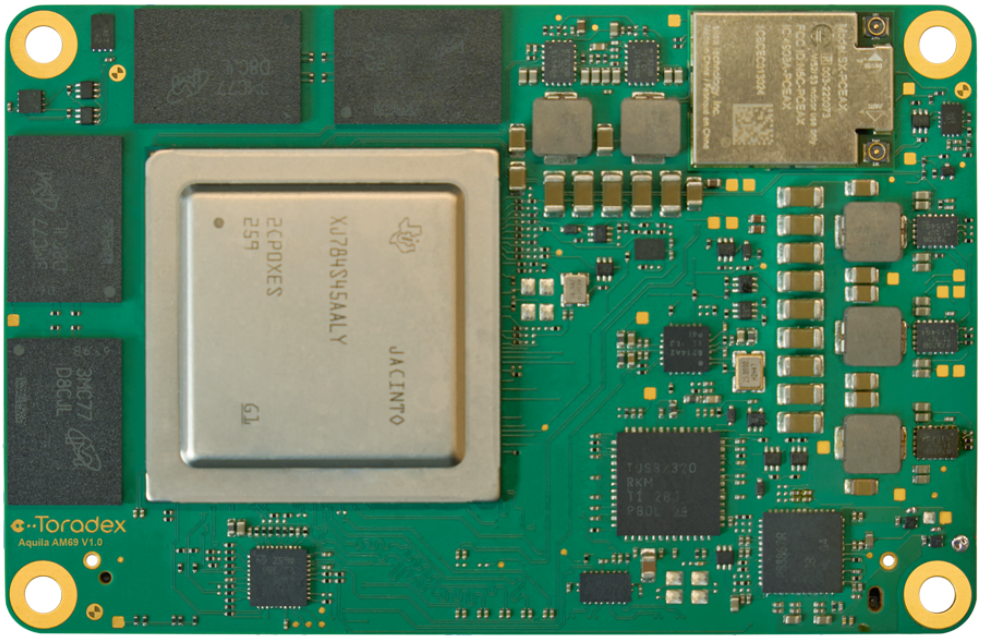
Aquila Family Specification



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
13-Sep-2024	Rev. 1.0	V1.0	Initial documentation

Contents

1 Introduction

1.1 Overview

This document is a specification that defines the Aquila Computer-on-Module family (referred to hereafter as “module”). It defines the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also defines the mechanical form factor, including key dimensions and possible thermal solutions.

1.2 Motivations

The following motivations are central to the definition of the Aquila family specification.

1. The Aquila Family unlocks new possibilities for artificial intelligence and computer vision applications and is a perfect fit for demanding verticals like robotics, and Industrial PCs.
2. It is designed for high-performance applications, capable of dealing with computationally intensive, demanding workloads. It is engineered with rugged durability and it has an industrial form factor.
3. Compared to x86 devices and other proprietary GPU-accelerated software, the Aquila family offers similar performance for a lower cost, being also more power-efficient.
4. Its architecture is designed to support and host a wide range of System-on-Chips (SoCs).
5. It also provides an increased CPU, GPU, NPU, and ISP performance.
6. It offers a modern, rich, future-proof feature set. With high-speed interfaces such as Gigabit Ethernet, SGMII, and PCIe, the Aquila family is ready to power next gen’s AI.
7. Based on a robust and reliable, high-performance board-to-board connector solution featuring 400 pins.
8. Following market trends, the regular I/O pins of the Aquila family modules have a logic voltage level of 1.8V, which reduces the power consumption of the overall system.
9. Using the Direct Breakout™ feature, the Aquila family encapsulates the complexities associated with cutting-edge electronic design, enabling and supporting the development and manufacturing of simple and cost-efficient carrier boards.
10. It also has integrated and modular thermal solutions addressing various use cases.

2 Module Overview

2.1 Interface Compatibility Classes

The interfaces of the Aquila modules are split into three distinct groups: “Always Compatible”, “Reserved”, and “Module-specific”.

“Always Compatible” interfaces are features that shall be present on each SoM in the Aquila Family. Customers can expect upgradeability and maximum scalability.

“Reserved” interfaces are features that are defined and reserved but possibly missing on some SoMs. The reason for that could be that certain SoCs do not feature an interface, or there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means that any Aquila SoM can be inserted into any Aquila carrier board without risking damage caused by incompatible reserved pins.

A “Module-specific” interface is a feature that is not guaranteed to be functionally or electrically compatible between modules. Different Aquila modules may provide various functionalities on the same sets of “Module-specific” pins. If a carrier board design relies on such features, the selection of Aquila modules suitable for being used with that particular carrier board design may be limited. An incompatible SoM/carrier board combination may disable all functionalities or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

2.1.1 “Always Compatible” Interfaces

The table in Figure 1 shows the interfaces that are provided by every Aquila module. The “GPIO Capable” column indicates whether the assigned pins can be used as GPIOs. The “Instances” column indicates the number of interfaces that the Aquila specification guarantees to be present for the “Always Compatible” interfaces. Customers should consult the datasheet for specific Aquila module variants to check for special features or restrictions on interfaces.

Table 1: Always Compatible Interfaces

Description	Instances	Name	Note	GPIO Capable
Gigabit Ethernet	1	ETH_1	Media-dependent interface (PHY on module), backward compatible with Fast Ethernet.	No
USB 2.0 Host	1	USB_2	High-Speed USB, backward compatible with Full and Low-Speed USB.	No
USB 2.0 DRP	1	USB_1	Can be configured for host or client usage. SoC usually uses this port in recovery mode.	No
PCIe (1x Lane)	1	PCIe_1	1 lane with reference clock. Supported PCIe generation depends on the module	No
I2C	1	I2C_1	Reserved for USB-C PD (might be usable as general purpose I2C)	Yes*
I2C / I3C	1	I2C_2	General Purpose. For some devices it can support also the I3C mode	Yes*
SPI	1	SPI_1	General Purpose, single CS pin	Yes*
SDIO	1	SD_1	4-bit interface, I/O voltage might be switchable between 1.8V and 3.3V for UHS-I support	Yes*
UART (RX, TX)	2	UART_1 UART_2	General Purpose	Yes*
UART (RX, TX)	1	UART_3	Primary operating system debug port (console)	Yes*
PWM	2	PWM_1 PWM_2	General Purpose	Yes*
GPIO	8	GPIO_1..8	General Purpose	Yes*
JTAG	1	JTAG_1		Yes*

2.1.2 “Reserved” Interfaces

Some of the “Reserved” interfaces are extending the functionality of an “Always Compatible” interface. For example, the additional USB 3.x SuperSpeed signals in the “Reserved” class must be used in conjunction with the USB 2.0 Host interface signals. There are additional RTS/CTS hardware flow control signals that need to be used in conjunction with the respective general-purpose UART that is in the “Always Compatible” class. Since the “Reserved” interfaces are possibly missing on some SoCs, it is mandatory to consult the module datasheet for further information. A useful tool is the Toradex Pinout Designer, which can help to compare the available features of different Aquila modules.

Table 2: Reserved Interfaces

Description	Instances	Name	Note	GPIO Capable
MIPI	1	DSI_1	DSI Display Interface	No
DP	1	DP_1	Display Port Interface	No
SGMII / USXGMII	1	ETH_2_XGMII	Depending on the device it can be 2.5Gb or 10Gb compatible	No
USB 3.x Host 2x2	1	USB_1	USB Super Speed signals 2x Lanes	No
USB 3.x Host	1	USB_2	Additional USB Super Speed 1x Lane	No
PCIe	1	PCIE_1	These lines extend the PCIE_1 (always compatible) with additional second lane	No
PCIe x2	1	PCIe_2	1 lane or 2 lanes with reference clock. Supported PCIe generation depends on the module	No
I2C	4	I2C_3_DSI1 I2C_4_CSI1 I2C_5_CSI2 I2C_6	1x Reserved for DSI (might be usable as general purpose I2C) 1x Reserved for CSI_1 (might be usable as general purpose I2C) 1x Reserved for CSI_2 (might be usable as general purpose I2C) General Purpose	Yes*
SPI	1	SPI_2	General Purpose, single CS pin	Yes*
QSPI / OSPI	1	QSPI_1	The related software drivers may prevent this interface from being used as a regular SPI interface. OSPI / QSPI support depend on the device	Yes*
UART (RX, TX)	1	UART_4	Secondary operating system (real-time OS) debug port. It might be usable as general purpose UART.	Yes*
UART (RTS, CTS)	2	UART_1 UART_2	Complementary hardware flow control signals for the fully compatible general purpose UART interfaces	Yes*
CAN	4	CAN_1 CAN_2 CAN_3 CAN_4	CAN or CAN FD compatible	Yes*
MIPI CSI	2	CSI_1 CSI_2	Up to 4 data lanes each	No
PWM	2	PWM_1_DSI PWM_4_DP	1x Reserved for DSI backlight control 1x Reserved for DP backlight control	Yes*
I2S	2	I2S_1 I2S_2	1x With master clock output 1x Without master clock output	Yes*
ADC	4	ADC_1..4		Yes*

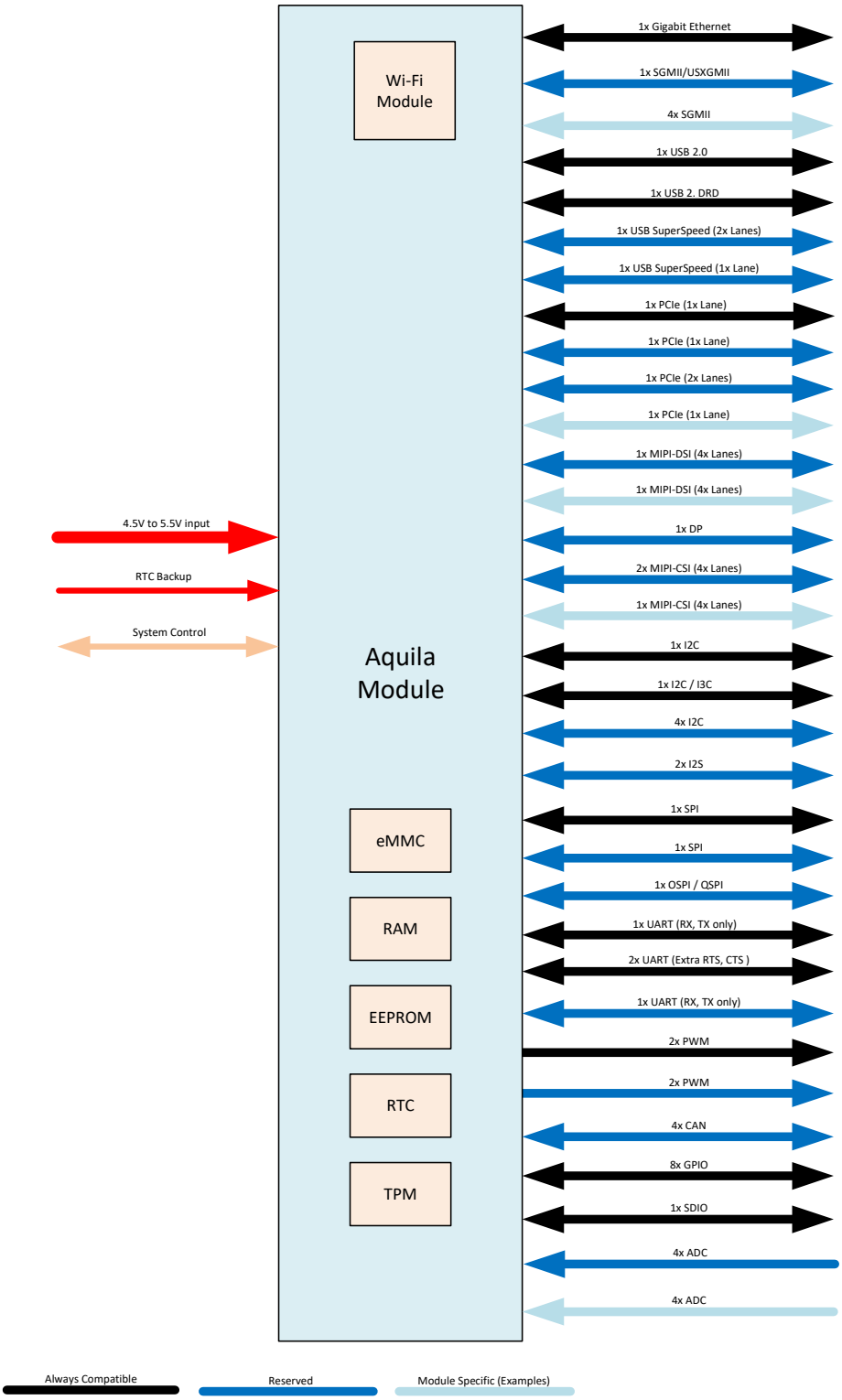
2.1.3 “Module-specific” Interfaces

”Module-specific” interfaces allow for the possibility of including interfaces that may not be widely adopted (yet) or interfaces that may be specific to a particular device or groups of devices. The concept provides a mechanism for extending features that are present on ”Always Compatible” or “Reserved” pins, e.g., providing additional PCI-Express lanes. It should be noted that Toradex does its best to keep “Module-specific” interfaces standard across modules that share such interfaces. For example, suppose both module A and module B have an LVDS interface available in the same configuration as a “Module-specific” interface. In that case, it is a priority to assign them to the same pins in the “Module-specific” area of the connector. Hence, both module A and module B would ideally share compatibility between this part of the “Module- specific” interface.

2.2 Architecture

The block diagram in Figure 3 shows the basic architecture of the Aquila module, depicting the “Always Compatible” interfaces, “Reserved” interfaces, and some examples of “Module-specific” interfaces.

Figure 1: Block Diagram



2.3 Module and Carrier Board Compatibility

To ensure that any carrier board design is compatible with all Aquila modules, only the standard functions of the "Always Compatible" and "Reserved" interfaces should be used. Alternate functions are not guaranteed to be compatible. Special care must be taken with the "Module-specific" signals. The "Module-specific" signals might be electrically incompatible between different Aquila modules. This means that the system might not work, and this may result in damage done to the module or the carrier board.

The Toradex Pinout Designer tool can be used for comparing available features and interfaces of different Aquila modules. Make sure to enable the note fields in the viewing options to get additional information. Even though the Pinout Designer is a very powerful tool, it is still recommended to read the datasheets of the different Aquila modules to check the functional and electrical compatibility of the interfaces/pins.

Check interface specifications when using "Module specific" interfaces
If a custom carrier board implements any "Module-specific" interfaces, it may not be 100% compatible with all Aquila modules. Where "Module-specific" interfaces are common between different Aquila modules, they shall be provided on the same pins where possible. Therefore, designs that make use of the "Module-specific" interfaces of a specific Aquila module may be compatible with other Aquila modules – please check the interface specifications of individual Aquila modules carefully.

3 Interface Specifications

3.1 Signal Naming Convention

Identical signals of different interfaces are distinguished by adding the interface index as a suffix (e.g., PWM_1, PWM_2, etc.). Interface indexing usually starts at one. Signals named after a standard or follow a widely acknowledged common naming convention (such as the Ethernet or LVDS interfaces) may use a zero-based index. Differential pair signal components are suffixed with either a "P" (for positive) or "N" (for negative). Active low signals are suffixed with a "#". The underscore ("_") is used as a separator to delimit fragments of the signal name (such as signal group, channel, and signal descriptor components) to make the signal name easy to read and interpret.

3.2 Standard Interfaces

Aquila standard interfaces are the common name for the "Always Compatible" and "Reserved" interfaces. Toradex Pinout Designer eases the configuration of standard interfaces to facilitate the development process.

3.2.1 Gigabit Ethernet

The gigabit Ethernet port is a media-dependent interface for 10/100/1000 Mbit Ethernet. The PHY is located on the module. Therefore, only the magnetics are required on the carrier board. The signals between the PHY and the magnetics operate in the "voltage" mode. This means there is no center tap voltage required.

3.2.2 SGMII / USXGMII

Serial Gigabit Media-Independent Interface allows the use of an additional Ethernet PHY on the Carrier Board. Depending on the SoC used it can support 1Gb / 2.5Gb / 10Gb. This interface is "Reserved"

3.2.3 USB 2.0 DRD

The USB 2.0 DRD interface consists of a USB 2.0 High-Speed interface which is part of the "Always Compatible" interfaces. This interface is backward compatible with Full- and Low-Speed USB 2.0. This

port can be used as a host or client port. Modules may use this interface to flash the firmware in recovery mode.

In the “Reserved” section, there are additional USB_1 SuperSpeed signals (2L) used in combination with the USB 2.0 data signals to provide a USB 3.x capable interface. The actual supported USB 3.x generation and maximum transfer rate depend on the Aquila module.

3.2.4 USB 2.0 Host

The USB 2.0 Host interface consists of a USB 2.0 High-Speed interface which is part of the “Always Compatible” interfaces. This interface is backward compatible with Full- and Low-Speed USB 2.0.

In the “Reserved” section, there are additional USB_2 SuperSpeed signals (1L) used in combination with the USB 2.0 data signals to provide a USB 3.x capable interface. The actual supported USB 3.x generation and maximum transfer rate depend on the Aquila module.

3.2.5 USB-SuperSpeed

There are two USB-SS interfaces available in the “Reserved” class. USB_1 is a 2-lane interface with USB mux integrated into the module or directly into the SoC. It requires an additional USB-C controller on the carrier board for providing cable orientation data or link capabilities. The I2C_1 interface is reserved for communicating with this controller. USB_2 is a 1-lane USB-SS interface that can be used for a USB 3.0 port or to connect an external hub. Please check availability in the module documentation.

3.2.6 I2C

There are two general-purpose I2C interfaces in the “Always Compatible” section (depending on the Aquila module they may or may not support the I3C mode). There are an additional four I2C interfaces in the “Reserved” class. These interfaces are reserved for the DSI display and the CSI camera. If a module does not feature one of these interfaces, the related I2C interface may also be missing. Whenever possible, the reserved I2C interface should be used in combination with its related primary interface. Whether a reservedI2C can also be used as a general-purpose interface depends on the Aquila module. In certain configurations, I2C ports tied to DSI and CSI may be used for general communication. Please check the datasheets of Aquila SoMs to understand if these I2C interfaces can be used as general-purpose interfaces.

3.2.7 SPI

There is one SPI interface in the “Always Compatible” class. Additionally, there is one SPI interface in the “Reserved” class. Both of these interfaces feature a single chip select pin.

3.2.8 QSPI / OSPI

The QuadSPI interface might be used for interfacing external memory devices (e.g., NAND and NOR flashes). OctaSPI is available as an extension (additional data pins) to the QSPI interface. Please check the Aquila SoM datasheet for availability.

3.2.9 UART

There are four standard UARTs available on the Aquila module. UART_1 and UART_2 are general-purpose interfaces. The RX and TX signals of these interfaces are in the “Always Compatible” section. In contrast, the additional RTS/CTS signals for hardware flow control are located in the “Reserved” interfaces section.
UART_3 is in the “Always Compatible” section and is intended to be used for the main OS debug log output. It could be used for general purposes, but we strongly recommend making this interface available for debugging purposes. UART_4 is in the “Reserved” class. On modules with a real-time core,

the interface is intended to be used as the debug log output of the real-time operating system. The interface may be used as a general-purpose UART.

3.2.10 PWM

There are 4 PWM signals on the Aquila standard. PWM_1 and PWM_2 are in the “Always Compatible” class. PWM_1, as well as PWM_2, are general-purpose pulse width modulation outputs. The third interface, PWM_3_DSI, is reserved for the DSI interface (for display backlight inverter control) and PWM_4_DP is reserved for the DP interface.

3.2.11 SDIO

The SDIO supports up to 4 data bits. Attention must be taken to the I/O voltage of this interface. To comply with the SD memory card specifications, the I/O pins can run with 3.3V. Aquila modules might integrate UHS-I modes in which the voltage is switched to 1.8V during card initialization. There is no need for pull-up resistors on the carrier board for the SDIO signals (CMD, DATAx, and CLK). Either the SoC has integrated pull-up resistors, or they are located on the module PCB.

3.2.12 MIPI DSI

The DSI interface supports up to four data lanes. The supported maximum DSI transfer rate depends on the module.

3.2.13 DP

DisplayPort availability depends on the SoM used in the Aquila module.

3.2.14 PCIe

PCIe_1 interface is 1-lane and it is the only one in the “Always Compatible” class. Additionally, it can be complemented with a second lane (PCIe_1.1) from the “Reserved” class - depending on the availability (please check SoM documentation). There is also a second PCIe interface in the reserved class, available depending on the SoM used (it can be either x1L or x2L). All interfaces include a 100MHz reference clock. The supported PCIe generation (interface speed) depends on the module.

3.2.15 CAN

There are up to four Controller Area Network interfaces available on Aquila modules. Depending on the particular module, besides CAN, CAN FD (flexible data rate) may be supported as well.

3.2.16 MIPI-CSI-2

There are two MIPI CSI-2 camera interfaces in the “Reserved” class with up to 4 data lanes. The supported interface speed and maximum resolution depend on the module.

3.2.17 ADC

There are four ADC inputs in the “Reserved” class. The inputs shall have at least an 8-bit resolution and an input voltage range of 0V to 1.8V.

3.2.18 JTAG

Depending on the module, the JTAG interface may be used for debugging purposes or boundary-scan testing in production. Even though the nominal I/O voltage of the JTAG pins is 1.8V, it is recommended to use the JTAG_1_VREF for the I/O voltage of the JTAG adapter. This offers more flexibility for Aquila modules with different JTAG I/O voltages.

3.3 "Module-specific" Interfaces

The "Module-specific" pins on the Aquila module may be used for allocating any types of interfaces not fitting in any of the "Always Compatible" and "Reserved" interfaces categories.

Do not use the module with an incompatible carrier board
Even the interface voltage depends on the module and could lead to malfunction if an Aquila module is used in an incompatible carrier board!

The "Module-specific" pins are allocated on the module edge connector in groups of five signals. Depending on the Aquila module, the pins may be used in different patterns. For example, if the 5 pins are used for a set of two differential pairs, the pin between the pairs can be connected to the ground on the module or might be used for low-speed signals. In this case, a stitching capacitor from the low-speed signal to GND on the module and the carrier board is recommended to provide a return path for the differential pair signals.

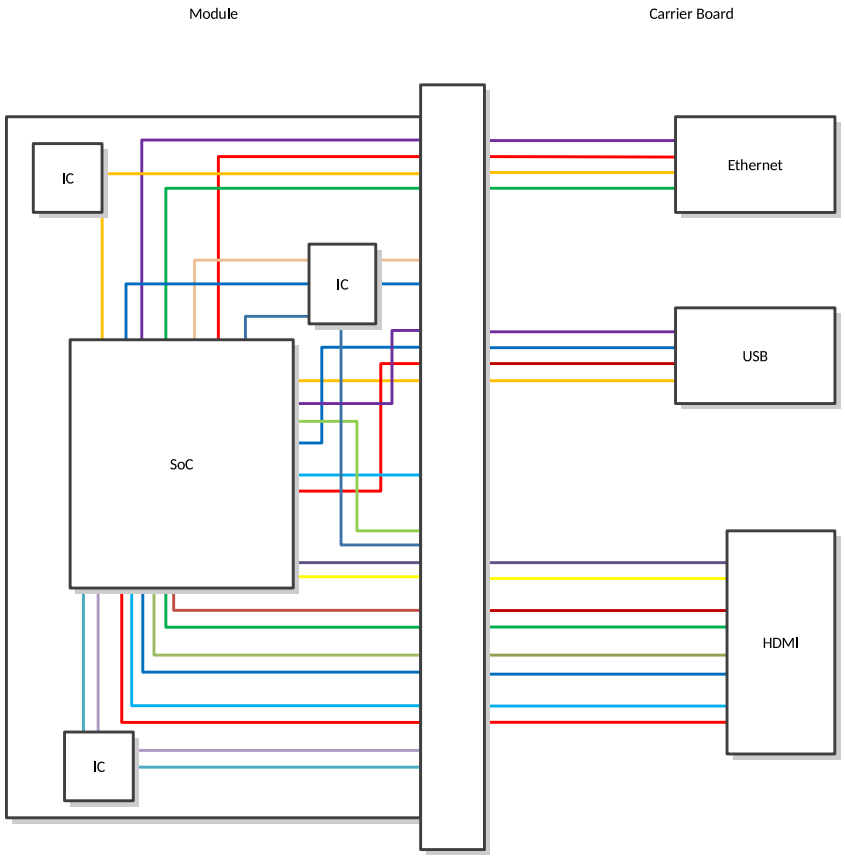
3.4 Physical Pin Definition and Location

The total number of usable pins on the module is 400. The ground pin count is 94 (23.5%). The main power supply (VCC) power pin count is 14.

3.5 Direct Breakout™

Direct Breakout™ aims to reduce the complexity of carrier board routing from the module connector to the real-world I/O ports by making it possible to route signals without traversing layers of crossing critical signals. Interfaces are physically grouped into functional "locations" on the board-to-board connector so that all signals associated with a specific interface are in one common location, reducing routing complexity. The pin order within an interface matches the pin order of commonly used connectors.

Figure 2: Direct Breakout Example



The image in Figure 5 shows the concept of a direct breakout by illustrating how complex routing and layout are encapsulated on the Aquila module, providing the potential for simple routing on the carrier board.

4 Mechanical Specifications

4.1 Overview

The Aquila module form factor mechanical dimensions have been specified based on careful analysis of required board space for typical device packages (SoC, memory ICs, power ICs, Wi-Fi module, and peripheral ICs) and certain key features. This has been balanced with the requirement to keep the form factor as small as reasonably possible. A single mechanical size has been defined.

4.2 Module Dimensions

All dimensions, if not otherwise noted, are in mm

Figure 3: Module dimensions top side (mm)

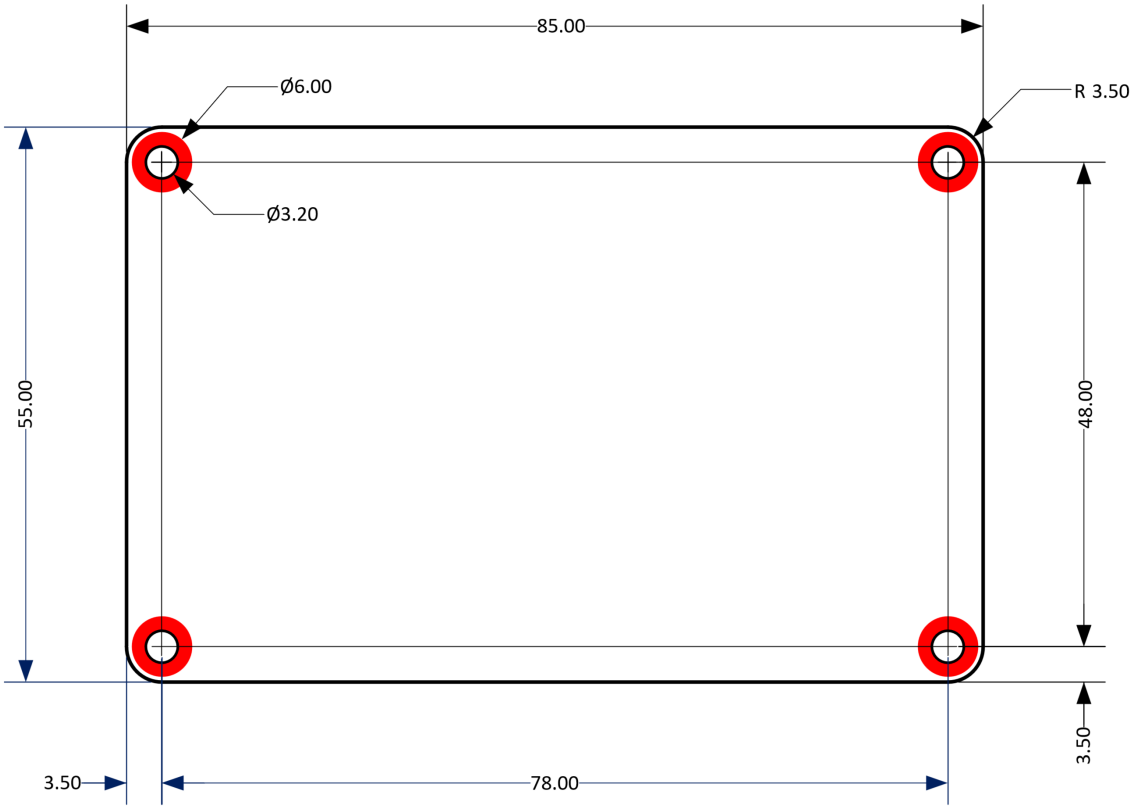
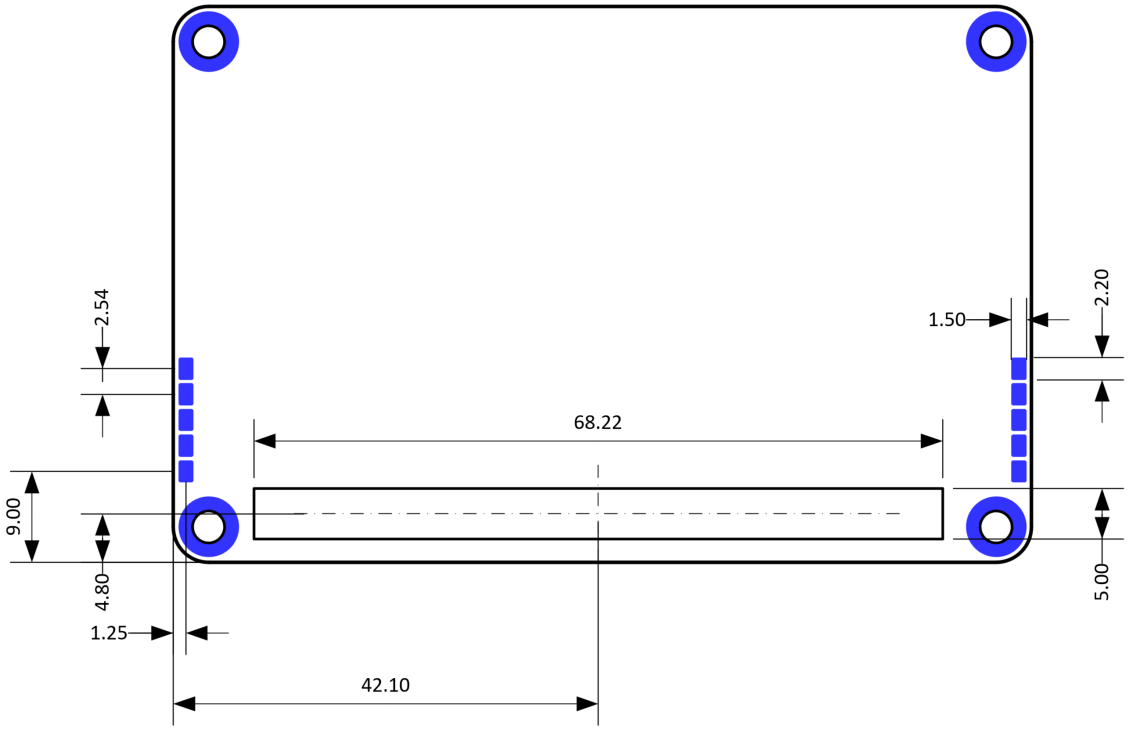


Figure 4: Module dimensions bottom side (mm)



4.3 Module Connector and Stacking Height

The Aquila modules use Samtec's Accelerate HP (High-Performance Array) Board-to-Board connector, for state-of-the-art robustness and reliability. This connector has 400 pins in a 100×4 organization with a 0.635mm pitch.

Please refer to the table below for the part numbers:

Table 3: Board-to-Board Connector Models

PN (Module Side)	Solder Balls	Remarks
Samtec APF6-100-03.5-L-04-0-A-FR	No	
Samtec APF6-100-03.5-L-04-2-TR	Yes	No alignment Pins

Mating parts for the Carrier side can have two stacking height options:

- 5mm stacking height
- 10mm stacking height

Table 4: Mating parts for the Carrier Side

PN(Carrier Side)	Solder Balls	Remarks	
Samtec APM6-100-01.5-L-04-0-A-FR	No		5mm stacking height
Samtec APM6-100-01.5-L-04-2-TR	Yes	No alignment Pins	5mm stacking height
Samtec APM6-100-06.5-L-04-0-A-FR	No		10mm stacking height
Samtec APM6-100-06.5-L-04-2-TR	Yes	No alignment Pins	10mm stacking height

The above PNs indicate 10um gold contacts. For 30um gold please change the -L- option to -S-

The following table compares the different mating parts options. The connector height is the stacking height of the connector. The board-to-board distance is the nominal space between the carrier board and the module. Please note that in worst-case situations, this distance can be smaller. The column "Component Height Carrier Board" indicates the recommended maximum height of components underneath the module.

Table 5: Connector stacking height

Connector height	Board-to-board distance	Component Height Carrier Board	Remarks
5 mm	5 mm	2mm	Recommended stacking height for Aquila modules

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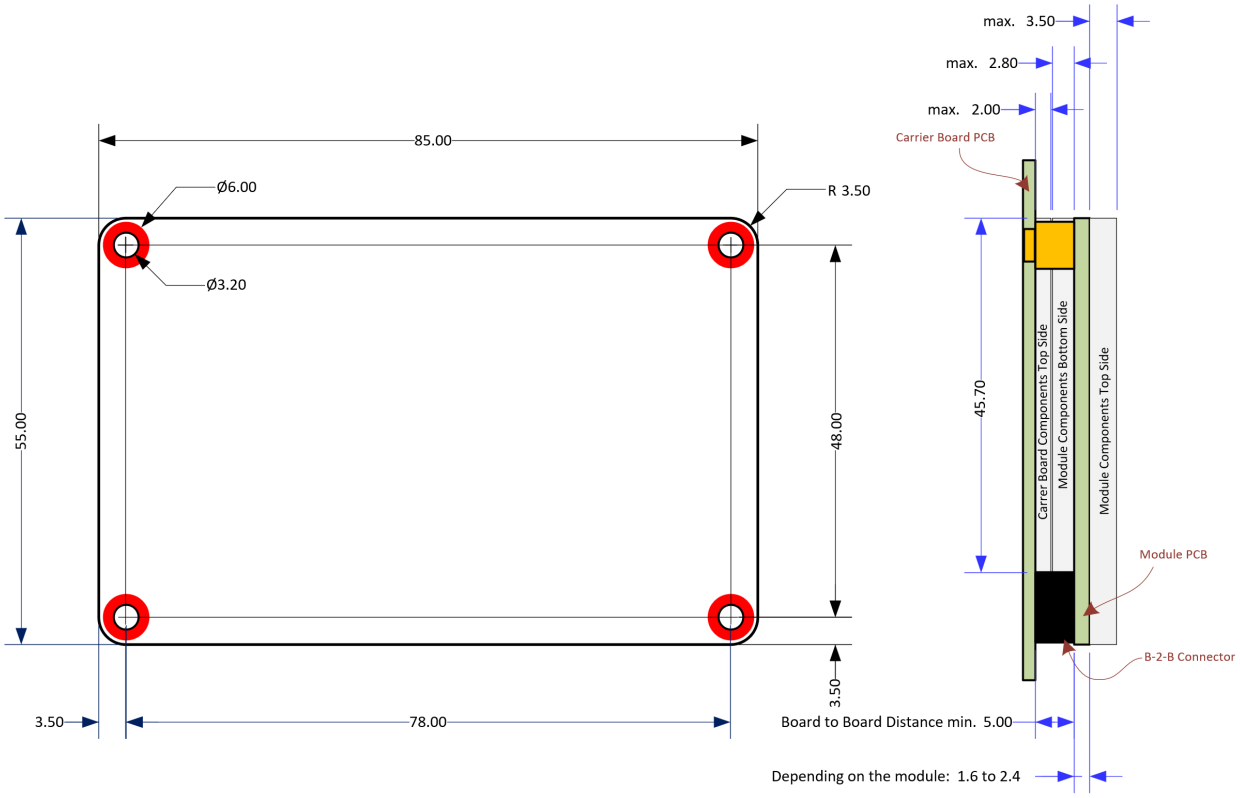
Table 5: Connector stacking height (Continued)

Connector height	Board-to-board distance	Component Height Carrier Board	Remarks
10 mm	10 mm	8mm	Recommended for special cases where high components under the module are required

Even if a module does not use up all the component height allowance, it is advisable not to squeeze in additional components between the module and the carrier board. Reserving the complete component height to the module guarantees mechanical compatibility with existing and future Aquila modules and module versions. If components need to be placed underneath the module, a connector with a larger stacking height is recommended.

Figure 5: Stacking Height



4.4 Fixation of the Module

TBA

4.5 Thermal Solution

TBA

4.6 Connector and Standoff Land Pattern

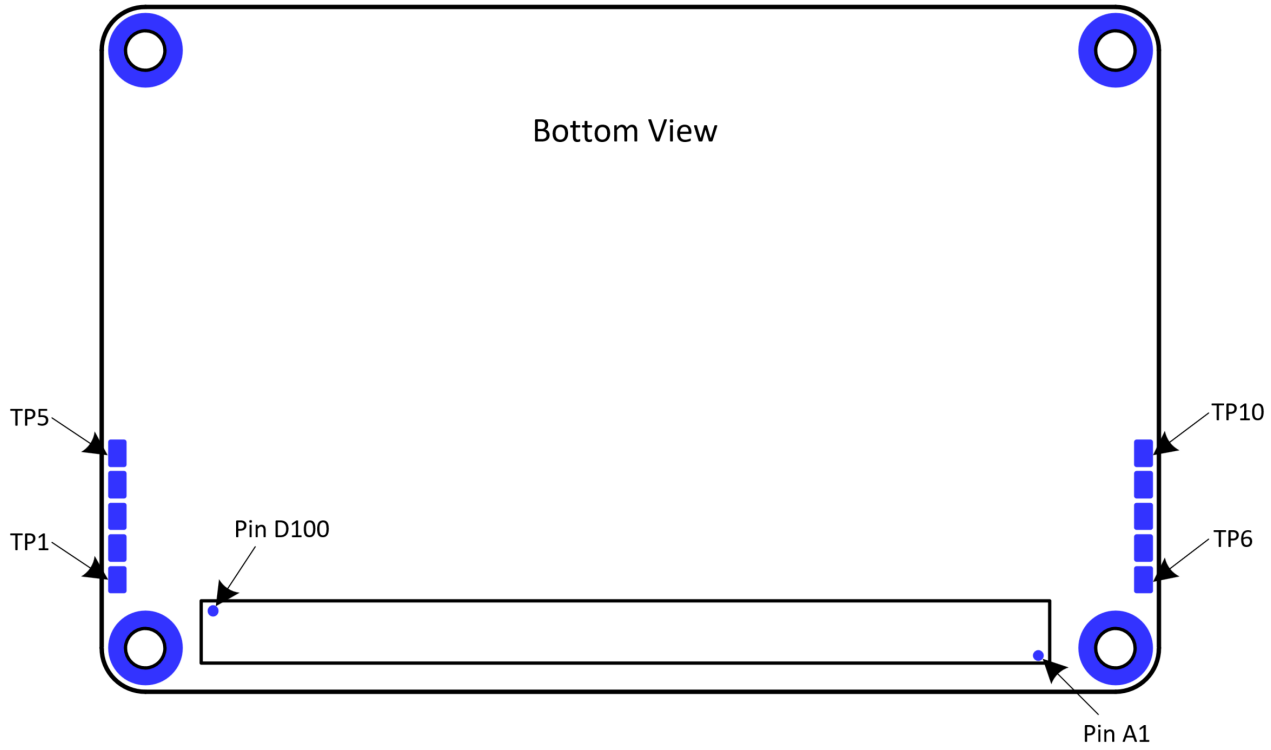
TBA

4.7 Carrier Board Space Requirements

Every Aquila module provides 10 test points on the module PCB's bottom side, as shown in the figure above. The test points are split into groups of 5 pads. Each set is symmetrical about the centered Y-axis (the Y plane is orthogonal to the connector edge).
The test points are "Module-specific" pins. The signals connected to these test points are defined for each Aquila module for factory testing purposes. Customer carrier boards shall leave these pads unconnected.

4.8 Pin Numbering

Figure 6: Pin Numbering



4.8.1 Generic Test Point Interfaces

Every Aquila module provides 10 test points on the module PCB's bottom side, as shown in the figure above. The test points are split into groups of 5 pads. Each set is symmetrical about the centered Y-axis (the Y plane is orthogonal to the connector edge).
The test points are "Module-specific" pins. The signals connected to these test points are defined for each Aquila module for factory testing purposes. Customer carrier boards shall leave these pads unconnected.

5 Electrical Specifications

5.1 Power Supplies

All Aquila modules are powered by a single voltage VCC and an optional low-current backup power supply for purposes such as Real Time Clock (RTC) support. The main power supply offers an input voltage of 5V ±10%. The Aquila form factor is specified for a maximum sustained power consumption of up to 26W and a maximum peak power consumption of up to 40W for the SoMs. Most of the GPIO-capable I/O pins run on a 1.8V logic level. The Aquila module provides a reference 1.8V output for the I/O rails (PWR_1V8_MOCI). The module provides up to 250mA on this pin. Carrier boards may use this module output rail directly as the only 1.8V supply for their peripherals. This saves complexity and costs on the carrier board. The carrier board needs to ensure that the maximum amount of current drawn from the PWR_1V8_MOCI output pin does not exceed 250mA. Drawing a higher current can lead to instability and damage to the module power supply.
Further carrier board power supply requirements (power rating, isolation, and decoupling, bulk capacitance, and characteristics such as ramp-up rate, etc.) are detailed in a separate carrier board design guide.

5.2 Power Supply and Power Management Signals

VCC is the only power supply required to be present for the module to become operational. Once VCC is present and is within specification, the module powers up and starts normal operation automatically. VCC_BACKUP is not required for the module to start normal operation. However, it is mandatory if the application requires features that rely on this supply being always on, such as the Real-Time Clock (RTC). Besides power supply pins, the Aquila module form factor supports several power-management signals. The signals are not mandatory to be used with carrier boards. However, they allow different power management schemes to be implemented on carrier boards: from a very simple approach to an advanced one with extra power-saving features.

For power management purposes, all Aquila modules feature the following system control signals:

Table 6: Power Management Control Signals

Aquila Pin	Aquila Signal Name	I	O	Type	Power Rail	Description
D5	CTRL_RESET_MOCI#		O	OD	3.3V Tolerant	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# does not get asserted. The output is an open-drain type without a pull-up resistor on the module. The signal is 3.3V tolerant. The carrier board can pull the signal up to 1.8V or 3.3V. This signal can be left floating on carrier boards.
B95	CTRL_PWR_EN_MOCI		O	CMOS	1.8V	Enable signal for the power rails of the carrier board peripherals. This output remains high during sleep modes.
B92	CTRL_RESET_MICO#	I		OD	1.8V	Open-drain input, which resets the module if shorted to ground on carrier board. There is a 100k on-module pull-up to the 1.8V STBY rail present. This means that this signal can be left floating on carrier boards.
B93	CTRL_PWR_BTN_MICO#	I		OD	1.8V	Long pulling down (>5s*) is shutting down the module. Short pulling down is turning on module from off-state. Open-drain input with 100k pull-up resistor to the 1.8V STBY rail is on the module. This signal can be left floating on carrier boards. (* the actual minimum duration depends on the module)
B91	CTRL_RECOVERY_MICO#	I		OD	1.8V	Shorting to the ground during power-up is setting the module into recovery mode. There is a 10k pull-up on the module. This signal can be left floating on carrier boards.

Continued on next page

Table 6: Power Management Control Signals (Continued)

Aquila Pin	Aquila Signal Name	I	O	Type	Power Rail	Description
D6	CTRL_WAKE1_MICO#	I		CMOS	1.8V	Wake capable pin, which allows resuming from sleep mode.There are no pull resistors on the module. The signal can be left floating on carrier boards if the wake feature is disabled in the software.
B94	CTRL_FORCE_OFF_MOCI#		O	OD	5V Tolerant	Output for forcing the turning-off of the main power rail. This signal needs to be blanked (ignored) for the first 400ms during the power-up sequence. The output is an open-drain type without a pull-up resistor on the module. The signal is 5V tolerant. The carrier board can pull the signal up to 1.8V, 3.3V, or 5V. This signal can be left floating on carrier boards.
C14	CTRL_TAMPER0					
C15	CTRL_TAMPER1					

To make the direction of the power management signals clear, the ending MICO or MOCI is appended to the signal names. MICO is the abbreviation for “Module Input, Carrier board Output,” while MOCI stands for “Module Output, Carrier board Input”. In general, every Aquila module shall start booting if the main power rail is applied. Most of the system control signals are optional to be used on the carrier board. The power management features of Aquila modules provide great flexibility and may support different carrier board power scenarios.
Detailed information on the possible carrier board power management schemes, power management states, and power up and down sequences can be found in the carrier board design guide.

5.3 Module Power Management States

Aquila modules support different power states. The following table describes what the various states mean. Depending on the carrier board power supply use case, some of the states may not be available.

Table 7: Power Management States

Name	Description
No VCC	The main VCC power rail is no applied to the module. The VCC_BACKUP is maybe available for keeping the RTC running. The CTRL_PWR_EN_MOCI and CTRL_SLEEP_MOCI# are both low to make sure no peripheral rails on the carrier board are enabled. CTRL_RESET_MOCI# and CTRL_FORCE_OFF_MOCI# are undefined. They can be high-z or driven low in this state.
Running	The module is running. Some unused module or carrier board peripherals maybe are switched off.
Reset	The module and the peripheral devices are in the reset state. The preferred reset mode is a “cold reset”. This means the PMIC shuts down all the rails on the module and drives the CTRL_PWR_EN_MOCI and CTRL_SLEEP_MOCI# low to turn off also the carrier board rails. Some modules may implement a “warm reset” instead. In this reset state, the rails on the module, including CTRL_PWR_EN_MOCI, are kept up and running while only the reset signals are asserted. The Aquila module datasheet contains information on which type of reset is implemented by the module. If the CTRL_RESET_MICO# is low, the module is kept in the reset mode. This allows the carrier board to prolong the reset cycle
Sleep	The CPU is in a low power suspend state. The peripherals on the module are either turned off or are put in a sleep state. The module can be woken up by an RTC event, a wake capable on-module peripherals, the CTRL_PWR_BTN_MICO# (power button), the CTRL_WAKE1_MICO#, or a wake-enabled GPIO (depending on the module).
Module OFF	The PMIC on the module has shut down all the power rails, but the VCC is still applied to the module. CTRL_PWR_EN_MOCI and CTRL_RESET_MOCI# are all set low to turn off peripheral power rails on the carrier board. The CTRL_FORCE_OFF_MOCI# output is also low. It depends on the carrier board power supply scheme whether this causes the module to stay in the “Module OFF” state or the VCC is removed, which means the module goes into “No VCC” mode. The power consumption of the module is in this state is very low. The VCC rail is only used for keeping the power management circuits and the RTC on. The actual consumption can be found in the datasheet of the Aquila module.

The module automatically transitions to the running mode when the VCC main power rail is applied to the module. In other words, all Aquila modules are ramping up the power rails and boot the system whenever the VCC is applied.

The CTRL_PWR_BTN_MICO# allows implementing a power button behavior like the ones used on regular personal computers and smartphones. Short pressing the power button is powering up the system from the “Module OFF” state or wakes the system from the sleep state. If the module is running, short pressing the power button generates a software interrupt. Depending on the operating system settings, this starts a software shutdown or opens a menu that lets the customer decide what to do. Pressing the power button longer than 5 seconds shuts down the system immediately (without software interaction).

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