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Verdin AM62 V1.2

HW Datasheet

Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
11-Sep-2023	Rev. 0.1	V1.1	Initial release
06-Mar-2024	Rev. 0.2	V1.1	Cover: Update product picture. Section 1.5.4: Add RAM controllers, channels, and bits. Section 1.5.3: Remove restriction on MCUSS peripherals. Section 1.7: Remove "Product Compliance" as it is better described in Section 9.2. Section 1.7: Add "Enabing Low Power" TI White Paper. Section 2.1: Remove non-existent connections. Section 3.2: Update pin assignment tables (Table 9 and Table 10). Section 4.2.2: Add signal multiplexer note. Section 5.2: Add Display section. Section 5.3: Add eFuse section. Section 5.4.1: Add GPIO wakeup section. Section 5.5: Rename section from Power Signals to Power. Section 5.5.1: Add Digital Supply section. Section 5.5.2: Add Analog Supply section. Section 5.5.3: Add Power Management Signals section. Section 5.6: Add Wi-Fi and Bluetooth section. Section 6: Add Low Power Modes section. Section 9.6: Fix missing section heading (Mechanical Characteristics). Improve admonitions. Minor changes.
26-Feb-2025	Rev. 0.3	V1.2	Section 1.2: Update Verdin family description. Section 1.5.1: Update SoC for Verdin AM62 Solo 512MB WB IT and Verdin AM62 Solo 512MB WB in Table 1. Section 1.5.4: Remove EEPROM Bus Speed from Table 4. Section 1.6: Add 1.8V limitation to one of the SD/MMC/SDIO interfaces in Table 7. Section 3.2: Add capacitor information to pin 92 in Table 10. Section 3.2: Add SoC connections to pins 172 and 174 in Table 10. Section 3.2: Remove pin 174 PCM_MCLK signal for Verdin AM62 revision 1.2 in Table 10. Section 3.2: Move NC entries from SoC ball name column to Non-SoC ball name column in Table 10. Section 4.2: Update abbreviations listed in Table 11. Section 4.2.1: Add pins 172 and 174 to Table 12. Section 4.2.1: Add color for boot source pin identification (pins 172 and 174) to Table 12. Section 4.2.1: Update color for module-specific interface identification in Table 12. Section 5: Add ADC section. Section 5.2.1: Update description of color depth modes. Section 5.2.1: Update pin 17 description in Table 16. Section 5.2.1: Update REFCLK signal in Table 18. Section 5.2.1: Fix DSI bridge I2C wrongly described as Display I2C in Table 18. Section 5.6: Remove pin 174 PCM_MCLK signal for Verdin AM62 revision 1.2 in Table 27. Section 9.7: Update maximum junction temperature for Verdin AM62 Solo 512MB from 105°C to 95°C in Table 36. Minor changes.

Contents

1 Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the Verdin AM62. For information on the actual features supported by software, please refer to the relevant SoM product page on the Toradex Developer website:

https://developer.toradex.com/hardware/verdin-som-family/modules/verdin-am62

1.2 Verdin SoM Family

The Verdin System on Module (SoM) family eliminates much of the complexity associated with modern-day electronic design. Complicated circuitry such as high-speed impedance-controlled layouts with high component density is encapsulated on the SoM. This allows the customer to create a carrier board that focuses solely on application-specific electronics, making the project substantially less complex.

The Verdin module takes this one step further and implements an interface pinout that allows direct connection of real-world I/O ports without the need to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high-speed serial technologies that require impedance-controlled differential pairs. Direct Breakout™ allows them to easily route such interfaces to common connectors in a simple, robust fashion.

The Verdin SoM features a wide input voltage range that allows it to be powered from a broad range of power sources (e.g., directly from a USB power supply or a single lithium cell). Due to increasing transistor density and the need for more power-efficient devices, the I/O voltage level is trending to decrease from 3.3V to 1.8V. For this reason, the Verdin family of SoMs supports a 1.8V I/O voltage level only. Both the wide input voltage range and the 1.8V I/O voltage make the power supply designs for a Verdin carrier board simple, easy, and cost-efficient. These features altogether make the Verdin family of SoMs perfectly suited for battery-powered applications as well.

1.3 TI AM62x Sitara SoC

The Verdin AM62 SoM is based on the Texas Instruments AM62x Sitara™ family of System on Chips (SoCs). The TI AM62x family consists of the AM625 and AM623 SoCs. The AM62x family features up to four Cortex®-A53 (often shortened to A53) cores as the main processor cluster. The cores provide complete 64-bit Arm®v8-A support while maintaining seamless backward compatibility with 32-bit Arm®v7-A software. The A53 cores run at up to 1.4GHz and feature improved integer operations, floating-point unit (FPU), and Arm® Neon™ SIMD extension.

In addition to the main CPU complex, the AM62x also offers a Cortex®-M4F (often shortened to M4F) processor designed to meet SIL-2 safety requirements. The M4F runs at up to 400MHz and may be used to run safety tasks or as a general-purpose MCU. This heterogeneous multicore system allows for running additional real-time operating systems for time- and security-critical tasks.

The SoC features a Programmable Real-time Unit Subsystem (PRUSS) with two 32-bit load/store RISC cores with a deterministic instruction set. Each core has an Interrupt Controller and access to some peripherals and I/O pins, providing flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The AM62x family features inline ECC (error-correcting code) for the LPDDR4 DRAM for high system reliability and safety.

The AM625 SoC features the *PowerVR Rogue AXE-1-16M* graphics processing unit (GPU) from Imagination Technologies. The GPU is capable of up to 16GFLOPs and supports OpenGL® ES 3.1 and Vulkan® 1.2.

1.4 Verdin AM62 SoM

The Verdin AM62 targets a wide range of applications, including Industrial Automation, Medical, Transportation, Smart Cities, Test and Measurement, and many more.

The module offers a wide range of native interfaces ranging from simple GPIOs, industry-standard I2C, SPI, USB, CAN FD, and UART buses to MIPI CSI camera interfaces. An optional MIPI DSI display interface is available on some SoM configurations. The Verdin AM62 module features a Gigabit Ethernet PHY with IEEE1588 support on the module and a second Ethernet MAC with an RGMII interface for adding a Gigabit Ethernet PHY on the carrier board for dual Ethernet applications. The SoM is available with an optional Wi-Fi and Bluetooth interface.

1.5 Main Features

1.5.1 CPU

Table 1: CPU features

Parameter	Verdin AM62 Quad 2GB WB IT	Verdin AM62 Dual 1GB WB IT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB ET	Verdin AM62 Solo 512MB WB IT	Verdin AM62 Solo 512MB
SoC	AM6254xTCGHAALW	AM6252xTCGHAALW	AM6252xTCGHAALW	AM6232xTCGHAALW	AM6231xSGGHAALW	AM6231xKGGHHALW
A53 Cores	4	2	2	2	1	1
M4F Cores	1	1	1	1	1	1
CPU Clock	A53: 1.4GHz M4F: 400MHz	A53: 1.4GHz M4F: 400MHz	A53: 1.4GHz M4F: 400MHz	A53: 1.4GHz M4F: 400MHz	A53: 1.0GHz M4F: 400MHz	A53: 1.0GHz M4F: 400MHz
Security *HSM*	Yes	Yes	Yes	Yes	No	No
Neon SIMD	Yes	Yes	Yes	Yes	Yes	Yes
L1 Instruction Cache *per core*	A53: 32kB	A53: 32kB	A53: 32kB	A53: 32kB	A53: 32kB	A53: 32kB
L1 Data Cache *per core*	A53: 32kB	A53: 32kB	A53: 32kB	A53: 32kB	A53: 32kB	A53: 32kB
L2 Cache *shared*	A53: 512kB	A53: 512kB	A53: 512kB	A53: 512kB	A53: 512kB	A53: 512kB
Tightly Coupled Memory	M4F: 256kB	M4F: 256kB	M4F: 256kB	M4F: 256kB	M4F: 256kB	M4F: 256kB

1.5.2 GPU

Table 2: GPU features

Parameter	Verdin AM62 Quad 2GB WB IT	Verdin AM62 Dual 1GB WB IT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB ET	Verdin AM62 Solo 512MB WB IT	Verdin AM62 Solo 512MB
GPU	Yes	Yes	Yes	No	No	No
2D Acceleration	Yes	Yes	Yes	–	–	–
3D Acceleration	Yes	Yes	Yes	–	–	–
GPU Model	PowerVR Rogue AXE-1-16M	PowerVR Rogue AXE-1-16M	PowerVR Rogue AXE-1-16M	–	–	–
Frequency	500MHz	500MHz	500MHz	–	–	–
FLOPs	FP32: 8GFLOPs FP16: 16GFLOPs	FP32: 8GFLOPs FP16: 16GFLOPs	FP32: 8GFLOPs FP16: 16GFLOPs	–	–	–
OpenGL ES	3.1	3.1	3.1	–	–	–
Vulkan	1.2	1.2	1.2	–	–	–

1.5.3 Interfaces

Table 3: SoM interfaces <details>

Parameter	Verdin AM62 Quad 2GB WB IT	Verdin AM62 Dual 1GB WB IT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB ET	Verdin AM62 Solo 512MB WB IT	Verdin AM62 Solo 512MB
Analog						
Analog input	4	4	4	4	4	4
Audio						
Digital Audio	2x McASP *I2S or TDM*	2x McASP *I2S or TDM*	2x McASP *I2S or TDM*	2x McASP *I2S or TDM*	2x McASP *I2S or TDM*	2x McASP *I2S or TDM*
Camera						
MIPI CSI-2	1x Quad Lane	1x Quad Lane	1x Quad Lane	1x Quad Lane	1x Quad Lane	1x Quad Lane
Display						
Display Controllers	Dual	Dual	Dual	Dual	Dual	Dual
LVDS	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080	1x up to 1920x1080
MIPI DSI	1x Quad Lane	1x Quad Lane	1x Quad Lane	1x Quad Lane	–	–
Low Speed						
CAN FD	3	3	3	3	3	3
GPIO	94	94	104	104	94	104
I^2C	4	4	4	4	4	4
JTAG	1	1	1	1	1	1
PWM	6	6	6	6	6	6
QSPI/OSPI	1	1	1	1	1	1
SPI	5	5	5	5	5	5
UART	10	10	10	10	9	9
Network						
Bluetooth	Classic / LE 5.2	Classic / LE 5.2	–	–	Classic / LE 5.2	–
Ethernet	GBE with TSN + 2^{nd} RGMII	GBE with TSN + 2^{nd} RGMII	GBE with TSN + 2^{nd} RGMII	GBE with TSN + 2^{nd} RGMII	GBE with TSN + 2^{nd} RGMII	GBE with TSN + 2^{nd} RGMII
Wi-Fi	Dual-band 1x1 802.11a/b/g/n	Dual-band 1x1 802.11a/b/g/n	–	–	Dual-band 1x1 802.11a/b/g/n	–
Storage						
SDIO/SD/MMC	1	1	2	2	1	2
USB						
USB 2.0 Host	1	1	1	1	1	1
USB 2.0 OTG	1	1	1	1	1	1

1.5.4 Memory

Table 4: Memory

Parameter	Verdin AM62 Quad 2GB WB IT	Verdin AM62 Dual 1GB WB IT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB ET	Verdin AM62 Solo 512MB WB IT	Verdin AM62 Solo 512MB
eMMC						
eMMC Configuration	3D TLC	2D MLC	2D MLC	2D MLC	2D MLC	2D MLC
eMMC Capacity	16GB	8GB	8GB	4GB	4GB	4GB
I²C EEPROM						
I²C EEPROM Capacity	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits	2kbit 256 × 8bits
RAM						
RAM Capacity						
RAM Configuration *ctrl. × ch. × bits*[1]	16-bit Single rank 1 × 1 × 16	16-bit Single rank 1 × 1 × 16	16-bit Single rank 1 × 1 × 16	16-bit Single rank 1 × 1 × 16	16-bit Single rank 1 × 1 × 16	16-bit Single rank 1 × 1 × 16
RAM Type	LPDDR4	LPDDR4	LPDDR4	LPDDR4	LPDDR4	LPDDR4
RAM Speed	1600MT/s	1600MT/s	1600MT/s	1600MT/s	1600MT/s	1600MT/s
Inline ECC	Yes	Yes	Yes	Yes	Yes	Yes

[1] Controllers × channels per controller × bits per channel.

1.5.5 Physical

Table 5: Physical features

Parameter	Verdin AM62 Quad 2GB WB IT	Verdin AM62 Dual 1GB WB IT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB ET	Verdin AM62 Solo 512MB WB IT	Verdin AM62 Solo 512MB
Module dimensions	69.6 × 35.0 × 6.0 mm					
Temperature range	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−20°C to +85°C	−40°C to +85°C	0°C to +70°C
Shock / Vibration	EN 60068-2-6/50g 20ms					

1.5.6 PRUSS

The Programmable Real-Time Unit Subsystem (PRUSS) can deliver fast real-time responses, specialized data handling operations, custom peripheral interfaces, and may also offload tasks from the other processor cores of the device.

The PRUSS is available in some versions of the Verdin AM62:

Table 6: Programmable Real-Time Unit Subsystem (PRUSS) features

Parameter	Verdin AM62 Quad 2GB WB IT	Verdin AM62 Dual 1GB WB IT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB ET	Verdin AM62 Solo 512MB WB IT	Verdin AM62 Solo 512MB
PRUSS	Yes	Yes	Yes	Yes	No	No
Core count	2	2	2	2	–	–
Frequency	333MHz	333MHz	333MHz	333MHz	–	–

Continued on next page

Table 6: Programmable Real-Time Unit Subsystem (PRUSS) features (Continued)

Parameter	Verdin AM62 Quad 2GB WB IT	Verdin AM62 Dual 1GB WB IT	Verdin AM62 Dual 1GB IT	Verdin AM62 Dual 1GB ET	Verdin AM62 Solo 512MB WB IT	Verdin AM62 Solo 512MB
Memory *data*	8kB	8kB	8kB	8kB	–	–
Memory *program*	12kB	12kB	12kB	12kB	–	–
Memory *general purpose*	32kB	32kB	32kB	32kB	–	–
CRC32/16 accelerator	Yes	Yes	Yes	Yes	–	–
Interrupt controller *per core*	1	1	1	1	–	–
Timers	1 × 64-bit	1 × 64-bit	1 × 64-bit	1 × 64-bit	–	–

The PRU subsystem consists of two 32-bit 4-Bus (1 instruction + 3 data) Harvard cores for simple, real-time tasks. The cores do not feature pipelining, neither superscalar or out-of-order execution.

Some PRU features are not available in the Verdin AM62 X1 connector, or may conflict with other reserved pins. As the PRU is not standard in the Verdin family, using it may limit upgradability in the future.

An overview of the PRUSS interfaces available on X1 can be found in section 4.2.2 on page 40.

1.6 Interface Overview

Features of the Verdin module are split into three distinct categories: “Always Compatible”, “Reserved”, and “Module-specific”. The “Always Compatible” and “Reserved” pins are also referred to as the “Verdin Standard” pins.

Additionally to this definition, the AM62 SoC allows for alternate functions. As an example, many pins can, apart from their primary function, also work as GPIOs.

“Always Compatible” interfaces are features that shall be present on each SoM in the Verdin Family. Customers can count on upgradability and maximum scalability regarding these interfaces.

“Reserved” interfaces are features that are defined and reserved but possibly missing on some SoM models due to lack of availability. It could be that a particular SoC does not provide a specific interface or that there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means any Verdin SoM can be reliably inserted into any Verdin carrier board without causing damage due to incompatible “Reserved” pins.

A “Module-specific” feature is a feature that is not guaranteed to be functionally or electrically compatible between modules. Suppose a carrier board design uses such features. In that case, it is possible that other modules in the Verdin module family do not provide these features and instead provide other features on the associated pins. In this case, Verdin modules that are suitable for use in the carrier board design may be restricted. An incompatible SoM/carrier board combination may disable all functionality or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

The alternate functions group means that an interface is provided as an additional function on an “Always Compatible”, “Reserved”, or “Module-specific” pin. These functions can only be used if the primary function of the pin is not used.

Table 7 shows the interfaces that are supported on the Verdin AM62 module along with the group in which that feature is provided: “Always Compatible”, “Reserved”, “Module-specific”, or alternate function.

Table 7: X1 interfaces

Feature	Total	“Always Compatible”	“Reserved”	“Module-specific” or Alternate Function
Analog				
Analog input	4	0	4	0
Audio				
I^2S	2	0	2	0
Camera				
MIPI CSI-2	1	0	1	0
Display				
LVDS	1	0	0	1
MIPI DSI	1^{DSI}	0	1^{DSI}	0
Low Speed				
CAN FD	$1+2^{M4F}$	0	$1+1^{M4F}$	1^{M4F}
GPIO	$94+10^{nWB}$	10	$4+10^{nWB}$	80
I^2C	4	1	3	0

Continued on next page

Table 7: X1 interfaces (Continued)

Feature	Total	"Always Compatible"	"Reserved"	"Module-specific" or Alternate Function
JTAG	1	0	1	0
OSPI	1[OSPI]	0	0	1[OSPI]
PWM	6	1	2	3
QSPI	1	0	1	0
SPI	5	1	0	4
UART	9+1[PRU]	3	1	5+1[PRU]
Network				
Gigabit Ethernet	1	1	0	0
RGMII *for 2nd Gigabit Ethernet*	1	0	1	0
Storage				
SDIO/SD/MMC	1+1[nWB,1V8]	1	0	1[nWB,1V8]
USB				
USB 2.0 Host	1	1	0	0
USB 2.0 OTG	1	1	0	0

1V8: 1.8V-only interface, may require a level shifter on the carrier board.
DSI: See the DSI availability in Table 3 on page 7.
M4F: Interrupts are available only on M4F core. Requires software polling on A53 cores which may reduce throughput.
nWB: On models without Wi-Fi/Bluetooth module.
OSPI: The OSPI is an extension to the QSPI interface, using the QSPI pins and module specific pins.
PRU: Only accessible to the Programmable Real-Time Subsystem (PRUSS).

1.7 Reference Documents

1.7.1 Verdin Carrier Board Design Guide

A custom carrier board should follow the Verdin Carrier Board Design Guide to make the board compatible with the Verdin module family. Please study this document in detail before starting your carrier board design.

https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

1.7.2 Verdin Family Specification

This document outlines the specification which defines the Verdin Computer-on-Module family. It describes the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also explains the mechanical form factor, including key dimensions and possible thermal solutions.

https://docs.toradex.com/109262-verdin-family-specification.pdf

1.7.3 Layout Design Guide

This document contains information about high-speed layout design and additional factors that help get the carrier board layout right the first time.

https://docs.toradex.com/102492-layout-design-guide.pdf

1.7.4 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information on a regular basis. You can find an abundance of additional information there.

Please note that the Developer Center is common to all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Verdin AM62.

https://developer.toradex.com

1.7.5 Verdin Carrier Board Schematics

We provide complete schematics plus an Altium project file which includes library symbols and IPC-7351 compliant footprints for the Verdin Development Board, as well as other carrier boards, free of charge. This resource is of great help when designing your own carrier board.

https://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.7.6 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin, Apalis, and Colibri Modules. The tool allows comparing the interfaces across different modules.

https://developer.toradex.com/knowledge-base/pinout-designer

1.7.7 TI AM62x Sitara

You may find additional details about the TI AM62x Sitara SoC in the Datasheet and Reference Manual provided by Texas Instruments.

AM623:
https://www.ti.com/product/AM623

AM625:
https://www.ti.com/product/AM625

1.7.8 Enabling Low Power Embedded Systems With AM62x Processors

TI's White Paper explaining low power modes, active power management, and analyzing power consumption on the AM62x SoC.

https://www.ti.com/lit/wp/sprad41/sprad41.pdf

1.7.9 ADC

Verdin AM62 utilizes a Texas Instrument TLA2024 12-bit, four-channel, I2C analog-to-digital converter.

https://www.ti.com/product/TLA2024

1.7.10 DSI Bridge

Some Verdin AM62 models have a Toshiba TC9594XBG Parallel Port (RGB) to MIPI DSI bridge. See the DSI availability in Table 3 on page 7.

https://toshiba.semicon-storage.com/us/semiconductor/product/interface-bridge-ics-for-mobile-peripheral-devices/display-interface-bridge-ics/detail.TC9594XBG.html

1.7.11 EEPROM

The Verdin AM62 has an on-module I2C EEPROM, the M24C02-FMC6TG from STMicroelectronics.

https://www.st.com/en/memories/m24c02-f.html

1.7.12 Ethernet Transceiver

The Verdin AM62 SoM utilizes the DP83867IR Industrial Temperature, robust gigabit Ethernet PHY transceiver from Texas Instruments.

https://www.ti.com/product/DP83867IR

1.7.13 PCB Temperature Sensor

The Verdin AM62 can be assembled with a PCB temperature sensor, the TI TMP1075DSGR.

https://www.ti.com/product/TMP1075

1.7.14 RTC

The Verdin AM62 features a low-power Epson RX8130CE real-time clock.

https://www5.epsondevice.com/en/products/rtc/rx8130ce.html

1.7.15 TPM 2.0 Module

The Verdin AM62 can be assembled with a Trusted Platform Module (TPM 2.0), the ST33KTPM2I from STMicroelectronics. The complete documentation is only available under a STMicroelectronics NDA.

https://www.st.com/en/secure-mcus/st33ktpm2xspi.html

1.7.16 Wi-Fi and Bluetooth Module

The WB versions of the Verdin AM62 utilize an u-blox MAYA-W160-00B Host-based multiradio module with Wi-Fi 4 802.11n dual-band and BT/BLE 5.2. This module uses two U.FL antennas.

https://www.u-blox.com/en/product/maya-w1-series

Information on pre-certified antennas and cables can be found here:

https://developer.toradex.com/hardware/hardware-resources/peripherals/wireless/wi-fi-cables-and-antennas-for-toradex-modules/

1.8 Naming Conventions

In this document, a consistent naming convention is used. It is essential to notice the punctuation and spaces in the names. Do not confuse the TI AM62x Sitara SoC with the Toradex Verdin AM62 SoM.

Table 8: Toradex naming conventions

Name	Description
AM62x	TI Sitara AM62x System on Chip family.
AM625	TI Sitara AM625 System on Chip.
Verdin AM62	Verdin module based on the TI AM62x Sitara SoC. Whenever this document uses the term Verdin AM62, all versions of the Verdin AM62 are meant.
Verdin AM62 Dual 1GB WB IT	Verdin module based on the TI AM62x Sitara SoC with 2 cores, 1GB RAM, Wi-Fi, Bluetooth, and industrial temperature range (IT).

1.9 Build-To-Order (BTO) Options

The Verdin AM62 module is available in different variants (see section 1.5 on page 6). In addition to these configurations, it is possible to order customized versions of the module. These versions are Build-To-Order (BTO). More information can be found on our Developer Website[1].

The following customization options are technically possible for the Verdin AM62:

Connectivity:

- Gigabit Ethernet PHY
- Wi-Fi 4 or Wi-Fi 6 module with Bluetooth 5.2

Features:

- Onboard ADC
- PCB temperature sensor
- Trusted Platform Module (TPM 2.0)

Memory:

- EEPROM capacity
- eMMC capacity
- RAM capacity

SoC variants:

- Contact us

Temperature range:

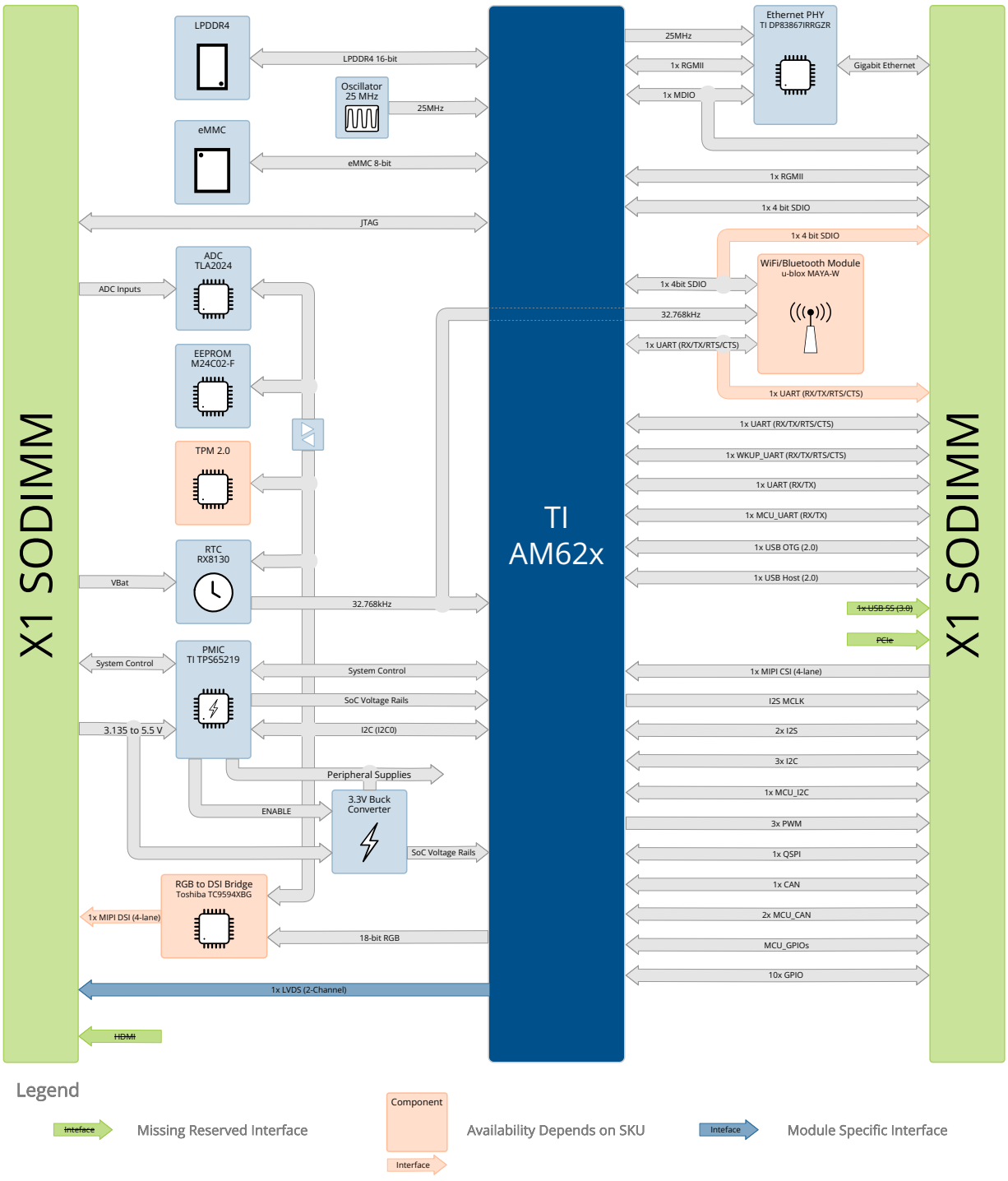
- Industrial, Extended or Consumer

[1] https://developer.toradex.com/knowledge-base/customized-computer-on-modules

2 Architecture Overview

2.1 Block Diagram

Figure 1: Block Diagram



3 Verdin AM62 Connector

3.1 Pin Numbering

The Verdin module follows the same pin numbering scheme as the SODIMM DDR4 standard. Pins on the top side of the module have an odd number, while the pins on the bottom side have an even number.

Figure 2: Pin numbering (top)

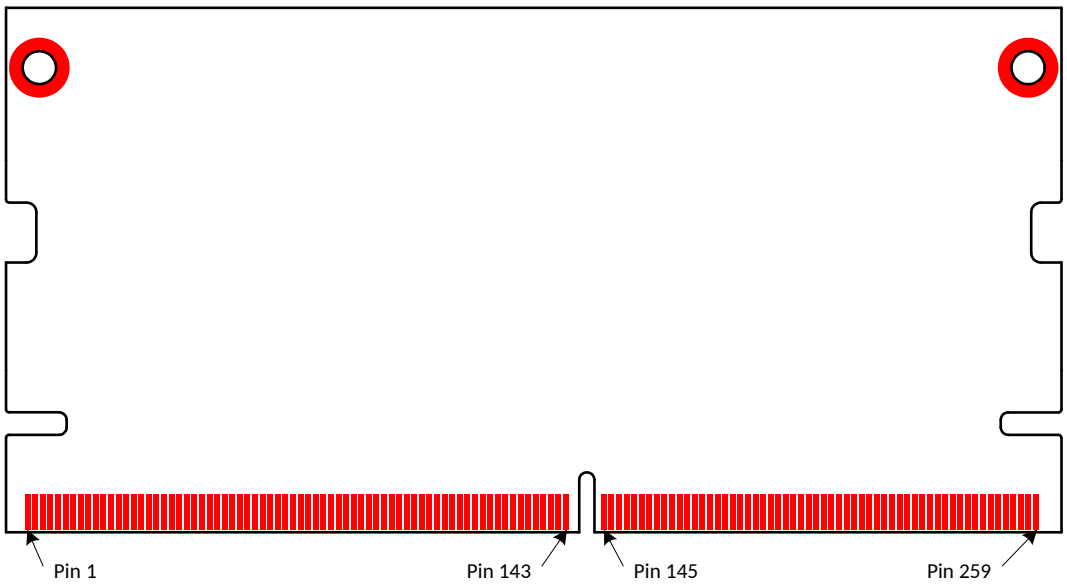
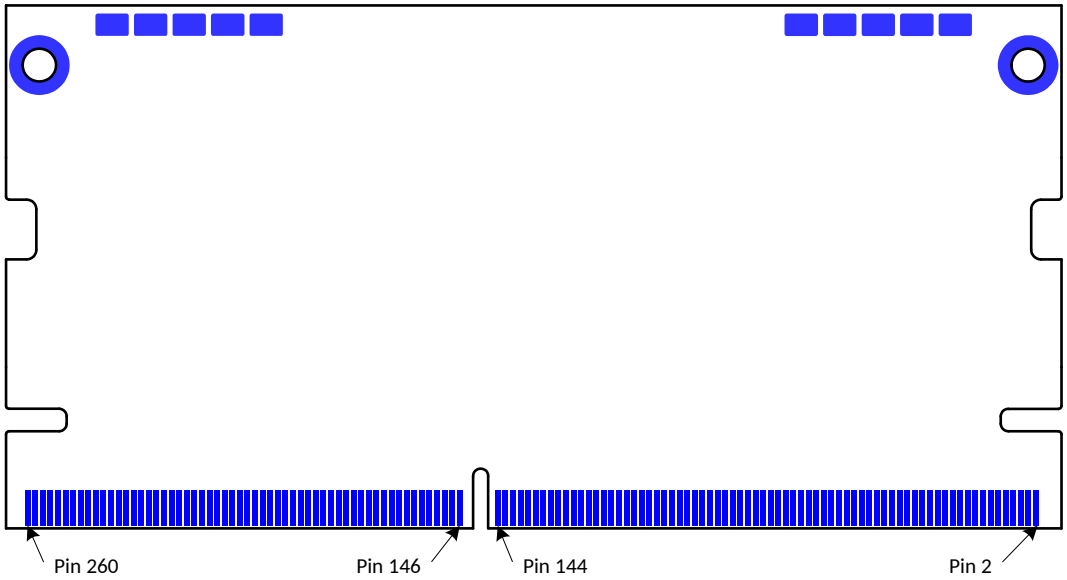


Figure 3: Pin numbering (bottom)



3.2 Pin Assignment

Table 9 and Table 10 describe the main connector (X1) pinout and highlight the pins' function compatibility with the family specification. A detailed explanation about the family specification compatibility groups is available in section 1.6 on page 10.

Table 9: X1 pin assignment – top side – odd pins even pins – alternate functions

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
1	JTAG_1_TDI	Yes	"Reserved"	TDI			
3	JTAG_1_TRST#	Yes	"Reserved"	TRSTn			
5	JTAG_1_TDO	Yes	"Reserved"	TDO			
7	JTAG_1_VREF	Yes	"Reserved"		1.8V		Reference output, 10mA max.
9	JTAG_1_TCK	Yes	"Reserved"	TCK			
11	GND	Yes	"Always Compatible"		GND		
13	JTAG_1_TMS	Yes	"Reserved"	TMS			
15	PWM_1	Yes	"Always Compatible"	SPI0_CS0			
17	GPIO_9_DSI	Yes	"Reserved"	MMC1_SDWP			
19	PWM_3_DSI	Yes	"Reserved"	SPI0_CLK			
21	GPIO_10_DSI	Yes	"Reserved"	GPMC0_AD15			
23	DSI_1_D3_N	Yes	"Reserved"		MIPI_D3N *DSI Bridge*		DSI data lane 3, N signal.
25	DSI_1_D3_P	Yes	"Reserved"		MIPI_D3P *DSI Bridge*		DSI data lane 3, P signal.
27	GND	Yes	"Always Compatible"		GND		
29	DSI_1_D2_N	Yes	"Reserved"		MIPI_D2N *DSI Bridge*		DSI data lane 2, N signal.
31	DSI_1_D2_P	Yes	"Reserved"		MIPI_D2P *DSI Bridge*		DSI data lane 2, P signal.
33	GND	Yes	"Always Compatible"		GND		
35	DSI_1_CLK_N	Yes	"Reserved"		MIPI_CN *DSI Bridge*		DSI clock, N signal.
37	DSI_1_CLK_P	Yes	"Reserved"		MIPI_CP *DSI Bridge*		DSI clock, P signal.
39	GND	Yes	"Always Compatible"		GND		

Continued on next page

Table 9: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
41	DSI_1_D1_N	Yes	"Reserved"		MIPI_D1N *DSI Bridge*		DSI data lane 1, N signal.
43	DSI_1_D1_P	Yes	"Reserved"		MIPI_D1P *DSI Bridge*		DSI data lane 1, P signal.
45	GND	Yes	"Always Compatible"		GND		
47	DSI_1_D0_N	Yes	"Reserved"		MIPI_D0N *DSI Bridge*		DSI data lane 0, N signal.
49	DSI_1_D0_P	Yes	"Reserved"		MIPI_D0P *DSI Bridge*		DSI data lane 0, P signal.
51	GND	Yes	"Always Compatible"		GND		
53	I2C_2_DSI_SDA	Yes	"Reserved"	GPMC0_CSn3			
55	I2C_2_DSI_SCL	Yes	"Reserved"	GPMC0_CSn2			
57	I2C_3_HDMI_SDA	Yes	"Reserved"	MCU_I2C0_SDA			
59	I2C_3_HDMI_SCL	Yes	"Reserved"	MCU_I2C0_SCL			
61	HDMI_1_HPD	No	"Reserved"	MCU_UART0_CTSn			HDMI not supported on Verdin AM62.
63	HDMI_1_CEC	No	"Reserved"	MCU_UART0_RTSn			HDMI not supported on Verdin AM62.
65	GND	Yes	"Always Compatible"		GND		
67	HDMI_1_TXC_N	No	"Reserved"				NC, HDMI not supported on Verdin AM62.
69	HDMI_1_TXC_P	No	"Reserved"				NC, HDMI not supported on Verdin AM62.
71	GND	Yes	"Always Compatible"		GND		
73	HDMI_1_TXD0_N	No	"Reserved"				NC, HDMI not supported on Verdin AM62.
75	HDMI_1_TXD0_P	No	"Reserved"				NC, HDMI not supported on Verdin AM62.
77	GND	Yes	"Always Compatible"		GND		
79	HDMI_1_TXD1_N	No	"Reserved"				NC, HDMI not supported on Verdin AM62.
81	HDMI_1_TXD1_P	No	"Reserved"				NC, HDMI not supported on Verdin AM62.

Continued on next page

Table 9: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
83	GND	Yes	"Always Compatible"		GND		
85	HDMI_1_TXD2_N	No	"Reserved"				NC, HDMI not supported on Verdin AM62.
87	HDMI_1_TXD2_P	No	"Reserved"				NC, HDMI not supported on Verdin AM62.
89	GND	Yes	"Always Compatible"		GND		
91	CSI_1_MCLK	Yes	"Reserved"	WKUP_CLKOUT0			
93	I2C_4_CSI_SDA	Yes	"Reserved"	UART0_RTSn			
95	I2C_4_CSI_SCL	Yes	"Reserved"	UART0_CTSn			
97	GND	Yes	"Always Compatible"		GND		
99	CSI_1_D3_P	Yes	"Reserved"	CSI0_RXP3			
101	CSI_1_D3_N	Yes	"Reserved"	CSI0_RXN3			
103	GND	Yes	"Always Compatible"		GND		
105	CSI_1_D2_P	Yes	"Reserved"	CSI0_RXP2			
107	CSI_1_D2_N	Yes	"Reserved"	CSI0_RXN2			
109	GND	Yes	"Always Compatible"		GND		
111	CSI_1_CLK_P	Yes	"Reserved"	CSI0_RXCLKP			
113	CSI_1_CLK_N	Yes	"Reserved"	CSI0_RXCLKN			
115	GND	Yes	"Always Compatible"		GND		
117	CSI_1_D1_P	Yes	"Reserved"	CSI0_RXP1			
119	CSI_1_D1_N	Yes	"Reserved"	CSI0_RXN1			
121	GND	Yes	"Always Compatible"		GND		
123	CSI_1_D0_P	Yes	"Reserved"	CSI0_RXP0			
125	CSI_1_D0_N	Yes	"Reserved"	CSI0_RXN0			
127	GND	Yes	"Always Compatible"		GND		

Continued on next page

Table 9: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
129	UART_1_RXD	Yes	"Always Compatible"	MCASP0_AFSR			
131	UART_1_TXD	Yes	"Always Compatible"	MCASP0_ACLKR			
133	UART_1_RTS	Yes	"Reserved"	MCASP0_AXR2			
135	UART_1_CTS	Yes	"Reserved"	MCASP0_AXR3			
137	UART_2_RXD	Yes	"Always Compatible"	WKUP_UART0_RXD			
139	UART_2_TXD	Yes	"Always Compatible"	WKUP_UART0_TXD			
141	UART_2_RTS	Yes	"Reserved"	WKUP_UART0_RTSn			
143	UART_2_CTS	Yes	"Reserved"	WKUP_UART0_CTSn			
145	GND	Yes	"Always Compatible"		GND		
147	UART_3_RXD	Yes	"Always Compatible"	UART0_RXD			
149	UART_3_TXD	Yes	"Always Compatible"	UART0_TXD			
151	UART_4_RXD	Yes	"Reserved"	MCU_UART0_RXD			
153	UART_4_TXD	Yes	"Reserved"	MCU_UART0_TXD			
155	USB_1_EN	Yes	"Always Compatible"	USB0_DRVVBUS			
157	USB_1_OC#	Yes	"Always Compatible"	MMC2_SDCD			
159	USB_1_VBUS	Yes	"Always Compatible"	USB0_VBUS			Voltage Divider on the Module.
161	USB_1_ID	Yes	"Always Compatible"	SPI0_D1			
163	USB_1_D_N	Yes	"Always Compatible"	USB0_DM			
165	USB_1_D_P	Yes	"Always Compatible"	USB0_DP			
167	GND	Yes	"Always Compatible"		GND		
169	USB_2_SSTX_N	No	"Reserved"				NC
171	USB_2_SSTX_P	No	"Reserved"				NC
173	GND	Yes	"Always Compatible"		GND		

Continued on next page

Table 9: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
175	USB_2_SSRX_N	No	"Reserved"				NC
177	USB_2_SSRX_P	No	"Reserved"				NC
179	GND	Yes	"Always Compatible"		GND		
181	USB_2_D_N	Yes	"Always Compatible"	USB1_DM			
183	USB_2_D_P	Yes	"Always Compatible"	USB1_DP			
185	USB_2_EN	Yes	"Always Compatible"	USB1_DRVVBUS			
187	USB_2_OC#	Yes	"Always Compatible"	MMC2_SDWP			
189	ETH_2_RGMII_INT#	Yes	"Reserved"	GPMC0_WAIT1			
191	ETH_2_RGMII_MDIO	Yes	"Reserved"	MDIO0_MDIO			Shared with on-module PHY.
193	ETH_2_RGMII_MDC	Yes	"Reserved"	MDIO0_MDC			Shared with on-module PHY.
195	GND	Yes	"Always Compatible"		GND		
197	ETH_2_RGMII_RXC	Yes	"Reserved"	RGMII2_RXC			
199	ETH_2_RGMII_RX_CTL	Yes	"Reserved"	RGMII2_RX_CTL			
201	ETH_2_RGMII_RXD_0	Yes	"Reserved"	RGMII2_RD0			
203	ETH_2_RGMII_RXD_1	Yes	"Reserved"	RGMII2_RD1			
205	ETH_2_RGMII_RXD_2	Yes	"Reserved"	RGMII2_RD2			
207	ETH_2_RGMII_RXD_3	Yes	"Reserved"	RGMII2_RD3			
209	GND	Yes	"Always Compatible"		GND		
211	ETH_2_RGMII_TX_CTL	Yes	"Reserved"	RGMII2_TX_CTL			
213	ETH_2_RGMII_TXC	Yes	"Reserved"	RGMII2_TXC			
215	ETH_2_RGMII_TXD_3	Yes	"Reserved"	RGMII2_TD3			
217	ETH_2_RGMII_TXD_2	Yes	"Reserved"	RGMII2_TD2			
219	ETH_2_RGMII_TXD_1	Yes	"Reserved"	RGMII2_TD1			

Continued on next page

Table 9: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
221	ETH_2_RGMII_TXD_0	Yes	"Reserved"	RGMII2_TD0			
223	GND	Yes	"Always Compatible"		GND		
225	ETH_1_MDI0_P	Yes	"Always Compatible"		TD_P_A *Ethernet PHY*		
227	ETH_1_MDI0_N	Yes	"Always Compatible"		TD_M_A *Ethernet PHY*		
229	GND	Yes	"Always Compatible"		GND		
231	ETH_1_MDI1_N	Yes	"Always Compatible"		TD_M_B *Ethernet PHY*		
233	ETH_1_MDI1_P	Yes	"Always Compatible"		TD_P_B *Ethernet PHY*		
235	ETH_1_LINK	Yes	"Always Compatible"		Circuit		
237	ETH_1_ACT	Yes	"Always Compatible"		Circuit		
239	ETH_1_MDI2_P	Yes	"Always Compatible"		TD_P_C *Ethernet PHY*		
241	ETH_1_MDI2_N	Yes	"Always Compatible"		TD_M_C *Ethernet PHY*		
243	GND	Yes	"Always Compatible"		GND		
245	ETH_1_MDI3_N	Yes	"Always Compatible"		TD_M_D *Ethernet PHY*		
247	ETH_1_MDI3_P	Yes	"Always Compatible"		TD_P_D *Ethernet PHY*		
249	VCC_BACKUP	Yes	"Always Compatible"		RTC battery		
251	VCC	Yes	"Always Compatible"		VCC		3.135 to 5.5V input.
253	VCC	Yes	"Always Compatible"		VCC		3.135 to 5.5V input.
255	VCC	Yes	"Always Compatible"		VCC		3.135 to 5.5V input.
257	VCC	Yes	"Always Compatible"		VCC		3.135 to 5.5V input.

Continued on next page

Table 9: X1 pin assignment – top side – odd pins even pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Reset state	Note
259	VCC	Yes	"Always Compatible"		VCC		3.135 to 5.5V input.

[1] The available pin functions fulfill the pin function defined in the family specification.

Table 10: X1 pin assignment – bottom side – even pins odd pins – alternate functions

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
2	ADC_1	Yes	"Reserved"		ADC_1 *ADC*	ADC channel 1.
4	ADC_2	Yes	"Reserved"		ADC_2 *ADC*	ADC channel 2.
6	ADC_3	Yes	"Reserved"		ADC_3 *ADC*	ADC channel 3.
8	ADC_4	Yes	"Reserved"		ADC_4 *ADC*	ADC channel 4.
10	GND	Yes	"Always Compatible"		GND	
12	I2C_1_SDA	Yes	"Always Compatible"	I2C1_SDA		
14	I2C_1_SCL	Yes	"Always Compatible"	I2C1_SCL		
16	PWM_2	Yes	"Reserved"	SPI0_CS1		
18	GND	Yes	"Always Compatible"		GND	
20	CAN_1_TX	Yes	"Reserved"	MCAN0_TX		
22	CAN_1_RX	Yes	"Reserved"	MCAN0_RX		
24	CAN_2_TX	Yes	"Reserved"	MCU_MCAN0_TX		Interrupts are available only on M4F core.
26	CAN_2_RX	Yes	"Reserved"	MCU_MCAN0_RX		Interrupts are available only on M4F core.
28	GND	Yes	"Always Compatible"		GND	
30	I2S_1_BCLK	Yes	"Reserved"	MCASP0_ACLKX		
32	I2S_1_SYNC	Yes	"Reserved"	MCASP0_AFSX		
34	I2S_1_D_OUT	Yes	"Reserved"	MCASP0_AXR0		
36	I2S_1_D_IN	Yes	"Reserved"	MCASP0_AXR1		
38	I2S_1_MCLK	Yes	"Reserved"	GPMC0_WPn		
40	GND	Yes	"Always Compatible"		GND	
42	I2S_2_BCLK	Yes	"Reserved"	GPMC0_BE0n_CLE		

Continued on next page

Table 10: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
44	I2S_2_SYNC	Yes	"Reserved"	GPMC0_WAIT0		
46	I2S_2_D_OUT	Yes	"Reserved"	GPMC0_WEn		
48	I2S_2_D_IN	Yes	"Reserved"	GPMC0_OEn_REn		
50	GND	Yes	"Always Compatible"		GND	
52	QSPI_1_CLK	Yes	"Reserved"	OSPI0_CLK		
54	QSPI_1_CS#	Yes	"Reserved"	OSPI0_CSn0		
56	QSPI_1_IO0	Yes	"Reserved"	OSPI0_D0		
58	QSPI_1_IO1	Yes	"Reserved"	OSPI0_D1		
60	QSPI_1_IO2	Yes	"Reserved"	OSPI0_D2		
62	QSPI_1_IO3	Yes	"Reserved"	OSPI0_D3		
64	QSPI_1_CS2#	Yes	"Reserved"	OSPI0_CSn1		
66	QSPI_1_DQS	Yes	"Reserved"	SPI0_D0		
68	GND	Yes	"Always Compatible"		GND	
70	SD_1_D2	Yes	"Always Compatible"	MMC1_DAT2		
72	SD_1_D3	Yes	"Always Compatible"	MMC1_DAT3		
74	SD_1_CMD	Yes	"Always Compatible"	MMC1_CMD		
76	SD_1_PWR_EN	Yes	"Always Compatible"	GPMC0_AD14		
78	SD_1_CLK	Yes	"Always Compatible"	MMC1_CLK		
80	SD_1_D0	Yes	"Always Compatible"	MMC1_DAT0		
82	SD_1_D1	Yes	"Always Compatible"	MMC1_DAT1		
84	SD_1_CD#	Yes	"Always Compatible"	MMC1_SDCD		
86	GND	Yes	"Always Compatible"		GND	
88	MSP_1	–	"Module-specific"	OLDI0_CLK0N		

Continued on next page

Table 10: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
90	MSP_2	–	"Module-specific"	OLDI0_CLK0P		
92	MSP_3	–	"Module-specific"		1nF to GND	
94	MSP_4	–	"Module-specific"	OLDI0_A0N		
96	MSP_5	–	"Module-specific"	OLDI0_A0P		
98	GND	Yes	"Always Compatible"		GND	
100	MSP_6	–	"Module-specific"	OLDI0_A1N		
102	MSP_7	–	"Module-specific"	OLDI0_A1P		
104	MSP_8	–	"Module-specific"	SOC_VPP		
106	MSP_9	–	"Module-specific"	OLDI0_A2N		
108	MSP_10	–	"Module-specific"	OLDI0_A2P		
110	GND	Yes	"Always Compatible"		GND	
112	MSP_11	–	"Module-specific"	OLDI0_A3N		
114	MSP_12	–	"Module-specific"	OLDI0_A3P		
116	MSP_13	–	"Module-specific"	MCU_MCAN1_RX		Interrupts are available only on M4F core.
118	MSP_14	–	"Module-specific"	OLDI0_CLK1N		
120	MSP_15	–	"Module-specific"	OLDI0_CLK1P		
122	GND	Yes	"Always Compatible"		GND	
124	MSP_16	–	"Module-specific"	OLDI0_A4N		
126	MSP_17	–	"Module-specific"	OLDI0_A4P		
128	MSP_18	–	"Module-specific"	MCU_MCAN1_TX		Interrupts are available only on M4F core.
130	MSP_19	–	"Module-specific"	OLDI0_A5N		
132	MSP_20	–	"Module-specific"	OLDI0_A5P		
134	GND	Yes	"Always Compatible"		GND	

Continued on next page

Table 10: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
136	MSP_21	–	"Module-specific"	OLDI0_A6N		
138	MSP_22	–	"Module-specific"	OLDI0_A6P		
140	MSP_23	–	"Module-specific"	RTC_IRQ#		
142	MSP_24	–	"Module-specific"	OLDI0_A7N		
144	MSP_25	–	"Module-specific"	OLDI0_A7P		
146	GND	Yes	"Always Compatible"		GND	
148	MSP_26	–	"Module-specific"			NC
150	MSP_27	–	"Module-specific"			NC
152	MSP_28	–	"Module-specific"			NC
154	MSP_29	–	"Module-specific"			NC
156	MSP_30	–	"Module-specific"	MMC2_CLK		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
158	GND	Yes	"Always Compatible"		GND	
160	MSP_31	–	"Module-specific"	MMC2_CMD		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
162	MSP_32	–	"Module-specific"	MMC2_DAT0		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
164	MSP_33	–	"Module-specific"	MMC2_DAT1		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
166	MSP_34	–	"Module-specific"	MMC2_DAT2		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
168	MSP_35	–	"Module-specific"	MMC2_DAT3		SDIO assembly option modules w/o Wi-Fi, 1.8V only!
170	GND	Yes	"Always Compatible"		GND	
172	MSP_36	–	"Module-specific"	GPMC0_AD1	BT_WAKE_HOST *Wi-Fi/BT module*	
174	MSP_37	–	"Module-specific"	GPMC0_AD0	WLAN_WAKE_HOST *Wi-Fi/BT module*	
176	MSP_38	–	"Module-specific"		NC	

Continued on next page

Table 10: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
178	MSP_39	–	"Module-specific"		WCI_SIN *Wi-Fi/BT module*	Wireless coexistence serial interface (WCI-2).
180	MSP_40	–	"Module-specific"		WCI_SOUT *Wi-Fi/BT module*	Wireless coexistence serial interface (WCI-2).
182	GND	Yes	"Always Compatible"		GND	
184	MSP_41	–	"Module-specific"	OSPI0_DQS		UART assembly option modules w/o Wi-Fi.
186	MSP_42	–	"Module-specific"	OSPI0_LBCLKO		UART assembly option modules w/o Wi-Fi.
188	MSP_43	–	"Module-specific"			NC
190	MSP_44	–	"Module-specific"	OSPI0_CSn3		UART assembly option modules w/o Wi-Fi.
192	MSP_45	–	"Module-specific"	OSPI0_CSn2		UART assembly option modules w/o Wi-Fi.
194	GND	Yes	"Always Compatible"		GND	
196	SPI_1_CLK	Yes	"Always Compatible"	OSPI0_D5		
198	SPI_1_MISO	Yes	"Always Compatible"	OSPI0_D7		
200	SPI_1_MOSI	Yes	"Always Compatible"	OSPI0_D6		
202	SPI_1_CS	Yes	"Always Compatible"	OSPI0_D4		
204	GND	Yes	"Always Compatible"		GND	
206	GPIO_1	Yes	"Always Compatible"	MCU_SPI0_CS1		
208	GPIO_2	Yes	"Always Compatible"	MCU_SPI0_CLK		
210	GPIO_3	Yes	"Always Compatible"	MCU_SPI0_D0		
212	GPIO_4	Yes	"Always Compatible"	MCU_SPI0_D1		
214	PWR_1V8_MOCI	Yes	"Always Compatible"		1.8V	
216	GPIO_5_CSI	Yes	"Always Compatible"	GPMC0_DIR		
218	GPIO_6_CSI	Yes	"Always Compatible"	GPMC0_BE1n		
220	GPIO_7_CSI	Yes	"Always Compatible"	GPMC0_CSn0		

Continued on next page

Table 10: X1 pin assignment – bottom side – even pins odd pins – alternate functions (Continued)

X1 pin	Verdin specification signal name	Family compatible function[1]	Verdin specification compatibility group	SoC ball name	Non-SoC ball name	Note
222	GPIO_8_CSI	Yes	"Always Compatible"	GPMC0_CSn1		
224	GND	Yes	"Always Compatible"		GND	
226	PCIE_1_CLK_N	No	"Reserved"		NC	
228	PCIE_1_CLK_P	No	"Reserved"		NC	
230	GND	Yes	"Always Compatible"		GND	
232	PCIE_1_L0_RX_N	No	"Reserved"		NC	
234	PCIE_1_L0_RX_P	No	"Reserved"		NC	
236	GND	Yes	"Always Compatible"		GND	
238	PCIE_1_L0_TX_N	No	"Reserved"		NC	
240	PCIE_1_L0_TX_P	No	"Reserved"		NC	
242	GND	Yes	"Always Compatible"		GND	
244	PCIE_1_RESET#	No	"Reserved"	MCU_SPI0_CS0		
246	CTRL_RECOVERY_MICO#	Yes	"Always Compatible"		Recovery Circuit	
248	CTRL_PWR_BTN_MICO#	Yes	"Always Compatible"		EN/BP/VSENSE *PMIC*	
250	CTRL_FORCE_OFF_MOCI#	Yes	"Always Compatible"		Circuit	
252	CTRL_WAKE1_MICO#	Yes	"Always Compatible"	GPMC0_ADVn_ALE		
254	CTRL_PWR_EN_MOCI	Yes	"Always Compatible"		Circuit	
256	CTRL_SLEEP_MOCI#	Yes	"Always Compatible"	GPMC0_CLK		
258	CTRL_RESET_MOCI#	Yes	"Always Compatible"		Circuit	
260	CTRL_RESET_MICO#	Yes	"Always Compatible"	MCU_PORz	PMIC: nRSTOUT RTC: $\overline{RST}$	

[1] The available pin functions fulfill the pin function defined in the family specification.

4 I/O Pins

4.1 Function Multiplexing

Most I/O pins of the TI AM62x SoC can be configured for up to ten alternate functions. Most of the pins can also be used as GPIOs (General-Purpose I/O, sometimes also referred to as Digital I/O). For example, the TI AM62x signal pin on the SODIMM finger pin 131 has the primary function UART1_TXD (Verdin standard function UART_1_TXD). Besides this UART function, the pin can also be configured as SPI2_CLK (SPI clock), GPIO1_14 (GPIO), MCASP0ACLKR (audio clock), EHRPWM0_B (enhanced PWM), and EQEP1_I (timer).

It is strongly recommended, whenever possible, to use a pin for a function that is compatible with all Verdin modules. This guarantees the best compatibility with the standard software and with other modules in the Verdin family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the Table 12 on page 33, there is a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

4.2 SoC Functions List

Table 12 on page 33 contains a list of all the SoC pins that are available on the SODIMM connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT7 function. The alternate functions used to provide the primary interfaces, done to ensure the best compatibility with other Verdin modules, are highlighted in **bold**.

Table 11: Function short forms

Short form	Name
ADC	Analog to Digital Converter input
CAN	Controller Area Network
CSI	Camera Serial Interface
CPTS	Common Platform Time Sync
DDR	Double Data Rate (RAM specification)
DSI	Display Serial Interface
EHRPWM	Enhanced High-Resolution Pulse-Width Modulator
ECAP	Enhanced Capture
ECC	Error-Correcting Code (RAM feature)
EMAC	Ethernet Media Access Control
EMMC	Embedded Multimedia Card
ENET	Ethernet
EQEP	Enhanced Quadrature Encoder Pulse
GPIO	General-Purpose Input Output
GPMC	General Purpose Memory Controller
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit

Continued on next page

Table 11: Function short forms (Continued)

Short form	Name
ISP	Image Signal Processor
JTAG	Joint Test Action Group (test/debug interface)
LVDS	FPD-Link/FlatLink Display interface
MCAN	Modular Controller Area Network
MCASP	Multichannel Audio Serial Port
MCU	Micro Conroller Unit
MIPI_CSI	MIPI CSI Subsystem
MIPI_DSI	MIPI DSI Subsystem
MSP	”Module-specific”
NAND	Interface for NAND Flash
NPU	Neural Processing Unit
OLDI	Open LVDS Display Interface
OSPI	Octal Serial Peripheral Interface
PCIE	PCI Express
PDM	Pulse-Density Modulation Microphone Input
PRU	Programmable Real-Time Unit
PRUSS	Programmable Real-Time Unit Subsystem
PWM	Pulse Width Modulation output
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
TRC	Trace (Arm TPIU compliant Trace Port interface)
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WKUP	Wake-Up

4.2.1 Alternate Functions

Table 12: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom)

X1 pin	SoC ball name	SoC ball ID *ALW package*	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
1	TDI	A11	**TDI**									
3	TRSTn	B10	**TRSTn**									
5	TDO	D12	**TDO**									
9	TCK	A10	**TCK**									
13	TMS	B11	**TMS**									
15	SPI0_CS0	A13	SPI0_CS0		**EHRPWM0_A**				PR0_ECAP0_SYNC_IN	GPIO1_15		
17	MMC1_SDWP	C17	MMC1_SDWP	UART6_TXD	TIMER_IO7	UART3_CTSn				**GPIO1_49**		
19	SPI0_CLK	A14	SPI0_CLK	CP_GEMAC_CPTS0_TS_SYNC	**EHRPWM1_A**					GPIO1_17		
21	GPMC0_AD15	U24	GPMC0_AD15	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA19	**GPIO0_30**	UART2_RTSn	
53	GPMC0_CSn3	K24	GPMC0_CSn3	**I2C2_SDA**	GPMC0_A20	UART4_TXD	MCASP1_AXR5		TRC_DATA18	GPIO0_44	MCASP1_ACLKR	
55	GPMC0_CSn2	K22	GPMC0_CSn2	**I2C2_SCL**	MCASP1_AXR4	UART4_RXD	PR0_PRU0_GPO19	PR0_PRU0_GPI19	TRC_DATA17	GPIO0_43	MCASP1_AFSR	
57	MCU_I2C0_SDA	D10	**MCU_I2C0_SDA**							MCU_GPIO0_18		
59	MCU_I2C0_SCL	A8	**MCU_I2C0_SCL**							MCU_GPIO0_17		
61	MCU_UART0_CTSn	A6	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7		
63	MCU_UART0_RTSn	B6	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8		
91	WKUP_CLKOUT0	A12	**WKUP_CLKOUT0**							MCU_GPIO0_23		
93	UART0_RTSn	B15	UART0_RTSn	SPI0_CS3	**I2C3_SDA**	UART2_TXD	TIMER_IO7	AUDIO_EXT_REFCLK1	PR0_ECAP0_IN_APWM_OUT	GPIO1_23	MCASP2_ACLKX	MMC2_SDWP
95	UART0_CTSn	A15	UART0_CTSn	SPI0_CS2	**I2C3_SCL**	UART2_RXD	TIMER_IO6	AUDIO_EXT_REFCLK0	PR0_ECAP0_SYNC_OUT	GPIO1_22	MCASP2_AFSX	MMC2_SDCD
99	CSI0_RXP3	AC13	**CSI0_RXP3**									
101	CSI0_RXN3	AB12	**CSI0_RXN3**									
105	CSI0_RXP2	AE13	**CSI0_RXP2**									
107	CSI0_RXN2	AD13	**CSI0_RXN2**									
111	CSI0_RXCLKP	AE15	**CSI0_RXCLKP**									

Continued on next page

Table 12: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *ALW package*	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
113	CSI0_RXCLKN	AD15	**CSI0_RXCLKN**									
117	CSI0_RXP1	AE14	**CSI0_RXP1**									
119	CSI0_RXN1	AD14	**CSI0_RXN1**									
123	CSI0_RXP0	AC15	**CSI0_RXP0**									
125	CSI0_RXN0	AB14	**CSI0_RXN0**									
129	MCASP0_AFSR	E19	MCASP0_AFSR	SPI2_CS0	**UART1_RXD**				EHRPWM0_A	GPIO1_13	EQEP1_S	
131	MCASP0_ACLKR	A20	MCASP0_ACLKR	SPI2_CLK	**UART1_TXD**				EHRPWM0_B	GPIO1_14	EQEP1_I	
133	MCASP0_AXR2	A19	MCASP0_AXR2	SPI2_D1	**UART1_RTSn**	UART6_TXD	PR0_IEP0_EDIO_DATA_IN_OUT29	ECAP2_IN_APWM_OUT	PR0_UART0_TXD	GPIO1_8	EQEP0_B	
135	MCASP0_AXR3	B19	MCASP0_AXR3	SPI2_D0	**UART1_CTSn**	UART6_RXD	PR0_IEP0_EDIO_DATA_IN_OUT28	ECAP1_IN_APWM_OUT	PR0_UART0_RXD	GPIO1_7	EQEP0_A	
137	WKUP_UART0_RXD	B4	**WKUP_UART0_RXD**		MCU_SPI0_CS2					MCU_GPIO0_9		
139	WKUP_UART0_TXD	C5	**WKUP_UART0_TXD**		MCU_SPI1_CS2					MCU_GPIO0_10		
141	WKUP_UART0_RTSn	A4	**WKUP_UART0_RTSn**	WKUP_TIMER_IO1		MCU_SPI1_CLK				MCU_GPIO0_12		
143	WKUP_UART0_CTSn	C6	**WKUP_UART0_CTSn**	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11		
147	UART0_RXD	D14	**UART0_RXD**	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A				GPIO1_20		
149	UART0_TXD	E14	**UART0_TXD**	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B				GPIO1_21		
151	MCU_UART0_RXD	B5	**MCU_UART0_RXD**							MCU_GPIO0_5		
153	MCU_UART0_TXD	A5	**MCU_UART0_TXD**							MCU_GPIO0_6		
155	USB0_DRVVBUS	C20	**USB0_DRVVBUS**							GPIO1_50		
157	MMC2_SDCD	A23	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD				**GPIO0_71**		
159	USB0_VBUS	AC11	**USB0_VBUS**									
161	SPI0_D1	B14	SPI0_D1	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM_TZn_IN0					**GPIO1_19**		
163	USB0_DM	AE11	**USB0_DM**									

Continued on next page

Table 12: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *ALW package*	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
165	USB0_DP	AD11	**USB0_DP**									
181	USB1_DM	AD10	**USB1_DM**									
183	USB1_DP	AE9	**USB1_DP**									
185	USB1_DRVVBUS	F18	**USB1_DRVVBUS**							GPIO1_51		
187	MMC2_SDWP	B23	MMC2_SDWP	MCASP1_AFSX		UART4_TXD				**GPIO0_72**		
189	GPMC0_WAIT1	V25	GPMC0_WAIT1	VOUT0_EXTPCLKIN	GPMC0_A21	UART6_RXD				**GPIO0_38**	EQEP2_I	
191	MDIO0_MDIO	AB22	**MDIO0_MDIO**							GPIO0_85		
193	MDIO0_MDC	AD24	**MDIO0_MDC**							GPIO0_86		
197	RGMII2_RXC	AD23	**RGMII2_RXC**	RMII2_REF_CLK	MCASP2_AXR1	PR0_PRU0_GPO1	PR0_PRU0_GPI1	PR0_ECAP0_SYNC_IN		GPIO1_2		
199	RGMII2_RX_CTL	AD22	**RGMII2_RX_CTL**	RMII2_RX_ER	MCASP2_AXR3	PR0_PRU0_GPO0	PR0_PRU0_GPI0			GPIO1_1		
201	RGMII2_RD0	AE23	**RGMII2_RD0**	RMII2_RXD0	MCASP2_AXR2	PR0_PRU0_GPO2	PR0_PRU0_GPI2		PR0_UART0_RTSn	GPIO1_3		
203	RGMII2_RD1	AB20	**RGMII2_RD1**	RMII2_RXD1	MCASP2_AFSR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	MCASP2_AXR7		GPIO1_4		
205	RGMII2_RD2	AC21	**RGMII2_RD2**		MCASP2_AXR0	PR0_PRU0_GPO4	PR0_PRU0_GPI4	PR0_UART0_RXD		GPIO1_5	EQEP2_A	
207	RGMII2_RD3	AE22	**RGMII2_RD3**		AUDIO_EXT_REFCLK0	PR0_PRU0_GPO16	PR0_PRU0_GPI16	PR0_UART0_TXD		GPIO1_6	EQEP2_B	
211	RGMII2_TX_CTL	AA19	**RGMII2_TX_CTL**	RMII2_TX_EN	MCASP2_AXR4	PR0_PRU1_GPO0	PR0_PRU1_GPI0			GPIO0_87		
213	RGMII2_TXC	AE21	**RGMII2_TXC**	RMII2_CRS_DV	MCASP2_AXR5	PR0_PRU1_GPO1	PR0_PRU1_GPI1			GPIO0_88		
215	RGMII2_TD3	AC20	**RGMII2_TD3**		MCASP2_ACLKX	PR0_PRU1_GPO16	PR0_PRU1_GPI16	PR0_ECAP0_SYNC_OUT	PR0_UART0_CTSn	GPIO1_0	EQEP2_S	
217	RGMII2_TD2	AD21	**RGMII2_TD2**		MCASP2_AFSX	PR0_PRU1_GPO4	PR0_PRU1_GPI4	PR0_ECAP0_IN_APWM_OUT		GPIO0_91	EQEP2_I	
219	RGMII2_TD1	AA18	**RGMII2_TD1**	RMII2_TXD1	MCASP2_ACLKR	PR0_PRU1_GPO3	PR0_PRU1_GPI3	MCASP2_AXR8		GPIO0_90		
221	RGMII2_TD0	Y18	**RGMII2_TD0**	RMII2_TXD0	MCASP2_AXR6	PR0_PRU1_GPO2	PR0_PRU1_GPI2			GPIO0_89		
12	I2C1_SDA	A17	**I2C1_SDA**	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO	DDR0_IO_PLL_REFCLK_TEST0P	DDR0_IO_PLL_REFCLK_TEST1P	GPIO1_29	EHRPWM2_B	MMC2_SDWP
14	I2C1_SCL	B17	**I2C1_SCL**	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI	DDR0_IO_PLL_TESTOUT0P	DDR0_IO_PLL_TESTOUT1P	GPIO1_28	EHRPWM2_A	MMC2_SDCD
16	SPI0_CS1	C13	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	**EHRPWM0_B**	ECAP0_IN_APWM_OUT				GPIO1_16		EHRPWM_TZn_IN5

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Table 12: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *ALW package*	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
20	MCAN0_TX	C15	**MCAN0_TX**	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I	PR0_UART0_RXD	GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3
22	MCAN0_RX	E15	**MCAN0_RX**	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S	PR0_UART0_TXD	GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4
24	MCU_MCAN0_TX	D6	**MCU_MCAN0_TX**	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13		
26	MCU_MCAN0_RX	B3	**MCU_MCAN0_RX**	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14		
30	MCASP0_ACLKX	B20	**MCASP0_ACLKX**	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A	
32	MCASP0_AFSX	D20	**MCASP0_AFSX**	SPI2_CS3	AUDIO_EXT_REFCLK1					GPIO1_12	EQEP1_B	
34	MCASP0_AXR0	E18	**MCASP0_AXR0**	PR0_ECAP0_IN_APWM_OUT	AUDIO_EXT_REFCLK0			PR0_UART0_TXD	EHRPWM1_B	GPIO1_10	EQEP0_I	
36	MCASP0_AXR1	B18	**MCASP0_AXR1**	SPI2_CS2	ECAP1_IN_APWM_OUT			PR0_UART0_RXD	EHRPWM1_A	GPIO1_9	EQEP0_S	
42	GPMC0_BE0n_CLE	M24	GPMC0_BE0n_CLE		**MCASP1_ACLKX**		PR0_PRU0_GPO12	PR0_PRU0_GPI12	TRC_DATA10	GPIO0_35		
44	GPMC0_WAIT0	U23	GPMC0_WAIT0		**MCASP1_AFSX**		PR0_PRU0_GPO14	PR0_PRU0_GPI14	TRC_DATA12	GPIO0_37		
46	GPMC0_WEn	L25	GPMC0_WEn		**MCASP1_AXR0**		PR0_PRU0_GPO11	PR0_PRU0_GPI11	TRC_DATA9	GPIO0_34		
48	GPMC0_OEn_REn	L24	GPMC0_OEn_REn		**MCASP1_AXR1**		PR0_PRU0_GPO10	PR0_PRU0_GPI10	TRC_DATA8	GPIO0_33		
52	OSPI0_CLK	H24	**OSPI0_CLK**							GPIO0_0		
54	OSPI0_CSn0	F23	**OSPI0_CSn0**							GPIO0_11		
56	OSPI0_D0	E25	**OSPI0_D0**							GPIO0_3		
58	OSPI0_D1	G24	**OSPI0_D1**							GPIO0_4		
60	OSPI0_D2	F25	**OSPI0_D2**							GPIO0_5		
62	OSPI0_D3	F24	**OSPI0_D3**							GPIO0_6		
64	OSPI0_CSn1	G21	**OSPI0_CSn1**							GPIO0_12		
66	SPI0_D0	B13	SPI0_D0	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B					GPIO1_18		
70	MMC1_DAT2	C21	**MMC1_DAT2**	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD				GPIO1_43		
72	MMC1_DAT3	D22	**MMC1_DAT3**	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD				GPIO1_42		
74	MMC1_CMD	A21	**MMC1_CMD**		TIMER_IO5	UART3_TXD				GPIO1_47		

Continued on next page

Table 12: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *ALW package*	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
76	GPMC0_AD14	U25	GPMC0_AD14	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA20	**GPIO0_29**	UART2_CTSn	
78	MMC1_CLK	B22	**MMC1_CLK**		TIMER_IO4	UART3_RXD				GPIO1_46		
80	MMC1_DAT0	A22	**MMC1_DAT0**	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_APWM_OUT			GPIO1_45		
82	MMC1_DAT1	B21	**MMC1_DAT1**	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APWM_OUT			GPIO1_44		
84	MMC1_SDCD	D17	**MMC1_SDCD**	UART6_RXD	TIMER_IO6	UART3_RTSn				GPIO1_48		
88	OLDI0_CLK0N	AD4	OLDI0_CLK0N									
90	OLDI0_CLK0P	AE3	OLDI0_CLK0P									
94	OLDI0_A0N	AA5	OLDI0_A0N									
96	OLDI0_A0P	Y6	OLDI0_A0P									
100	OLDI0_A1N	AD3	OLDI0_A1N									
102	OLDI0_A1P	AB4	OLDI0_A1P									
106	OLDI0_A2N	Y8	OLDI0_A2N									
108	OLDI0_A2P	AA8	OLDI0_A2P									
112	OLDI0_A3N	AB6	OLDI0_A3N									
114	OLDI0_A3P	AA7	OLDI0_A3P									
116	MCU_MCAN1_RX	D4	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16		
118	OLDI0_CLK1N	AE4	OLDI0_CLK1N									
120	OLDI0_CLK1P	AD5	OLDI0_CLK1P									
124	OLDI0_A4N	AC6	OLDI0_A4N									
126	OLDI0_A4P	AC5	OLDI0_A4P									
128	MCU_MCAN1_TX	E5	MCU_MCAN1_TX	MCU_TIMER_IO2		MCU_SPI1_CS1	MCU_EXT_REFCLK0			MCU_GPIO0_15		
130	OLDI0_A5N	AE5	OLDI0_A5N									
132	OLDI0_A5P	AD6	OLDI0_A5P									

Continued on next page

Table 12: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *ALW package*	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
136	OLDI0_A6N	AE6	OLDI0_A6N									
138	OLDI0_A6P	AD7	OLDI0_A6P									
142	OLDI0_A7N	AD8	OLDI0_A7N									
144	OLDI0_A7P	AE7	OLDI0_A7P									
156	MMC2_CLK	D25	MMC2_CLK	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD				GPIO0_69		
160	MMC2_CMD	C24	MMC2_CMD	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD				GPIO0_70		
162	MMC2_DAT0	B24	MMC2_DAT0	MCASP1_AXR0						GPIO0_68		
164	MMC2_DAT1	C25	MMC2_DAT1	MCASP1_AXR1						GPIO0_67		
166	MMC2_DAT2	E23	MMC2_DAT2	MCASP1_AXR2		UART5_TXD				GPIO0_66		
168	MMC2_DAT3	D24	MMC2_DAT3	MCASP1_AXR3		UART5_RXD				GPIO0_65		
172	WiFi_BT_WKUP_HOST#	GPMC0_AD1	GPMC0_AD1	PR0_PRU1_GPO9	PR0_PRU1_GPI9	MCASP2_AXR5	PR0_PRU0_GPO1	PR0_PRU0_GPI1	TRC_CTL	GPIO0_16		
174	WiFi_W_WKUP_HOST#	GPMC0_AD0	GPMC0_AD0	PR0_PRU1_GPO8	PR0_PRU1_GPI8	MCASP2_AXR4	PR0_PRU0_GPO0	PR0_PRU0_GPI0	TRC_CLK	GPIO0_15		
184	OSPI0_DQS	J24	OSPI0_DQS					UART5_CTSn		GPIO0_2		
186	OSPI0_LBCLKO	G25	OSPI0_LBCLKO					UART5_RTSn		GPIO0_1		
190	OSPI0_CSn3	E24	OSPI0_CSn3	OSPI0_RESET_OUT0	OSPI0_ECC_FAIL	MCASP1_ACLKR	MCASP1_AXR3	UART5_TXD		GPIO0_14		
192	OSPI0_CSn2	H21	OSPI0_CSn2	SPI1_CS1	OSPI0_RESET_OUT1	MCASP1_AFSR	MCASP1_AXR2	UART5_RXD		GPIO0_13		
196	OSPI0_D5	J25	OSPI0_D5	**SPI1_CLK**	MCASP1_AXR0	UART6_TXD				GPIO0_8		
198	OSPI0_D7	J22	OSPI0_D7	**SPI1_D1**	MCASP1_AFSX	UART6_CTSn				GPIO0_10		
200	OSPI0_D6	H25	OSPI0_D6	**SPI1_D0**	MCASP1_ACLKX	UART6_RTSn				GPIO0_9		
202	OSPI0_D4	J23	OSPI0_D4	**SPI1_CS0**	MCASP1_AXR1	UART6_RXD				GPIO0_7		
206	MCU_SPI0_CS1	B8	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			**MCU_GPIO0_1**		
208	MCU_SPI0_CLK	A7	MCU_SPI0_CLK							**MCU_GPIO0_2**		
210	MCU_SPI0_D0	D9	MCU_SPI0_D0							**MCU_GPIO0_3**		

Continued on next page

Table 12: Alternate functions X1 pin assignment: odd pins (top) – even pins (bottom) (Continued)

X1 pin	SoC ball name	SoC ball ID *ALW package*	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
212	MCU_SPI0_D1	C9	MCU_SPI0_D1							**MCU_GPIO0_4**		
216	GPMC0_DIR	M22	GPMC0_DIR	PR0_ECAP0_IN_APWM_OUT		MCASP2_AXR13	PR0_PRU0_GPO16	PR0_PRU0_GPI16	TRC_DATA14	**GPIO0_40**	EQEP2_S	
218	GPMC0_BE1n	N20	GPMC0_BE1n			MCASP2_AXR12	PR0_PRU0_GPO13	PR0_PRU0_GPI13	TRC_DATA11	**GPIO0_36**		
220	GPMC0_CSn0	M21	GPMC0_CSn0			MCASP2_AXR14	PR0_PRU0_GPO17	PR0_PRU0_GPI17	TRC_DATA15	**GPIO0_41**		
222	GPMC0_CSn1	L21	GPMC0_CSn1	PR0_PRU1_GPO16	PR0_PRU1_GPI16	MCASP2_AXR15	PR0_PRU0_GPO18	PR0_PRU0_GPI18	TRC_DATA16	**GPIO0_42**		
244	MCU_SPI0_CS0	E8	MCU_SPI0_CS0				WKUP_TIMER_IO1			**MCU_GPIO0_0**		
252	GPMC0_ADVn_ALE	L23	GPMC0_ADVn_ALE		MCASP1_AXR2		PR0_PRU0_GPO9	PR0_PRU0_GPI9	TRC_DATA7	**GPIO0_32**		
256	GPMC0_CLK	P25	GPMC0_CLK		MCASP1_AXR3	GPMC0_FCLK_MUX	PR0_PRU0_GPO8	PR0_PRU0_GPI8	TRC_DATA6	**GPIO0_31**		

***Bold** text*: Alternate function which provides maximum compatibility between modules of the same family.
Rows in : "Module-specific" interface.
Rows in : "Boot source selection pin at startup (also "Module-specific").

4.2.2 PRUSS Interfaces

The PRUSS has a second signal multiplexer.
The PRUSS contains a second layer of peripheral signal multiplexing to enable additional functionality on the PRU GPO and GPI signals.

Table 13: X1-connected PRUSS I/O alternate functions

SoC signal	X1 pin	Description
ECAP		**Every signal available**
PR0_ECAP0_IN_APWM_OUT	34 ALT1 93 ALT6 216 ALT1 217 ALT5	
PR0_ECAP0_SYNC_IN	15 ALT6 197 ALT5	
PR0_ECAP0_SYNC_OUT	95 ALT6 215 ALT5	
GPI		**Some signals available**
PR0_PRU0_GPI0	199 ALT4	General purpose input 0 from PRU 0
PR0_PRU0_GPI1	197 ALT4	General purpose input 1 from PRU 0
PR0_PRU0_GPI2	76 ALT5 201 ALT4	General purpose input 2 from PRU 0
PR0_PRU0_GPI3	21 ALT5 203 ALT4	General purpose input 3 from PRU 0
PR0_PRU0_GPI4	205 ALT4	General purpose input 4 from PRU 0
PR0_PRU0_GPI8	256 ALT5	General purpose input 8 from PRU 0
PR0_PRU0_GPI9	252 ALT5	General purpose input 9 from PRU 0
PR0_PRU0_GPI10	48 ALT5	General purpose input 10 from PRU 0
PR0_PRU0_GPI11	46 ALT5	General purpose input 11 from PRU 0
PR0_PRU0_GPI12	42 ALT5	General purpose input 12 from PRU 0
PR0_PRU0_GPI13	218 ALT5	General purpose input 14 from PRU 0
PR0_PRU0_GPI14	44 ALT5	General purpose input 16 from PRU 0
PR0_PRU0_GPI16	207 ALT4 216 ALT5	General purpose input 16 from PRU 0
PR0_PRU0_GPI17	220 ALT5	General purpose input 17 from PRU 0
PR0_PRU0_GPI18	222 ALT5	General purpose input 18 from PRU 0
PR0_PRU0_GPI19	55 ALT5	General purpose input 19 from PRU 0
PR0_PRU1_GPI0	211 ALT4	General purpose input 0 from PRU 1
PR0_PRU1_GPI1	213 ALT4	General purpose input 1 from PRU 1
PR0_PRU1_GPI2	221 ALT4	General purpose input 2 from PRU 1
PR0_PRU1_GPI3	219 ALT4	General purpose input 3 from PRU 1
PR0_PRU1_GPI4	217 ALT4	General purpose input 4 from PRU 1
PR0_PRU1_GPI16	215 ALT4 222 ALT2	General purpose input 16 from PRU 1
GPO		**Some signals available**
PR0_PRU0_GPO0	199 ALT3	General purpose output 0 from PRU 0

Continued on next page

Table 13: X1-connected PRUSS I/O alternate functions (Continued)

SoC signal	X1 pin	Description
PR0_PRU0_GPO1	197 ALT3	General purpose output 1 from PRU 0
PR0_PRU0_GPO2	76 ALT4 201 ALT3	General purpose output 2 from PRU 0
PR0_PRU0_GPO3	21 ALT4 203 ALT3	General purpose output 3 from PRU 0
PR0_PRU0_GPO4	205 ALT3	General purpose output 4 from PRU 0
PR0_PRU0_GPO8	256 ALT4	General purpose output 8 from PRU 0
PR0_PRU0_GPO9	252 ALT4	General purpose output 9 from PRU 0
PR0_PRU0_GPO10	48 ALT4	General purpose output 10 from PRU 0
PR0_PRU0_GPO11	46 ALT4	General purpose output 11 from PRU 0
PR0_PRU0_GPO12	42 ALT4	General purpose output 12 from PRU 0
PR0_PRU0_GPO13	218 ALT4	General purpose output 13 from PRU 0
PR0_PRU0_GPO14	44 ALT4	General purpose output 14 from PRU 0
PR0_PRU0_GPO16	207 ALT3 216 ALT4	General purpose output 16 from PRU 0
PR0_PRU0_GPO17	220 ALT4	General purpose output 17 from PRU 0
PR0_PRU0_GPO18	222 ALT4	General purpose output 18 from PRU 0
PR0_PRU0_GPO19	55 ALT4	General purpose output 19 from PRU 0
PR0_PRU1_GPO0	211 ALT3	General purpose output 0 from PRU 1
PR0_PRU1_GPO1	213 ALT3	General purpose output 1 from PRU 1
PR0_PRU1_GPO2	221 ALT3	General purpose output 2 from PRU 1
PR0_PRU1_GPO3	219 ALT3	General purpose output 3 from PRU 1
PR0_PRU1_GPO4	217 ALT3	General purpose output 4 from PRU 1
PR0_PRU1_GPO16	215 ALT3 222 ALT1	General purpose output 16 from PRU 1
IEP		**Missing critical signals for proper use**
PR0_IEP0_EDIO_DATA_IN_OUT28	133 ALT4	
PR0_IEP0_EDIO_DATA_IN_OUT29	135 ALT4	
MDIO		**No pins available**
UART		**Every signal available**
PR0_UART0_TXD	22 ALT6 34 ALT5 133 ALT6 207 ALT5	PRUSS UART0 TX
PR0_UART0_RXD	20 ALT6 36 ALT5 135 ALT6 205 ALT5	PRUSS UART0 RX
PR0_UART0_RTSn	201 ALT6	PRUSS UART0 RTS
PR0_UART0_CTSn	215 ALT6	PRUSS UART0 CTS

5 Interface Description

5.1 ADC – Analog to Digital Converter

The Verdin AM62 has four analog inputs, with 0 to 3.3V input range, 12-bit resolution, and a sampling rate of up to 3300 samples per second. The analog inputs can be used in single-ended mode, or in differential mode with either ADC_1 or ADC_3 as inverted input.

The analog-to-digital conversion is handled by the TLA2024 ADC from Texas Instruments, as the AM62 SoC does not feature an analog-to-digital converter. The TLA2024 is a low-power delta-sigma ADC with integrated voltage reference and oscillator. See the TLA2024 Datasheet[2] for more information on the ADC functional modes, specifications, and register maps.

The AM62 SoC communicates with the TLA2024 ADC through the SoC's I2C0 I²C interface, with the ADC on address `0x49`. The I2C0 port is also shared with other peripherals such as the on-module PMIC, RTC, TPM, and EEPROM.

The ADC features a programmable gain amplifier, allowing input ranges from 256mV (0.125mV/LSB) to 3.3V (2mV/LSB). To use the 3.3V range, the Full-Scale Range (FSR) of the amplifier should be set to 4.096V, although the full 4.096V range is not achievable due to the amplifier's supply voltage of 3.3V.

Table 14: ADC voltage ranges

ADC FSR mode	Input voltage range	ADC resolution	Remark
±0.256 V	0 to 256 mV	0.125 mV/LSB	
±0.512 V	0 to 512 mV	0.25 mV/LSB	
±1.024 V	0 to 1.024 V	0.5 mV/LSB	
±2.048 V	0 to 2.048 V	1 mV/LSB	
±4.096 V	0 to 3.3 V	2 mV/LSB	Input voltage range is limited by ADC's supply voltage (3.3V)
±6.144 V	0 to 3.3 V	3 mV/LSB	Input voltage range is limited by ADC's supply voltage (3.3V)

To maintain compatibility with other Verdin modules, it is recommended to keep the analog signal voltages in the 0 to 1.8V range as per Verdin family specification. The differential input mode is not part of the Verdin standard and potentially not compatible with other modules.

The analog input pins are part of a reserved Verdin interface, with guaranteed electrical compatibility within modules of the Verdin family.

Table 15: ADC pins even pins (bottom)

X1 pin	Verdin spec. signal name	TLA2024 pin name	I/O *SoM perspective*	Description
2	ADC_1	AIN3	I	Analog input 1, may be also used as inverted input in differential mode with ADC_2, ADC_3, and ADC_4
4	ADC_2	AIN2	I	Analog input 2
6	ADC_3	AIN1	I	Analog input 3, may be also used as inverted input in differential mode with ADC_4
8	ADC_4	AIN0	I	Analog input 4

[2] https://www.ti.com/lit/ds/symlink/tla2024.pdf

5.2 Display

The Verdin AM62 supports up to two displays while providing independent video pipelines, overlay managers, and video port output processors. The LVDS interface is available as a "module-specific" interface, while the DSI interface is a "reserved" interface provided by the Toshiba TC9594XBG bridge.

The module is capable of driving two 1920×1080p displays at 60fps, although a lower resolution is recommended for the secondary display – such as 1280×720p – due to DDR bandwidth constraints.

The TI AM62x SoC display subsystem offloads some of the GPU work by leveraging features such as multi-layer blending with transparency to enable on-the-fly composition, various pixel processing capabilities such as color space conversion and scaling, and the display subsystem DMA engine allows direct access to the frame buffer in the device system memory.

5.2.1 DSI

The DSI interface is not available on some product variants.
See the DSI availability on the Interfaces table (Table 3 on page 7) on the *MIPI DSI* row.

Some Verdin AM62 variants support DSI video output via the Toshiba TC9594XBG Parallel Port (RGB) to MIPI DSI bridge, attached to the Display Parallel Interface of the SoC. The DSI bridge is compliant to the MIPI DSI standard version 1.02.

The DSI interface supports 16, 18, and 24-bit color modes. The 24-bit mode has an image color depth of 18 bits (same depth of the 18-bit mode), as the 2 LSBs of each color channel copy the 2 MSBs.

The DSI bridge provides up-to 4 data lanes, each capable of up-to 1Gbps. Bi-directional data transmission is available on lane 0. Other signals such as backlight brightness control, display interrupt, and I2C display control are provided directly by the SoC.

The DSI bridge is configured in I^2C mode and may be accessed through the I2C0 interface on address `0x0E`. This I2C interface is shared with the PMIC and other peripherals.

Modifying the SoC CLKOUT0 frequency is strongly discouraged.
The DSI bridge shares the REFCLK clock signal with the Ethernet PHY (XI pin), which expects a 25MHz signal.

The DSI signals are split into 3 tables:

SoC ⇔ X1 on Table 16
Bridge ⇔ X1 on Table 17
SoC ⇔ Bridge on Table 18

Table 16: SoC DSI signals – X1 alternate functions

X1 pin	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
17	MMC1_SDWP	ALT7	GPIO1_49	I	Display interrupt input, intended to be used as hot-plug detect or for interrupt messages from DSI bridges on carrier board
19 36	SPI0_CLK MCASP0_AXR1	ALT2 ALT6	EHRPWM1_A	O	Display backlight brightness control
21	GPMC0_AD15	ALT7	GPIO0_30	O	Display backlight enable
53	GPMC0_CSn3	ALT1	I2C2_SDA	I/O	DSI bridge I2C data
55	GPMC0_CSn2	ALT1	I2C2_SCL	I/O	DSI bridge I2C clock

Table 17: DSI bridge signals – X1 alternate functions

X1 pin	TC9594XBG pin name	I/O *SoM perspective*	Description
DSI clock			
35	DSI_1_CLK_N	O	DSI clock N
37	DSI_1_CLK_P	O	DSI clock P
DSI data			
23	DSI_1_D3_N	O	DSI data lane 3, N signal
25	DSI_1_D3_P	O	DSI data lane 3, P signal
29	DSI_1_D2_N	O	DSI data lane 2, N signal
31	DSI_1_D2_P	O	DSI data lane 2, P signal
41	DSI_1_D1_N	O	DSI data lane 1, N signal
43	DSI_1_D1_P	O	DSI data lane 1, P signal
47	DSI_1_D0_N	I/O	DSI data lane 0, N signal
49	DSI_1_D0_P	I/O	DSI data lane 0, P signal

Table 18: DSI bridge signals – SoC

TC9594XBG pin name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
Bridge control					
I2C_SCL	I2C0_SCL	ALT0	I2C0_SCL	I/O	Bridge I2C clock
I2C_SDA	I2C0_SDA	ALT0	I2C0_SDA	I/O	Bridge I2C data
REFCLK	EXT_REFCLK1	ALT5	CLKOUT0	O	25MHz reference clock
RESX	GPMC0_AD5	ALT7	GPIO0_20	O	Bridge reset *active low*
Parallel input control					
VSYNC	VOUT0_VSYNC	ALT0	VOUT0_VSYNC	O	VSYNC signal
HSYNC	VOUT0_HSYNC	ALT0	VOUT0_HSYNC	O	HSYNC signal
DE	VOUT0_DE	ALT0	VOUT0_DE	O	DE signal
PCLK	VOUT0_PCLK	ALT0	VOUT0_PCLK	O	PCLK signal
Parallel input data					
PD0	VOUT0_DATA4	ALT0	VOUT0_DATA4	O	Parallel data 0
PD1	VOUT0_DATA5	ALT0	VOUT0_DATA5	O	Parallel data 1
PD2	VOUT0_DATA0	ALT0	VOUT0_DATA0	O	Parallel data 2
PD3	VOUT0_DATA1	ALT0	VOUT0_DATA1	O	Parallel data 3
PD4	VOUT0_DATA2	ALT0	VOUT0_DATA2	O	Parallel data 4
PD5	VOUT0_DATA3	ALT0	VOUT0_DATA3	O	Parallel data 5
PD6	VOUT0_DATA4	ALT0	VOUT0_DATA4	O	Parallel data 6
PD7	VOUT0_DATA5	ALT0	VOUT0_DATA5	O	Parallel data 7
PD8	VOUT0_DATA10	ALT0	VOUT0_DATA10	O	Parallel data 8
PD9	VOUT0_DATA11	ALT0	VOUT0_DATA11	O	Parallel data 9

Continued on next page

Table 18: DSI bridge signals – SoC (Continued)

TC9594XBG pin name	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
PD10	VOUT0_DATA6	ALT0	VOUT0_DATA6	O	Parallel data 10
PD11	VOUT0_DATA7	ALT0	VOUT0_DATA7	O	Parallel data 11
PD12	VOUT0_DATA8	ALT0	VOUT0_DATA8	O	Parallel data 12
PD13	VOUT0_DATA9	ALT0	VOUT0_DATA9	O	Parallel data 13
PD14	VOUT0_DATA10	ALT0	VOUT0_DATA10	O	Parallel data 14
PD15	VOUT0_DATA11	ALT0	VOUT0_DATA11	O	Parallel data 15
PD16	VOUT0_DATA16	ALT0	VOUT0_DATA16	O	Parallel data 16
PD17	VOUT0_DATA17	ALT0	VOUT0_DATA17	O	Parallel data 17
PD18	VOUT0_DATA12	ALT0	VOUT0_DATA12	O	Parallel data 18
PD19	VOUT0_DATA13	ALT0	VOUT0_DATA13	O	Parallel data 19
PD20	VOUT0_DATA14	ALT0	VOUT0_DATA14	O	Parallel data 20
PD21	VOUT0_DATA15	ALT0	VOUT0_DATA15	O	Parallel data 21
PD22	GPMC0_AD8	ALT1	VOUT0_DATA16	I[1]/O	Parallel data 22
PD23	GPMC0_AD9	ALT1	VOUT0_DATA17	I[1]/O	Parallel data 23

[1] SoC pin used as input while booting.

5.2.2 LVDS

The native LVDS signals are located on module-specific pins.
Using module-specific interfaces may prevent compatibility with other Verdin modules. If a LVDS display is used and compatibility with other modules from Verdin Family is required, a MIPI DSI to LVDS bridge on the carrier board should be considered.

The Verdin AM62 supports native LVDS video output at up-to 24-bit color depth through the Open LVDS Display Interface (OLDI) on the SoC (OLDITX0), providing 8 data lanes (pairs) split into 2 channels. The SoC OLDITX1 interface is not available on the X1 connector.

A single channel LVDS interface can support resolutions up to 1920×1080p at 60 frames per second (165MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual-channel configuration, the odd bits are transmitted in the first channel, and the even bits are sent in the second channel.

The LVDS interface is classified as “module-specific”, meaning it may not be present on other modules or even when present it may not share the same pins, although we try to keep module-specific interfaces on the same pins to improve module compatibility.

The ammount of active data lanes depend on the selected data format. A list with the correlation between active lanes and selected mode can be found on Table 20 on page 47. Detailed information about color mappings and signal timings can be found on the TI AM62x SoC Technical Reference Manual[3].

[3] https://www.ti.com/lit/ug/spruiv7b/spruiv7b.pdf

Table 19: LVDS signals – X1 alternate functions

X1 pin	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
Channel 0					
88	OLDI0_CLK0N	ALT0	OLDI0_CLK0N	O	LVDS clock lane, N polarity signal, channel 0
90	OLDI0_CLK0P	ALT0	OLDI0_CLK0P	O	LVDS clock lane, P polarity signal, channel 0
94	OLDI0_A0N	ALT0	OLDI0_A0N	O	LVDS data lane 0, N polarity signal, channel 0
96	OLDI0_A0P	ALT0	OLDI0_A0P	O	LVDS data lane 0, P polarity signal, channel 0
100	OLDI0_A1N	ALT0	OLDI0_A1N	O	LVDS data lane 1, N polarity signal, channel 0
102	OLDI0_A1P	ALT0	OLDI0_A1P	O	LVDS data lane 1, P polarity signal, channel 0
106	OLDI0_A2N	ALT0	OLDI0_A2N	O	LVDS data lane 2, N polarity signal, channel 0
108	OLDI0_A2P	ALT0	OLDI0_A2P	O	LVDS data lane 2, P polarity signal, channel 0
112	OLDI0_A3N	ALT0	OLDI0_A3N	O	LVDS data lane 3, N polarity signal, channel 0
114	OLDI0_A3P	ALT0	OLDI0_A3P	O	LVDS data lane 3, P polarity signal, channel 0
Channel 1					
118	OLDI0_CLK1N	ALT0	OLDI0_CLK1N	O	LVDS clock lane, N polarity signal, channel 1
120	OLDI0_CLK1P	ALT0	OLDI0_CLK1P	O	LVDS clock lane, P polarity signal, channel 1
124	OLDI0_A4N	ALT0	OLDI0_A4N	O	LVDS data lane 0, N polarity signal, channel 1
126	OLDI0_A4P	ALT0	OLDI0_A4P	O	LVDS data lane 0, P polarity signal, channel 1
130	OLDI0_A5N	ALT0	OLDI0_A5N	O	LVDS data lane 1, N polarity signal, channel 1
132	OLDI0_A5P	ALT0	OLDI0_A5P	O	LVDS data lane 1, P polarity signal, channel 1
136	OLDI0_A6N	ALT0	OLDI0_A6N	O	LVDS data lane 2, N polarity signal, channel 1
138	OLDI0_A6P	ALT0	OLDI0_A6P	O	LVDS data lane 2, P polarity signal, channel 1
142	OLDI0_A7N	ALT0	OLDI0_A7N	O	LVDS data lane 3, N polarity signal, channel 1
144	OLDI0_A7P	ALT0	OLDI0_A7P	O	LVDS data lane 3, P polarity signal, channel 1

Table 20: LVDS modes × Active lanes

Signal pair	Single channel 16-bit	Single channel 24-bit	Dual channel 16-bit	Dual channel 24-bit
Channel 0				
Ch. 0 Clock	Yes	Yes	Yes	Yes
Ch. 0 Data 0	Yes	Yes	Yes	Yes
Ch. 0 Data 1	Yes	Yes	Yes	Yes
Ch. 0 Data 2	Yes	Yes	Yes	Yes
Ch. 0 Data 3	No	Yes	No	Yes
Channel 1				
Ch. 1 Clock	No	No	Yes	Yes
Ch. 1 Data 0	No	No	Yes	Yes
Ch. 1 Data 1	No	No	Yes	Yes
Ch. 1 Data 2	No	No	Yes	Yes
Ch. 1 Data 3	No	No	No	Yes

5.3 eFuse

eFuse programing requires specific power-up sequence and software.
The eFuse programming on the Verdin AM62 requires the SoC VPP (pin 104, MSP_8) to be driven at 1.8V ±5% after the SoC is powered up, and may consume up to 400mA.
The eFuse programming software is provided by TI.

The TI AM62x One-Time Programmable eFuses may be used to configure the MAC address, security keys, or provide reset values to some registers.

If you are not planning to use eFuses, the MSP_8 signal (X1 pin 104) may be left unconnected. Otherwise, it should be driven to 0V when not programming the eFuses. More information on eFuse programming can be found on the TI AM62x SoC Datasheet[4].

[4] https://www.ti.com/lit/ds/sprsp58b/sprsp58b.pdf

5.4 GPIOs

The SoC does not support level-triggered interrupts.
The TI AM62x GPIOs only support edge-triggered interrupts, which may be configured to trigger on rising-edge, falling-edge, or both edges. See the *Interrupt and Event Generation* section on the TI AM62x Technical Reference Manual for more information on GPIO interrupts.

The Verdin form factor features ten dedicated general-purpose input-output (GPIO) pins. Four are reserved for the MIPI CSI camera interface and two for the MIPI DSI display interface. Besides these 10 GPIOs, several pins can be used as GPIO if their primary function is not used. For compatibility reasons, it is recommended to use the ten dedicated GPIOs first.

Table 21: Dedicated GPIOs alternate functions

X1 pin	Verdin specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
206	GPIO_1	MCU_SPI0_CS1	ALT7	MCU_GPIO0_1	I/O	
208	GPIO_2	MCU_SPI0_CLK	ALT7	MCU_GPIO0_2	I/O	
210	GPIO_3	MCU_SPI0_D0	ALT7	MCU_GPIO0_3	I/O	
212	GPIO_4	MCU_SPI0_D1	ALT7	MCU_GPIO0_4	I/O	
216	GPIO_5_CSI	GPMC0_DIR	ALT7	GPIO0_40	I/O	Reserved GPIO for MIPI CSI camera interface
218	GPIO_6_CSI	GPMC0_BE1n	ALT7	GPIO0_36	I/O	Reserved GPIO for MIPI CSI camera interface
220	GPIO_7_CSI	GPMC0_CSn0	ALT7	GPIO0_41	I/O	Reserved GPIO for MIPI CSI camera interface
222	GPIO_8_CSI	GPMC0_CSn1	ALT7	GPIO0_42	I/O	Reserved GPIO for MIPI CSI camera interface
17	GPIO_9_DSI	MMC1_SDWP	ALT7	GPIO1_49	I/O	Reserved GPIO for MIPI DSI display interface
21	GPIO_10_DSI	GPMC0_AD15	ALT7	GPIO0_30	I/O	Reserved GPIO for MIPI DSI display interface

5.4.1 GPIO Wakeup

The pin 252 on the X1 connector is the default wakeup source for the Verdin Family, and only this pin is guaranteed to be wakeup compatible with other Verdin modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Verdin modules.

See the available low power modes in Section 6.
The AM62x SoC supports four low power modes – Standby, MCU-Only, DeepSleep, and Partial I/O – which are explained in Section 6 on page 55.

Any GPIO may wake up the module from Standby state. This is not the case for the other low power modes such as Partial I/O, DeepSleep (suspend), and MCU-Only. The pin 252 is capable of waking up the SoC only from Standby mode.

Under Partial I/O low power mode, only CANUART I/O bank pins are capable of waking up the module. The CANUART pins available on X1 are listed on Table 22.

Table 22: Wake up pins – Partial I/O state alternate functions

X1 pin	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
24	MCU_MCAN0_TX	ALT7	MCU_GPIO0_13	I/O	CAN_2 TX
26	MCU_MCAN0_RX	ALT7	MCU_GPIO0_14	I/O	CAN_2 RX

Continued on next page

Table 22: Wake up pins – Partial I/O state alternate functions (Continued)

X1 pin	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
61	MCU_UART0_CTSn	ALT7	MCU_GPIO0_7	I/O	
63	MCU_UART0_RTSn	ALT7	MCU_GPIO0_8	I/O	
116	MCU_MCAN1_RX	ALT7	MCU_GPIO0_16	I/O	CAN_3 RX
128	MCU_MCAN1_TX	ALT7	MCU_GPIO0_15	I/O	CAN_3 TX
151	MCU_UART0_RXD	ALT7	MCU_GPIO0_5	I/O	UART_4 RX
153	MCU_UART0_TXD	ALT7	MCU_GPIO0_6	I/O	UART_4 TX

Under DeepSleep and MCU-Only, MCU_GPIO0 pins may wake up the module. The MCU_GPIO0 pins available on X1 are listed on Table 23.

Table 23: Wake up pins – DeepSleep state alternate functions

X1 pin	SoC ball name	SoC alternate function	SoC alternate function name	I/O *SoC perspective*	Description
24	MCU_MCAN0_TX	ALT7	MCU_GPIO0_13	I/O	CAN_2 TX
26	MCU_MCAN0_RX	ALT7	MCU_GPIO0_14	I/O	CAN_2 RX
57	MCU_I2C0_SDA	ALT7	MCU_GPIO0_18	I/O	I2C_3 SDA
59	MCU_I2C0_SCL	ALT7	MCU_GPIO0_17	I/O	I2C_3 SCL
61	MCU_UART0_CTSn	ALT7	MCU_GPIO0_7	I/O	
63	MCU_UART0_RTSn	ALT7	MCU_GPIO0_8	I/O	
91	WKUP_CLKOUT0	ALT7	MCU_GPIO0_23	I/O	CSI_1 MCLK
116	MCU_MCAN1_RX	ALT7	MCU_GPIO0_16	I/O	CAN_3 RX
128	MCU_MCAN1_TX	ALT7	MCU_GPIO0_15	I/O	CAN_3 TX
137	WKUP_UART0_RXD	ALT7	MCU_GPIO0_9	I/O	UART_2 RX
139	WKUP_UART0_TXD	ALT7	MCU_GPIO0_10	I/O	UART_2 TX
141	WKUP_UART0_RTSn	ALT7	MCU_GPIO0_12	I/O	UART_2 RTS
143	WKUP_UART0_CTSn	ALT7	MCU_GPIO0_11	I/O	UART_2 CTS
151	MCU_UART0_RXD	ALT7	MCU_GPIO0_5	I/O	UART_4 RX
153	MCU_UART0_TXD	ALT7	MCU_GPIO0_6	I/O	UART_4 TX
206	MCU_SPI0_CS1	ALT7	MCU_GPIO0_1	I/O	GPIO_1
208	MCU_SPI0_CLK	ALT7	MCU_GPIO0_2	I/O	GPIO_2
210	MCU_SPI0_D0	ALT7	MCU_GPIO0_3	I/O	GPIO_3
212	MCU_SPI0_D1	ALT7	MCU_GPIO0_4	I/O	GPIO_4
244	MCU_SPI0_CS0	ALT7	MCU_GPIO0_0	I/O	

5.5 Power

5.5.1 Digital Supply

The carrier board should supply the power to the SoM, through the X1 connector. The SoM uses a TPS65219 PMIC and a mix of switched and linear converters to feed the power rails.

Table 24: Power Supply pins

X1 pin	Verdin signal name	I/O	Description	Remarks
251, 253, 255, 257, 259	VCC	I	3.135V to 5.5V	Use decoupling capacitors on the carrier board
10, 11, 18, 27, 28, 33, 39, 40, 45, 50, 51, 65, 68, 71, 77, 83, 86, 89, 97, 98, 103, 109, 110, 115, 121, 122, 127, 134, 145, 146, 158, 167, 170, 173, 179, 182, 194, 195, 204, 209, 223, 224, 229, 230, 236, 242, 243	GND	I	Digital ground	
214	PWR_1V8_MOCI	O	1.8V output	Max. 250mA
249	VCC_BACKUP	I	RTC power supply backup battery	May be left unconnected

5.5.2 Analog Supply

The analog power rail is supplied by an LDO on the SoM, drawing power from the VCC rail. No external analog supplies are required.

5.5.3 Power Management Signals

Power sequence and timings are available in another document.
The power sequence to start up the module or to switch between power states, as well as the required timings, can be found on the Verdin Carrier Board Design Guide.

The power management signals allow the carrier board to power on/off, reset, and wake-up the module, and may force the module into recovery mode. The signals also indicate to the carrier board when to power off the main power rail and peripherals.

Table 25: Power Management pins

X1 pin	Verdin signal name	I/O	Description	Remarks
246	CTRL_RECOVERY_MICO#	I	1.8V OD	Shorting to the ground during power-up is setting the module into recovery mode. There is a 10k pull-up on the module. It can be left floating on the carrier board.
248	CTRL_PWR_BTN_MICO#	I	1.8V OD	Long[1] pulling down is shutting down the module. Short pulling down is turning on module from off state. Open-drain input with on-module 10k pull-up resistor to the 1.8V_STBY rail. It can be left floating on the carrier board.
250	CTRL_FORCE_OFF_MOCI#	O	5V OD	Output for forcing the turning-off of the main power rail. This signal needs to be ignored for the first 400ms during the power-up sequence. The signal is 5V tolerant. The carrier board can pull the signal up to 1.8V, 3.3V, or 5V. It can be left floating on the carrier board.

Continued on next page

Table 25: Power Management pins (Continued)

X1 pin	Verdin signal name	I/O	Description	Remarks
252	CTRL_WAKE1_MICO#	I	1.8V	Wake-capable pin, which allows you to resume from sleep mode. There are no pull resistors on the module. It can be left floating on the carrier board if the wake feature is disabled in the software. It is a regular SoC GPIO.
254	CTRL_PWR_EN_MOCI	O	1.8V	Enable signal for the power rails of the carrier board peripherals. This output remains high during sleep modes.
256	CTRL_SLEEP_MOCI#	O	1.8V	Enable signal for the power rails on the carrier board peripherals, which need to be turned off during sleep mode. It is only high during the running mode. The signal is standard GPIO with an on-module 10k pull-down resistor. The signal is defined during the power-up sequence. The signal can be left floating on the carrier board.
258	CTRL_RESET_MOCI#	O	3.3V OD	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# does not get asserted. The output is an open-drain type without a pull-up resistor on the module. The signal is 3.3V tolerant. The carrier board can pull the signal up to 1.8V or 3.3V. It can be left floating on the carrier board.
260	CTRL_RESET_MICO#	I	1.8V OD	Open-drain input, which resets the module if shorted to ground on carrier board. There is a 10k on-module pull-up to the 1.8V rail. This means it can be left floating on the carrier board.

[1] More than 5s.

5.6 Wi-Fi and Bluetooth

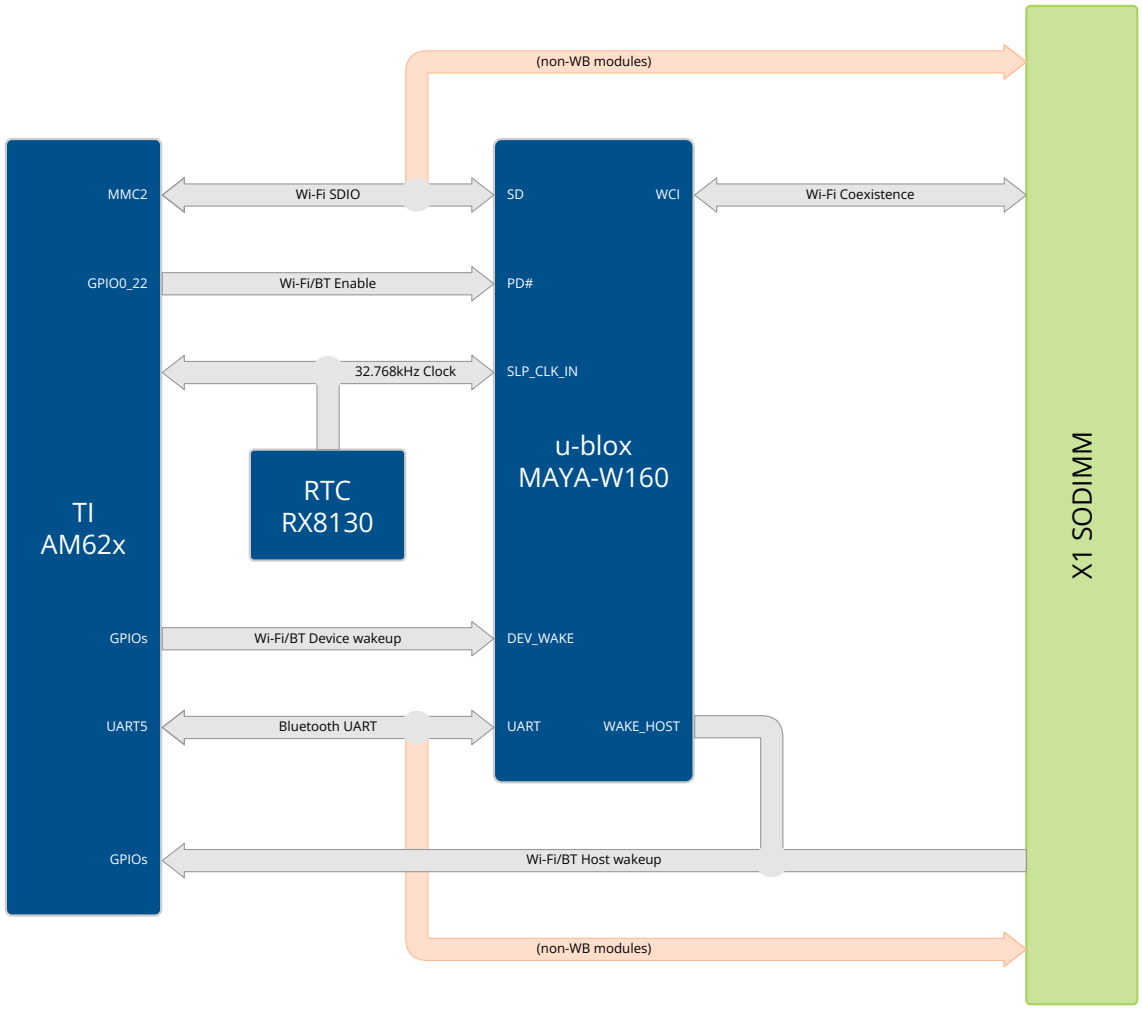
"WB" indicates Wi-Fi/Bluetooth.
The addition of "WB" in the product name indicates that a version features Wi-Fi and Bluetooth.

The Verdin AM62 is available with optional on-module Wi-Fi and Bluetooth interfaces. These Verdin module versions make use of the u-blox MAYA-W160-00B Host-based multiradio module based on the NXP IW416 SoC, capable of up to 150 Mbps (MCS7) data rate.

The Wi-Fi/BT module features:

- Wi-Fi 4 802.11n dual-band
- Bluetooth classic and full-featured Bluetooth Low Energy 5.2
- Support for long range Bluetooth Low Energy
- Access-point up to eight stations
- Wi-Fi direct
- Two separate U.FL connectors for Wi-Fi and Bluetooth

Figure 4: Wi-Fi/BT Block Diagram



The Wi-Fi/BT module requires external antennas.
The u-blox MAYA-W160-00B needs two U.FL external antennas for Wi-Fi and Bluetooth. The MHF-4 antennas used by some modules are not compatible with the U.FL connectors.

The Wi-Fi module is connected over a 4-bit SDIO interface with the TI AM62x Sitara SoC. It uses the MMC2 instance of the SoC. The sleep clock input (SLP_CLK_IN) is provided by the RTC (32.768kHz).

Table 26: Wi-Fi/BT module signals – SoC

MAYA W160 pin name	SoC ball name	SoC alternate function name	I/O *SoC perspective*	Description
PD#	GPMC0_AD7	GPIO0_22	O	Power down of complete Wi-Fi/BT module (active low). Firmware needs to be re-downloaded after powering on again.
SD_CLK	MMC2_CLK	MMC2_CLK	O	SDIO clock
SD_CMD	MMC2_CMD	MMC2_CMD	I/O	SDIO command
SD_DAT0	MMC2_DAT0	MMC2_DAT0	I/O	SDIO data 0
SD_DAT1	MMC2_DAT1	MMC2_DAT1	I/O	SDIO data 1
SD_DAT2	MMC2_DAT2	MMC2_DAT2	I/O	SDIO data 2
SD_DAT3	MMC2_DAT3	MMC2_DAT3	I/O	SDIO data 3
UART_SIN	OSPI0_CSn3	UART5_TXD	O	UART serial data in
UART_SOUT	OSPI0_CSn2	UART5_RXD	I	UART serial data out
UART_RTSn	OSPI0_LBCLKO	UART5_RTSn	I	UART RTS (active low)
UART_CTSn	OSPI0_DQS	UART5_CTSn	O	UART CTS (active low)
WLAN_DEV_WAKE	GPMC0_AD12	GPIO0_27	O	Wi-Fi transceiver wake-up
BT_DEV_WAKE	GPMC0_AD11	GPIO0_26	O	Bluetooth transceiver wake-up
WLAN_WAKE_HOST[1]	GPMC0_AD0	GPIO0_15	I	Wi-Fi transceiver to SoC wake-up
BT_WAKE_HOST[1]	GPMC0_AD1	GPIO0_16	I	Bluetooth transceiver to SoC wake-up

[1] This signal is also available on X1 connector, see Table 27.

Table 27: Wi-Fi/BT module signals – X1 alternate functions

MAYA W160 pin name	X1 pin name	I/O *SoM perspective*	Description
BT_WAKE_HOST	MSP_36	I[1]/O	Bluetooth transceiver to SoC wake-up
WLAN_WAKE_HOST	MSP_37	I[1]/O	Wi-Fi transceiver to SoC wake-up
WCI_SIN	MSP_39	I	WCI-2 serial interface
WCI_SOUT	MSP_40	O	WCI-2 serial interface

[1] On modules without Wi-Fi/BT.

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. More information can be found on our developer website[5].

[5] https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products

6 Low Power Modes

Disable SoM ICs to save more power.
The SoC low power modes do not affect other ICs on the SoM, such as the Wi-Fi/Bluetooth module. To achieve minimum power consumption, first disable the other ICs on the SoM then enable a low power mode on the SoC.

The TI AM62x SoC is capable of four low power modes. The most aggressive low power mode – Partial I/O – disables the entire SoC except the CANUART I/O pins to maintain wakeup capability. More information on the AM62x Low Power Modes can be found on TI's Enabling Low Power Embedded Systems With AM62x Processors[6] Technical White Paper.

Table 28 contains a brief description of each low power mode.

Table 28: SoC low power modes

Mode	Description
Partial I/O	The entire SoC is OFF except I/O pins in CANUART I/O bank.
DeepSleep	Used for suspend to RAM.
MCU-Only	The system is in DeepSleep except the MCU subsystem.
Standby	A53 and M4F are in WFI or power down, any interrupt event is capable of waking up the SoC.

[6] https://www.ti.com/lit/wp/sprad41/sprad41.pdf

7 Recovery Mode

The recovery mode (USB loader) can be used to download new software to the Verdin AM62 even when the bootloader is no longer capable of booting the module. When the module is in recovery mode, the USB_1 interface connects it to a host computer. You may find additional information in our Developer Website under Recovery Mode[7].

The dedicated recovery pin (SODIMM pin 246) needs to be pulled down with ≤1kΩ during the initial power on (cold boot) of the module to enter recovery mode. The CTRL_RECOVERY_MICO# function on the SODIMM pin 246 is standardized in the Verdin module specifications. It is highly recommended to add at least a test point on the carrier board to the pin 246 to be able to enter recovery mode. There is no need for a pull-up resistor on the carrier board.

[7] https://developer.toradex.com/hardware/hardware-resources/recovery-mode/ti-am62x-recovery-mode/

8 Known Issues

Up-to-date information about all known hardware issues can be found in the errata document, which can be downloaded from our Developer Website under Verdin AM62[8].

[8] https://developer.toradex.com/hardware/verdin-som-family/modules/verdin-am62/#erratakown-issues

9 Technical Specifcations

9.1 Absolute Maximum Ratings

Table 29: Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
VCC	Main power supply	-0.3	6	V
VCC_BACKUP	RTC power supply	-0.3	6	V
IO_1.8V	SoC IO pins with 1.8V logic level	-0.3	2.1	V
IO_3.3V	SoC IO pins with 3.3V logic level (SDIO)	-0.3	3.6	V
ADC	ADC analog input	-0.3	3.6	V
USB_1_VBUS	Input voltage at USB_1_VBUS	-0.3	5.5	V

9.2 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website[9].

9.3 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Verdin product family. Following those recommendations ensures that the carrier board being designed will be compatible with all existing and future Verdin modules. For details, please refer to the Verdin Family Specification or the Verdin Carrier Board Design Guide.

Detailed information about the Verdin AM62 power consumption can be found on our Developer Website under Verdin AM62 Power Consumption[10]. Please note that scaling the carrier board power supplies for a particular module may cause compatibility issues with other existing and future modules within the Verdin family.

9.4 Power Ramp-Up Requirements

Backfeeding may prevent the module from powering up.
The PMIC is sensitive to residual voltages on the power rails and may halt in the boot sequence before ramping up the voltages.

The carrier board needs to follow the power supply ramp-up requirements of the Verdin module standard. This specification can be found in the Verdin Carrier Board Design Guide[11].

Extra care should be taken to reduce backfeeding, as the module will not power up when the residual voltages on the PMIC rails are greater than 220mV. Some HDMI displays are prone to back-feed through the TMDS channels.

[9] https://www.toradex.com/support/product-compliance
[10] https://developer.toradex.com/hardware/hardware-resources/power-consumption/verdin-am62-power-consumption/
[11] https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

9.5 Recommended Operation Conditions

Table 30: Recommended operation conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Main power supply	3.135	3.3 or 5	5.5	V
VCC_BACKUP	RTC power supply	1.1	3.0	5.5	V

9.6 Mechanical Characteristics

9.6.1 Sockets for Verdin Modules

The Verdin module uses the SODIMM DDR4 memory module edge connector. This connector has 260 pins and is available from different manufacturers in various stacking heights from 4mm to 9.2mm. Toradex recommends using the TE Connectivity 2309409-2 with a stacking height of 5.2mm, which provides a board-to-board distance of 2.62mm.

A list of other SODIMM DDR4 connector manufacturers is given below:

Amphenol:
https://www.amphenol-icc.com/product-series/ddr4-so-dimm.html

TE Connectivity:
https://www.te.com/usa-en/products/connectors/card-socket-connectors/memory-sockets.html

9.7 Thermal Specification

The Verdin AM62 incorporates dynamic frequency scaling on the Cortex-A53 cores, enabling the system to continuously adjust the operating frequency in response to the changes in workload and temperature.

The Verdin AM62 modules come with embedded temperature sensors. The sensors measure the die (junction) temperature and determine whether the cores need to be throttled to prevent overheating. If the SoC reaches the maximum permitted temperature, the system will automatically shut down.

Temperature affects power consumption.
A lower die temperature will also lower the power consumption due to the smaller leakage currents while idle.

Table 31: Thermal specification – Verdin AM62 Quad 2GB WB IT

Description	Min.	Typ.	Max.	Unit
Operating temperature range	–40		+85	°C
Storage temperature	–40		+85	°C
SoC junction temperature	–40		+105	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		22.3		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		3.7		°C/W

Table 32: Thermal specification – Verdin AM62 Dual 1GB WB IT

Description	Min.	Typ.	Max.	Unit
Operating temperature range	–40		+85	°C
Storage temperature	–40		+85	°C
SoC junction temperature	–40		+105	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		22.3		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		3.7		°C/W

Table 33: Thermal specification – Verdin AM62 Dual 1GB IT

Description	Min.	Typ.	Max.	Unit
Operating temperature range	–40		+85	°C
Storage temperature	–40		+85	°C
SoC junction temperature	–40		+105	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		22.3		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		3.7		°C/W

Table 34: Thermal specification – Verdin AM62 Dual 1GB ET

Description	Min.	Typ.	Max.	Unit
Operating temperature range	–20		+85	°C
Storage temperature	–40		+85	°C
SoC junction temperature	–40		+105	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		22.3		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		3.7		°C/W

Table 35: Thermal specification – Verdin AM62 Solo 512MB WB IT

Description	Min.	Typ.	Max.	Unit
Operating temperature range	–40		+85	°C
Storage temperature	–40		+85	°C
SoC junction temperature	–40		+105	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		22.3		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		3.7		°C/W

Table 36: Thermal specification – Verdin AM62 Solo 512MB

Description	Min.	Typ.	Max.	Unit
Operating temperature range	0		+70	°C
Storage temperature	–40		+85	°C

Continued on next page

Table 36: Thermal specification – Verdin AM62 Solo 512MB (Continued)

Description	Min.	Typ.	Max.	Unit
SoC junction temperature	−40		+95	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		22.3		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		3.7		°C/W

10 Device and Documentation Support

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