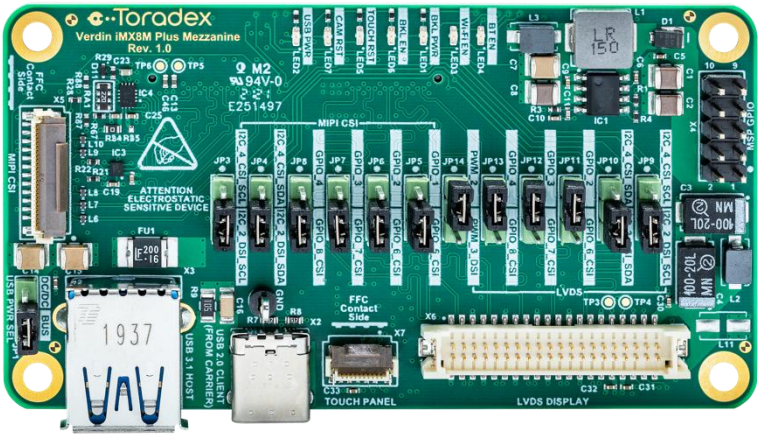
Toradex
Swiss. Embedded. Computing.

Verdin iMX8M Plus Mezzanine

Datasheet



Revision History

Date	Doc. Rev.	Board Version	Changes
23-Nov-2021	Rev. 1.00	V1.0	Initial document release
28-Feb-2022	Rev. 1.01	V1.0	Sections 3.4: CSI GPIOs signal names updated to be in line with the Verdin family specifications Addition of the section “Purpose of the Datasheet” Minor cosmetic improvements

Contents

1 Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the Verdin iMX8M Plus Mezzanine. For information on the actual features supported by software, please refer to the relevant product page on the Toradex Website: https://www.toradex.com/accessories/verdin-imx8m-plus-mezzanine.

1.2 Verdin iMX8M Plus Mezzanine

The Verdin iMX8M Plus Mezzanine is an add-on board for the Verdin Development Board that provides access to and allows the evaluation of the *"Module-specific"* interfaces and features available on the Verdin iMX8M Plus SoM.

Since *"Module-specific"* features are dependent on the particular Verdin SoMs, specific mezzanine boards will be available for the various Verdin SoMs. Customers are free to develop their own *"Module-specific"* mezzanine boards for prototyping and development purposes. Please refer to the datasheets of the individual Verdin SoMs for more information on *"Module-specific"* interfaces and features.

Please refer to the chapters of this datasheet to learn more about the interfaces and features of the Verdin iMX8M Plus Mezzanine.

1.3 Reference Documents

For detailed technical information and reference documents, please refer to the following sections:

1.3.1 Verdin Development Board Datasheet

https://docs.toradex.com/109463-verdin_development_board_datasheet_v1.1.pdf

1.3.2 Verdin iMX8M Plus SoM Datasheet

https://docs.toradex.com/108784-verdin_imx8m_plus_datasheet.pdf

1.3.3 Capacitive Touch Display 10.1" LVDS Datasheet

https://docs.toradex.com/105952-10-1-inch-lvds-capacitive-touch-display-1280x800-datasheet.pdf

1.3.4 CSI Camera Set 5MP AR0521 Color Datasheet

https://docs1.toradex.com/110394-csi-camera-set-5mp-ar0521-color-datasheet.pdf

1.3.5 Toradex Developer Website

http://developer.toradex.com/

2 Features

2.1 Overview

The Verdin iMX8M Plus Mezzanine provides the following interfaces and features:

- 1x MIPI CSI-2 Camera Connector
- 1x LVDS Display Connector
- 1x Capacitive Touch Connector (LVDS display)
- 1x 2x5-pin Low-speed Extension Header, providing access to the low-speed *"Module-specific"* signals of the Verdin iMX8M Plus SoM
- 1x USB 3.1 Gen 1 Type-A Host Connector (downstream for external peripherals)
- 1x USB 2.0 Type-C Client Connector (upstream for internal connection to the USB 2.0 OTG port of the Verdin Development Board)
- Test Points for the HDMI eARC feature
- 7x Indicator LEDs
- 13x Jumpers for configuration purposes

2.2 Hardware Architecture Block Diagram

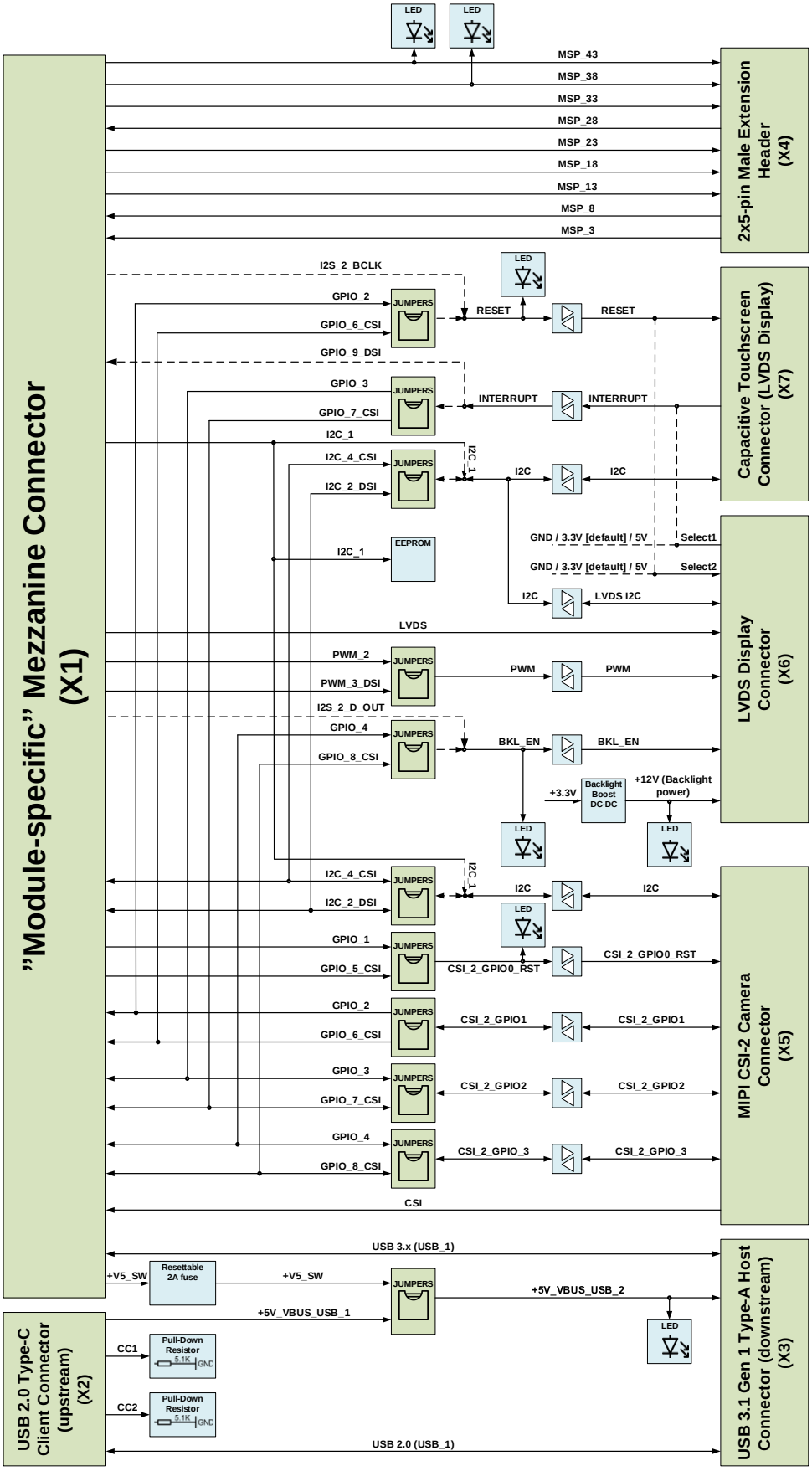


Fig. 1. Verdin iMX8M Plus Mezzanine – Hardware Architecture

2.3 Physical Drawings

2.3.1 Top Side Connectors

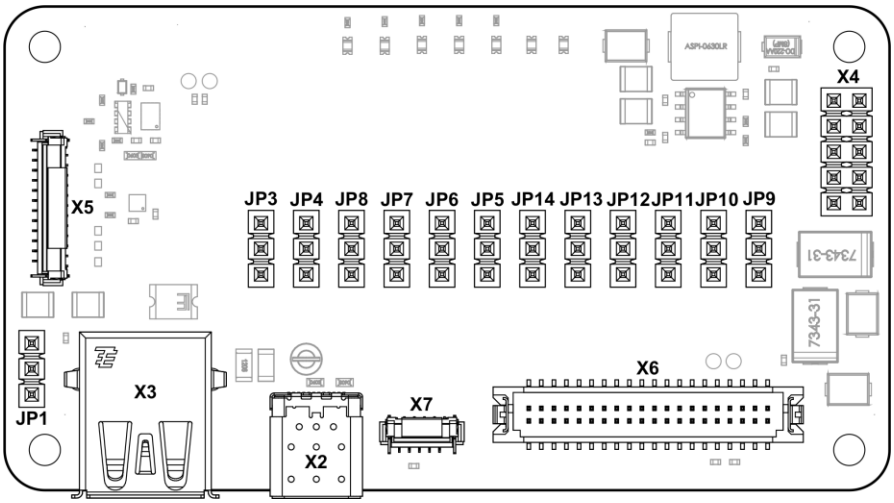


Fig. 2. Verdin iMX8M Plus Mezzanine (top side, top view)

2.3.2 Bottom Side Connector

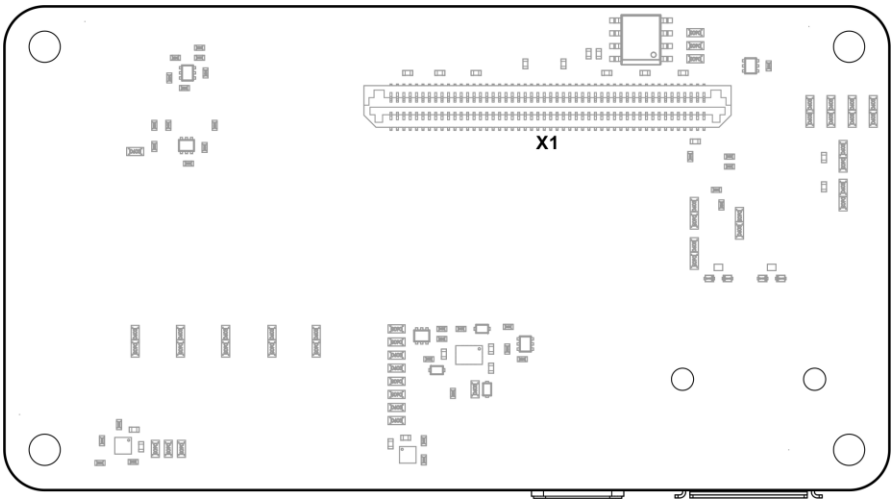


Fig. 3. Verdin iMX8M Plus Mezzanine (bottom side, bottom view)

Ref	Description	Remarks
X1	*"Module-specific"* Mezzanine Connector	
X2	USB 2.0 Type-C Client Connector (upstream)	
X3	USB 3.1 Gen 1 Type-A Host Connector (downstream)	
X4	2x5-pin Extension Header	
X5	MIPI CSI-2 Camera Connector	
X6	LVDS Display Connector	
X7	Capacitive Touchscreen Connector (LVDS Display)	

2.3.3 Hardware Setup

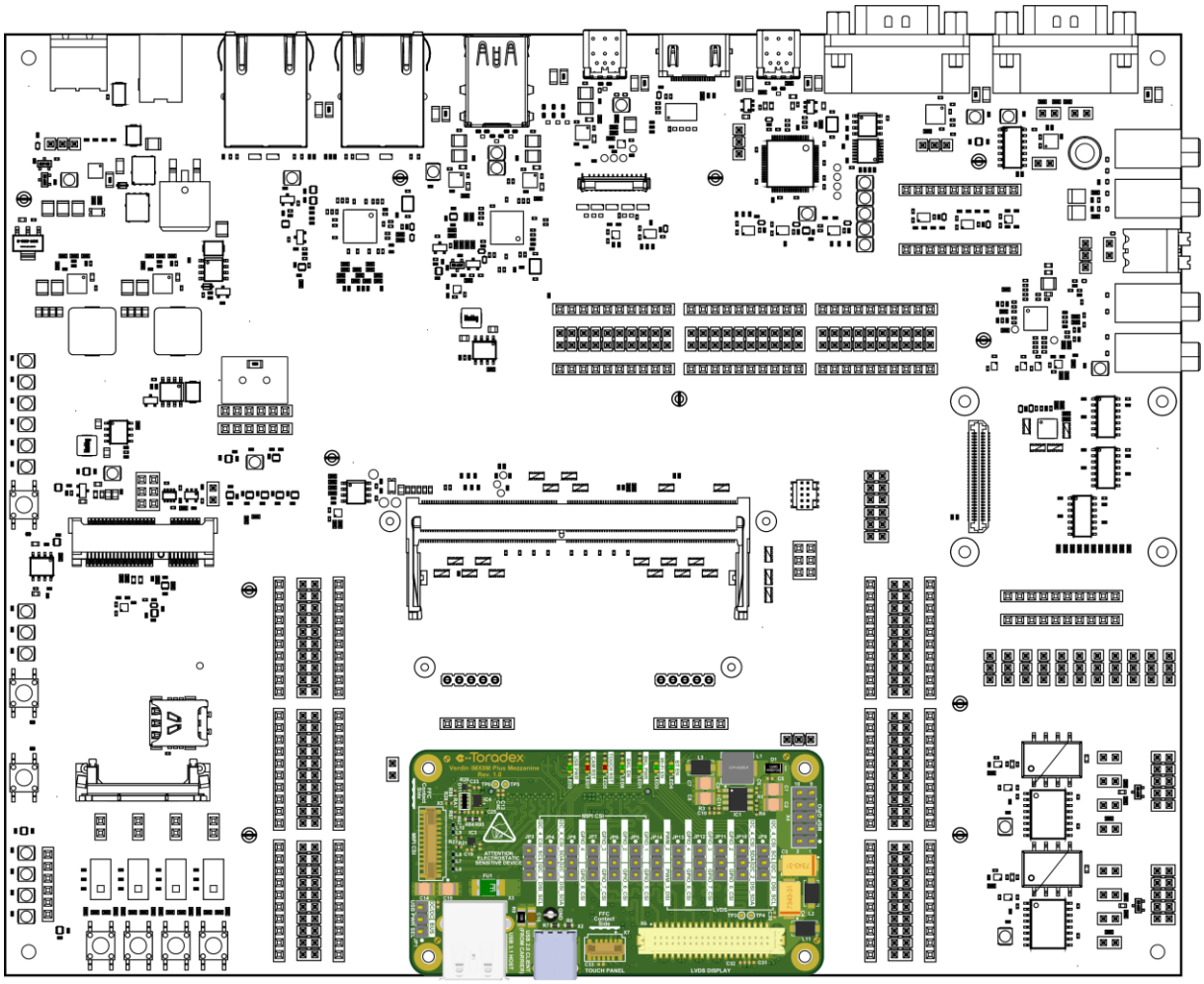


Fig. 4. Verdin iMX8M Plus Mezzanine – installed on the Verdin Development Board

3 Interface Description

3.1 *"Module-specific"* Mezzanine Connector (X1)

Connector type: Samtec LSS-150-03-L-DV-A-K-TR

Type: High-Speed Socket

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	NC				Not connected
3	GND	PWR			
5	USB_1_SSTX_P	I			Differential USB 3.1 Gen 1 transmit signal positive
7	USB_1_SSTX_N	I			Differential USB 3.1 Gen 1 transmit signal negative
9	MSP_38	I/O			Single-ended *"Module-specific"* signal 38
11	CSI_2_D3_P	O			Differential CSI-2 data lane 3 signal positive
13	CSI_2_D3_N	O			Differential CSI-2 data lane 3 signal negative
15	GND	PWR			
17	CSI_2_D2_P	O			Differential CSI-2 data lane 2 signal positive
19	CSI_2_D2_N	O			Differential CSI-2 data lane 2 signal negative
21	MSP_33	I/O			Single-ended *"Module-specific"* signal 33
23	CSI_2_CLK_P	O			Differential CSI-2 clock lane signal positive
25	CSI_2_CLK_N	O			Differential CSI-2 clock lane signal negative
27	GND	PWR			
29	CSI_2_D1_P	O			Differential CSI-2 data lane 1 signal positive
31	CSI_2_D1_N	O			Differential CSI-2 data lane 1 signal negative
33	MSP_28	I/O			Single-ended *"Module-specific"* signal 28
35	CSI_2_D0_P	O			Differential CSI-2 data lane 0 signal positive
37	CSI_2_D0_N	O			Differential CSI-2 data lane 0 signal negative
39	GND	PWR			
41	LVDS_1_B_TX3_P	I			Differential LVDS channel B data lane 3 signal for positive
43	LVDS_1_B_TX3_N	I			Differential LVDS channel B data lane 3 signal for negative
45	MSP_23	I/O			Single-ended *"Module-specific"* signal 23
47	LVDS_1_B_TX2_P	I			Differential LVDS channel B data lane 2 signal positive
49	LVDS_1_B_TX2_N	I			Differential LVDS channel B data lane 2 signal negative
51	GND	PWR			

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
53	LVDS_1_B_TX1_P	I			Differential LVDS channel B data lane 1 signal positive
55	LVDS_1_B_TX1_N	I			Differential LVDS channel B data lane 1 signal negative
57	MSP_18	I/O			MSP interface single-ended signal 18
59	LVDS_1_B_TX0_P	I			Differential LVDS channel B data lane 0 signal positive
61	LVDS_1_B_TX0_N	I			Differential LVDS channel B data lane 0 signal negative
63	GND	PWR			
65	LVDS_1_B_CLK_P	I			Differential LVDS channel B clock lane signal positive
67	LVDS_1_B_CLK_N	I			Differential LVDS channel B clock lane signal negative
69	MSP_13	I/O			Single-ended *"Module-specific"* signal 13
71	LVDS_1_A_TX3_P	I			Differential LVDS channel A data lane 3 signal positive
73	LVDS_1_A_TX3_N	I			Differential LVDS channel A data lane 3 signal negative
75	GND	PWR			
77	LVDS_1_A_TX2_P	I			Differential LVDS channel A data lane 2 signal positive
79	LVDS_1_A_TX2_N	I			Differential LVDS channel A data lane 2 signal negative
81	MSP_8	I/O			Single-ended *"Module-specific"* signal 8
83	LVDS_1_A_TX1_P	I			Differential LVDS channel A data lane 1 signal A positive
85	LVDS_1_A_TX1_N	I			Differential LVDS channel A data lane 1 signal negative
87	GND	PWR			
89	LVDS_1_A_TX0_P	I			Differential LVDS channel A data lane 0 signal positive
91	LVDS_1_A_TX0_N	I			Differential LVDS channel A data lane 0 signal negative
93	MSP_3	I/O			Single-ended *"Module-specific"* signal 3
95	LVDS_1_A_CLK_P	I			Differential LVDS channel A clock lane signal positive
97	LVDS_1_A_CLK_N	I			Differential LVDS channel A clock lane signal negative
99	GND	PWR			
2	GND	PWR			
4	EARC_P_UTIL	I/O			
6	EARC_N_HPD	I/O			
8	MSP_43	I/O			Single-ended *"Module-specific"* signal 43
10	USB_1_SSRX_P	O			Differential USB 3.1 Gen 1 receive signal positive
12	USB_1_SSRX_N	O			Differential USB 3.1 Gen 1 receive signal negative
14	GND	PWR			

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
16	I2C_4_CSI_SCL	I	+1.8V	Depending on jumper configuration	I2C_4 Verdin I2C bus clock signal
18	I2C_4_CSI_SDA	I/O	+1.8V	Depending on jumper configuration	I2C_4 Verdin I2C bus data signal
20	SODIMM_222 (GPIO_8_CSI)	I/O	+1.8V	Depending on jumper configuration	General-purpose I/Os, dedicated to the MIPI CSI-2 Camera interface
22	SODIMM_220 (GPIO_7_CSI)	I/O	+1.8V	Depending on jumper configuration	
24	SODIMM_218 (GPIO_6_CSI)	I/O	+1.8V	Depending on jumper configuration	
26	SODIMM_216 (GPIO_5_CSI)	I/O	+1.8V	Depending on jumper configuration	
28	GPIO_4	I/O	+1.8V	Depending on jumper configuration	General-purpose I/Os
30	GPIO_3	I/O	+1.8V	Depending on jumper configuration	
32	GPIO_2	I/O	+1.8V	Depending on jumper configuration	
34	GPIO_1	I/O	+1.8V	Depending on jumper configuration	
36	MSP_CSI_2_MCLK	I	+1.8V		CSI-2 Camera master clock signal
38	NC				Not connected
40	NC				
42	NC				
44	NC				
46	NC				
48	NC				
50	NC				
52	NC				
54	I2C_1_SCL	I	+1.8V	Depending on jumper configuration	I2C_1 Verdin I^2C bus clock signal
56	I2C_1_SDA	I/O	+1.8V	Depending on jumper configuration	I2C_1 Verdin I^2C bus data signal
58	NC				Not connected
60	+V1.8_SW	PWR	+1.8V		+1.8V power supply output
62	+V1.8_SW	PWR	+1.8V		
64	+V3.3_SW	PWR	+3.3V		+3.3V power supply output
66	+V3.3_SW	PWR	+3.3V		
68	+V5_SW	PWR	+5V		+5V power supply output
70	+V5_SW	PWR	+5V		
72	+V_SUPPLY_FILT_SW	PWR	7-24V ±10%		7-24V ±10% power supply output
74	+V_SUPPLY_FILT_SW	PWR	7-24V ±10%		
76	GND	PWR			

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
78	NC				Not connected
80	I2S_2_D_OUT	I	+1.8V	Depending on jumper configuration	Serial audio output data signal
82	NC				Not connected
84	I2S_2_BCLK	I	+1.8V	Depending on jumper configuration	Serial audio bit clock signal
86	NC				Not connected
88	SODIMM_17 (GPIO_9_DSI)	O (OD)	+1.8V	Depending on jumper configuration	Dedicated general purpose IO for the DSI display adapters
90	SODIMM_19 (PWM_3_DSI)	I	+1.8V	Depending on jumper configuration	PWM output, dedicated for the MIPI DSI display backlight brightness control
92	PWM_2	I	+1.8V	Depending on jumper configuration	General-purpose PWM outputs
94	NC				Not connected
96	GND	PWR			
98	I2C_2_DSI_SCL	I	+1.8V	Depending on jumper configuration	I2C_2 Verdin I^2C bus clock signal
100	I2C_2_DSI_SDA	I/O	+1.8V	Depending on jumper configuration	I2C_2 Verdin I^2C bus data signal

3.2 USB Interface

The USB interface consists of two USB connectors: an USB 2.0 Type-C Client connector and an USB 3.1 Gen 1 Type-A Host connector.

The USB 2.0 Type-C Client connector (featuring power) is available for looping in the USB 2.0 interface signals from the Verdin Development Board's USB 2.0 DRP connector (using USB Type-C to USB Type-C cable). With the additional USB SuperSpeed signals available in the *"Module-specific"* category of the Verdin iMX8M Plus SoM, these signals are combined to serve the USB 3.1 Gen 1 Type-A Host connector. The interface is available for connecting peripheral devices and supports a data rate of up to 5 Gbps.

For providing power to peripheral devices on the USB 3.1 Gen 1 Type-A Host connector (X3), power can be sourced through the USB 2.0 Type-C Client connector (X2) (directly from the Verdin Development Board's USB 2.0 DRP port) or directly from the +5V power supply of the Verdin Development Board. Both power sources have an overcurrent protection of 1A and 2A, respectively.

The power source for the USB 3.1 Gen 1 Host connector can be selected with the jumper JP1.

Jumper type: 1x3 Pin Header Male, 2.54 mm pitch

Jumper position	Description
1 - 2	USB HOST power sourced through the USB 2.0 Type-C Client connector (X2)
2 - 3	USB HOST power sourced directly from the +5V power supply of the Verdin Development Board

By default, the jumper JP1 is installed in position 1-2.

3.2.1 USB 2.0 Type-C Client Connector (X2)

Connector type: USB-C, Amphenol 12401598E4#2A

Pin	Signal Name	I/O Type	Voltage	Description
A1	GND	PWR		
A2	NC			Not connected
A3	NC			Not connected
A4	+V5_VBUS_USB_1	PWR	+5V	+5V USB power output
A5	USB_1_CC1			Type-C configuration channel signal 1
A6	USB_1_D_CON_P	I/O		Differential USB 2.0 signal positive
A7	USB_1_D_CON_N	I/O		Differential USB 2.0 signal negative
A8	NC			Not connected
A9	+V5_VBUS_USB_1	PWR	+5V	+5V USB power output
A10	NC			Not connected
A11	NC			Not connected
A12	GND	PWR		
B1	GND	PWR		
B2	NC			Not connected
B3	NC			Not connected
B4	+V5_VBUS_USB_1	PWR	+5V	+5V USB power output
B5	USB_1_CC2			Type-C configuration channel signal 1
B6	USB_1_D_CON_P	I/O		Differential USB 2.0 signal positive

Pin	Signal Name	I/O Type	Voltage	Description
B7	USB_1_D_CON_N	I/O		Differential USB 2.0 signal negative
B8	NC			Not connected
B9	+V5_VBUS_USB_1	PWR	+5V	+5V USB power output
B10	NC			Not connected
B11	NC			Not connected
B12	GND	PWR		
SH1/SH 2	GND_CHASSIS	PWR		
SH3/SH 4	GND_CHASSIS	PWR		

3.2.2 USB 3.1 Gen 1 Type-A Host Connector (X3)

Connector type: USB 3.1 Type-A, TE Connectivity 1932258-1

Pin	Signal Name	I/O Type	Voltage	Description
1	+V5_VBUS_USB_2	PWR	+5V	+5V USB power output
2	USB_1_CON_D_N	I/O		Differential USB 2.0 signal negative
3	USB_1_CON_D_P	I/O		Differential USB 2.0 signal positive
U4	GND	PWR		
5	USB_1_SSRX_CON_N	I		Differential USB 3.1 gen 1 receive signal negative
6	USB_1_SSRX_CON_P	I		Differential USB 3.1 gen 1 receive signal positive
7	GND	PWR		
8	USB_1_SSTX_CON_N	O		Differential USB 3.1 gen 1 transmit signal negative
9	USB_1_SSTX_CON_P	O		Differential USB 3.1 gen 1 transmit signal positive
S1/S2	GND_CHASSIS	PWR		

3.3 LVDS Display Interface

The LVDS Display Interface connection is provided by two connectors: the LVDS Display Connector and the Capacitive Touch Connector.

Sources of the interfaces and control signals serving the LVDS Display Connector, and the Capacitive Touch Connector can be set up with the jumpers JP9 – JP14 and the resistor assembly options R35, R36, R42, R45, R52, R53, R56, R58, R61 and R62. Possible jumper and resistor configurations are shown in the table below.

WARNING!

Before setting up the configuration jumpers or changing resistor assembly options, please check the Verdin Development Board jumper section and its schematic to avoid short-circuits and other conflicts.

Jumper type: 1x3 Pin Header Male, 2.54 mm pitch

Signal (Net)	Description	Resistor	Jumper	Position	Connected net
I2C_LVDS_SCL	LVDS Display interface I²C bus clock	**R36**	JP9	1-2	I2C_4_CSI_SCL
				2-3	I2C_2_DSI_SCL
		R35			I2C_1_SCL
I2C_LVDS_SDA	LVDS Display interface I²C bus data	**R45**	JP10	1-2	I2C_4_CSI_SDA
				2-3	I2C_2_DSI_SDA
		R42			I2C_1_SDA
LVDS_TOUCH_RST#	LVDS Display Touch Controller Reset signal	**R53**	JP11	**1-2**	GPIO_2
				2-3	GPIO_6_CSI
		R52			I2S_2_BCLK
LVDS_TOUCH_INT#	LVDS Display Touch Controller Interrupt signal	**R58**	JP12	**1-2**	GPIO_3
				2-3	GPIO_7_CSI
		R56			GPIO_9_DSI
LVDS_BKL_EN	LVDS Display Backlight Enable signal	**R62**	JP13	**1-2**	GPIO_4
				2-3	GPIO_8_CSI
		R61			I2S_2_D_OUT
LVDS_PWM	LVDS Display Backlight brightness control PWM signal		JP14	**1-2**	PWM_2
				2-3	PWM_3_DSI

The default resistor assemblies and the default jumper positions are marked in bold (with grey background).

3.3.1 LVDS Display Connector (X6)

Manufacturer: Hirose DF13EA-40DP-1.25V(76)
Type: Header connector

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	LVDS_1_A_TX3_P	O			Differential LVDS channel A data lane 3 signal positive
3	LVDS_1_A_TX3_N	O			Differential LVDS channel A data lane 3 signal negative
5	GND	PWR			
7	LVDS_1_A_TX2_P	O			Differential LVDS channel A data lane 2 signal positive
9	LVDS_1_A_TX2_N	O			Differential LVDS channel A data lane 2 signal negative
11	GND	PWR			
13	LVDS_1_A_TX1_P	O			Differential LVDS channel A data lane 1 signal positive
15	LVDS_1_A_TX1_N	O			Differential LVDS channel A data lane 1 signal negative
17	GND	PWR			
19	LVDS_1_A_TX0_P	O			Differential LVDS channel A data lane 0 signal positive
21	LVDS_1_A_TX0_N	O			Differential LVDS channel A data lane 0 signal negative
23	GND	PWR			
25	LVDS_1_A_CLK_P	O			Differential LVDS channel A clock signal positive
27	LVDS_1_A_CLK_N	O			Differential LVDS channel A clock signal negative
29	GND	PWR			
31	RESERVED (SEL1)		+3.3V		Not connected (0R resistor assembly option)
33	RESERVED (SEL2)		+3.3V		Not connected (0R resistor assembly option)
35	LVDS_PWM_CON	O	+3.3V		Display brightness control output[1]
37	LVDS_BKL_EN_CON	O	+3.3V		Display backlight ENABLE output
39	+V12_BL	PWR	+12V		Display backlight power output
2	GND	PWR			
4	LVDS_1_B_CLK_N	O			Differential LVDS channel B clock signal negative
6	LVDS_1_B_CLK_P	O			Differential LVDS channel B clock signal positive
8	GND	PWR			
10	LVDS_1_B_TX0_N	O			Differential LVDS channel B data lane 0 signal negative
12	LVDS_1_B_TX0_P	O			Differential LVDS channel B data lane 0 signal positive
14	GND	PWR			
16	LVDS_1_B_TX1_N	O			Differential LVDS channel B data lane 1 signal negative
18	LVDS_1_B_TX1_P	O			Differential LVDS channel B data lane 1 signal positive
20	GND	PWR			
22	LVDS_1_B_TX2_N	O			Differential LVDS channel B

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
					data lane 2 signal negative
24	LVDS_1_B_TX2_P	O			Differential LVDS channel B data lane 2 signal positive
26	GND	PWR			
28	LVDS_1_B_TX3_N	O			Differential LVDS channel B data lane 3 signal negative
30	LVDS_1_B_TX3_P	O			Differential LVDS channel B data lane 3 signal positive
32	+V3.3_SW	PWR	+3.3V		LVDS display power output
34	+V5_SW	PWR	+5V		LVDS display power output
36	I2C_LVDS_DISP_SDA	I/O	+3.3V	4.7k to +V3.3_SW	LVDS display configuration I^2C bus data signal
38	I2C_LVDS_DISP_SCL	O	+3.3V	4.7k to +V3.3_SW	LVDS display configuration I^2C bus clock signal
40	+V12_BL	PWR	+12V		Display backlight power output

1: Backlight Brightness = 100% if PWM = 0. Backlight Brightness = 0% if PWM = 100%

3.3.2 Capacitive Touchscreen Connector (X7)

Manufacturer: Hirose FH12-10S-0.5SVA(54)
Type: Receptacle FPC/FFC connector

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	I2C_LVDS_CTI_SDA	I/O	+3.3V	4.7k to +V3.3_SW	Capacitive touch controller I^2C bus data signal
2	I2C_LVDS_CTI_SCL	O	+3.3V	4.7k to +V3.3_SW	Capacitive touch controller I^2C bus clock signal
3	GND	PWR			
4	LVDS_TOUCH_INT_CON#	I	+3.3V	100k to +V3.3_SW	Touch controller interrupt input
5	LVDS_TOUCH_RESET_CON#	O	+3.3V		Touch controller RESET output
6	+V3.3_SW	PWR	+3.3V		Touch controller power output
7	NC				Not connected
8	NC				
9	NC				
10	NC				

3.4 MIPI CSI-2 Camera Interface

The MIPI CSI-2 Camera Interface on connector X7 is intended for applications requiring image capture capability from CMOS or CDD image sensors.

Sources of the interfaces, control signals and GPIOs serving the CSI-2 Camera Connector can be setup with the jumpers JP3 – JP8 and the resistor assembly options R19, R20, R23 and R24. Possible jumper and resistor configurations are shown in the table below.

WARNING!

Before setting up the configuration jumpers or changing resistor assembly options, please check the Verdin Development Board jumper section and its schematic to avoid short-circuits and other conflicts.

Jumper type: 1x3 Pin Header Male, 2.54 mm pitch

Signal (Net)	Description	Resistor	Jumper	Position	Signal source
I2C_CSI_2_SCL	CSI-2 Camera I²C bus clock	**R20**	JP3	1-2	I2C_4_CSI_SCL
				2-3	I2C_2_DSI_SCL
		R19		-	I2C_1_SCL
I2C_CSI_2_SDA	CSI-2 Camera I²C bus data	**R24**	JP4	1-2	I2C_4_CSI_SDA
				2-3	I2C_2_DSI_SDA
		R23		-	I2C_1_SDA
CSI_2_GPIO_0_RST	Camera RESET		JP5	1-2	GPIO_1
				2-3	GPIO_5_CSI
CSI_2_GPIO_1	Camera control GPIO		JP6	1-2	GPIO_2
				2-3	GPIO_6_CSI
CSI_2_GPIO_2	Camera control GPIO		JP7	1-2	GPIO_3
				2-3	GPIO_7_CSI
CSI_2_GPIO_3	Camera control GPIO		JP8	1-2	GPIO_4
				2-3	GPIO_8_CSI

The default resistor assemblies and the default jumper positions are marked in bold (with grey background).

3.4.1 MIPI CSI-2 Camera Connector (X7)

Manufacturer: Hirose FH12-24S-0.5SVA(54)

Connector type: 24 Position FFC, FPC, vertical 0.5mm

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND	PWR			
2	CSI_2_D0_CON_N	I/O			Differential CSI-2 data lane 0 signal negative
3	CSI_2_D0_CON_P	I/O			Differential CSI-2 data lane 0 signal positive
4	GND	PWR			
5	CSI_2_D1_CON_N	I			Differential CSI-2 data lane 1 signal negative
6	CSI_2_D1_CON_P	I			Differential CSI-2 data lane 1 signal positive
7	GND	PWR			
8	CSI_2_CLK_CON_N	I			Differential CSI-2 clock signal negative
9	CSI_2_CLK_CON_P	I			Differential CSI-2 clock signal positive
10	GND	PWR			
11	CSI_2_GPIO_0_RST_CON	O			Camera GPIO 0 (RESET)
12	SCI_1_MCLK	O			CSI-2 camera master clock
13	I2C_4_CSI_CON_SCL	O	+3.3V	10k to +V3.3_SW	Verdin I2C_4_CSI I^2C bus clock signal
14	I2C_4_CSI_CON_SDA	I/O	+3.3V	10k to + V3.3_SW	Verdin I2C_4_CSI I^2C bus data signal
15	+V3.3_SW	PWR	+3.3V		+3.3V power out
16	CSI_2_D2_CON_N	I			Differential CSI-2 data lane 2 signal negative
17	CSI_2_D2_CON_P	I			Differential CSI-2 data lane 2 signal positive
18	GND	PWR			
19	CSI_2_D3_CON_N	I			Differential CSI-2 data lane 3 signal negative
20	CSI_2_D3_CON_P	I			Differential CSI-2 data lane 3 signal positive
21	+V5_SW	PWR	+5V		+5V power output
22	CSI_2_GPIO_1_CON	I/O	+3.3V		Camera control GPIO 1
23	CSI_2_GPIO_2_CON	I/O	+3.3V		Camera control GPIO 2
24	CSI_2_GPIO_3_CON	I/O	+3.3V		Camera control GPIO 3

3.5 Low-speed Extension Header (X4)

Connector type: 2x5 Pin Header Male, 2.54 mm pitch

Pin	Signal Name	I/O Type	Voltage	SoC Pin Name	Device	Device Pin Name	Note
1	MSP_3	I	+1.8V		Wi-Fi/BT	GPIO[22]/ PCIE_W_DISABLEn	PCIe Wireless Disable Input (active low), the pull-up resistor is on the module, can be left floating
2	MSP_8	I	+1.8V		Wi-Fi/BT	CONFIG_HOST[0]	Strapping input, can be left floating. Connect to the ground for the UART Bluetooth feature (contact Toradex)
3	MSP_13	O	+1.8V	ECSPI2_MISO	Wi-Fi/BT	GPIO[14]/TCK/ WLAN Wake Host	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output, the signal is also connected to the SoC
4	MSP_18	O	+1.8V	ECSPI2_SS0	Wi-Fi/BT	GPIO[13]/ BT Wake Host	BT_WKUP_HOST: AW-CM276NF Bluetooth wake output, the signal is also connected to the SoC
5	MSP_23	O (OD[1])			RTC	IRQ#	Interrupts output for the Alarm and Timer events from RTC RX8130
6	MSP_28	I	+1.8V	ECSPI2_MOSI	Wi-Fi/BT	GPIO[9]/ UART_SIN	BT UART mode: RX data, the signal is also connected to the SoC
7	MSP_33	O	+1.8V	ECSPI2_SCLK	Wi-Fi/BT	GPIO[8]/ UART_SOUT	BT UART mode: TX data, the signal is also connected to the SoC
8	MSP_38	O	+1.8V		Wi-Fi/BT	GPIO[3]/ BT_LED	Bluetooth activity LED
9	MSP_43	O	+1.8V		Wi-Fi/BT	GPIO[2]/ WLAN_LED	Wi-Fi activity LED
10	GND	PWR					

[1] Open Drain

For the detailed description of the respective Low-speed "Module-specific" GPIOs functions, please check the Verdin iMX8M Plus SoM datasheet.

3.6 LED Indicators

The Verdin iMX8M Plus Mezzanine board features 7x LEDs. These LEDs show the status of the power supply and additional control signals.

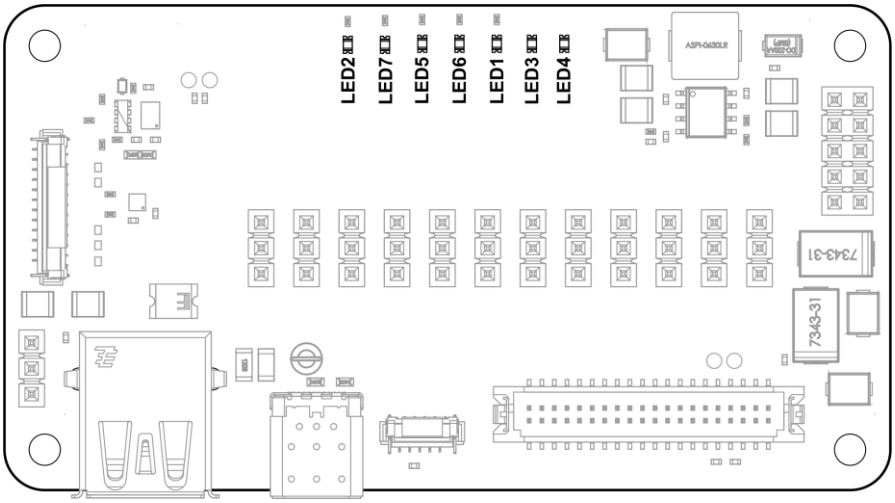


Fig. 5. Verdin iMX8M Plus Mezzanine - Indicator LEDs (top side, top view)

The LEDs and their functions are listed below.

Designator	Silkscreen name	Description
LED1	BKL PWR	The LED is lit when the +12V output of the DC-DC converter for powering the backlight of the display is available.
LED2	USB PWR	The LED is lit when +5V power is available on the USB 3.1 Gen 1 Type-A Host connector (X3).
LED3	Wi-Fi EN	The LED is lit when the Wi-Fi connection of the SoM is enabled.
LED4	BT EN	The LED is lit when the Bluetooth connection of the SoM is enabled.
LED5	TOUCH RST	The LED is lit when the touch controller of the LVDS Display is in a “RESET” state.
LED6	BKL EN	The LED is lit when the backlight of the LVDS Display is enabled.
LED7	CAM RST	The LED is lit when the MIPI CSI-2 camera is in a “RESET” state.

3.7 Test Points

The Verdin iMX8M Plus Mezzanine features 5x test points.

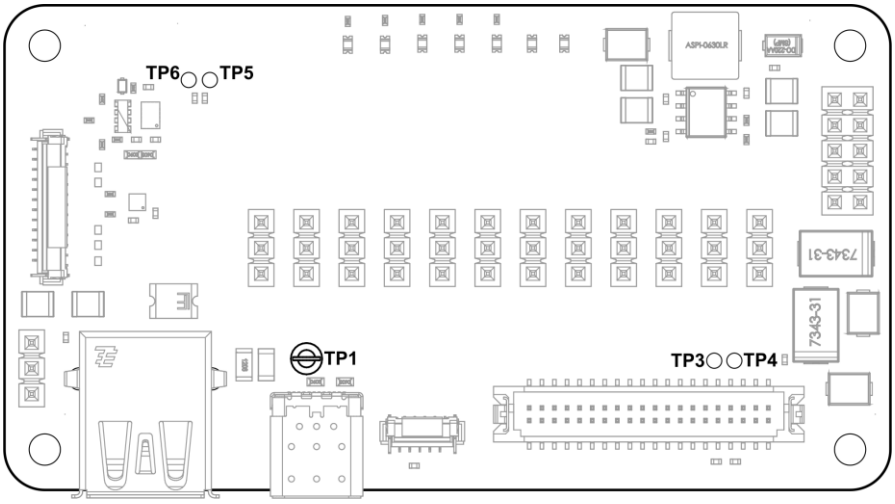


Fig. 6. Verdin iMX8M Plus Mezzanine - Test Points (top side, top view)

The Test Points and their purposes are listed in the table below.

Designator	Description
TP1	Through-hole test point pin (GND).
TP3	The test point is connected to pin 31 of the LVDS Display Connector (X6) and is reserved for future displays.
TP4	The test point is connected to pin 33 of the LVDS Display Connector (X6) and is reserved for future displays.
TP5	The test point is connected to the EARC_N_HPD net. It provides access to the eARC feature of the SoM.
TP6	The test point is connected to the EARC_P_UTIL net. It provides access to the eARC feature of the SoM.

4 Operating Conditions

4.1 Operating Temperature Range

- -30°C to +85°C

5 Mechanical Data

5.1 Mechanical Dimensions

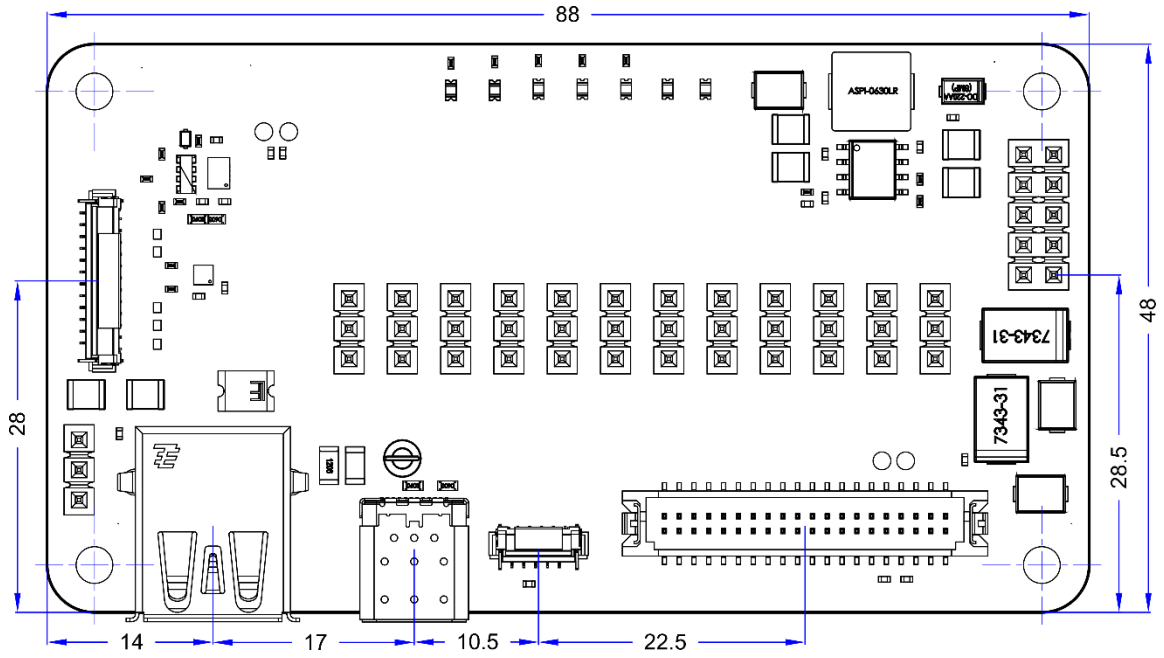


Fig. 7. Verdin iMX8M Plus Mezzanine – mechanical dimensions in mm (top side, top view)

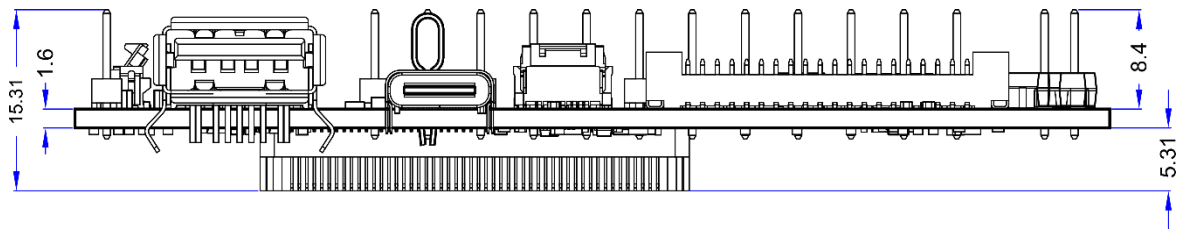


Fig. 8. Verdin iMX8M Plus Mezzanine – mechanical dimensions in mm (front side, front view)

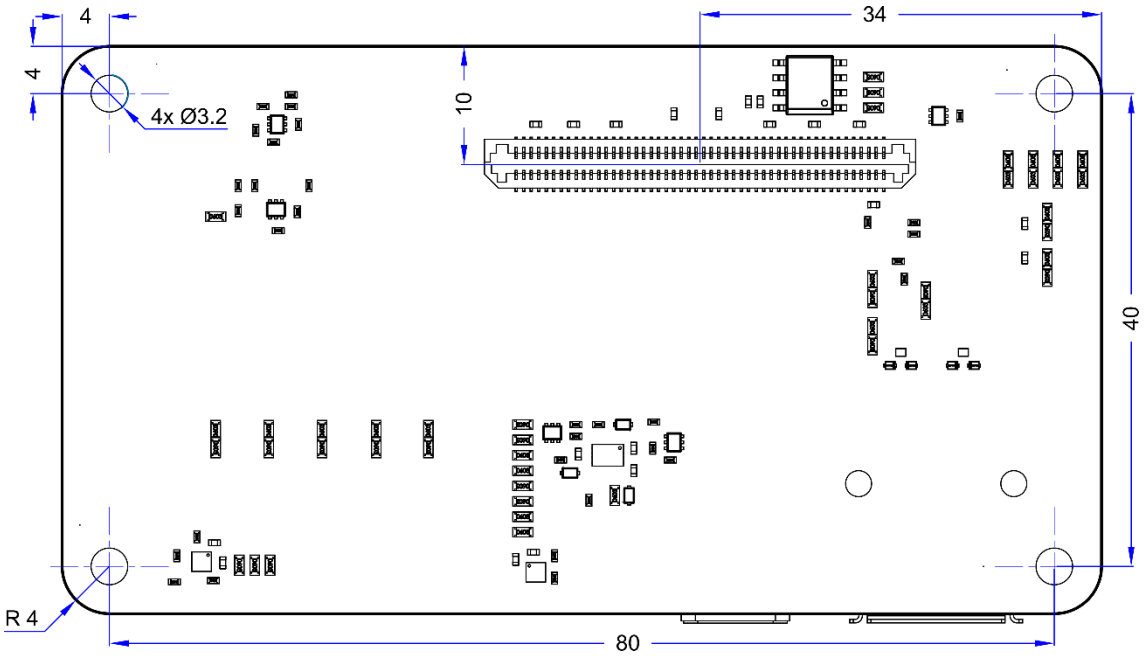


Fig. 9. Verdin iMX8M Plus Mezzanine – mechanical dimensions in mm (bottom side bottom view)

6 Design Data

The design data for the Toradex carrier boards and adapter boards are freely available in the Altium Designer format. The design data includes the schematics, the layout and the component libraries as well.

To download the board design data, please use the link below:

https://developer.toradex.com/products/verdin-imx8m-plus-mezzanine

7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance