Verdin Development Board
Datasheet
# Revision History

<table>
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<tr>
<th>Date</th>
<th>Doc. Rev.</th>
<th>Board Version</th>
<th>Changes</th>
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<td>20-Apr-2021</td>
<td>Rev. 1.00</td>
<td>V1.1</td>
<td>Initial Release.</td>
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<tr>
<td>22-Jun-2021</td>
<td>Rev. 1.01</td>
<td>V1.1</td>
<td>Updated the PHY status LED signal names according to the 1.3 version of the Verdin Family Specification throughout the whole document</td>
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<tr>
<td>25-Aug-2022</td>
<td>Rev. 1.02</td>
<td>V1.1</td>
<td>Section 1.1, Reference documents links have been updated.</td>
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<td>Section 1.4, Typo has been fixed on the Figure 1.</td>
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<td></td>
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<td>Section 2.4, LED17 color has been changed from “Green” to “Red”.</td>
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<td>Section 2.12.1, Typo has been fixed on the Figure 7.</td>
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<td>Section 2.18, Temperature sensor has been added.</td>
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<td>Section 2.19, EEPROM has been added.</td>
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<td>Section 2.21, Typo has been fixed on the Figure 11.</td>
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<td></td>
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<td>Minor Changes.</td>
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<tr>
<td>26-Oct-2023</td>
<td>Rev. 1.03</td>
<td>V1.1</td>
<td>Section 1: Added note about Verdin DSI to HDMI adapter</td>
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<td></td>
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<td>Section 1.1.18: Added to document</td>
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1 Introduction

The Verdin Development Board is a flexible development board with which you can explore and evaluate the functionality and performance of the Verdin product family. Complementing the Verdin computer on module, Verdin Development Board supports a wide variety of industry-standard interfaces while at the same time providing advanced multimedia and high-speed connectivity options, making it suitable for an almost unlimited number of applications. Verdin interfaces can be easily accessed using physical connectors and standard pitch headers. The Verdin Development Board is built on a 4-layer printed circuit board (PCB), and only one layer is used for high-speed signal routing. This demonstrates how Direct Breakout technology makes it incredibly easy to implement leading-edge interfaces with minimal risk and effort. CAE data for the board, including schematics, layout, and IPC-7351 compliant component libraries, are freely downloadable from the Toradex developer website. To ensure optimal compatibility and user experience with the Verdin Development Board, it must be ordered with the Verdin DSI to HDMI Adapter. This adapter uses a MIPI DSI interface to provide an HDMI output that seamlessly integrates with all Verdin System on Modules, guaranteeing an enhanced and comprehensive user experience.

1.1 Reference Documents

For detailed technical information, please refer to the documents listed below.

1.1.1 Verdin Family Specification
https://docs.toradex.com/109262-verdin-family-specification.pdf

1.1.2 Verdin Carrier Board Design Guide

1.1.3 Verdin Computer on Module family overview
https://www.toradex.com/computer-on-modules/Verdin-arm-family

1.1.4 Toradex Developer Website – Verdin Computer on Module documents

1.1.5 Carrier Board Layout Guide
https://docs.toradex.com/102492-layout-design-guide.pdf

1.1.6 Toradex Developer Website – Verdin Development Board Design Files

1.1.7 Pushbutton On/Off controller datasheet

1.1.8 EEPROM datasheet

1.1.9 Temperature sensor datasheet
1.1.10  USB HUB datasheet

1.1.11  Gigabit Ethernet Transceiver datasheet

1.1.12  RS232 Transceiver datasheet
https://www.ti.com/lit/ds/symlink/trs3122e.pdf

1.1.13  RS485 Transceiver datasheet

1.1.14  Audio Codec datasheet

1.1.15  USB Type-C Configuration Channel Logic IC datasheet

1.1.16  UV/OV and Reverse Protection Controller datasheet

1.1.17  GPIO expander datasheet

1.1.18  Toradex Developer Website – Verdin DSI to HDMI Adapter
## 1.2 Abbreviations

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<tr>
<th>Abbreviation</th>
<th>Explanation</th>
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</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>CAN</td>
<td>Controller Area Network, a bus that is mainly used in the automotive and industrial environment</td>
</tr>
<tr>
<td>CAN FD</td>
<td>Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.</td>
</tr>
<tr>
<td>CEC</td>
<td>Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processor Unit</td>
</tr>
<tr>
<td>CSI</td>
<td>Camera Serial Interface</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DDC</td>
<td>Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I²C) is always meant</td>
</tr>
<tr>
<td>DFP</td>
<td>Downstream Facing Port, USB Type-C port that acts as a host</td>
</tr>
<tr>
<td>DRP</td>
<td>Dual-Role Port, USB Type-C port that can operate as power sink and source</td>
</tr>
<tr>
<td>DSI</td>
<td>Display Serial Interface</td>
</tr>
<tr>
<td>DVI</td>
<td>Digital Visual Interface, digital signals are electrically compatible with HDMI</td>
</tr>
<tr>
<td>EDID</td>
<td>Extended Display Identification Data, timing setting information provided by the display in a PROM</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference, high-frequency disturbances</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices</td>
</tr>
<tr>
<td>FPD-Link</td>
<td>Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.</td>
</tr>
<tr>
<td>GBE</td>
<td>Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>GND_CHASSIS</td>
<td>Chassis Ground</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input/Output, pin that can be configured as an input or output</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communications</td>
</tr>
<tr>
<td>HDA</td>
<td>High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec</td>
</tr>
<tr>
<td>I²C</td>
<td>Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals</td>
</tr>
<tr>
<td>I²S</td>
<td>Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices</td>
</tr>
<tr>
<td>I/O</td>
<td>Input-Output</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group, widely used debug interface</td>
</tr>
<tr>
<td>LCD</td>
<td>Liquid Crystal Display</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonym for this interface. In this document, the term LVDS is used for the FPD-Link interface.</td>
</tr>
<tr>
<td>MAC</td>
<td>Medium Access Control is part of the second layer (data link layer) in the Ethernet stack</td>
</tr>
<tr>
<td>MIPI</td>
<td>Mobile Industry Processor Interface Alliance</td>
</tr>
<tr>
<td>MDI</td>
<td>Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector</td>
</tr>
<tr>
<td>MDIO</td>
<td>Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.</td>
</tr>
<tr>
<td>mini PCIe</td>
<td>PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Explanation</td>
</tr>
<tr>
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</tr>
<tr>
<td>MMC</td>
<td>MultiMediaCard, flash memory card</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>NC</td>
<td>Not Connected</td>
</tr>
<tr>
<td>OD</td>
<td>Open-Drain</td>
</tr>
<tr>
<td>OTG</td>
<td>USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PCI</td>
<td>Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals</td>
</tr>
<tr>
<td>PCIe</td>
<td>PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus</td>
</tr>
<tr>
<td>PCM</td>
<td>Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio</td>
</tr>
<tr>
<td>PD</td>
<td>Pull-Down Resistor</td>
</tr>
<tr>
<td>PHY</td>
<td>The physical layer of the OSI model</td>
</tr>
<tr>
<td>PU</td>
<td>Pull-up Resistor</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse-Width Modulation</td>
</tr>
<tr>
<td>PWR</td>
<td>Power</td>
</tr>
<tr>
<td>QSPI</td>
<td>Quad SPI, SPI interface with four bidirectional data signals</td>
</tr>
<tr>
<td>RGMII</td>
<td>Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s</td>
</tr>
<tr>
<td>RJ45</td>
<td>Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring</td>
</tr>
<tr>
<td>RS232</td>
<td>The single-ended serial port interface</td>
</tr>
<tr>
<td>RS485</td>
<td>Differential signaling serial port interface, half-duplex, multi-drop configuration possible</td>
</tr>
<tr>
<td>R-UIM</td>
<td>Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card</td>
</tr>
<tr>
<td>SD</td>
<td>Secure Digital, flash memory card</td>
</tr>
<tr>
<td>SDIO</td>
<td>Secure Digital Input Output, an external bus for peripherals that uses the SD interface</td>
</tr>
<tr>
<td>SIM</td>
<td>Subscriber Identification Module, an identification card for GSM phones</td>
</tr>
<tr>
<td>SMBus</td>
<td>System Management Bus (SMB), a two-wire bus based on the I²C specifications, is used in x86 designs for system management.</td>
</tr>
<tr>
<td>SoC</td>
<td>System on a Chip, IC which integrates the main component of a computer on a single chip</td>
</tr>
<tr>
<td>SoM</td>
<td>System on a Module, PCB which integrates the main component of a computer on a single board</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink</td>
</tr>
<tr>
<td>TMDS</td>
<td>Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI</td>
</tr>
<tr>
<td>TVS Diode</td>
<td>Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes</td>
</tr>
<tr>
<td>UFP</td>
<td>Upstream Facing Port, USB Type-C port that acts as a client</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus, serial interface for internal and external peripherals</td>
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1.3 Main Features

The Verdin Development Board provides the following features and communication interfaces:

- 1x stacked USB 3.0 Type-A connector, featuring 2x USB ports through the on-board USB HUB
- 1x USB-C connector providing USB Dual-Role-Port (DRP) or host/client functionality
- 1x USB-C debug connector (optionally connected to UART3, UART4, and JTAG through the multipurpose USB to serial converter based on the FT4232HL IC)
- 2x RJ45 connectors featuring 10/100/1000 Mbps Ethernet interfaces (1x Ethernet transceiver placed on the Development Board)
- 1x Mini PCIe Connector
- 1x HDMI Type A connector
- 1x “Module-specific” Board Connector
- 1x MIPI CSI Camera Interface connector
- 1x MIPI DSI Display interface with a board-to-board connector which allows for connecting various DSI display adapters: DSI to HDMI, DSI to LVDS, DSI to parallel RGB, etc.
- 1x JTAG connector
- 1x 4-bit SD Card connector
- 1x I2C 2Kb EEPROM IC
- 1x Digital Temperature Sensor
- Audio I/O on 3.5mm stereo jacks (MIC IN, AUX IN, HEADPHONE OUT, AUX OUT), terminal block/pin header connectors (SPEAKER OUT), and on-board electret microphone
- 1x RS232 Serial Interface on a 9-pin D-Sub Connector
- 1x RS485 Serial Interface on a 9-pin D-Sub Connector
- 4x I2C, 1x SPI and 3x PWM interfaces
- 4x ADC inputs
- 2x CAN interface headers, both supporting regular CAN (up to 1Mbps) and CAN FD (up to 5Mbps)
- 1x Real-time clock backup battery holder
- 4x dedicated GPIOs
- 4x general-purpose LEDs, switches and pushbuttons
- 10x level-shifted GPIOs (1.8V to 3.3V and vice versa)
- Power gating circuit (allows Power ON and OFF control of various development board peripherals)
- Extremely flexible and easy to use low-speed signal breakout and jumper area allowing easy signal re-routing, external connection, and measurement/probing
- Undervoltage, overvoltage, overcurrent and reverse voltage protected power input
1.4 Hardware Architecture Block Diagram

Figure 1: Verdin Development Board Hardware Architecture
1.5 Physical Drawing

1.5.1 Connectors

Figure 2: Verdin Development Board connectors and controls
<table>
<thead>
<tr>
<th>Ref</th>
<th>Description</th>
<th>Remarks</th>
</tr>
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<tbody>
<tr>
<td>X1</td>
<td>Verdin module edge connector (DDR4 SO-DIMM)</td>
<td></td>
</tr>
<tr>
<td>X2</td>
<td>Verdin edge connector breakout section 1</td>
<td></td>
</tr>
<tr>
<td>X3</td>
<td>Verdin edge connector breakout section 1</td>
<td></td>
</tr>
<tr>
<td>X4</td>
<td>Verdin edge connector breakout section 1</td>
<td></td>
</tr>
<tr>
<td>X5</td>
<td>Verdin edge connector breakout section 2</td>
<td></td>
</tr>
<tr>
<td>X6</td>
<td>Verdin edge connector breakout section 2</td>
<td></td>
</tr>
<tr>
<td>X7</td>
<td>Verdin edge connector breakout section 2</td>
<td></td>
</tr>
<tr>
<td>X8</td>
<td>I²C GPIO Expander I/Os header</td>
<td></td>
</tr>
<tr>
<td>X9</td>
<td>Power out header</td>
<td></td>
</tr>
<tr>
<td>X10</td>
<td>I²C GPIO Expander I/Os header</td>
<td></td>
</tr>
<tr>
<td>X11</td>
<td>Power out header</td>
<td></td>
</tr>
<tr>
<td>X13</td>
<td>Analog audio SPEAKER OUT 3-pin header</td>
<td>Stereo</td>
</tr>
<tr>
<td>X14</td>
<td>Analog audio AUX OUT jack</td>
<td>Auxiliary out / Line out (Stereo)</td>
</tr>
<tr>
<td>X15</td>
<td>Verdin edge connector breakout section 3</td>
<td></td>
</tr>
<tr>
<td>X16</td>
<td>Verdin edge connector breakout section 3</td>
<td></td>
</tr>
<tr>
<td>X17</td>
<td>Verdin edge connector breakout section 3</td>
<td></td>
</tr>
<tr>
<td>X18</td>
<td>POGO pins</td>
<td></td>
</tr>
<tr>
<td>X19</td>
<td>POGO pins</td>
<td></td>
</tr>
<tr>
<td>X20</td>
<td>Analog audio HEADPHONE OUT jack</td>
<td>Stereo</td>
</tr>
<tr>
<td>X21</td>
<td>Analog audio AUX IN jack</td>
<td>Auxiliary in / Line in (Stereo)</td>
</tr>
<tr>
<td>X22</td>
<td>Analog audio MIC IN jack</td>
<td>Stereo</td>
</tr>
<tr>
<td>X23</td>
<td>User button and switch header</td>
<td></td>
</tr>
<tr>
<td>X24</td>
<td>User button and switch header</td>
<td></td>
</tr>
<tr>
<td>X25</td>
<td>Ethernet connector</td>
<td>Ethernet_1</td>
</tr>
<tr>
<td>X26</td>
<td>User button and switch header</td>
<td></td>
</tr>
<tr>
<td>X27</td>
<td>User button and switch header</td>
<td></td>
</tr>
<tr>
<td>X28</td>
<td>Analog audio SPEAKER OUT connector</td>
<td>Mono (screwless connector)</td>
</tr>
<tr>
<td>X29</td>
<td>Analog audio SPEAKER OUT 2-pin header</td>
<td>Mono</td>
</tr>
<tr>
<td>X33</td>
<td>Mini PCIe connector</td>
<td></td>
</tr>
<tr>
<td>X34</td>
<td>USB DRP connector</td>
<td>USB-C (USB 2.0 only)</td>
</tr>
<tr>
<td>X35</td>
<td>Ethernet connector</td>
<td>Ethernet_2</td>
</tr>
<tr>
<td>X36</td>
<td>SIM Card Holder</td>
<td>Nano SIM</td>
</tr>
<tr>
<td>X37</td>
<td>HDMI connector</td>
<td></td>
</tr>
<tr>
<td>X38</td>
<td>User LEDs header</td>
<td></td>
</tr>
<tr>
<td>X39</td>
<td>Level shifter header</td>
<td>3.3V</td>
</tr>
<tr>
<td>X40</td>
<td>Level shifter header</td>
<td>1.8V</td>
</tr>
<tr>
<td>X47</td>
<td>MIPI CSI Camera connector</td>
<td></td>
</tr>
<tr>
<td>X48</td>
<td>MIPI DSI Display Adapter connector</td>
<td></td>
</tr>
<tr>
<td>X49</td>
<td>ADC input header</td>
<td></td>
</tr>
<tr>
<td>X50</td>
<td>RS485 connector</td>
<td>9-pin D-Sub</td>
</tr>
<tr>
<td>X51</td>
<td>RS232 connector</td>
<td>9-pin D-Sub</td>
</tr>
<tr>
<td>X52</td>
<td>“Module-specific” mezzanine board connector</td>
<td></td>
</tr>
<tr>
<td>X53</td>
<td>2x USB3.x HOST connector</td>
<td>UPPER: USBH3 – LOWER: USBH2</td>
</tr>
<tr>
<td>Ref</td>
<td>Description</td>
<td>Remarks</td>
</tr>
<tr>
<td>-----</td>
<td>--------------------------------------------------</td>
<td>--------------------</td>
</tr>
<tr>
<td>X54</td>
<td>Power control header</td>
<td></td>
</tr>
<tr>
<td>X55</td>
<td>SD Card 4-bit connector</td>
<td></td>
</tr>
<tr>
<td>X56</td>
<td>JTAG connector</td>
<td></td>
</tr>
<tr>
<td>X57</td>
<td>Terminal Block Power Supply connector</td>
<td>7-24V ±10%</td>
</tr>
<tr>
<td>X58</td>
<td>Barrel Jack Power Supply connector</td>
<td>7-24V ±10%</td>
</tr>
<tr>
<td>X59</td>
<td>CAN1 interface header</td>
<td>Isolated</td>
</tr>
<tr>
<td>X60</td>
<td>CAN2 interface header</td>
<td>Isolated</td>
</tr>
<tr>
<td>X62</td>
<td>POGO pin header</td>
<td></td>
</tr>
<tr>
<td>X63</td>
<td>POGO pin header</td>
<td></td>
</tr>
<tr>
<td>X66</td>
<td>USB to Serial, USB to JTAG interface connector</td>
<td>USB-C connector (USB 2.0 only)</td>
</tr>
<tr>
<td>X67</td>
<td>USB Debugger to JTAG interface jumper array</td>
<td></td>
</tr>
</tbody>
</table>
2 Interface Description

2.1 Verdin Computer-On-Module

Type: 260 pin DDR4 SO-DIMM socket. Manufacturer: TE 2309409-2
For the pinout of the Verdin module, please refer to the applicable Verdin module datasheet or to the Verdin Family Specification / Verdin Carrier Board Design guide for the abstract pinout.
Stand-offs are available on Verdin Development Board for affixing the Verdin module to the Development Board. It is recommended to use M2x0.4 size screws to fasten the Verdin module with the stand-offs.

2.2 Power Supply

The Verdin Development Board has two different power connectors that can power the board: X57, X58 is both wide input range connectors tied together.

WARNING!
The Barrel Jack Power Connector X58 and the Terminal Block Power Connector X57 are electrically connected, and only one of these connectors should be used for powering the board. The simultaneous connection of two power supplies is not allowed. Violating this requirement may cause power supplies or Development Board damage.

NOTE!
Input voltage can vary across a range of 7-24V ±10%. The maximum input current is limited to 5A. If your application dissipates more than 35W, please work with a higher input voltage, up to 24V.

Several power domains are available on the Development Board. The board’s power supply architecture is shown in the picture below.

The on-board power supplies provide the following nominal voltages and currents.

<table>
<thead>
<tr>
<th>Nominal voltage, V</th>
<th>Maximum current, A</th>
<th>Maximum power, W</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>8</td>
<td>40</td>
</tr>
<tr>
<td>3.3</td>
<td>8</td>
<td>26.4</td>
</tr>
<tr>
<td>1.8</td>
<td>2</td>
<td>3.6</td>
</tr>
</tbody>
</table>
2.2.1 Terminal Block Power Supply Connector (X57)

Connector type: AUK TB5102PRB-H

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Voltage / Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>+V_PWR_IN_1</td>
<td>7-24V ±10%</td>
</tr>
</tbody>
</table>

2.2.2 Barrel Jack Power Supply Connector (X58)

Connector type: SWC RAPC722X

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Voltage / Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+V_PWR_IN_1</td>
<td>7-24V ±10%</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td></td>
</tr>
</tbody>
</table>

2.2.3 Power Out Header (X9, X11)

Two female pin headers X9, X11, with main system voltages are available on it, can be used for powering external boards and modules. Pinout of the X9, X11 connectors is identical.

Connector type: 1x6 Pin Header Female, 2.54mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+V_SUPPLY_FILT_SW</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>+V5_SW</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>+V3.3_SW</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>+V3.3_SW</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>+V1.8_SW</td>
<td></td>
</tr>
</tbody>
</table>

2.2.4 Power Control

The Verdin Development Board power control is implemented using the Linear LTC2954 Pushbutton On/Off controller and with the signal CTRL_PWR_EN_MOCI, used to enable the peripheral power supplies.

For further information about the signals provided by the LTC2954 controller, please refer to its datasheet. For more information regarding the power-up sequence implemented on the board, please refer to the document “Verdin Carrier Board Design Guide”.

The switches SW1 and SW2 have been assigned to the RESET and ON/OFF functions, respectively. The SW3 is used to put the installed Verdin Computer Module into RECOVERY mode. Board power also can be controlled by the Verdin Computer Module with an open drain (OD) CTRL_FORCE_OFF_MOCI# signal. This feature allows the Verdin module to perform a proper power-down procedure. For more details, please refer to the “Verdin Carrier Board Design Guide”.

The Power CTRL connector X54 allows the Reset and Power Button control signals to be accessed externally.
2.2.4.1 Power Control Header (X54)

Connector type: 2x3 Pin Header Female, 2.54mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>IO Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PWR_BTN#</td>
<td>I/O (OD)</td>
<td>+1.9V</td>
<td>100k to +1.9V</td>
<td>It is connected to the POWER ON/OFF button SW2. Pulled-up to 1.9V inside pushbutton controller IC. Short pulling down turning on Development Board power and Computer Module. Long pulling down forcing Development Board power off.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td>Behaviour is similar to the “Always On” Jumper JP7. HIGH level on the PWR_CTRL input forcing on the Verdin Development Board power.</td>
</tr>
<tr>
<td>3</td>
<td>PWR_CTRL</td>
<td>I</td>
<td>+3.3V max</td>
<td>100k to GND</td>
<td>Pulling down for a longer period of time is shutting down the module. Short pulling down is turning on module from off state. Open-drain input with 100k pull-up resistor to the 1.8V RTC rail is on the module. The signal can be left floating on carrier boards</td>
</tr>
<tr>
<td>4</td>
<td>CTRL_PWR_BTN_MICO#</td>
<td>I/O (OD)</td>
<td>+1.8V</td>
<td></td>
<td>Forcing the turning-off of the main power rail. This signal is ignored for the first 512ms during the power-up sequence. The signal is 5V tolerant.</td>
</tr>
<tr>
<td>5</td>
<td>CTRL_FORCE_OFF_MOCI #</td>
<td>I/O (OD)</td>
<td>+5V</td>
<td>100k to +V5_STB</td>
<td>Open-drain input, which resets the module if shorted to ground. There is an on-module pull-up. This means it can be left floating on the carrier board.</td>
</tr>
</tbody>
</table>

Pin 3 of the X54 connector can be used to override the Pushbutton controller. The following table shows the behavior of the board according to the level of the PWR_CTRL signal:

<table>
<thead>
<tr>
<th>PWR_CTRL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>The Pushbutton controller is working normally</td>
</tr>
<tr>
<td>3.3V</td>
<td>The Verdin Development Board is Always On when power is applied</td>
</tr>
</tbody>
</table>

2.2.4.2 Always-ON Jumper (JP7)

Jumper JP7 can be used to configure the “Always On” behaviour.

Type: 1x2 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Jumper position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPEN</td>
<td>The board power supply is controlled with Power On/Off buttons.</td>
</tr>
<tr>
<td>CLOSED</td>
<td>The board power supply will be in the “Always On” state. Verdin Development Board will be powered up as soon as external power is applied to the connector X57 or X58.</td>
</tr>
</tbody>
</table>

By default, jumper JP7 is open.
2.2.5 Power supply input protection

Supply input is protected against ESD strikes, reverse voltage polarity, overvoltage, undervoltage, and short circuits. The protection circuit is based on an LTC4368 IC from Analog Devices. For detailed information, please refer to the LTC4368 datasheet https://www.analog.com/media/en/technical-documentation/data-sheets/LTC4368.pdf.

Power supply input ratings

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (Absolute maximum, limited with an ESD diode)</td>
<td>±30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Undervoltage threshold</td>
<td>4.82</td>
<td>4.99</td>
<td>5.17</td>
<td>V</td>
</tr>
<tr>
<td>Overvoltage threshold</td>
<td>26.11</td>
<td>27.08</td>
<td>28.09</td>
<td>V</td>
</tr>
<tr>
<td>Overcurrent protection</td>
<td>3.96</td>
<td>5</td>
<td>6.06</td>
<td>A</td>
</tr>
<tr>
<td>Reverse current protection</td>
<td>99</td>
<td>300</td>
<td>505</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Recommended input voltage</strong></td>
<td>6.3</td>
<td>7-24</td>
<td>26.4</td>
<td>V</td>
</tr>
</tbody>
</table>

Jumper Jumper JP23 can be used to turn ON or OFF the retry function of the power supply input protection circuit.

**Type:** 1x3 Pin Header Male, 2.54 mm pitch

**Jumper position** | **Description** |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>Power supply input will restart automatically after a forward overcurrent fault. The restart delay time is defined by capacitor C300 (5.5ms/nF). The typical value for the Verdin Development Board is 550ms</td>
</tr>
<tr>
<td>2-3</td>
<td>Power supply input stays OFF after a forward overcurrent fault. The external power supply should be switched OFF and ON to restore the board power.</td>
</tr>
</tbody>
</table>

By default, jumper JP23 is in position 1-2.

A current, voltage and power measurement IC INA219 (IC27) is also available on Verdin Development Boards. This IC provides an option to measure the power consumption of Verdin modules. IC27 is accessible on the I²C_1 bus at address 0x40.

2.3 Power gating circuit.

The Verdin development board contains a power gating circuit. This circuit allows for switching ON and OFF separate peripheral modules and provides LEDs to show the respective peripheral module's power state.

There are 3 sources of power gating signals: CTRL_PWR_EN_MOCI, CTRL_SLEEP_MOCI#, EX_1 – EX_11 (from I²C GPIO expander). Please note that when EX_1 – EX_11 signals are High, then the respective peripheral is powered up. PWR_CTRL_1 – PWR_CTRL_11 signals which are going directly to peripherals are not inverted! The source of the power gating signal for each peripheral can be selected via jumpers.

![Figure 4: Part of the power gating schematic](image-url)

**Connector type: 1x3 Pin Header Male, 2.54 mm pitch**

<table>
<thead>
<tr>
<th>Designator</th>
<th>Jumper position</th>
<th>Power gating signal</th>
<th>GPIO expander signal</th>
<th>Usage on carrier</th>
<th>Power gated peripheral</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP11</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX1</td>
<td>PWR_CTRL_1</td>
<td>USB HUB</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MOCI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP14</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX2</td>
<td>PWR_CTRL_2</td>
<td>CAN1 transceiver</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MOCI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP15</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX3</td>
<td>PWR_CTRL_3</td>
<td>CAN2 transceiver</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MOCI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP16</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX4</td>
<td>PWR_CTRL_4</td>
<td>Ethernet_2 transceiver</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MOCI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP17</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX5</td>
<td>PWR_CTRL_5</td>
<td>Audio codec</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MOCI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP18</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX6</td>
<td>PWR_CTRL_6</td>
<td>PCIe power</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MOCI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP19</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX7</td>
<td>PWR_CTRL_7</td>
<td>PCIe Wireless enable</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MICI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP20</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX8</td>
<td>PWR_CTRL_8</td>
<td>RS232 transceiver</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MICI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP21</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX9</td>
<td>DSI_PWR_EN</td>
<td>MIPI DSI display adapter</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MICI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP22</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX10</td>
<td>PWR_CTRL_11</td>
<td>&quot;Module-specific&quot; mezzanine board</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MICI#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP29</td>
<td>1-2</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>EX11</td>
<td>PWR_CTRL_12</td>
<td>RS485 transceiver</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>CTRL_SLEEP_MICI#</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>


A PCAL6416AHF GPIO expander IC is used on the board. For more details, please refer to the PCAL6416AHF datasheet. EX_1 – EX_16 signals from the GPIO expander are available on headers X8, X10.
2.3.1 GPIO expander header (X8)

Connector type: 1x10 Pin Header Female, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EX_1</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>3</td>
<td>EX_2</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>4</td>
<td>EX_3</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>5</td>
<td>EX_4</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>6</td>
<td>EX_5</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>7</td>
<td>EX_6</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>8</td>
<td>EX_7</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>9</td>
<td>EX_8</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>10</td>
<td>+V1.8_SW</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
</tr>
</tbody>
</table>

EX_12-EX_16 signals are not connected to any peripheral on the Verdin Development Board and can be used as needed.

2.3.2 GPIO expander header (X10)

Connector type: 1x10 Pin Header Female, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EX_9</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>3</td>
<td>EX_10</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>4</td>
<td>EX_11</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>5</td>
<td>EX_12</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>EX_13</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>EX_14</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>EX_15</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>EX_16</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>+V1.8_SW</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
</tr>
</tbody>
</table>
### 2.4 Indicator LEDs

The Verdin Development Board features 33 LEDs. These LEDs indicate the statuses of the main power supplies, all power gated peripherals. LEDs are also used for indicating the activity of some peripherals.

![Diagram of Verdin Development Board with LED connections](image)

Figure 5: Indicator LEDs

The LEDs and their functions are listed in the table below.

<table>
<thead>
<tr>
<th>Designator</th>
<th>Color</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED1</td>
<td>Green</td>
<td>LED is lit when CAN_1 transceiver power is ON</td>
</tr>
<tr>
<td>LED2</td>
<td>Green</td>
<td>LED is lit when CAN_2 transceiver power is ON</td>
</tr>
<tr>
<td>LED3</td>
<td>Green</td>
<td>LED is lit when USB_1 port power is ON (Connector X34)</td>
</tr>
<tr>
<td>LED4</td>
<td>Green</td>
<td>LED is lit when USBH3 Host power is ON (Connector X53 UPPER)</td>
</tr>
<tr>
<td>LED5</td>
<td>Green</td>
<td>LED is lit when USBH2 Host power is ON (Connector X53 LOWER)</td>
</tr>
<tr>
<td>LED6</td>
<td>Red</td>
<td>LED is lit when SoM and board is in a &quot;RESET&quot; state (CTRL_RESET_MOCI# is LOW).</td>
</tr>
<tr>
<td>LED7</td>
<td>Green</td>
<td>LED is lit when SD Card power is ON</td>
</tr>
<tr>
<td>LED8</td>
<td>Green</td>
<td>LED is lit when +V5 power is available</td>
</tr>
<tr>
<td>LED9</td>
<td>Green</td>
<td>LED is lit when +V5_SW power is available</td>
</tr>
<tr>
<td>LED10</td>
<td>Green</td>
<td>LED is lit when +V3.3_SW power is available</td>
</tr>
<tr>
<td>LED11</td>
<td>Green</td>
<td>LED is lit when +V1.2_SW power is available (Power for USB HUB and Ethernet_2 transceiver)</td>
</tr>
<tr>
<td>LED12</td>
<td>Green</td>
<td>LED is lit when +V1.8_SW power is available</td>
</tr>
<tr>
<td>LED13</td>
<td>Green</td>
<td>LED is lit when USB HUB power is ON</td>
</tr>
<tr>
<td>LED14</td>
<td>Green</td>
<td>Mini PCIe status indicator: WWAN. (Indication depend on the installed card)</td>
</tr>
<tr>
<td>Designator</td>
<td>Color</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>LED15</td>
<td>Green</td>
<td>Mini PCIe status indicator: WLAN. (Indication depend on the installed card)</td>
</tr>
<tr>
<td>LED16</td>
<td>Green</td>
<td>Mini PCIe status indicator: WPAN. (Indication depend on the installed card)</td>
</tr>
<tr>
<td>LED17</td>
<td>Red</td>
<td>LED is lit when power supply input protection is fault due to the forward Overcurrent</td>
</tr>
<tr>
<td>LED18</td>
<td>Green</td>
<td>LED is lit when Mini PCIe connector power is ON</td>
</tr>
<tr>
<td>LED19</td>
<td>Green</td>
<td>LED is lit when Ethernet_2 transceiver power is ON</td>
</tr>
<tr>
<td>LED20</td>
<td>Green</td>
<td>LED is lit when Audio Codec power is ON</td>
</tr>
<tr>
<td>LED21</td>
<td>Green</td>
<td>User LED. It is lit when the LED_1 signal is High</td>
</tr>
<tr>
<td>LED22</td>
<td>Green</td>
<td>User LED. It is lit when the LED_2 signal is High</td>
</tr>
<tr>
<td>LED23</td>
<td>Green</td>
<td>User LED. It is lit when the LED_3 signal is High</td>
</tr>
<tr>
<td>LED24</td>
<td>Green</td>
<td>User LED. It is lit when the LED_4 signal is High</td>
</tr>
<tr>
<td>LED25</td>
<td>Green</td>
<td>LED is lit when +V5_STB (Development Board Standby power) is available</td>
</tr>
<tr>
<td>LED26</td>
<td>Green</td>
<td>LED is lit when USB Debugger (IC41) power is available - USB Debugger is connected to the PC</td>
</tr>
<tr>
<td>LED27</td>
<td>Yellow</td>
<td>FTDI JTAG activity</td>
</tr>
<tr>
<td>LED28</td>
<td>Yellow</td>
<td>LED is blinking when data transmission on FTDI_UARTC_3.3V_TXD occurs</td>
</tr>
<tr>
<td>LED29</td>
<td>Yellow</td>
<td>LED is blinking when data transmission on FTDI_UARTC_3.3V_RXD occurs</td>
</tr>
<tr>
<td>LED30</td>
<td>Yellow</td>
<td>LED is blinking when data transmission on FTDI_UARTD_3.3V_TXD occurs</td>
</tr>
<tr>
<td>LED31</td>
<td>Yellow</td>
<td>LED is blinking when data transmission on FTDI_UARTD_3.3V_RXD occurs</td>
</tr>
<tr>
<td>LED32</td>
<td>Green</td>
<td>LED is lit when the RS485 transceiver is ON</td>
</tr>
<tr>
<td>LED33</td>
<td>Green</td>
<td>LED is lit when RS232 &quot;FORCEOFF&quot; mode is disabled. Check RS232 datasheet for details</td>
</tr>
</tbody>
</table>

More details are available in the Verdin Development Board schematics.
2.5 Test Points

SMD and through-hole test points are available on the Verdin Development Board to allow customers to measure critical signals during the development and debugging process.

![Verdin Development Board Test Points](image)

Figure 6: Verdin Development Board test points

The Test Points and their purposes are listed in the table below.

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP1</td>
<td>SD Card Serial Data 0</td>
</tr>
<tr>
<td>TP2</td>
<td>SD Card Serial Data 1</td>
</tr>
<tr>
<td>TP3</td>
<td>SD Card Serial Data 2</td>
</tr>
<tr>
<td>TP4</td>
<td>SD Card Serial Data 3</td>
</tr>
<tr>
<td>TP5</td>
<td>SD Card Command line</td>
</tr>
<tr>
<td>TP6</td>
<td>SD Card Serial Clock</td>
</tr>
<tr>
<td>TP7</td>
<td>SD Card Detection</td>
</tr>
<tr>
<td>TP8</td>
<td>SD Card Write Protection input</td>
</tr>
<tr>
<td>TP9</td>
<td>SoM power supply voltage</td>
</tr>
<tr>
<td>TP10</td>
<td>Through-hole test point pin (GND)</td>
</tr>
<tr>
<td>TP11</td>
<td></td>
</tr>
<tr>
<td>TP12</td>
<td></td>
</tr>
<tr>
<td>TP13</td>
<td></td>
</tr>
<tr>
<td>TP14</td>
<td></td>
</tr>
<tr>
<td>Designator</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>-------------</td>
</tr>
<tr>
<td>TP15</td>
<td>Through-hole test point pin (GND)</td>
</tr>
<tr>
<td>TP16</td>
<td>TP17</td>
</tr>
<tr>
<td>TP18</td>
<td>TP19</td>
</tr>
<tr>
<td>TP20</td>
<td>TP21 SoM power supply current sensing resistor (High side)</td>
</tr>
<tr>
<td>TP22</td>
<td>SoM power supply current sensing resistor (Low side)</td>
</tr>
<tr>
<td>TP23</td>
<td>SD Card power supply</td>
</tr>
<tr>
<td>TP24</td>
<td>Open Drain “ALERT” output of the temperature sensing IC50</td>
</tr>
<tr>
<td>TP25</td>
<td>RLINE/GPIO3 pin of the Audio Codec IC28</td>
</tr>
<tr>
<td>TP26</td>
<td>Open Drain “VCONN_FAULT” output of the IC53 pulled up to +V1.8_SW with 100k resistor</td>
</tr>
<tr>
<td>TP27</td>
<td>Open Drain “OUT2” output of the IC53 for the current mode detection logic</td>
</tr>
<tr>
<td>TP28</td>
<td>Open Drain “OUT1” output of the IC53 for the current mode detection logic</td>
</tr>
<tr>
<td>TP29</td>
<td>Open Drain “DIR” output of the IC53 for the USB-C plug orientation indication</td>
</tr>
<tr>
<td>TP30</td>
<td>CSB/GPIO1 pin of the Audio Codec IC28</td>
</tr>
<tr>
<td>TP31</td>
<td>CDBUS2 pin of the universal USB converter IC41 (USB Debugger 3.3V RTS output)</td>
</tr>
<tr>
<td>TP32</td>
<td>CDBUS3 pin of the universal USB converter IC41 (USB Debugger 3.3V CTS input)</td>
</tr>
<tr>
<td>TP33</td>
<td>DDBUS2 pin of the universal USB converter IC41 (USB Debugger 3.3V RTS output)</td>
</tr>
<tr>
<td>TP34</td>
<td>DDBUS3 pin of the universal USB converter IC41 (USB Debugger 3.3V CTS input)</td>
</tr>
<tr>
<td>TP35</td>
<td>HDMI eARC differential line positive signal</td>
</tr>
<tr>
<td>TP36</td>
<td>HDMI eARC differential line negative signal</td>
</tr>
<tr>
<td>TP37</td>
<td>Ethernet_2 transceiver interrupt output. It can be used as a regular GPIO if R332 is removed</td>
</tr>
<tr>
<td>TP38</td>
<td>Ethernet_2 transceiver MDIO data signal. It can be used as a regular GPIO if R150 is removed</td>
</tr>
<tr>
<td>TP39</td>
<td>Ethernet_2 transceiver MDIO clock signal. It can be used as a regular GPIO if R147 is removed</td>
</tr>
</tbody>
</table>
2.6 Ethernet Interface

The Verdin Development Board provides 2x RJ45 connectors with integrated magnetics for 10/100/1000Mb Ethernet. The Ethernet_1 transceiver is located on the SoM while the Ethernet_2 transceiver is placed on the Verdin Development Board. Some modules do not feature both Ethernet interfaces. Please refer to the datasheet of the respective Verdin SoM.

2.6.1 Ethernet_1 Connector (X25)

**Connector type:** RJ45, BEL A829-1J1T-KM / LINK-PP LPJK7436A98NL

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ETH_1_CTREF_2</td>
<td>241</td>
<td>I/O (Analog)</td>
<td></td>
<td>Integrated magnetics center tap 2</td>
</tr>
<tr>
<td>2</td>
<td>ETH_1_MDI2_N</td>
<td>239</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>3</td>
<td>ETH_1_MDI2_P</td>
<td>233</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>4</td>
<td>ETH_1_MDI1_N</td>
<td>231</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>5</td>
<td>ETH_1_MDI1_P</td>
<td>227</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>6</td>
<td>ETH_1_CTREF_1</td>
<td>225</td>
<td>I/O (Analog)</td>
<td></td>
<td>Integrated magnetics center tap 1</td>
</tr>
<tr>
<td>7</td>
<td>ETH_1_CTREF_3</td>
<td>224</td>
<td>I/O (Analog)</td>
<td></td>
<td>Integrated magnetics center tap 3</td>
</tr>
<tr>
<td>8</td>
<td>ETH_1_MDI3_P</td>
<td>222</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>9</td>
<td>ETH_1_MDI3_N</td>
<td>220</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>10</td>
<td>ETH_1_MDI0_P</td>
<td>218</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>11</td>
<td>ETH_1_MDI0_N</td>
<td>216</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>12</td>
<td>ETH_1_CTREF_0</td>
<td>215</td>
<td>O (OD)</td>
<td>+3.3V</td>
<td>LED for indication Ethernet activity</td>
</tr>
<tr>
<td>13</td>
<td>ETH_1_LED_1_C</td>
<td>214</td>
<td>PWR</td>
<td>+3.3V</td>
<td>Power supply for the indication LEDs</td>
</tr>
<tr>
<td>14</td>
<td>ETH_1_LED_2_C</td>
<td>213</td>
<td>O (OD)</td>
<td>+3.3V</td>
<td>LED for indication established Ethernet link</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>16</td>
<td>ETH_1_LED_2_C</td>
<td>212</td>
<td>O (OD)</td>
<td>+3.3V</td>
<td>Power supply for the indication LEDs</td>
</tr>
<tr>
<td>17</td>
<td>GND_CHASSIS</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.6.2 Ethernet_2 Connector (X35)

The Ethernet_2 interface is based on the KSZ9131RNXI 10/100/1000 Mbps Ethernet PHY which is using ETH_2_RGMII interface of the module. For more information, refer to the KSZ9131RNX IC datasheet.

**Connector type:** RJ45, BEL A829-1J1T-KM / LINK-PP LPJK7436A98NL

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ETH_2_CTREF_2</td>
<td>I/O (Analog)</td>
<td></td>
<td>Integrated magnetics center tap 2</td>
</tr>
<tr>
<td>2</td>
<td>ETH_2_MDI2_N</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>3</td>
<td>ETH_2_MDI2_P</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>4</td>
<td>ETH_2_MDI1_P</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>5</td>
<td>ETH_2_MDI1_N</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>6</td>
<td>ETH_2_CTREF_1</td>
<td>I/O (Analog)</td>
<td></td>
<td>Integrated magnetics center tap 1</td>
</tr>
<tr>
<td>7</td>
<td>ETH_2_CTREF_3</td>
<td>I/O (Analog)</td>
<td></td>
<td>Integrated magnetics center tap 3</td>
</tr>
<tr>
<td>8</td>
<td>ETH_2_MDI3_P</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>9</td>
<td>ETH_2_MDI3_N</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>10</td>
<td>ETH_2_MDI0_P</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>11</td>
<td>ETH_2_MDI0_N</td>
<td>I/O (Analog)</td>
<td></td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>12</td>
<td>ETH_2_CTREF_0</td>
<td>I/O (Analog)</td>
<td></td>
<td>Integrated magnetics center tap 0</td>
</tr>
<tr>
<td>13</td>
<td>ETH_1_LED_1_C</td>
<td>O (OD)</td>
<td></td>
<td>LED for indication Ethernet activity</td>
</tr>
<tr>
<td>Pin</td>
<td>Signal Name</td>
<td>I/O Type</td>
<td>Voltage</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-------------</td>
<td>----------</td>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td>14</td>
<td>+V3.3_SW</td>
<td>PWR</td>
<td>+3.3V</td>
<td>Power supply for the indication LEDs</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>16</td>
<td>+V3.3_SW</td>
<td>PWR</td>
<td>+3.3V</td>
<td>Power supply for the indication LEDs</td>
</tr>
<tr>
<td>17</td>
<td>ETH_1_LED_2_C</td>
<td>O (OD)</td>
<td></td>
<td>LED for indication established Ethernet link</td>
</tr>
<tr>
<td>S1/S2</td>
<td>GND_CHASSIS</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 2.7 Verdin USB_1 Port

The Verdin Development Board integrates a USB-C connector X34, connected to the Verdin USB_1 port (USB 2.0 interface only). This port is usually used in the recovery mode for loading new software onto the module and can work as a dual-role-port (DRP), which means Host or Device. This behaviour is similar to the On-The-Go (OTG) functionality, but the term USB OTG is only used in conjunction with the USB Micro-AB or the obsolete USB Mini-AB receptacle. ID pin is absent on the USB Type-C receptacle. The determination of Host or Device functionality is handled differently in Type-C using the configuration channel (CC) pins. The CC pins perform the same functions that the ID pin previously performed: they indicate the role of equipment as host, device, or both. The CC pins also detect if the connection is being made or if it is broken.

To handle all the operations required for the USB dual-role-port TUSB321AI chip has been used. It can function as an upstream-facing port (UFP), downstream-facing port (DFP), or a dual-role port (DRP) product based on a pin configuration. The device handles all aspects of the USB Type-C connection process (including the CC pins that mirror the micro-A/B ID pin behavior) to determine the port role. When connected as a peripheral (UFP), the TUSB321AI indicates the VBUS current provided by the attached host through the general-purpose input/output (GPIO) pins. When connected as a DFP, these devices advertise VBUS current to the attached peripheral. For the details, please check the TUSB321AI datasheet.

On the Development Board, this port is configured as a dual-role port (DRP) by default, and its output current is limited to 1A.

#### 2.7.1 USB_1 Connector (X34)

Connector type: USB-C, Amphenol 12401598E4#2A

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>A3</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>A4</td>
<td>+V5_VBUS_USB_1</td>
<td>159</td>
<td>PWR</td>
<td>+5V</td>
<td>+5V USB power output</td>
</tr>
<tr>
<td>A5</td>
<td>USB_1_CC1</td>
<td></td>
<td></td>
<td></td>
<td>Type-C configuration channel signal 1</td>
</tr>
<tr>
<td>A6</td>
<td>USB_1_D_CON_P</td>
<td>165</td>
<td>I/O</td>
<td></td>
<td>Positive differential USB 2.0 Signal</td>
</tr>
<tr>
<td>A7</td>
<td>USB_1_D_CON_N</td>
<td>163</td>
<td>I/O</td>
<td></td>
<td>Negative differential USB 2.0 Signal</td>
</tr>
<tr>
<td>A8</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>A9</td>
<td>+V5_VBUS_USB_1</td>
<td>159</td>
<td>PWR</td>
<td>+5V</td>
<td>+5V USB power output</td>
</tr>
<tr>
<td>A10</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>A11</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>A12</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>B3</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>B4</td>
<td>+V5_VBUS_USB_1</td>
<td>159</td>
<td>PWR</td>
<td>+5V</td>
<td>+5V USB power output</td>
</tr>
</tbody>
</table>
### 2.8 Verdin USB_2 Port

The Verdin Development Board integrates a 4 port USB hub (Microchip USB5744T-I/2G) connected the SoM’s USB_2 port, providing 4x USB 3.x / USB 2.0 Host interfaces. The level of USB 3.x standard supported depends on the SoM. Some SoMs may not support USB 3.x interface at all. Refer to the respective SoM datasheet to get the detailed information about supported USB interfaces and their speed. The hub itself support USB 3.2 Gen 1 / USB 2.0 standards.

The naming schemes of USB 3.x (SuperSpeed) interface can be a bit confusing. There are different names for the same speed grade, depending on the revision of the specifications that are taken. In a table below a short comparison of the different transfer modes and their naming schemes has been done. Not all the USB 3.x transfer modes are possible with the Verdin modules, since in the Verdin standard only one lane of SuperSpeed signals are reserved.

<table>
<thead>
<tr>
<th>Marketing Name</th>
<th>USB 3.2 Name</th>
<th>USB 3.1 Name</th>
<th>USB 3.0 Name</th>
<th>Nominal Speed</th>
<th>SuperSpeed Lanes</th>
<th>Supported by Verdin</th>
</tr>
</thead>
<tbody>
<tr>
<td>SuperSpeed USB</td>
<td>USB 3.2 Gen 1x1</td>
<td>USB 3.1 Gen 1</td>
<td>USB 3.0</td>
<td>5 Gbit/s0.5 GByte/s</td>
<td>1</td>
<td>Possible</td>
</tr>
<tr>
<td>SuperSpeed USB 10 Gbit/s</td>
<td>USB 3.2 Gen 1x2</td>
<td></td>
<td></td>
<td>10 Gbit/s1 GByte/s</td>
<td>2</td>
<td>No</td>
</tr>
<tr>
<td>SuperSpeed USB 10 Gbit/s</td>
<td>USB 3.2 Gen 2x1</td>
<td>USB 3.1 Gen 2</td>
<td></td>
<td>10 Gbit/s1.2 GByte/s</td>
<td>1</td>
<td>Possible</td>
</tr>
<tr>
<td>SuperSpeed USB 20 Gbit/s</td>
<td>USB 3.2 Gen 2x2</td>
<td></td>
<td></td>
<td>20 Gbit/s2.4 GByte/s</td>
<td>2</td>
<td>No</td>
</tr>
</tbody>
</table>

The OC sensing pin of the USB_2 port is not used, and the USB hub handles OC conditions. Port 1 of the USB hub is disabled; on Port 4, only the USB 2.0 interface is used, and it is routed to the Mini PCIe connector (X33). Port 2 and Port 3 are routed to a stacked USB 3.0 Type-A connector (X53). Maximum data rate for this connector is 5Gbit/s. For further information about the USB hub, please refer to its datasheet.
2.8.1 USB_2 Connector (X53)

Connector type: Stacked USB 3.0 Type-A, Amphenol GSB311231HR
(Pins starting with U connect to the UPPER, pins starting with L connect to the LOWER port)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>+V5_VBUS_USBH3</td>
<td>PWR</td>
<td>+5V</td>
<td>+5V USB power output</td>
</tr>
<tr>
<td>U2</td>
<td>USBH3_CON_D_N</td>
<td>I/O</td>
<td></td>
<td>Negative differential USB 2.0 signal</td>
</tr>
<tr>
<td>U3</td>
<td>USBH3_CON_D_P</td>
<td>I/O</td>
<td></td>
<td>Positive differential USB 2.0 signal</td>
</tr>
<tr>
<td>U4</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U5</td>
<td>USBH3_SSRX_CON_N</td>
<td>I</td>
<td></td>
<td>Negative differential USB 3.x receive signal</td>
</tr>
<tr>
<td>U6</td>
<td>USBH3_SSRX_CON_P</td>
<td>I</td>
<td></td>
<td>Positive differential USB 3.x receive signal</td>
</tr>
<tr>
<td>U7</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U8</td>
<td>USBH3_SSTX_CON_N</td>
<td>O</td>
<td></td>
<td>Negative differential USB 3.x transmit signal</td>
</tr>
<tr>
<td>U9</td>
<td>USBH3_SSTX_CON_P</td>
<td>O</td>
<td></td>
<td>Positive differential USB 3.x transmit signal</td>
</tr>
<tr>
<td>L1</td>
<td>+V5_VBUS_USBH2</td>
<td>PWR</td>
<td>+5V</td>
<td>+5V USB power output</td>
</tr>
<tr>
<td>L2</td>
<td>USBH2_CON_D_N</td>
<td>I/O</td>
<td></td>
<td>Negative differential USB 2.0 signal</td>
</tr>
<tr>
<td>L3</td>
<td>USBH2_CON_D_P</td>
<td>I/O</td>
<td></td>
<td>Positive differential USB 2.0 signal</td>
</tr>
<tr>
<td>L4</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L5</td>
<td>USBH2_SSRX_CON_N</td>
<td>I</td>
<td></td>
<td>Negative differential USB 3.x receive signal</td>
</tr>
<tr>
<td>L6</td>
<td>USBH2_SSRX_CON_P</td>
<td>I</td>
<td></td>
<td>Positive differential USB 3.x receive signal</td>
</tr>
<tr>
<td>L7</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L8</td>
<td>USBH2_SSTX_CON_N</td>
<td>O</td>
<td></td>
<td>Negative differential USB 3.x transmit signal</td>
</tr>
<tr>
<td>L9</td>
<td>USBH2_SSTX_CON_P</td>
<td>O</td>
<td></td>
<td>Positive differential USB 3.x transmit signal</td>
</tr>
<tr>
<td>S1/S2</td>
<td>GND_CHASSIS</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S3/S4</td>
<td>GND_CHASSIS</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.9 PCIe Interface

The Verdin Development Board makes the standard PCIe interface on the Verdin SoMs available on a Mini PCIe slot. PCI Express Mini Card is a replacement for the Mini PCI form factor. Mini PCIe provides both the standard PCI Express and USB 2.0 signals, allowing flexibility in peripheral design. PCI Express Mini Card edge connectors provide multiple connections and buses, such as listed below:

- PCI Express 1 lane (with SMBus)
- USB 2.0
- Indication LEDs for wireless network status
- SIM card for cellular applications (UIM signals)

2.9.1 Mini PCIe Connector (X33)

Connector type: Mini PCIe Card Connector and Latch, Molex 67910-5700, 48099-5701

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCIE_1_WAKE#</td>
<td>252</td>
<td>O (OD)</td>
<td>+1.8V</td>
<td>5.1k to +V1.8_SW</td>
<td>Wake-up to SoM</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin</td>
<td>Signal Name</td>
<td>SODIMM Pin</td>
<td>I/O Type</td>
<td>Voltage</td>
<td>Pull-up/Pull-down</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>----------------------</td>
<td>------------</td>
<td>----------</td>
<td>---------</td>
<td>-------------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>11</td>
<td>PCIE_1_CLK_N</td>
<td>226</td>
<td>I</td>
<td></td>
<td></td>
<td>Negative differential PCIe reference clock signal</td>
</tr>
<tr>
<td>13</td>
<td>PCIE_1_CLK_P</td>
<td>228</td>
<td>I</td>
<td></td>
<td></td>
<td>Positive differential PCIe reference clock signal</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>17</td>
<td>NC</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>19</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>PCIE_1_L0_RX_N</td>
<td>232</td>
<td>O</td>
<td></td>
<td></td>
<td>Negative differential PCIe receive signal</td>
</tr>
<tr>
<td>25</td>
<td>PCIE_1_L0_RX_P</td>
<td>234</td>
<td>O</td>
<td></td>
<td></td>
<td>Positive differential PCIe receive signal</td>
</tr>
<tr>
<td>27</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>PCIE_1_L0_TX_N</td>
<td>238</td>
<td>I</td>
<td></td>
<td></td>
<td>Negative differential PCIe transmit signal</td>
</tr>
<tr>
<td>33</td>
<td>PCIE_1_L0_TX_P</td>
<td>240</td>
<td>I</td>
<td></td>
<td></td>
<td>Positive differential PCIe transmit signal</td>
</tr>
<tr>
<td>35</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>+V3.3_PCIE_1</td>
<td>PWR</td>
<td>+3.3V</td>
<td></td>
<td></td>
<td>+3.3V Power input</td>
</tr>
<tr>
<td>41</td>
<td>+V3.3_PCIE_1</td>
<td>PWR</td>
<td>+3.3V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>47</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>49</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>+V3.3_PCIE_1</td>
<td>PWR</td>
<td>+3.3V</td>
<td></td>
<td></td>
<td>+3.3V Power input</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>+V1.5_PCIE_1</td>
<td>PWR</td>
<td>+1.5V</td>
<td></td>
<td></td>
<td>+1.5V Power input</td>
</tr>
<tr>
<td>8</td>
<td>PCIE_1_UIM_PWR</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td>SIM Card Power</td>
</tr>
<tr>
<td>10</td>
<td>PCIE_1_UIM_DATA</td>
<td>I/O</td>
<td></td>
<td></td>
<td></td>
<td>SIM Card Data</td>
</tr>
<tr>
<td>12</td>
<td>PCIE_1_UIM_CLK</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td>SIM Card Clock</td>
</tr>
<tr>
<td>14</td>
<td>PCIE_1_UIM_RESET</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td>SIM Card RESET</td>
</tr>
<tr>
<td>16</td>
<td>PCIE_1_UIM_VPP</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td>SIM Card Programming voltage</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>PCIE_1_WDISABLE#</td>
<td>I (OD)</td>
<td></td>
<td></td>
<td></td>
<td>PCIe Wireless interface disable</td>
</tr>
<tr>
<td>22</td>
<td>PERST#</td>
<td>244</td>
<td>I (OD)</td>
<td></td>
<td></td>
<td>PCIe Power enable/RESET</td>
</tr>
<tr>
<td>24</td>
<td>+V3.3_SW</td>
<td>PWR</td>
<td>+3.3V</td>
<td></td>
<td></td>
<td>+3.3V Standby power input</td>
</tr>
<tr>
<td>26</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>+V1.5_PCIE_1</td>
<td>PWR</td>
<td>+1.5V</td>
<td></td>
<td></td>
<td>+1.5V Power input</td>
</tr>
<tr>
<td>30</td>
<td>PCIE_1_SMCLK</td>
<td>12</td>
<td>I</td>
<td>+3.3V</td>
<td></td>
<td>PCIe SMBus Clock</td>
</tr>
<tr>
<td>32</td>
<td>PCIE_1_SMDAT</td>
<td>14</td>
<td>I/O</td>
<td>+3.3V</td>
<td></td>
<td>PCIe SMBus Data</td>
</tr>
</tbody>
</table>
## 2.9.2 SIM Card Holder (X36)

**Connector type: NANO SIM, Molex 1042240820**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>PCIE1_B_UIM_PWR</td>
<td>PWR</td>
<td></td>
<td></td>
<td>SIM Card Power</td>
</tr>
<tr>
<td>S2</td>
<td>PCIE1_B_UIM_RESET</td>
<td>I</td>
<td></td>
<td></td>
<td>SIM Card RESET</td>
</tr>
<tr>
<td>S3</td>
<td>PCIE1_B_UIM_CLK</td>
<td>I</td>
<td></td>
<td></td>
<td>SIM Card Clock</td>
</tr>
<tr>
<td>S4</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S5</td>
<td>PCIE1_B_UIM_VPP</td>
<td>PWR</td>
<td></td>
<td></td>
<td>SIM Card Programming voltage</td>
</tr>
<tr>
<td>S6</td>
<td>PCIE1_B_UIM_DATA</td>
<td>I/O</td>
<td></td>
<td></td>
<td>SIM Card Data</td>
</tr>
<tr>
<td>G1/G2</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G3/G4</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2.10 SD Card Interface

The Verdin Development Board has a 4-bit SDIO interface and a hardware-supported card detection function (CD). SD Card write-protection status can be verified using the related test point on the board. The Verdin family supports SD Card Low Voltage Signalling mode. So, if the SD card itself also supports this mode, then communication will start at 3.3V and switch to 1.8V after the card has been initialized.

The SD_1_PWR_EN signal allows to power ON and OFF SD the Card power supply (+V3.3_SD).

2.10.1 SD Card 4bit Connector (X19)

Connector type: SD Card, Würth 693063020911

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SD_1_D3</td>
<td>72</td>
<td>I/O</td>
<td>+1.8/3.3V</td>
<td>Pull-up on a SoM</td>
<td>Serial Data 3</td>
</tr>
<tr>
<td>2</td>
<td>SD_1_CMD</td>
<td>74</td>
<td>I/O</td>
<td>+1.8/3.3V</td>
<td>Pull-up on a SoM</td>
<td>Command</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>+V3.3_SD</td>
<td>PWR</td>
<td></td>
<td>+3.3V</td>
<td></td>
<td>SD Card power input</td>
</tr>
<tr>
<td>5</td>
<td>SD_1_CLK</td>
<td>78</td>
<td>O</td>
<td>+1.8/3.3V</td>
<td></td>
<td>Serial Clock</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>SD_1_D0</td>
<td>80</td>
<td>I/O</td>
<td>+1.8/3.3V</td>
<td>Pull-up on a SoM</td>
<td>Serial Data 0</td>
</tr>
<tr>
<td>8</td>
<td>SD_1_D1</td>
<td>82</td>
<td>I/O</td>
<td>+1.8/3.3V</td>
<td>Pull-up on a SoM</td>
<td>Serial Data 1</td>
</tr>
<tr>
<td>9</td>
<td>SD_1_D2</td>
<td>70</td>
<td>I/O</td>
<td>+1.8/3.3V</td>
<td>Pull-up on a SoM</td>
<td>Serial Data 2</td>
</tr>
<tr>
<td>10</td>
<td>SD_1_CD#</td>
<td>84</td>
<td>I</td>
<td>+1.8/3.3V</td>
<td>Pull-up on a SoM</td>
<td>Card Detect</td>
</tr>
<tr>
<td>11</td>
<td>SD1_WP</td>
<td>(TP8)</td>
<td>I</td>
<td></td>
<td></td>
<td>Write Protection</td>
</tr>
</tbody>
</table>
2.11 Display Interface

The Verdin Development Board provides two options for connecting LCD panels and monitors via the following two interfaces supported:

- HDMI
- MIPI DSI

Almost any TFT display can be connected to the Verdin module by HDMI port X37 or via the DSI interface connector X48. X48 features a universal mezzanine board connector. This solution allows for connecting various types of display interface mezzanine boards and converters, e.g., DSI to HDMI, DSI to LVDS, DSI to RGB, etc. Custom boards with the appropriate MIPI DSI connector can also be used.

2.11.1 HDMI Connector (X11)

Connector type: HDMI Connector Right Angle, Amphenol 10029449-111RLF

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
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### 2.11.2 DSI Display Adapter Connector (X48)

**Connector type:** Samtec LSS-130-03-DV-A-K-TR

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<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
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</tr>
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<td>7-24V power supply output</td>
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<td>7-24V ±10%</td>
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<td>I/O Type</td>
<td>Voltage</td>
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<td>Description</td>
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<td>DSI Interface differential clock, negative</td>
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<td>1.8k to +V1.8_SW</td>
<td>DSI adapters DDC Data</td>
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<td>+1.8V</td>
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</table>
2.12 Audio

The Verdin Development Board offers two audio interfaces: an analog audio interface and a digital audio interface (routed to DSI display adapter connector X48).

2.12.1 Analog Audio

The analog audio interface is based on the NAU88C22YG audio codec IC from Nuvoton. The analog audio interfaces are available on connectors X14, X20, X21, X22, which are standard 3.5mm stereo connectors for AUX OUT, HEADPHONE OUT, AUX IN, and MIC IN. The NAU88C22YG audio codec IC also contains a speaker driver, and its output is available on connectors X13, X28, X29.

2.12.1.1 AUX OUT Audio Jack (X14)

Connector type: 3.5mm Jack, CUI SJ1-3535NG

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
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<td>4.7k to GND</td>
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<td>Auxiliary output 1 / Line out Right</td>
</tr>
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<td></td>
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<td></td>
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</tr>
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<td>5</td>
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Figure 7: Analog Audio architecture
### 2.12.1.2 AUX IN Audio Jack (X21)

**Connector type:** 3.5mm Jack, CUI SJ1-3535NG-BE

<table>
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<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
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<td>PWR</td>
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<td>(Analog)</td>
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<td>Auxiliary input 1 / Line input Right</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 2.12.1.3 HEADPHONES OUT Audio Jack (X20)

**Connector type:** 3.5mm Jack, CUI SJ1-3535NG-GR

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>AAP_HP_CON_L</td>
<td>(Analog)</td>
<td>10k to GND</td>
<td></td>
<td>Headphones output Left</td>
</tr>
<tr>
<td>3</td>
<td>AAP_HP_CON_R</td>
<td>(Analog)</td>
<td>10k to GND</td>
<td></td>
<td>Headphones output Right</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>5</td>
<td>AAP_LLIN_CON_GPIO2</td>
<td></td>
<td>+1.8V</td>
<td>47k to +V1.8_AAP_VDDB</td>
<td>Headphones connect detection</td>
</tr>
</tbody>
</table>

### 2.12.1.4 MIC IN Audio Jack (X22)

**Connector type:** 3.5mm Jack, CUI SJ1-3535NG-PI

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>AAP_LMIC_CON_P</td>
<td>I</td>
<td>2.2k to AAP_MICBIAS</td>
<td>Microphone input Left</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>AAP_RMIC_CON_P</td>
<td>I</td>
<td>2.2k to AAP_MICBIAS</td>
<td>Microphone input Right</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>AAP_MIC_1_OUT</td>
<td>O</td>
<td></td>
<td></td>
<td>On-board microphone output</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Microphone MIC1, located on the board, is be used when the external microphone is disconnected.

### 2.12.1.5 SPEAKER OUT 2-pin header (X22)

**Connector type:** 1x3 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AAP_SPKOUT_CON_R</td>
<td>O</td>
<td>47k to GND</td>
<td>Right speaker output</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>AAP_SPKOUT_CON_L</td>
<td>O</td>
<td>47k to GND</td>
<td>Left speaker output</td>
<td></td>
</tr>
</tbody>
</table>

### 2.12.1.6 SPEAKER OUT 3-pin header (X29)

**Connector type:** 1x2 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AAP_SPKOUT_R</td>
<td>O</td>
<td></td>
<td>BTL1 Speaker Positive Output</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>AAP_SPKOUT_L</td>
<td>O</td>
<td></td>
<td>BTL1 Speaker Negative Output</td>
<td></td>
</tr>
</tbody>
</table>
2.12.1.7 SPEAKER OUT Connector (X28)

Connector type: 1x2 Terminal block, CUI TBLH10-500-02BK

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AAP_SPKOUT_R</td>
<td>O</td>
<td></td>
<td></td>
<td>BTL Speaker Positive Output</td>
</tr>
<tr>
<td>2</td>
<td>AAP_SPKOUT_L</td>
<td>O</td>
<td></td>
<td></td>
<td>BTL Speaker Negative Output</td>
</tr>
</tbody>
</table>

1: BTL – Bridge-Tied-Load speaker output configuration. The two channels of a stereo amplifier are fed the same monaural audio signal, with one channel’s electrical polarity reversed. A loudspeaker is connected between the two amplifier outputs, bridging the output terminals. This doubles the available voltage swing at the load compared with the same amplifier used without bridging.

2.12.2 Digital Audio

Digital audio on the Verdin Development Board is available as an I²S interface (I²S_2). It is provided on the X48 connector (MIPI DSI interface) to provide the option of using an audio interface along with display solutions. For detailed information, refer to the X48 connector pinout.

2.13 “Module-specific” Interface

The “Module-specific” mezzanine board connector provides access to the “Module-specific” interfaces on the Verdin SoM. The range of available interfaces depends on the Verdin module being used. For this reason, “Module-specific” (MSP) signals can be both differential pairs or single-ended signals. All potential differential signals are routed as differential lines with impedance control (100 Ohm for differential and 55 Ohm for single-ended) and equal length. This allows them to be used for any high-speed interface a module may provide.

“Module-specific” mezzanine boards are available for most Verdin SoMs and are connected to this interface to provide access to the “Module-specific” features of those SoMs. Please refer to the datasheets of the individual “Module-specific” mezzanine boards and respective Verdin SoMs for more information.

Customers are free to develop their own “Module-specific” mezzanine boards for prototyping and development purposes. If high-speed differential signals available on MSP pins are used in a custom application, then stitching capacitors should be placed on single-ended MSP signal lines (please check the schematic of the Verdin Development Board). The stitching capacitors provide a return path for the MSP differential signal’s currents, improving signal integrity and reducing EMI.

2.13.1 “Module-specific” Mezzanine Board Connector (X52)

Connector type: Samtec LSS-150-03-L-DV-A-K-TR

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PWR_1V8_MOCI</td>
<td>214</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
<td>+1.8V SoM power output, 250 mA max</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>MSP_39/40_P</td>
<td>180</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 39/40 positive signal</td>
</tr>
<tr>
<td>7</td>
<td>MSP_39/40_N</td>
<td>178</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 39/40 negative signal</td>
</tr>
<tr>
<td>9</td>
<td>MSP_38</td>
<td>176</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 38</td>
</tr>
<tr>
<td>11</td>
<td>MSP_36/37_P</td>
<td>174</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 36/37 positive signal</td>
</tr>
<tr>
<td>13</td>
<td>MSP_36/37_N</td>
<td>172</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 36/37 negative signal</td>
</tr>
<tr>
<td>Pin</td>
<td>Signal Name</td>
<td>SODIMM Pin</td>
<td>I/O Type</td>
<td>Voltage</td>
<td>Pull-up/Pull-down</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
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<td>---------</td>
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<td>-------------</td>
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<tr>
<td>17</td>
<td>MSP_34/35_P</td>
<td>168</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 34/35 positive signal</td>
</tr>
<tr>
<td>19</td>
<td>MSP_34/35_N</td>
<td>166</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 34/35 negative signal</td>
</tr>
<tr>
<td>21</td>
<td>MSP_33</td>
<td>164</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 33</td>
</tr>
<tr>
<td>23</td>
<td>MSP_31/32_P</td>
<td>162</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 31/32 positive signal</td>
</tr>
<tr>
<td>25</td>
<td>MSP_31/32_N</td>
<td>160</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 31/32 negative signal</td>
</tr>
<tr>
<td>27</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>MSP_29/30_P</td>
<td>156</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 29/30 positive signal</td>
</tr>
<tr>
<td>31</td>
<td>MSP_29/30_N</td>
<td>154</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 29/30 negative signal</td>
</tr>
<tr>
<td>33</td>
<td>MSP_28</td>
<td>152</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 28</td>
</tr>
<tr>
<td>35</td>
<td>MSP_26/27_P</td>
<td>150</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 26/27 positive signal</td>
</tr>
<tr>
<td>37</td>
<td>MSP_26/27_N</td>
<td>148</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 26/27 negative signal</td>
</tr>
<tr>
<td>39</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>MSP_24/25_P</td>
<td>144</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 24/25 positive signal</td>
</tr>
<tr>
<td>43</td>
<td>MSP_24/25_N</td>
<td>142</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 24/25 negative signal</td>
</tr>
<tr>
<td>45</td>
<td>MSP_23</td>
<td>140</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 23</td>
</tr>
<tr>
<td>47</td>
<td>MSP_21/22_P</td>
<td>138</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 21/22 positive signal</td>
</tr>
<tr>
<td>49</td>
<td>MSP_21/22_N</td>
<td>136</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 21/22 negative signal</td>
</tr>
<tr>
<td>51</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>MSP_19/20_P</td>
<td>132</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 19/20 positive signal</td>
</tr>
<tr>
<td>55</td>
<td>MSP_19/20_N</td>
<td>130</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 19/20 negative signal</td>
</tr>
<tr>
<td>57</td>
<td>MSP_18</td>
<td>128</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 18</td>
</tr>
<tr>
<td>59</td>
<td>MSP_16/17_P</td>
<td>126</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 16/17 positive signal</td>
</tr>
<tr>
<td>61</td>
<td>MSP_16/17_N</td>
<td>124</td>
<td>I/O</td>
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<td>MSP interface differential pair 16/17 negative signal</td>
</tr>
<tr>
<td>63</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>MSP_14/15_P</td>
<td>120</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 14/15 positive signal</td>
</tr>
<tr>
<td>67</td>
<td>MSP_14/15_N</td>
<td>118</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 14/15 negative signal</td>
</tr>
<tr>
<td>69</td>
<td>MSP_13</td>
<td>116</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 13</td>
</tr>
<tr>
<td>71</td>
<td>MSP_11/12_P</td>
<td>114</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 11/12 positive signal</td>
</tr>
<tr>
<td>73</td>
<td>MSP_11/12_N</td>
<td>112</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 11/12 negative signal</td>
</tr>
<tr>
<td>75</td>
<td>GND</td>
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<td>PWR</td>
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<tr>
<td>Pin</td>
<td>Signal Name</td>
<td>SODIMM Pin</td>
<td>I/O Type</td>
<td>Voltage</td>
<td>Pull-up/Pull-down</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>---------------------</td>
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<td>----------</td>
<td>---------</td>
<td>------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>77</td>
<td>MSP_9/10_P</td>
<td>108</td>
<td>I/O</td>
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<td></td>
<td>MSP interface differential pair 9/10 positive signal</td>
</tr>
<tr>
<td>79</td>
<td>MSP_9/10_N</td>
<td>106</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 9/10 negative signal</td>
</tr>
<tr>
<td>81</td>
<td>MSP_8</td>
<td>104</td>
<td>I/O</td>
<td></td>
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<td>MSP interface single-ended signal 8</td>
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<tr>
<td>83</td>
<td>MSP_6/7_P</td>
<td>102</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 6/7 positive signal</td>
</tr>
<tr>
<td>85</td>
<td>MSP_6/7_N</td>
<td>100</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 6/7 negative signal</td>
</tr>
<tr>
<td>87</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>89</td>
<td>MSP_4/5_P</td>
<td>96</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 4/5 positive signal</td>
</tr>
<tr>
<td>91</td>
<td>MSP_4/5_N</td>
<td>94</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 4/5 negative signal</td>
</tr>
<tr>
<td>93</td>
<td>MSP_3</td>
<td>92</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 3</td>
</tr>
<tr>
<td>95</td>
<td>MSP_1/2_P</td>
<td>90</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 1/2 positive signal</td>
</tr>
<tr>
<td>97</td>
<td>MSP_1/2_N</td>
<td>88</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 1/2 negative signal</td>
</tr>
<tr>
<td>99</td>
<td>GND</td>
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<td>PWR</td>
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<td>PWR</td>
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<td></td>
</tr>
<tr>
<td>4</td>
<td>MSP_44/45_P</td>
<td>192</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 44/45 positive signal</td>
</tr>
<tr>
<td>6</td>
<td>MSP_44/45_N</td>
<td>190</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 44/45 negative signal</td>
</tr>
<tr>
<td>8</td>
<td>MSP_43</td>
<td>188</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface single-ended signal 43</td>
</tr>
<tr>
<td>10</td>
<td>MSP_41/42_P</td>
<td>186</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 41/42 positive signal</td>
</tr>
<tr>
<td>12</td>
<td>MSP_41/42_N</td>
<td>184</td>
<td>I/O</td>
<td></td>
<td></td>
<td>MSP interface differential pair 41/42 negative signal</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
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<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>I2C_4_CSI_SCL</td>
<td>95</td>
<td>O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
<td>CSI Camera I²C bus Clock</td>
</tr>
<tr>
<td>18</td>
<td>I2C_4_CSI_SDA</td>
<td>93</td>
<td>I/O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
<td>CSI Camera I²C bus Data</td>
</tr>
<tr>
<td>20</td>
<td>SODIMM_222 (GPIO_8_CSI)</td>
<td>222</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/Os, dedicated for the MIPI CSI camera interface</td>
</tr>
<tr>
<td>22</td>
<td>SODIMM_220 (GPIO_7_CSI)</td>
<td>220</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>SODIMM_218 (GPIO_6_CSI)</td>
<td>218</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>SODIMM_216 (GPIO_5_CSI)</td>
<td>216</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>GPIO_4</td>
<td>212</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/O</td>
</tr>
<tr>
<td>30</td>
<td>GPIO_3</td>
<td>210</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/O</td>
</tr>
<tr>
<td>32</td>
<td>GPIO_2</td>
<td>208</td>
<td>I/O</td>
<td>+1.8V</td>
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<td>General-purpose I/O</td>
</tr>
<tr>
<td>34</td>
<td>GPIO_1</td>
<td>206</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/O</td>
</tr>
<tr>
<td>36</td>
<td>MSP_CSI_1_MCLK</td>
<td>91</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>CSI camera master clock</td>
</tr>
<tr>
<td>38</td>
<td>CTRL_RESET_MOCI#</td>
<td>258</td>
<td>O (OD)</td>
<td>+3.3V</td>
<td>10k to +V3.3_SW</td>
<td>General reset signal</td>
</tr>
<tr>
<td>40</td>
<td>CTRL_SLEEP_MOCI#</td>
<td>256</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>General power enable signal</td>
</tr>
<tr>
<td>42</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>254</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>CTRL_WAKE1_MICO#</td>
<td>252</td>
<td>I</td>
<td>+1.8V</td>
<td>5.1k to +V1.8_SW</td>
<td></td>
</tr>
<tr>
<td>Pin</td>
<td>Signal Name</td>
<td>SODIMM Pin</td>
<td>I/O Type</td>
<td>Voltage</td>
<td>Pull-up/Pull-down</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-------------------------</td>
<td>------------</td>
<td>----------</td>
<td>---------</td>
<td>-------------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>46</td>
<td>SPI_1_CS</td>
<td>202</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>SPI Slave Select</td>
</tr>
<tr>
<td>48</td>
<td>SPI_1_MOSI</td>
<td>200</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>SPI Master Output, Slave Input</td>
</tr>
<tr>
<td>50</td>
<td>SPI_1_MISO</td>
<td>198</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
<td>SPI Master Input, Slave Output</td>
</tr>
<tr>
<td>52</td>
<td>SPI_1_CLK</td>
<td>196</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>SPI Serial Clock</td>
</tr>
<tr>
<td>54</td>
<td>I2C_1_SCL</td>
<td>14</td>
<td>O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
<td>Generic I²C bus Clock</td>
</tr>
<tr>
<td>56</td>
<td>I2C_1_SDA</td>
<td>12</td>
<td>I/O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
<td>Generic I²C bus Data</td>
</tr>
<tr>
<td>58</td>
<td>PWR_CTRL_10</td>
<td></td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>MSP mezzanine board power enable</td>
</tr>
<tr>
<td>60</td>
<td>+V1.8_SW</td>
<td></td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
<td>+1.8V power supply output</td>
</tr>
<tr>
<td>62</td>
<td>+V1.8_SW</td>
<td></td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
<td>+1.8V power supply output</td>
</tr>
<tr>
<td>64</td>
<td>+V3.3_SW</td>
<td></td>
<td>PWR</td>
<td>+3.3V</td>
<td></td>
<td>+3.3V power supply output</td>
</tr>
<tr>
<td>66</td>
<td>+V3.3_SW</td>
<td></td>
<td>PWR</td>
<td>+3.3V</td>
<td></td>
<td>+3.3V power supply output</td>
</tr>
<tr>
<td>68</td>
<td>+V5_SW</td>
<td></td>
<td>PWR</td>
<td>+5V</td>
<td></td>
<td>+5V power supply output</td>
</tr>
<tr>
<td>70</td>
<td>+V5_SW</td>
<td></td>
<td>PWR</td>
<td>+5V</td>
<td></td>
<td>+5V power supply output</td>
</tr>
<tr>
<td>72</td>
<td>+V_SUPPLY_FILT_SW</td>
<td></td>
<td>PWR</td>
<td>7-24V</td>
<td>±10%</td>
<td>7-24V ±10% power supply output</td>
</tr>
<tr>
<td>74</td>
<td>+V_SUPPLY_FILT_SW</td>
<td></td>
<td>PWR</td>
<td>7-24V</td>
<td>±10%</td>
<td>7-24V ±10% power supply output</td>
</tr>
<tr>
<td>76</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>78</td>
<td>I2S_2_D_IN</td>
<td>48</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
<td>Serial audio input data</td>
</tr>
<tr>
<td>80</td>
<td>I2S_2_D_OUT</td>
<td>46</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>Serial audio output data</td>
</tr>
<tr>
<td>82</td>
<td>I2S_2_SYNC</td>
<td>44</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>Synchronization/ field select/ left-right channel select</td>
</tr>
<tr>
<td>84</td>
<td>I2S_2_BCLK</td>
<td>42</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>Serial audio bit clock</td>
</tr>
<tr>
<td>86</td>
<td>SODIMM_21 (GPIO_10_DSI)</td>
<td>21</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose IOs, dedicated for the MIPI DSI display adapters</td>
</tr>
<tr>
<td>88</td>
<td>SODIMM_17 (GPIO_9_DSI)</td>
<td>17</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td>SODIMM_19 (PWM_3_DSI)</td>
<td>19</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>P WM output, dedicated for the MIPI DSI display backlight brightness control</td>
</tr>
<tr>
<td>92</td>
<td>PWM_2</td>
<td>16</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose PWM outputs</td>
</tr>
<tr>
<td>94</td>
<td>PWM_1</td>
<td>15</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>96</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>98</td>
<td>I2C_2_DSI_SCL</td>
<td>55</td>
<td>O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
<td>DSI adapters DDC Clock</td>
</tr>
<tr>
<td>100</td>
<td>I2C_2_DSI_SDA</td>
<td>53</td>
<td>I/O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
<td>DSI adapters DDC Data</td>
</tr>
</tbody>
</table>
## 2.14 MIPI CSI Camera Interface

The MIPI CSI Camera Interface on connector X47 is intended for applications requiring image capture capability from CMOS or CDD image sensors. For details, please see the relevant Verdin module datasheet.

### 2.14.1 MIPI CSI Camera Connector (X47)

Connector type: 24 Position FFC, FPC, vertical 0.5mm, Hirose FH12-24S-0.5SV(54)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>CSI_1_D0_CON_N</td>
<td>125</td>
<td>I/O</td>
<td></td>
<td></td>
<td>CSI differential data lane 0, negative</td>
</tr>
<tr>
<td>3</td>
<td>CSI_1_D0_CON_P</td>
<td>123</td>
<td>I/O</td>
<td></td>
<td></td>
<td>CSI differential data lane 0, positive</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>CSI_1_D1_CON_N</td>
<td>119</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential data lane 1, negative</td>
</tr>
<tr>
<td>6</td>
<td>CSI_1_D1_CON_P</td>
<td>117</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential data lane 1, positive</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CSI_1_CLK_CON_N</td>
<td>113</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential clock, negative</td>
</tr>
<tr>
<td>9</td>
<td>CSI_1_CLK_CON_P</td>
<td>111</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential clock, positive</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>CAM_1_CON_RST</td>
<td>216</td>
<td>O</td>
<td></td>
<td></td>
<td>Camera RESET</td>
</tr>
<tr>
<td>12</td>
<td>SCI_1_MCLK</td>
<td>91</td>
<td>O</td>
<td></td>
<td></td>
<td>CSI camera master clock</td>
</tr>
<tr>
<td>13</td>
<td>I2C_4_CSI_CON_SCL</td>
<td>95</td>
<td>O</td>
<td>+3.3V</td>
<td>10k to +V3.3_SW</td>
<td>CSI Camera I2C bus Clock</td>
</tr>
<tr>
<td>14</td>
<td>I2C_4_CSI_CON_SDA</td>
<td>93</td>
<td>I/O</td>
<td>+3.3V</td>
<td>10k to +V3.3_SW</td>
<td>CSI Camera I2C bus Data</td>
</tr>
<tr>
<td>15</td>
<td>+V3.3_SW</td>
<td>PWR</td>
<td>+3.3V</td>
<td></td>
<td></td>
<td>+3.3V power out</td>
</tr>
<tr>
<td>16</td>
<td>CSI_1_D2_CON_N</td>
<td>107</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential data lane 2, negative</td>
</tr>
<tr>
<td>17</td>
<td>CSI_1_D2_CON_P</td>
<td>105</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential data lane 2, positive</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td></td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>CSI_1_D3_CON_N</td>
<td>101</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential data lane 3, negative</td>
</tr>
<tr>
<td>20</td>
<td>CSI_1_D3_CON_P</td>
<td>99</td>
<td>I</td>
<td></td>
<td></td>
<td>CSI differential data lane 3, positive</td>
</tr>
<tr>
<td>21</td>
<td>+V5_SW</td>
<td>PWR</td>
<td>+5V</td>
<td></td>
<td></td>
<td>+5V power output</td>
</tr>
<tr>
<td>22</td>
<td>CAM_1_CON_PWRDWN</td>
<td>218</td>
<td>O</td>
<td>+3.3V</td>
<td></td>
<td>Camera Power Down</td>
</tr>
<tr>
<td>23</td>
<td>CAM_1_CON_IC_DETECT</td>
<td>220</td>
<td>I</td>
<td>+3.3V</td>
<td></td>
<td>Camera Identification</td>
</tr>
<tr>
<td>24</td>
<td>CAM_1_CON_PWRCTRL</td>
<td>222</td>
<td>O</td>
<td>+3.3V</td>
<td></td>
<td>Power Supply Control</td>
</tr>
</tbody>
</table>
2.15 Digital and Analog I/O

2.15.1 Communication Interface

2.15.1.1 CAN

The Verdin Development Board uses the Texas Instruments isolated ISO1042BDWR CAN transceiver to implement two CAN FD interfaces in conjunction with the two CAN interface on the Verdin module.

CAN ports are electrically isolated from the system power supply and provide an isolated 5V power supply output with a load capacity of 126 mA for each port.

The CAN interfaces are available on connectors X59 and X60. Pin header-to-DSUB9 adapters can be used with X59, X60 connectors.

The jumpers JP1, JP2, JP3, JP4 provide hardware configuration for these interfaces:

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Status</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1, JP2</td>
<td>CLOSED</td>
<td>CAN1 split terminated.</td>
</tr>
</tbody>
</table>

By default, the jumpers JP1, JP2, JP3, JP4 are closed.

2.15.1.1.1 CAN1 Connector (X59)

Connector type: 2x5 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>2</td>
<td>CAN_1_PGND</td>
<td>PWR</td>
<td></td>
<td>CAN_1 isolated GND</td>
</tr>
<tr>
<td>3</td>
<td>CAN_1_L</td>
<td>I/O</td>
<td></td>
<td>Low-level CAN_1 bus line</td>
</tr>
<tr>
<td>4</td>
<td>CAN_1_H</td>
<td>I/O</td>
<td></td>
<td>High-level CAN_1 bus line</td>
</tr>
<tr>
<td>5</td>
<td>GND_CAN_1_ISO</td>
<td></td>
<td></td>
<td>Connected through 100 Ohm</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>8</td>
<td>CAN_1_PWR</td>
<td>PWR</td>
<td>+5V</td>
<td>CAN_1 isolated power out</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
</tbody>
</table>

2.15.1.1.2 CAN2 Connector (X60)

Connector type: 2x5 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>2</td>
<td>CAN_2_PGND</td>
<td>PWR</td>
<td></td>
<td>CAN_2 isolated GND</td>
</tr>
<tr>
<td>3</td>
<td>CAN_2_L</td>
<td>I/O</td>
<td></td>
<td>Low-level CAN_1 bus line</td>
</tr>
<tr>
<td>4</td>
<td>CAN_2_H</td>
<td>I/O</td>
<td></td>
<td>High-level CAN_1 bus line</td>
</tr>
<tr>
<td>5</td>
<td>GND_CAN_1_ISO</td>
<td></td>
<td></td>
<td>Connected through 100 Ohm</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>8</td>
<td>CAN_2_PWR</td>
<td>PWR</td>
<td>+5V</td>
<td>CAN_2 isolated power out</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td></td>
<td></td>
<td>Not connected</td>
</tr>
</tbody>
</table>
2.15.1.2 UART Interfaces

The Verdin Development Board features 4 UART interfaces that are connected to the following connectors:

- UART1 to the connector X50 through an RS485 transceiver.
- UART2 to the connector X51 through an RS232 transceiver.
- UART3 to a built-in USB to Serial transceiver (Primary debug log output for Cortex-A cores).
- UART4 to a built-in USB to Serial transceiver (Primary debug log output for Cortex-M core).

2.15.1.2.1 RS485 Connector (X50)

Connector type: D-Sub 9 Male, Assmann WSW A-DS 09 A/KG-T4S

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>RS485_CON_A</td>
<td>I/O</td>
<td>Digital</td>
<td>bus I/O, A</td>
</tr>
<tr>
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<td>RS485_CON_B</td>
<td>I/O</td>
<td>Digital</td>
<td>bus I/O, B</td>
</tr>
</tbody>
</table>

S1/S2: GND_CHASSIS

Jumpers JP6, JP9, and JP10 provide hardware configuration for this interface:

- Connector type: 1x2 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Status</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP6</td>
<td>CLOSED</td>
<td>The slew rate is reduced to 250 kbps. The default is 20 Mbps.</td>
</tr>
<tr>
<td>JP9</td>
<td>CLOSED</td>
<td>Insert the 120ohm bus termination for RS485</td>
</tr>
<tr>
<td>JP10</td>
<td>CLOSED</td>
<td>ECHO disabled (the sender cannot read the message just sent)</td>
</tr>
</tbody>
</table>

By default, the jumpers JP6, JP9, JP10 are closed.

2.15.1.2.2 RS232 Connector (X51)

Connector type: D-Sub 9-pin Male, Assmann WSW A-DS 09 A/KG-T4S

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RS232_RXD</td>
<td>I</td>
<td>RS232</td>
<td>Receive Data</td>
</tr>
<tr>
<td>3</td>
<td>RS232_TXD</td>
<td>O</td>
<td>RS232</td>
<td>Transmit Data</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RS232_RTS</td>
<td>O</td>
<td>RS232</td>
<td>Request to Send (RTS)</td>
</tr>
<tr>
<td>8</td>
<td>RS232_CTS</td>
<td>I</td>
<td>RS232</td>
<td>Clear to Send (CTS)</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

S1/S2: GND_CHASSIS

By using the jumper JP12, it is possible to configure the Auto Powerdown Plus function of the RS232 transceiver. The following table shows the JP12 connection possibilities.
Connector type: 1x3 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Jumper position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - 2</td>
<td>Auto Powerdown Plus disabled</td>
</tr>
<tr>
<td>2 - 3</td>
<td>Auto Powerdown Plus enabled</td>
</tr>
</tbody>
</table>

By default, the jumper JP12 is installed in position 1-2.

For detailed information about the Auto Powerdown Plus function, please refer to the TRS3122ERGER transceiver datasheet (FORCEON and FORCENOFF# pins functions).

2.16 Digital interfaces

2.16.1 Switches / LEDs

The Verdin Development Board features four general-purpose green LEDs, four general-purpose switches, and four general-purpose buttons. Pins of these devices are available on connectors X23, X24, X26, X27, and X38 (See Figure 8 and 9). They can be directly connected to the GPIO breakout connectors or specific custom hardware. Please note that the buttons and switches are not de-bounced.

2.16.1.1 Switches Connector (X23)
Connector type: 1x2 Pin Header Female, 2.54 mm pitch, Samtec SSW-102-01-G-S

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW_4</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>2</td>
<td>SW_8</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to GND</td>
</tr>
</tbody>
</table>

2.16.1.2 Switches Connector (X24)
Connector type: 1x2 Pin Header Female, 2.54 mm pitch, Samtec SSW-102-01-G-S

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW_5</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>2</td>
<td>SW_9</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to GND</td>
</tr>
</tbody>
</table>

2.16.1.3 Switches Connector (X26)
Connector type: 1x2 Pin Header Female, 2.54 mm pitch, Samtec SSW-102-01-G-S

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW_6</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>2</td>
<td>SW_10</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
</tbody>
</table>

2.16.1.4 Switches Connector (X27)
Connector type: 1x2 Pin Header Female, 2.54 mm pitch, Samtec SSW-102-01-G-S

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW_7</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>2</td>
<td>SW_11</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
</tbody>
</table>
### 2.16.1.1.5 LEDs Connector (X38)

Connector type: 1x2 Pin Header Female, 2.54 mm pitch, Samtec SSW-102-01-G-S

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Linked LED</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+V1.8_SW</td>
<td>-</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>LED_1</td>
<td>LED21</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>3</td>
<td>LED_2</td>
<td>LED22</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>4</td>
<td>LED_3</td>
<td>LED23</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>5</td>
<td>LED_4</td>
<td>LED24</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>-</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
</tr>
</tbody>
</table>

Figure 8: General-purpose switches' schematic

Figure 9: General-purpose LEDs' schematic
2.16.2 Level shifters

Two level-shifters with push-pull outputs (IC31, IC32) and one with open-drain outputs (IC33) have been placed on the Verdin Development Board. The I/O pins of these level shifters are connected to female pin headers X39, X40. These general-purpose level shifters can be used to connect external 3.3V compatible hardware with the jumper wires.

2.16.2.1.1 Level Shifter Connector (X39)

**Connector type: 1x10 Pin Header Female, 2.54 mm pitch**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LS_1.8V_GPIO_1</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>General-purpose 1.8V level-shifted inputs</td>
</tr>
<tr>
<td>2</td>
<td>LS_1.8V_GPIO_2</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>General-purpose 1.8V level-shifted outputs</td>
</tr>
<tr>
<td>3</td>
<td>LS_1.8V_GPIO_3</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>General-purpose 1.8V level-shifted outputs</td>
</tr>
<tr>
<td>4</td>
<td>LS_1.8V_GPIO_4</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>General-purpose 1.8V level-shifted outputs</td>
</tr>
<tr>
<td>5</td>
<td>LS_1.8V_GPIO_5</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose 1.8V level-shifted inputs</td>
</tr>
<tr>
<td>6</td>
<td>LS_1.8V_GPIO_6</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose 1.8V level-shifted outputs</td>
</tr>
<tr>
<td>7</td>
<td>LS_1.8V_GPIO_7</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose 1.8V level-shifted outputs</td>
</tr>
<tr>
<td>8</td>
<td>LS_1.8V_GPIO_8</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose 1.8V level-shifted outputs</td>
</tr>
<tr>
<td>9</td>
<td>LS_1.8V_SCL</td>
<td>I/O (OD)</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
<td>General-purpose 1.8V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration</td>
</tr>
<tr>
<td>10</td>
<td>LS_1.8V_SDA</td>
<td>I/O (OD)</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
<td>General-purpose 1.8V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration</td>
</tr>
</tbody>
</table>

2.16.2.1.2 Level Shifter Connector (X40)

**Connector type: 1x10 Pin Header Female, 2.54 mm pitch**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LS_3.3V_GPIO_1</td>
<td>O</td>
<td>+3.3V</td>
<td></td>
<td>General-purpose 3.3V level-shifted outputs</td>
</tr>
<tr>
<td>2</td>
<td>LS_3.3V_GPIO_2</td>
<td>O</td>
<td>+3.3V</td>
<td></td>
<td>General-purpose 3.3V level-shifted outputs</td>
</tr>
<tr>
<td>3</td>
<td>LS_3.3V_GPIO_3</td>
<td>O</td>
<td>+3.3V</td>
<td></td>
<td>General-purpose 3.3V level-shifted outputs</td>
</tr>
<tr>
<td>4</td>
<td>LS_3.3V_GPIO_4</td>
<td>O</td>
<td>+3.3V</td>
<td></td>
<td>General-purpose 3.3V level-shifted outputs</td>
</tr>
<tr>
<td>5</td>
<td>LS_3.3V_GPIO_5</td>
<td>I</td>
<td>+3.3V</td>
<td>100k to GND</td>
<td>General-purpose 3.3V level-shifted inputs</td>
</tr>
<tr>
<td>6</td>
<td>LS_3.3V_GPIO_6</td>
<td>I</td>
<td>+3.3V</td>
<td>100k to GND</td>
<td>General-purpose 3.3V level-shifted inputs</td>
</tr>
<tr>
<td>7</td>
<td>LS_3.3V_GPIO_7</td>
<td>I</td>
<td>+3.3V</td>
<td>100k to GND</td>
<td>General-purpose 3.3V level-shifted inputs</td>
</tr>
<tr>
<td>8</td>
<td>LS_3.3V_GPIO_8</td>
<td>I</td>
<td>+3.3V</td>
<td>100k to GND</td>
<td>General-purpose 3.3V level-shifted inputs</td>
</tr>
<tr>
<td>9</td>
<td>LS_3.3V_SCL</td>
<td>I/O (OD)</td>
<td>+3.3V</td>
<td>10k to +V3.3_SW</td>
<td>General-purpose 3.3V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration</td>
</tr>
<tr>
<td>10</td>
<td>LS_3.3V_SDA</td>
<td>I/O (OD)</td>
<td>+3.3V</td>
<td>10k to +V3.3_SW</td>
<td>General-purpose 3.3V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration</td>
</tr>
</tbody>
</table>
2.16.3 Analog Interface

The Analog inputs of a Verdin module are connected to the dedicated connector X49. For detailed information about ADC features, please refer to the respective Verdin module datasheet.

2.16.3.1 ADC Input (X49)

Type: 2x3 Pin Header Female, 2.54mm pitch

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ADC_1</td>
<td>2</td>
<td>I (Analog)</td>
<td>+1.8V</td>
<td>Analog Input 1</td>
</tr>
<tr>
<td>2</td>
<td>ADC_2</td>
<td>4</td>
<td>I (Analog)</td>
<td>+1.8V</td>
<td>Analog Input 2</td>
</tr>
<tr>
<td>3</td>
<td>ADC_3</td>
<td>6</td>
<td>I (Analog)</td>
<td>+1.8V</td>
<td>Analog Input 3</td>
</tr>
<tr>
<td>4</td>
<td>ADC_4</td>
<td>8</td>
<td>I (Analog)</td>
<td>+1.8V</td>
<td>Analog Input 4</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PWR_1V8_MOCI</td>
<td>214</td>
<td>PWR</td>
<td>+1.8V</td>
<td>SoM’s 1.8V power output</td>
</tr>
</tbody>
</table>
2.17 Backup battery

A backup battery holder (BAT1) is available on the Verdin Development Board to provide backup power to the RTC of a Verdin module when the main power is turned off. Jumper (JP8) is used to connect or disconnect the backup battery.

Connector type: 1x2 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Status</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP8</td>
<td>CLOSED</td>
<td>Battery backup voltage, connected to the Verdin module internal RTC.</td>
</tr>
<tr>
<td>JP8</td>
<td>OPEN</td>
<td>Battery backup voltage disconnected from the Verdin module internal RTC.</td>
</tr>
</tbody>
</table>

By default, jumper JP8 is closed.

For more details on how the backup voltage is used, please refer to the respective Verdin computer-on-module datasheet.

2.17.1 Battery Holder (BAT1)

A 20 mm (diameter) coin cell/battery should be used with the Battery Holder (BAT1). A coin-cell battery can be used to provide power backup to the Verdin module RTC circuit when an external power supply is not available.

Supported batteries: CR2032 or compatible coin-cell batteries.

Connector type: Renata HU2032-LF

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+V_BAT</td>
<td>+3.0V</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td></td>
</tr>
</tbody>
</table>

2.18 Temperature sensor

Verdin Development Board provides the Digital Temperature Sensor feature (IC50) with an I²C interface. The sensor is connected to the general-purpose I2C_1 bus. The default I²C address of the sensor is 0x4F. For details, please check the TMP75CIDGKR sensor datasheet.

2.19 EEPROM

A 2-Kbit EEPROM (IC29) with a I²C interface is installed on the Development Board. The EEPROM can be used to store important data or for board identification. For EEPROM's technical details, please check the M24C02-FMN6TP datasheet. The EEPROM is accessible at the address 0x57 on the generic serial bus I2C_1.

Jumper JP5 can be used to control the EEPROM’s “Write Protection” function.

Type: 1x3 Pin Header Male, 2.54 mm pitch

<table>
<thead>
<tr>
<th>Jumper position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>EEPROM’s “Write Control” (WC) pin is driven “High”. Write operations are disabled to the entire memory array.</td>
</tr>
<tr>
<td>2-3</td>
<td>EEPROM’s “Write Control” (WC) pin is driven “Low”. Write operations are enabled.</td>
</tr>
</tbody>
</table>

By default, jumper JP5 is in position 1-2.
2.20 JTAG

The Verdin Development Board provides a JTAG interface to the JTAG port available on Verdin modules. Connector X56 provides an interface to an external JTAG device via a Cortex Debug Connector, which is a 10-pin 1.27mm header. The Verdin Development Board also has an on-board JTAG debugger feature. Please check the USB Debugger section of this datasheet and the Verdin Development Board schematic file for detailed information. This document is available on the Toradex developer website, on the Development Board Design page.

**WARNING!**

If an external JTAG debugger is used with a Verdin Development Board, jumpers X67A – X67F should be removed. Simultaneous use of the on-board and external JTAG Debugger is not allowed. Violating this requirement may damage the debugger or the Verdin Development Board.

### 2.20.1 JTAG Connector (X56)

Connector Type: 2x5 Pin Shrouded Header Male, 1.27mm, Samtec FTSH-105-01-L-DV-K

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>SODIMM Pin</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>JTAG_1_VREF</td>
<td>7</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
<td>1.8V reference output for JTAG adapter</td>
</tr>
<tr>
<td>2</td>
<td>JTAG_1_TMS</td>
<td>13</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
<td>Test Mode Select</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>JTAG_1_TCK</td>
<td>9</td>
<td>I</td>
<td>+1.8V</td>
<td>Pull-down on SOM</td>
<td>Test Clock</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>JTAG_1_TDO</td>
<td>5</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>Test Data Out</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>8</td>
<td>JTAG_1_TDI</td>
<td>1</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
<td>Test Data In</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Not Connected</td>
</tr>
<tr>
<td>10</td>
<td>JTAG_1_TRST#</td>
<td>3</td>
<td>I (OD)</td>
<td>+1.8V</td>
<td></td>
<td>Test Reset</td>
</tr>
</tbody>
</table>
2.21 USB Debugger

The Verdin Development Board provides an on-board Universal USB Debugger (IC41). The debugger is based on the FT4232HL chip and provides the following features:

- 2x UART ports connected to Verdin Module Cortex-A and Cortex-M core debug outputs
- JTAG Debugger/Programmer
- 4x GPIO used for performing basic Development Board control features: Power ON/OFF, Reset etc.

Simplified USB Debugger architecture is shown below.

The pin assignments of the FT4232HL are shown in the table below.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin Name</th>
<th>I/O Type</th>
<th>Interface</th>
<th>Connected/Controlled Net</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>ADBUS4</td>
<td>O</td>
<td>GPIO</td>
<td>CTRL_FORCE_OFF_MOCI#</td>
<td>Verdin Development Board FORCE OFF</td>
</tr>
<tr>
<td>22</td>
<td>ADBUS5</td>
<td>O</td>
<td>GPIO</td>
<td>CTRL_RESET_MICO#</td>
<td>Verdin Module RESET</td>
</tr>
<tr>
<td>23</td>
<td>ADBUS6</td>
<td>O</td>
<td>GPIO</td>
<td>PWR_BTN#</td>
<td>Verdin Development Board POWER ON/OFF</td>
</tr>
<tr>
<td>24</td>
<td>ADBUS7</td>
<td>O</td>
<td>GPIO</td>
<td>CTRL_RECOVERY_MICO#</td>
<td>Verdin Module RECOVERY mode</td>
</tr>
<tr>
<td>26</td>
<td>BDBUS0</td>
<td>O</td>
<td>JTAG</td>
<td>JTAG_TCK</td>
<td>JTAG Test Mode Select</td>
</tr>
<tr>
<td>27</td>
<td>BDBUS1</td>
<td>O</td>
<td>JTAG</td>
<td>JTAG_TDI</td>
<td>JTAG Test Data Input</td>
</tr>
<tr>
<td>28</td>
<td>BDBUS2</td>
<td>I</td>
<td>JTAG</td>
<td>JTAG_TDO</td>
<td>JTAG Test Data Output</td>
</tr>
<tr>
<td>29</td>
<td>BDBUS3</td>
<td>O</td>
<td>JTAG</td>
<td>JTAG_TMS</td>
<td>JTAG Test Mode Set</td>
</tr>
<tr>
<td>30</td>
<td>BDBUS4</td>
<td>O</td>
<td>JTAG</td>
<td>JTAG_TRST#</td>
<td>JTAG Test Mode Reset</td>
</tr>
<tr>
<td>34</td>
<td>BDBUS7</td>
<td>O</td>
<td>JTAG</td>
<td>JTAG_LED</td>
<td>JTAG activity LED</td>
</tr>
<tr>
<td>38</td>
<td>CDBUS0</td>
<td>O</td>
<td>UART</td>
<td>UART_4_RXD</td>
<td>Receiver Data of Cortex-M debug UART</td>
</tr>
<tr>
<td>39</td>
<td>CDBUS1</td>
<td>I</td>
<td>UART</td>
<td>UART_4_TXD</td>
<td>Transmitter Data of Cortex-M debug UART</td>
</tr>
<tr>
<td>48</td>
<td>DDBUS0</td>
<td>O</td>
<td>UART</td>
<td>UART_3_RXD</td>
<td>Receiver Data of Cortex-A debug UART</td>
</tr>
<tr>
<td>52</td>
<td>DDBUS1</td>
<td>I</td>
<td>UART</td>
<td>UART_3_TXD</td>
<td>Transmitter Data of Cortex-A debug UART</td>
</tr>
</tbody>
</table>
The debug interface is accessible via the separate USB-C connector X66.

### 2.21.1.1 USB Debugger Connector (X66)

**Connector type: USB-C, Amphenol 12401598E4#2A**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>+V5_DBG</td>
<td>PWR</td>
<td>+5V</td>
<td></td>
<td>FTDI debugger power supply input</td>
</tr>
<tr>
<td>A5</td>
<td>USB_DBG_CC1</td>
<td></td>
<td>5.1k to GND</td>
<td></td>
<td>Type-C configuration channel signal 1</td>
</tr>
<tr>
<td>A6</td>
<td>USB_DBG_CON_P</td>
<td>I/O</td>
<td></td>
<td></td>
<td>Positive Differential USB 2.0 Signal</td>
</tr>
<tr>
<td>A7</td>
<td>USB_DBG_CON_N</td>
<td>I/O</td>
<td></td>
<td></td>
<td>Negative Differential USB 2.0 Signal</td>
</tr>
<tr>
<td>A8</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A9</td>
<td>+V5_DBG</td>
<td>PWR</td>
<td>+5V</td>
<td></td>
<td>FTDI debugger power supply input</td>
</tr>
<tr>
<td>A10</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A11</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A12</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B3</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B4</td>
<td>+V5_DBG</td>
<td>PWR</td>
<td>+5V</td>
<td></td>
<td>FTDI debugger power supply input</td>
</tr>
<tr>
<td>B5</td>
<td>USB_DBG_CC2</td>
<td></td>
<td>5.1k to GND</td>
<td></td>
<td>Type-C configuration channel signal 2</td>
</tr>
<tr>
<td>B6</td>
<td>USB_DBG_CON_P</td>
<td>I/O</td>
<td></td>
<td></td>
<td>Positive Differential USB 2.0 Signal</td>
</tr>
<tr>
<td>B7</td>
<td>USB_DBG_CON_N</td>
<td>I/O</td>
<td></td>
<td></td>
<td>Negative Differential USB 2.0 Signal</td>
</tr>
<tr>
<td>B8</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B9</td>
<td>+V5_DBG</td>
<td>PWR</td>
<td>+5V</td>
<td></td>
<td>FTDI debugger power supply input</td>
</tr>
<tr>
<td>B10</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B11</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B12</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**The FTDI JTAG interface is connected to the SoM and the Verdin Development Board via the X67 jumper area.**

### 2.21.1.1.1 Jumper Area (X67)

**Connector type: 2x6 Pin Header Male, 2.54 mm pitch**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O Type</th>
<th>Pin</th>
<th>Pin</th>
<th>I/O Type</th>
<th>Signal Name</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>FTDI_JTAG_TCK</td>
<td>O</td>
<td>B1</td>
<td>A1</td>
<td>I</td>
<td>JTAG_1_TCK</td>
<td>+1.8V</td>
</tr>
<tr>
<td>FTDI_JTAG_TDI</td>
<td>O</td>
<td>B2</td>
<td>A2</td>
<td>I</td>
<td>JTAG_1_TDI</td>
<td>+1.8V</td>
</tr>
<tr>
<td>FTDI_JTAG_TDO</td>
<td>I</td>
<td>B3</td>
<td>A3</td>
<td>O</td>
<td>JTAG_1_TDO</td>
<td>+1.8V</td>
</tr>
<tr>
<td>FTDI_JTAG_TMS</td>
<td>O</td>
<td>B4</td>
<td>A4</td>
<td>I</td>
<td>JTAG_1_TMS</td>
<td>+1.8V</td>
</tr>
<tr>
<td>FTDI_JTAG_TRST#</td>
<td>O</td>
<td>B5</td>
<td>A5</td>
<td>I</td>
<td>JTAG_1_TRST#</td>
<td>+1.8V</td>
</tr>
<tr>
<td>FTDI_JTAG_VREF</td>
<td>PWR</td>
<td>B6</td>
<td>A6</td>
<td>PWR</td>
<td>JTAG_1_VREF</td>
<td>+1.8V</td>
</tr>
</tbody>
</table>
By changing the configuration of the jumpers X67A-X67F, the user can connect or disconnect the on-board JTAG Debugger to/from the SoM.

**Connector type: 2x6 Pin Header Male, 2.54 mm pitch**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Status</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>X67A, X67B, X67C, X67D, X67E, X67F</td>
<td>CLOSED</td>
<td>FTDI JTAG Debugger connected to SoM</td>
</tr>
<tr>
<td>X67A, X67B, X67C, X67D, X67E, X67F</td>
<td>OPEN</td>
<td>FTDI JTAG Debugger disconnected from SoM</td>
</tr>
</tbody>
</table>

By default, jumpers X67A, X67B, X67C, X67D, X67E, X67F are closed.

**WARNING!**

If an external JTAG debugger is used with a Verdin Development Board, jumpers X67A – X67F should be removed. Simultaneous use of the on-board and external JTAG Debugger is not allowed. Violating this requirement may damage the debugger or the Verdin Development Board.

The FTDI GPIO pins are connected via the X6 pin header. For details, please refer to the X6 pinout.

The FTDI GPIO pins can be used to control the Development Board or as regular GPIO (outputs only) to control other parts of the board.

Jumper JP30 should be configured according to the desired FTDI GPIO pins functionality. Possible configurations are listed in the table below.

**Type: 1x3 Pin Header Male, 2.54 mm pitch**

<table>
<thead>
<tr>
<th>Jumper position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>FTDI GPIO pins can be used to control Verdin Development Board modes.</td>
</tr>
<tr>
<td>2-3</td>
<td>FTDI GPIO pins can be used as regular GPIO (outputs only)</td>
</tr>
</tbody>
</table>

By default, jumper JP30 is installed in position 1-2.

### 2.22 Low-speed IO pins configuration

The Low-speed IO pins’ breakout connectors offer the flexibility to map the IO pins of the Verdin module to either the on-board function or to external hardware.

The factory setting is a straight-through jumper setting, meaning that the X3-A row is connected straight to the X3-B row. This is also true for the connectors X6 and X16.

All signals residing on the male header are also available on a female connector in parallel to allow easy measurement, probing, and re-routing.

To map the SODIMM pin with the corresponding SoC ball name, which is specific to individual Verdin modules, please refer to the applicable Verdin module datasheet.
2.22.1 Low-speed IO pins 1 Male (X3 Row A and B)

Connector Type: 2x30Pin Male, 2.54mm

<table>
<thead>
<tr>
<th>SODIMM Pin</th>
<th>Pin</th>
<th>Signal Name</th>
<th>Signal Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>A1</td>
<td>SODIMM_12</td>
<td>I2C_1_SDA</td>
<td>I/O</td>
<td>+1.8V</td>
<td>Generic I²C Data</td>
</tr>
<tr>
<td>14</td>
<td>A2</td>
<td>SODIMM_14</td>
<td>I2C_1_SCL</td>
<td>O</td>
<td>+1.8V</td>
<td>Generic I²C Clock</td>
</tr>
<tr>
<td>15</td>
<td>A3</td>
<td>SODIMM_15</td>
<td>PWM_1</td>
<td>O</td>
<td>+1.8V</td>
<td>General-purpose PWM</td>
</tr>
<tr>
<td>16</td>
<td>A4</td>
<td>SODIMM_16</td>
<td>PWM_2</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>A5</td>
<td>SODIMM_20</td>
<td>CAN_1_TX</td>
<td>I</td>
<td>+1.8V</td>
<td>CAN port 1 transmit pin</td>
</tr>
<tr>
<td>22</td>
<td>A6</td>
<td>SODIMM_22</td>
<td>CAN_1_RX</td>
<td>I</td>
<td>+1.8V</td>
<td>CAN port 1 receive pin</td>
</tr>
<tr>
<td>24</td>
<td>A7</td>
<td>SODIMM_24</td>
<td>CAN_2_TX</td>
<td>O</td>
<td>+1.8V</td>
<td>CAN port 2 transmit pin</td>
</tr>
<tr>
<td>26</td>
<td>A8</td>
<td>SODIMM_26</td>
<td>CAN_2_RX</td>
<td>I</td>
<td>+1.8V</td>
<td>CAN port 2 receive pin</td>
</tr>
<tr>
<td>GND</td>
<td>A9</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td>+1.8V</td>
<td>+1.8V power supply output</td>
</tr>
<tr>
<td></td>
<td>A10</td>
<td>+V1.8_SW</td>
<td>PWR</td>
<td>+1.8V</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>A11</td>
<td>SODIMM_30</td>
<td>I2S_1_BCLK</td>
<td>O</td>
<td>+1.8V</td>
<td>I²S Serial Clock (Transmit Bit Clock)</td>
</tr>
<tr>
<td>32</td>
<td>A12</td>
<td>SODIMM_32</td>
<td>I2S_1_SYNC</td>
<td>O</td>
<td>+1.8V</td>
<td>I²S Field Select (Transmit Frame Sync)</td>
</tr>
<tr>
<td>34</td>
<td>A13</td>
<td>SODIMM_34</td>
<td>I2S_1_D_OUT</td>
<td>O</td>
<td>+1.8V</td>
<td>I²S Data Output</td>
</tr>
<tr>
<td>36</td>
<td>A14</td>
<td>SODIMM_36</td>
<td>I2S_1_D_IN</td>
<td>I</td>
<td>+1.8V</td>
<td>I²S Data Input</td>
</tr>
<tr>
<td>38</td>
<td>A15</td>
<td>SODIMM_38</td>
<td>I2S_1_MCLK</td>
<td>O</td>
<td>+1.8V</td>
<td>I²S Master clock output</td>
</tr>
<tr>
<td>GND</td>
<td>A16</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A17</td>
<td>+V1.8_SW</td>
<td>PWR</td>
<td>+1.8V</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>A18</td>
<td>SODIMM_42</td>
<td>I2S_2_BCLK</td>
<td>O</td>
<td>+1.8V</td>
<td>I²S Serial Clock (Transmit Bit Clock)</td>
</tr>
<tr>
<td>44</td>
<td>A19</td>
<td>SODIMM_44</td>
<td>I2S_2_SYNC</td>
<td>O</td>
<td>+1.8V</td>
<td>I²S Field Select (Transmit Frame Sync)</td>
</tr>
<tr>
<td>46</td>
<td>A20</td>
<td>SODIMM_46</td>
<td>I2S_2_D_OUT</td>
<td>O</td>
<td>+1.8V</td>
<td>I²S Data Output</td>
</tr>
<tr>
<td>48</td>
<td>A21</td>
<td>SODIMM_48</td>
<td>I2S_2_D_IN</td>
<td>I</td>
<td>+1.8V</td>
<td>I²S Data Input</td>
</tr>
<tr>
<td>52</td>
<td>A22</td>
<td>SODIMM_52</td>
<td>QSPI_1_CLK</td>
<td>O</td>
<td>+1.8V</td>
<td>QSPI Serial Clock</td>
</tr>
<tr>
<td>54</td>
<td>A23</td>
<td>SODIMM_54</td>
<td>QSPI_1_CS#</td>
<td>O</td>
<td>+1.8V</td>
<td>QSPI Chip Select 0</td>
</tr>
<tr>
<td>56</td>
<td>A24</td>
<td>SODIMM_56</td>
<td>QSPI_1_IO0</td>
<td>I/O</td>
<td>+1.8V</td>
<td>QSPI Serial I/Os for command, address, and data</td>
</tr>
<tr>
<td>58</td>
<td>A25</td>
<td>SODIMM_58</td>
<td>QSPI_1_IO1</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>SODIMM Pin</td>
<td>Signal Name</td>
<td>Pin</td>
<td>Pin</td>
<td>Signal Name</td>
<td>I/O Type</td>
<td>Voltage</td>
</tr>
<tr>
<td>------------</td>
<td>-------------</td>
<td>-----</td>
<td>-----</td>
<td>-------------</td>
<td>----------</td>
<td>---------</td>
</tr>
<tr>
<td>60</td>
<td>SODIMM_60</td>
<td>A25</td>
<td>B25</td>
<td>QSPI_1_IO2</td>
<td>I/O</td>
<td>+1.8V</td>
</tr>
<tr>
<td>62</td>
<td>SODIMM_62</td>
<td>A26</td>
<td>B26</td>
<td>QSPI_1_IO3</td>
<td>I/O</td>
<td>+1.8V</td>
</tr>
<tr>
<td>64</td>
<td>SODIMM_64</td>
<td>A27</td>
<td>B27</td>
<td>QSPI_1_CS2#</td>
<td>O</td>
<td>+1.8V</td>
</tr>
<tr>
<td>66</td>
<td>SODIMM_66</td>
<td>A28</td>
<td>B28</td>
<td>QSPI_1_DQS</td>
<td>I</td>
<td>+1.8V</td>
</tr>
<tr>
<td>76</td>
<td>SODIMM_76</td>
<td>A29</td>
<td>B29</td>
<td>SD_1_PWR_EN</td>
<td>O</td>
<td>+1.8V</td>
</tr>
<tr>
<td>84</td>
<td>SODIMM_84</td>
<td>A30</td>
<td>B30</td>
<td>SD_1_CD#</td>
<td>I</td>
<td>+1.8/3.3V</td>
</tr>
</tbody>
</table>

2.22.2 Low-speed IO pins 1 Female (X2)

Connector Type: 1x30Pin Female, 2.54mm
Pinout identical to X3 Pins A1 to A30

2.22.3 Function 1 Female (X4)

Connector Type: 1x30Pin Female, 2.54mm
Pinout identical to X3 Pins B1 to B30
2.22.4 Low-speed IO pins 2 Male (X6 Row A and B)

**Connector Type: 2x30Pin Male**

<table>
<thead>
<tr>
<th>SODIMM Pin</th>
<th>Signal Name</th>
<th>SoM Side</th>
<th>Signal Name</th>
<th>Peripheral Side</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>196</td>
<td>SODIMM_196</td>
<td>A1</td>
<td>B1</td>
<td>SPI_1_CLK</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>SPI Serial Clock</td>
</tr>
<tr>
<td>198</td>
<td>SODIMM_198</td>
<td>A2</td>
<td>B2</td>
<td>SPI_1_MISO</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
<td>SPI Master Input, Slave Output</td>
</tr>
<tr>
<td>200</td>
<td>SODIMM_200</td>
<td>A3</td>
<td>B3</td>
<td>SPI_1_MOSI</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>SPI Master Output, Slave Input</td>
</tr>
<tr>
<td>202</td>
<td>SODIMM_202</td>
<td>A4</td>
<td>B4</td>
<td>SPI_1_CS</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>SPI Slave Select</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>A5</td>
<td>B5</td>
<td>GND</td>
<td>PWR</td>
<td></td>
<td></td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>206</td>
<td>SODIMM_206</td>
<td>A6</td>
<td>B6</td>
<td>GPIO_1</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>208</td>
<td>SODIMM_208</td>
<td>A7</td>
<td>B7</td>
<td>GPIO_2</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>210</td>
<td>SODIMM_210</td>
<td>A8</td>
<td>B8</td>
<td>GPIO_3</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>212</td>
<td>SODIMM_212</td>
<td>A9</td>
<td>B9</td>
<td>GPIO_4</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>214</td>
<td>SODIMM_PWR_1V8_MOCl</td>
<td>A10</td>
<td>B10</td>
<td>PWR_1V8_MOCl</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
<td>+1.8V SoM power output</td>
</tr>
<tr>
<td>216</td>
<td>SODIMM_216</td>
<td>A11</td>
<td>B11</td>
<td>GPIO_5_CSI</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>General-purpose I/Os dedicated for the CSI camera interface</td>
</tr>
<tr>
<td>218</td>
<td>SODIMM_218</td>
<td>A12</td>
<td>B12</td>
<td>GPIO_6_CSI</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>220</td>
<td>SODIMM_220</td>
<td>A13</td>
<td>B13</td>
<td>GPIO_7_CSI</td>
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<td>+1.8V</td>
<td></td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>222</td>
<td>SODIMM_222</td>
<td>A14</td>
<td>B14</td>
<td>GPIO_8_CSI</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>General-purpose I/Os</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>A15</td>
<td>B15</td>
<td>GND</td>
<td>PWR</td>
<td></td>
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<td>General-purpose I/Os</td>
</tr>
<tr>
<td>216</td>
<td>FTDI_GPIOL3</td>
<td>A16</td>
<td>B16</td>
<td>DBG_RECOVERY#</td>
<td>I</td>
<td>+1.8V</td>
<td>10k to +V1.8_DBG</td>
<td>SoM RECOVERY mode debugger control input</td>
</tr>
<tr>
<td>218</td>
<td>FTDI_GPIOL2</td>
<td>A17</td>
<td>B17</td>
<td>DBG_PWR_BTN#</td>
<td>I</td>
<td>+1.8V</td>
<td>10k to +V1.8_DBG</td>
<td>Board POWER button debugger control input</td>
</tr>
<tr>
<td>220</td>
<td>FTDI_GPIOL1</td>
<td>A18</td>
<td>B18</td>
<td>DBG_RESET#</td>
<td>I</td>
<td>+1.8V</td>
<td>10k to +V1.8_DBG</td>
<td>General board RESET debugger control input</td>
</tr>
<tr>
<td>222</td>
<td>FTDI_GPIOL0</td>
<td>A19</td>
<td>B19</td>
<td>DBG_FORCE_OFF#</td>
<td>I</td>
<td>+1.8V</td>
<td>10k to +V1.8_DBG</td>
<td>General board FORCE OFF debugger control input</td>
</tr>
<tr>
<td>+V1.8_SW</td>
<td></td>
<td>A20</td>
<td>B20</td>
<td>+V1.8_SW</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
<td>+1.8V Power supply output</td>
</tr>
<tr>
<td>246</td>
<td>SODIMM_246</td>
<td>A21</td>
<td>B21</td>
<td>CTRL_RECOVERY_MICO#</td>
<td>(OD)</td>
<td>+1.8V</td>
<td></td>
<td>SoM RECOVERY mode control</td>
</tr>
<tr>
<td>248</td>
<td>SODIMM_248</td>
<td>A22</td>
<td>B22</td>
<td>CTRL_PWR_BTN_MICO#</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
<td>SoM POWER button control input</td>
</tr>
<tr>
<td>250</td>
<td>SODIMM_250</td>
<td>A23</td>
<td>B23</td>
<td>CTRL_FORCE_OFF_MOCI#</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to +V5_STB</td>
<td>General board FORCE OFF control</td>
</tr>
<tr>
<td>SODIMM Pin</td>
<td>Signal Name</td>
<td>Pin</td>
<td>Pin</td>
<td>Signal Name</td>
<td>I/O Type</td>
<td>Voltage</td>
<td>Pull-up/Pull-down</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>---------------</td>
<td>-----</td>
<td>-----</td>
<td>------------------</td>
<td>----------</td>
<td>---------</td>
<td>-------------------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>252</td>
<td>SODIMM_252</td>
<td>A24</td>
<td>B24</td>
<td>CTRL_WAKE1_MICO#</td>
<td>I</td>
<td>+1.8V</td>
<td>5.1k to +V1.8_SW</td>
<td>WAKE signal to out SoM from SLEEP mode</td>
</tr>
<tr>
<td>254</td>
<td>SODIMM_254</td>
<td>A25</td>
<td>B25</td>
<td>CTRL_PWR_EN_MOCI</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
<td>Power enable for the on-board peripherals</td>
</tr>
<tr>
<td>256</td>
<td>SODIMM_256</td>
<td>A26</td>
<td>B26</td>
<td>CTRL_SLEEP_MOCI#</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
<td>Sleep signal for the on-board peripherals</td>
</tr>
<tr>
<td>258</td>
<td>SODIMM_258</td>
<td>A27</td>
<td>B27</td>
<td>CTRL_RESET_MOCI#</td>
<td>O</td>
<td>+3.3V</td>
<td>10k to +V3.3_SW</td>
<td>Reset for the on-board peripherals</td>
</tr>
<tr>
<td>260</td>
<td>SODIMM_260</td>
<td>A28</td>
<td>B28</td>
<td>CTRL_RESET_MICO#</td>
<td>I (OD)</td>
<td>+1.8V</td>
<td></td>
<td>SoM’s RESET signal</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>A29</td>
<td>B29</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>196</td>
<td>+V1.8_SW</td>
<td>A30</td>
<td>B30</td>
<td>+V1.8_SW</td>
<td>PWR</td>
<td>+1.8V</td>
<td></td>
<td>+1.8V Power supply output</td>
</tr>
</tbody>
</table>

2.22.5 Function 2 Female (X5)

Connector Type: 1x30Pin Female, 2.54mm
Pinout identical to X6 Pins A1 to A30

2.22.6 Low-speed IO pins 2 Female (X7)

Connector Type: 1x30Pin Female, 2.54mm
Pinout identical to X6 Pins B1 to B30
### 2.22.7  Low-speed IO pins 3 Male (X16 Row A and B)

**Connector Type:** 2x30Pin Male

<table>
<thead>
<tr>
<th>SODIMM Pin</th>
<th>SoM Side</th>
<th>Peripheral Side</th>
<th>I/O Type</th>
<th>Voltage</th>
<th>Pull-up/Pull-down</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>187</td>
<td>SODIMM_187</td>
<td>A1 B1</td>
<td>USB_2_OC#</td>
<td>I (OD)</td>
<td>+1.8V</td>
<td>100k to +V1.8_SW</td>
</tr>
<tr>
<td>185</td>
<td>SODIMM_185</td>
<td>A2 B2</td>
<td>USB_2_EN</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>161</td>
<td>SODIMM_161</td>
<td>A3 B3</td>
<td>USB_1_ID</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to +V1.8_SW</td>
</tr>
<tr>
<td>157</td>
<td>SODIMM_157</td>
<td>A4 B4</td>
<td>USB_1_OC#</td>
<td>I</td>
<td>+1.8V</td>
<td>100k to +V1.8_SW</td>
</tr>
<tr>
<td>155</td>
<td>SODIMM_155</td>
<td>A5 B5</td>
<td>USB_1_EN</td>
<td>O</td>
<td>+1.8V</td>
<td>100k to GND</td>
</tr>
<tr>
<td>95</td>
<td>SODIMM_95</td>
<td>A6 B6</td>
<td>I2C_4_CSI_SCL</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>93</td>
<td>SODIMM_93</td>
<td>A7 B7</td>
<td>I2C_4_CSI_SDA</td>
<td>I/O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>91</td>
<td>SODIMM_91</td>
<td>A8 B8</td>
<td>CSI_1_MCLK</td>
<td>O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>SODIMM_63</td>
<td>A9 B9</td>
<td>HDMI_1_CEC</td>
<td>I/O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>61</td>
<td>SODIMM_61</td>
<td>A10 B10</td>
<td>HDMI_1_HP</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>SODIMM_59</td>
<td>A11 B11</td>
<td>I2C_3_HDMI_SCL</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>57</td>
<td>SODIMM_57</td>
<td>A12 B12</td>
<td>I2C_3_HDMI_SDA</td>
<td>I/O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>153</td>
<td>SODIMM_153</td>
<td>A13 B13</td>
<td>UART_4_TXD</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
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<tr>
<td>151</td>
<td>SODIMM_151</td>
<td>A14 B14</td>
<td>UART_4_RXD</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>149</td>
<td>SODIMM_149</td>
<td>A15 B15</td>
<td>UART_3_TXD</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>147</td>
<td>SODIMM_147</td>
<td>A16 B16</td>
<td>UART_3_RXD</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>SODIMM_55</td>
<td>A17 B17</td>
<td>I2C_2_DSI_SCL</td>
<td>O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
</tr>
<tr>
<td>53</td>
<td>SODIMM_53</td>
<td>A18 B18</td>
<td>I2C_2_DSI_SDA</td>
<td>I/O</td>
<td>+1.8V</td>
<td>1.8k to +V1.8_SW</td>
</tr>
<tr>
<td>21</td>
<td>SODIMM_21</td>
<td>A19 B19</td>
<td>GPIO_10_DSI</td>
<td>I/O</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>SODIMM_19</td>
<td>A20 B20</td>
<td>PWM_3_DSI</td>
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<td>SODIMM_17</td>
<td>A21 B21</td>
<td>GPIO_9_DSI</td>
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<td>143</td>
<td>SODIMM_143</td>
<td>A22 B22</td>
<td>UART_2_CTS</td>
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<td>+1.8V</td>
<td></td>
</tr>
<tr>
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<td>A23 B23</td>
<td>UART_2_RTS</td>
<td>O</td>
<td>+1.8V</td>
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</tr>
<tr>
<td>SODIMM Pin</td>
<td>Signal Name</td>
<td>Pin</td>
<td>Pin</td>
<td>I/O Type</td>
<td>Voltage</td>
<td>Pull-up/Pull-down</td>
</tr>
<tr>
<td>------------</td>
<td>---------------</td>
<td>-----</td>
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<td>139</td>
<td>SODIMM_139</td>
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<td>B24</td>
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</tr>
<tr>
<td>137</td>
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<td>B25</td>
<td>I</td>
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<tr>
<td>135</td>
<td>SODIMM_135</td>
<td>A26</td>
<td>B26</td>
<td>I</td>
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</tr>
<tr>
<td>133</td>
<td>SODIMM_133</td>
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<td>B27</td>
<td>O</td>
<td>+1.8V</td>
<td>10k to +V1.8_SW</td>
</tr>
<tr>
<td>131</td>
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<td>B28</td>
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<td></td>
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<td>129</td>
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<td>B29</td>
<td>I</td>
<td>+1.8V</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>A30</td>
<td>B30</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.22.8 Low-speed IO pins 3 Female (X15)

Connector Type: 1x30 Pin Female, 2.54mm
Pinout identical to X16 Pins A1 to A30

2.22.9 Function 3 Female (X17)

Connector Type: 1x30 Pin Female, 2.54mm
Pinout identical to X16 Pins B1 to B30
Figure 12: Verdin Development Board dimensions (in millimeters)
4 Design Data

The design data for Toradex Development Board is freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the Development Board design data, please use the link below:
http://developer.toradex.com/carrier-board-design

5 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at http://www.toradex.com/support/product-compliance
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