

Verdin Family Specification



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1. Introduction

1.1 Overview

This document is a specification that defines the Verdin Computer-on-Module family (referred to hereafter as “module”). It defines the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also defines the mechanical form factor, including key dimensions and possible thermal solutions.

1.2 Motivations

The following motivations are central to the definition of the Verdin module specification. Verdin is a long-term successor of the very popular Colibri module form factor. Both are very complementary to one another, and while they may overlap in terms of suitability for some specific applications, they differ significantly in a variety of areas, including, but not limited to, size, features, and cost.

1. As ARM-based SoC (System-on-Chip) technology continues to evolve, support for a broader range of interfaces is being added, such as PCI-express, Gigabit Ethernet, HDMI, etc. The Verdin module enables customers to benefit from these evolutions on a small and cost-optimized form factor.
2. With the increasing demand for battery-operated devices, the I/O voltage is trending to decrease from 3.3V to 1.8V. Some SoCs do not offer 3.3V capable I/O pins anymore. The regular I/O pins of the Verdin module have a logic level of 1.8V. This reduces power consumption and eases the usage of a single lithium cell as the primary power source.
3. The Verdin module features a wide input voltage range (3.135V to 5.5V) for the primary power source. This makes it easy to run directly from a USB power supply or a single lithium cell.
4. As the pace in performance advancement accelerates faster than the increase in power efficiency, we see a trend towards increasing power consumption in high-performance ARM-based SoCs. While passive cooling is still perfectly viable in many applications, this increase in power consumption means that allowances for additional cooling solutions, such as heat spreaders for conduction cooling, must be made. The Verdin module provides a robust, easy-to-use, rigid mounting mechanism to support such thermal solutions.
5. The Verdin module has been developed from in-depth research into various technologies, rather than basing it on a specific SoC. This renders the Verdin module architecture future proof and makes it suitable for supporting a wide range of SoCs.
6. The Verdin PCB is thicker than the Colibri PCB. This makes the module mechanically more robust and provides space for additional electrical layers, which allows developing more complex designs on a small form factor.
7. The Verdin module encapsulates the complexities associated with cutting-edge electronic design, such as high-speed impedance-controlled layouts with high component density

utilizing blind and buried via technologies. This allows the customer to create simpler and more cost-efficient carrier board designs. The Verdin module takes this one step further and implements an interface pinout that allows direct connection of I/O ports without a need to cross traces or traverse layers, referred to as Direct Breakout™. This becomes important for customers as more interfaces move toward high speeds and serial technologies that rely on impedance-controlled differential pairs. Direct Breakout™ allows them to easily route such interfaces to common connectors in a simple, robust fashion.

2. Module Overview

2.1 Interface Compatibility Classes

Interfaces of the Verdin module are split into three distinct groups: “Always Compatible”, “Reserved”, and “Module-specific”.

“Always Compatible” interfaces are features that shall be present on each SoM in the Verdin Family. Customers can expect upgradeability and maximum scalability.

“Reserved” interfaces are features that are defined and reserved but possibly missing on some SoMs. The reason for that could be that certain SoCs do not feature an interface, or there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means that any Verdin SoM can be inserted into any Verdin carrier board without risking damage caused by incompatible reserved pins.

A “Module-specific” interface is a feature that is not guaranteed to be functionally or electrically compatible between modules. Different Verdin modules may provide various functionalities on the same sets of “Module-specific” pins. If a carrier board design relies on such features, the selection of Verdin modules suitable for being used with that particular carrier board design may be limited. An incompatible SoM/carrier board combination may disable all functionalities or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

2.1.1 “Always Compatible” Interfaces

The table in Figure 1 shows the interfaces that are provided by every Verdin module. The “GPIO Capable” column indicates whether the assigned pins can be used as GPIOs.

The “Instances” column indicates the number of interfaces that the Verdin specification guarantees to be present for the “Always Compatible” interfaces. Customers should consult the datasheet for specific Verdin module variants to check for special features or restrictions on interfaces.

Description	Instances	Name	Note	GPIO Capable
Gigabit Ethernet	1	ETH_1	Media-dependent interface (PHY on module), backward compatible with Fast Ethernet.	No
USB 2.0 Host	1	USB_2	High-Speed USB, backward compatible with Full and Low-Speed USB.	No
USB 2.0 OTG	1	USB_1	Can be configured for host or client usage. SoC usually uses this port in recovery mode.	No
I ² C	1	I2C_1	General Purpose	Yes*
SPI	1	SPI_1	Single chip select pin	Yes*
UART (RX, TX)	2	UART_1 UART_2	General Purpose	Yes*
UART (RX, TX)	1	UART_3	Primary operating system debug port (console)	Yes*
PWM	1	PWM_1	General Purpose	Yes*
SDIO	1	SD_1	4-bit interface, I/O voltage might be switchable between 1.8V and 3.3V for UHS-I support	Yes*
GPIO	4	GPIO_1..4	General Purpose	Yes
JTAG	1	JTAG_1		Yes*

Figure 1: “Always Compatible” Interfaces

*GPIO function can be limited on some modules. Please check the datasheet of the respective module or the Pinout Designer tool.

2.1.2 “Reserved” Interfaces

The table in Figure 2 shows “Reserved” interfaces.

Some of the “Reserved” interfaces are extending the functionality of an “Always Compatible” interface. For example, the additional USB 3.x SuperSpeed signals in the “Reserved” class must be used in conjunction with the USB 2.0 Host interface signals. There are additional RTS/CTS hardware flow control signals that need to be used in conjunction with the respective general-purpose UART that is in the “Always Compatible” class.

Since the “Reserved” interfaces are possibly missing on some SoC, it is mandatory to consult the module datasheet for further information. A useful tool is the Toradex Pinout Designer, which can help to compare the available features of different Verdin modules.

Description	Standard	Names	Note	GPIO Capable
MIPI DSI	1	DSI_1	Primary display interface, up to 4 data lanes.	No
HDMI	1	HDMI_1	Secondary display interface	No
RGMII	1	ETH_2_RGMII	Backward compatibility with RMI is not mandatory	Yes*
USB 3.x Host	1	USB_2	Additional SuperSpeed signals that need to be used in conjunction with the USB 2.0 Host interface	No
PCIe	1	PCIE_1	1 lane with reference clock. Supported PCIe generation depends on the module	No
I ² C	3	I2C_2_DSI	1x Reserved for DSI (might be usable as general purpose I ² C)	Yes*
		I2C_3_HDMI	1x Reserved for HDMI (might be usable as general purpose I ² C)	
		I2C_4_CSI	1x Reserved for CSI (might be usable as general purpose I ² C)	
QSPI	1	QSPI_1	The related software drivers may prevent this interface from being used as a regular SPI interface.	Yes*
UART (RX, TX)	1	UART_4	Secondary operating system (real-time OS) debug port. It might be usable as general purpose UART.	Yes*
UART (RTS, CTS)	2	UART_1 UART_2	Complementary hardware flow control signals for the fully compatible general purpose UART interfaces	Yes*
CAN	2	CAN_1 CAN_2	CAN or CAN FD compatible	Yes*
MIPI CSI-2	1	CSI_1	Up to 4 data lanes	No
PWM	2	PWM_2 PWM_3_DSI	1x General purpose 1x Reserved for display backlight control	Yes*
I ² S	2	I2S_1	1x With master clock output	Yes*
		I2S_2	1x Without master clock output	
GPIO	6	GPIO_5..8_CSI GPIO_9..10_DSI	2x Reserved for DSI 4x Reserved for CSI	Yes
ADC	4	ADC_1..4		Yes*

Figure 2: “Reserved” Interfaces

*GPIO functionality may be limited on some modules. Please check the datasheet of the respective module or the Pinout Designer tool.

2.1.3 “*Module-specific*” Interfaces

“*Module-specific*” interfaces allow for the possibility of including interfaces that may not be widely adopted (yet) or interfaces that may be specific to a particular device or groups of devices. The concept provides a mechanism for extending features that are present on “*Always Compatible*” or “*Reserved*” pins, e.g., providing additional PCI-Express lanes.

It should be noted that Toradex does its best to keep “*Module-specific*” interfaces standard across modules that share such interfaces. For example, suppose both module A and module B have an LVDS interface available in the same configuration as a “*Module-specific*” interface. In that case, it is a priority to assign them to the same pins in the “*Module-specific*” area of the connector. Hence, both module A and module B would ideally share compatibility between this part of the “*Module-specific*” interface.

2.2 Architecture

The block diagram in Figure 3 shows the basic architecture of the Verdin module, depicting the “*Always Compatible*” interfaces, “*Reserved*” interfaces, and some examples of “*Module-specific*” interfaces.

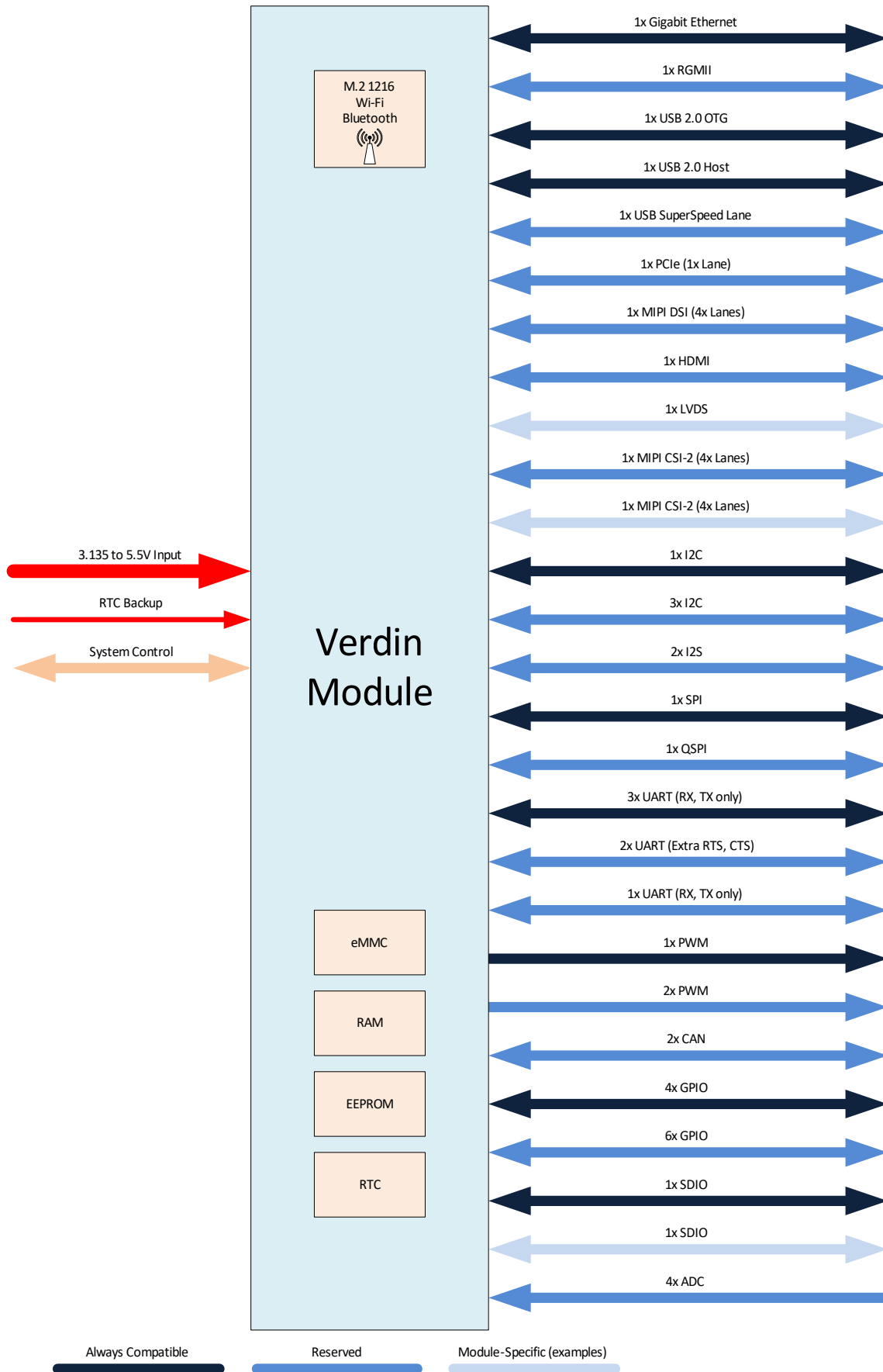


Figure 3: Verdin Module Architecture

2.3 Module and Carrier Board Compatibility

To ensure that any carrier board design is compatible with all Verdin modules, only the standard functions of the “Always Compatible” and “Reserved” interfaces should be used. Alternate functions are not guaranteed to be compatible. Special care must be taken with the “Module-specific” signals. The “Module-specific” signals might be electrically incompatible between different Verdin modules. This means that the system might not work, and this may result in damage done to the module or the carrier board.

The Toradex Pinout Designer tool can be used for comparing available features and interfaces of different Verdin modules. Make sure to enable the note fields in the viewing options in order to get additional information. Even though the Pinout Designer is a very powerful tool, it is still recommended to read the datasheets of the different Verdin modules in order to check the functional and electrical compatibility of the interfaces/pins.



If a custom carrier board implements any “Module-specific” interfaces, it may not be 100% compatible with all Verdin modules. Where “Module-specific” interfaces are common between different Verdin modules, they shall be provided on the same pins where possible. Therefore, designs that make use of the “Module-specific” interfaces of a specific Verdin module may be compatible with other Verdin modules – please check the interface specifications of individual Verdin modules carefully.

3. Interface Specifications

3.1 Signal Naming Convention

Identical signals of different interfaces are distinguished by adding the interface index as a suffix (e.g., PWM_1, PWM_2, etc.). Interface indexing usually starts at one. Signals named after a standard or follow a widely acknowledged common naming convention (such as the Ethernet or LVDS interfaces) may use a zero-based index.

Differential pair signal components are suffixed with either a "P" (for positive) or "N" (for negative). Active low signals are suffixed with a "#".

The underscore ("_") is used as a separator to delimit fragments of the signal name (such as signal group, channel, and signal descriptor components) to make the signal name easy to read and interpret.

3.2 Standard Interfaces

The Verdin standard interfaces are the common name for the "Always Compatible" and "Reserved" interfaces. Toradex Pinout Designer eases the configuration of standard interfaces to facilitate the development process.

3.2.1 Gigabit Ethernet

The gigabit Ethernet port is a media-dependent interface for 10/100/1000 Mbit Ethernet. The PHY is located on the module. Therefore, only the magnetics are required on the carrier board. The signals between the PHY and the magnetics operate in the "voltage" mode. This means there is no center tap voltage required.

3.2.2 USB Host

The USB Host interface consists of a USB 2.0 High-Speed interface which is part of the "Always Compatible" interfaces. This interface is backward compatible with Full- and Low-Speed USB 2.0. In the "Reserved" section, there are additional SuperSpeed signals used in combination with the USB 2.0 data signals to provide a USB 3.x capable interface. The actual supported USB 3.x generation and maximum transfer rate depend on the Verdin module.

3.2.3 USB OTG

The USB OTG port is only USB 2.0 High/Full/Low-Speed capable. There are no additional SuperSpeed signals available for the USB OTG as Verdin standard pins. The USB OTG port can be used as a host or client port. Modules may use this interface to flash the firmware in recovery mode.

3.2.4 I²C

There is one general-purpose I²C interface in the "Always Compatible" section. There are additional three I²C interfaces in the "Reserved" class. These interfaces are reserved for the DSI display, HDMI output, and the CSI camera. If a module does not feature one of these interfaces, the related I²C interface may also be missing. Whenever possible, the reserved I²C interface should be used in combination with its related primary interface. Whether a reserved I²C can also be used as a general-purpose interface depends on the Verdin module. In certain configurations, the I²C port reserved for HDMI cannot be used as a general-purpose interface, and I²C ports tied to DSI and CSI may be used for general communication. Please check the datasheets of Verdin SoMs to understand if these I²C interfaces can be used as general-purpose interfaces.

3.2.5 SPI

There is one SPI interface in the “Always Compatible” class. The interface features a single chip select pin.

3.2.6 QSPI

The QuadSPI interface might be used for interfacing external memory devices (e.g., NAND and NOR flashes).

3.2.7 UART

There are four standard UARTs available on the Verdin module. UART_1 and UART_2 are general-purpose interfaces. The RX and TX signals of these interfaces are in the “Always Compatible” section. In contrast, the additional RTS/CTS signals for hardware flow control are located in the “Reserved” interfaces section.

UART_3 is in the “Always Compatible” section and is intended to be used for main OS debug log output. It could be used for general purposes, but we strongly recommend making this interface available for debugging purposes. UART_4 is in the “Reserved” class. On modules with a real-time core, the interface is intended to be used as the debug log output of the real-time operating system. The interface may be used as a general-purpose UART.

3.2.8 PWM

There are 3 PWM signals on the Verdin standard. PWM_1 is the only one in the “Always Compatible” class. PWM_1, as well as PWM_2, are general purpose pulse width modulation outputs. The third interface, PWM_3_DSI, is reserved for the DSI interface (for display backlight inverter control).

3.2.9 SDIO

The SDIO supports up to 4 data bits. Attention must be taken to the I/O voltage of this interface. To comply with the SD memory card specifications, the I/O pins can run with 3.3V. Verdin modules might integrate UHS-I modes in which the voltage is switched to 1.8V during card initialization. There is no need for pull-up resistors on the carrier board for the SDIO signals (CMD, DATAx, and CLK). Either the SoC has integrated pull-up resistors, or they are located on the module PCB.

3.2.10 MIPI DSI

The MIPI DSI is the primary Verdin display interface and supports up to four data lanes. The supported maximum DSI transfer rate depends on the module.

Simple bridge ICs can be placed on the carrier board to support standard display interfaces such as HDMI and LVDS. The Verdin ecosystem provides a wide range of display adapters that are meant to be reference designs and implementation examples (e.g., Verdin DSI to HDMI Adapter, Verdin DSI to LVDS Adapter, Verdin DSI to RGB Adapter).

3.2.11 HDMI

The HDMI output is the secondary Verdin display interface. The supported HDMI version depends on the Verdin module. Some modules might support DisplayPort as an alternate function.

3.2.12 PCIe

Verdin supports one lane of PCI Express, including a 100MHz reference clock. The supported PCIe generation (interface speed) depends on the module.

3.2.13 CAN

There are up to two Controller Area Network interfaces available on Verdin modules. Depending on the particular module, besides CAN, CAN FD (flexible data rate) may be supported as well.

3.2.14 MIPI CSI-2

There is one MIPI CSI-2 camera interface in the "Reserved" class with up to 4 data lanes. The supported interface speed and maximum resolution depend on the module.

3.2.15 ADC

There are four ADC inputs in the "Reserved" class. The inputs shall have at least an 8-bit resolution and an input voltage range of 0V to 1.8V.

3.2.16 JTAG

Depending on the module, the JTAG interface may be used for debugging purposes or boundary-scan testing in production. Even though the nominal I/O voltage of the JTAG pins is 1.8V, it is recommended to use the JTAG_1_VREF for the I/O voltage of the JTAG adapter. This offers more flexibility for Verdin modules with different JTAG I/O voltages.

3.3 "Module-specific" Interfaces

There is a total of 45 "Module-specific" pins on the Verdin module. These pins may be used for allocating any types of interfaces not fitting in any of the "Always Compatible" and "Reserved" interfaces categories.



Even the interface voltage depends on the module and could lead to malfunction if a Verdin module is used in an incompatible carrier board!

The "Module-specific" pins are allocated on the module edge connector in groups of five signals. Depending on the Verdin module, the pins may be used in different patterns. For example, if the 5 pins are used for a set of two differential pairs, the pin between the pairs can be connected to the ground on the module or might be used for low-speed signals. In this case, a stitching capacitor from the low-speed signal to GND on the module and the carrier board is recommended to provide a return path for the differential pair signals.

Module-Specific Pin	Used as Single Ended	Used as Differential Pair with Ground	Combination of Differential Pair and Low-Speed Single Ended
GND	GND	GND	GND
MSP_1	Single-Ended Pin 1	Diff Pair A Positive	Diff Pair A Positive
MSP_2	Single-Ended Pin 2	Diff Pair A Negative	Diff Pair A Negative
MSP_3	Single-Ended Pin 3	GND	Low-Speed Signal with 1nF Stitching
MSP_4	Single-Ended Pin 4	Diff Pair B Positive	Diff Pair B Positive
MSP_5	Single-Ended Pin 5	Diff Pair B Negative	Diff Pair B Negative
GND	GND	GND	GND

Figure 4: "Module-specific" Pin Group Examples



The assignment of the positive and negative components of differential pairs in Figure 4 is only an example. The module might assign the positive and negative components swapped.

3.4 Physical Pin Definition and Location

Signal definitions in terms of physical pins and their locations on the Verdin module can be found in the appendix. The table in Appendix C defines the physical pins and their location on the Verdin module.

The total number of usable pins on the module is 260. The ground pin count is 47 (~18%). The main power supply (VCC) power pin count is 5.

3.5 Direct Breakout™

Direct Breakout™ aims to reduce the complexity of carrier board routing from the module connector to the real-world I/O ports by making it possible to route signals without traversing layers of crossing critical signals. Interfaces are physically grouped into functional “locations” on the SODIMM connector so that all signals associated with a specific interface are in one common location, reducing routing complexity. The pin order within an interface matches the pin order of commonly used connectors.

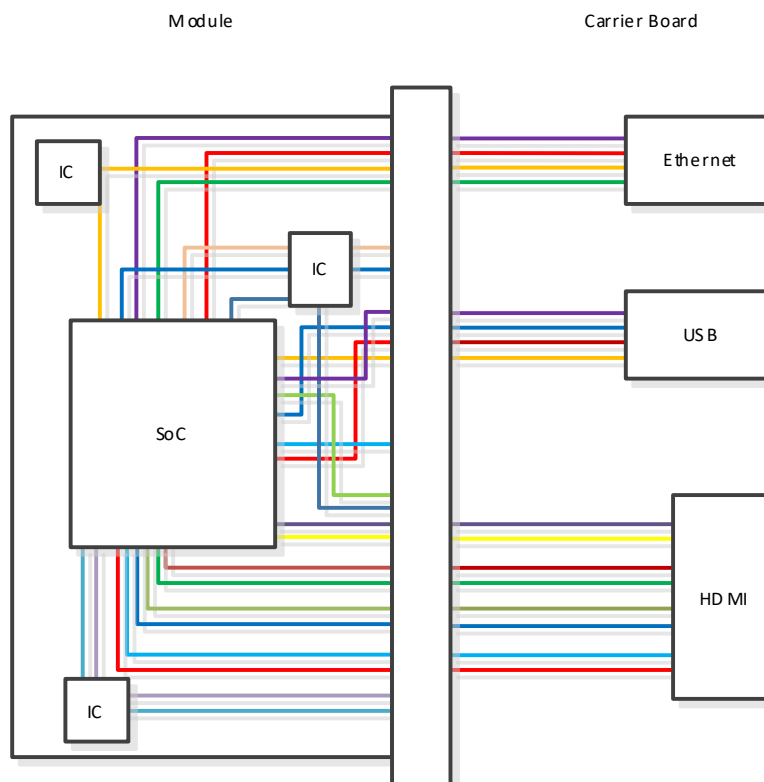


Figure 5: Direct Breakout Example

The image in Figure 5 shows the concept of a direct breakout by illustrating how complex routing and layout are encapsulated on the Verdin module, providing the potential for simple routing on the carrier board.

4. Mechanical Specifications

4.1 Overview

The Verdin module form factor mechanical dimensions have been specified based on careful analysis of required board space for typical device packages (SoC, memory ICs, power ICs, Wi-Fi module, and peripheral ICs) and certain key features. This has been balanced with the requirement to keep the form factor as small as reasonably possible. A single mechanical size has been defined.

4.2 Mounting and Fixation

The SO-DIMM DDR4 connector features latches on the sides for locking the module into the socket. This provides a fast and convenient fixation of the module, which is suitable for typical use cases.

For higher vibration and shock resistance, especially with a mounted heatsink, the Verdin module features two additional M2 mounting holes. This allows for a tight mounting of the module to the carrier board (with stand-offs and screws).

4.3 Module Connector and Stacking Height

The Verdin module uses the SO-DIMM (Small Outline Dual In-line Memory Module) DDR4 memory module edge connector. This connector has 260 pins with a 0.5mm pitch. The nominal PCB thickness of the Verdin module is 1.2mm. This leads to a stiffness that is well suited for harsh environments (with vibrations) and facilitates thermal solutions.

Suitable connectors are available from different manufacturers in various board-to-board stacking heights. Manufacturers such as Amphenol or TE Connectivity use the term stacking height for the connector's overall height. This is not the actual distance between the module and the carrier board, like on board-to-board connector. Amphenol and TE Connectivity provide four different connector heights from 4mm to 9.2mm.

The following table compares the different options. The connector height is the connector's total height that can also be found in the connector's name. The board-to-board distance is the nominal space between the carrier board and the module. Please note that in worst-case situations, this distance can be smaller. The column "Component Height Carrier Board" indicates the recommended maximum height of components underneath the module. Close to the SODIMM connector, there is an area that allows for higher components such as decoupling capacitors or series resistors. The maximum height in this area is listed in the column "Component Height Carrier Board (next to connector)".

Connector Height	Board-to-board distance	Component Height Carrier Board	Component Height Carrier Board (next to connector)	Remarks
4 mm	1.52 mm			Connector not suitable for Verdin modules due to the too-small board-to-board distance
5.2 mm	2.62 mm	0 mm	0.8 mm	Recommended stacking height for Verdin modules
8 mm	5.42 mm	2.8 mm	3.6 mm	
9.2 mm	6.62 mm	4 mm	4.8 mm	

Table 1: SODIMM Connector Stacking Height

There are also reverse angle connectors available. These connectors are not recommended for modules that require a cooling solution. Toradex recommends using the TE Connectivity 2309409-2 which has a connector height of 5.2mm that provides a board-to-board distance of 2.62mm.

The Verdin module does not follow the JEDEC specifications that allow only a maximum of 1.2 mm for components on the top and bottom side of the module. The components on the top side of the Verdin module are limited to 3.0 mm in height. The absolute maximum height for components on the bottom side is limited to 2.0 mm, except for an area next to the edge connector in which the module components are limited to 1.2 mm height. This allows for an extra 0.8 mm for decoupling capacitors and series resistors to be placed on the carrier board.

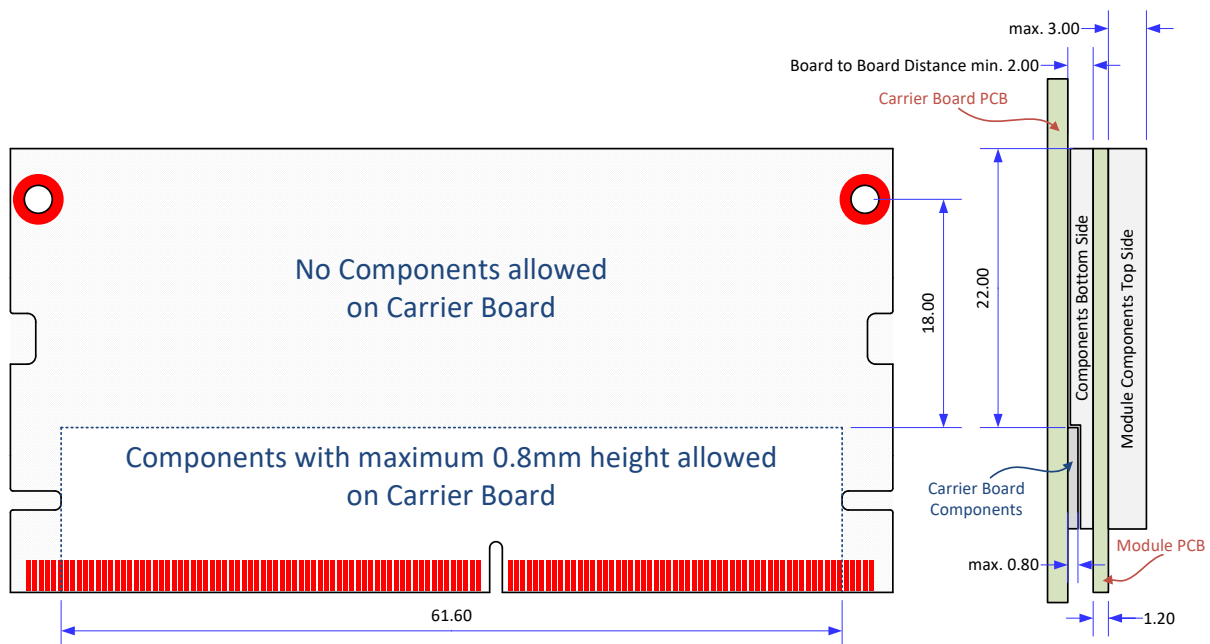


Figure 6: Maximum Component Height with a 5.2 mm SODIMM Connector

Even though a SODIMM with 5.2 mm height provides a nominal board-to-board distance of 2.62 mm, it is not recommended to place any components underneath the module (except for those next to the edge connector). The clip mechanism of the SODIMM connector is not rigid. This means that the module can be pushed a bit further down towards the carrier board for inserting the module. With the additional tolerances of the connector and the module PCB thickness, there is no space left for components on the carrier board.

Even if a module does not use up its total component height allowance, it is not advisable to squeeze in additional components between the module and the carrier board. Reserving the complete component height to the module guarantees mechanical compatibility with existing and future modules and module versions within the Verdin module family. If components need to be placed underneath the module, a connector with a larger stacking height is recommended.

4.4 Module Size

Figure 7 shows a mechanical drawing of the outline of the Verdin module together with key dimensions.

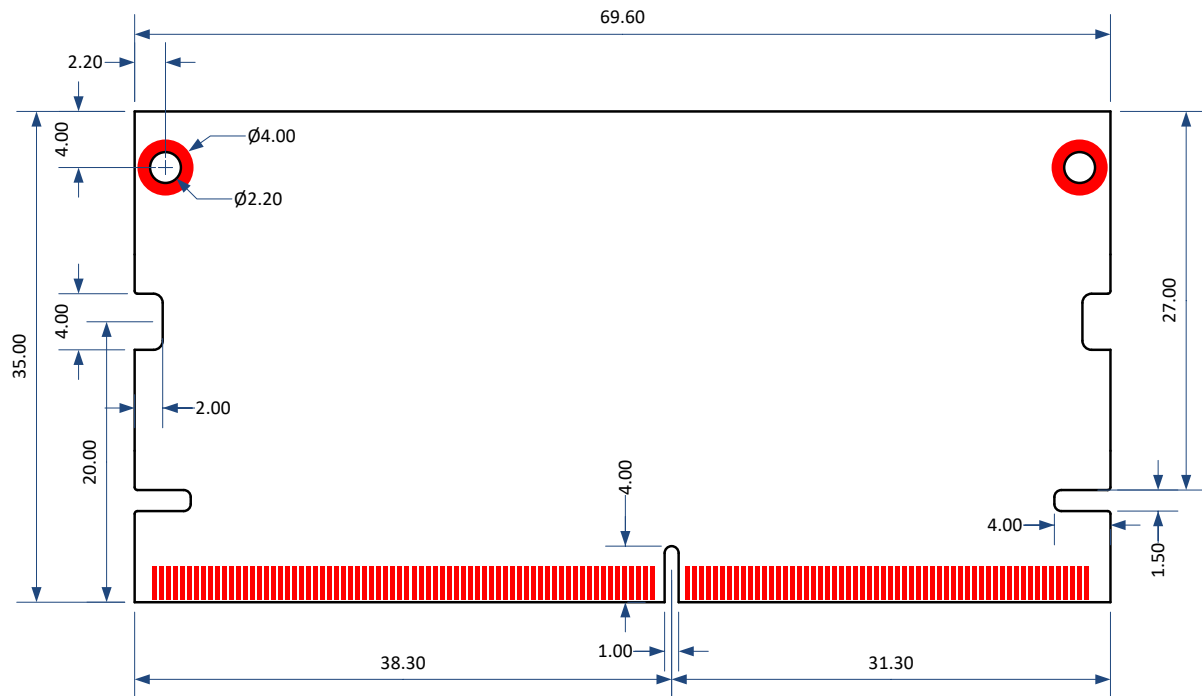


Figure 7: Verdin Module Mechanical Dimensions Top View (mm)

The dimensions of the Verdin module are different from a regular SODIMM DDR4 memory module. The notches on the sides of the module are reserved for mounting the heatsink solution to the module.

4.5 Pin Numbering

The Verdin module follows the same pin numbering scheme as the SO-DIMM DDR4 standard. Pins on the top side of the module have an odd number, while the pins on the bottom side have an even number.

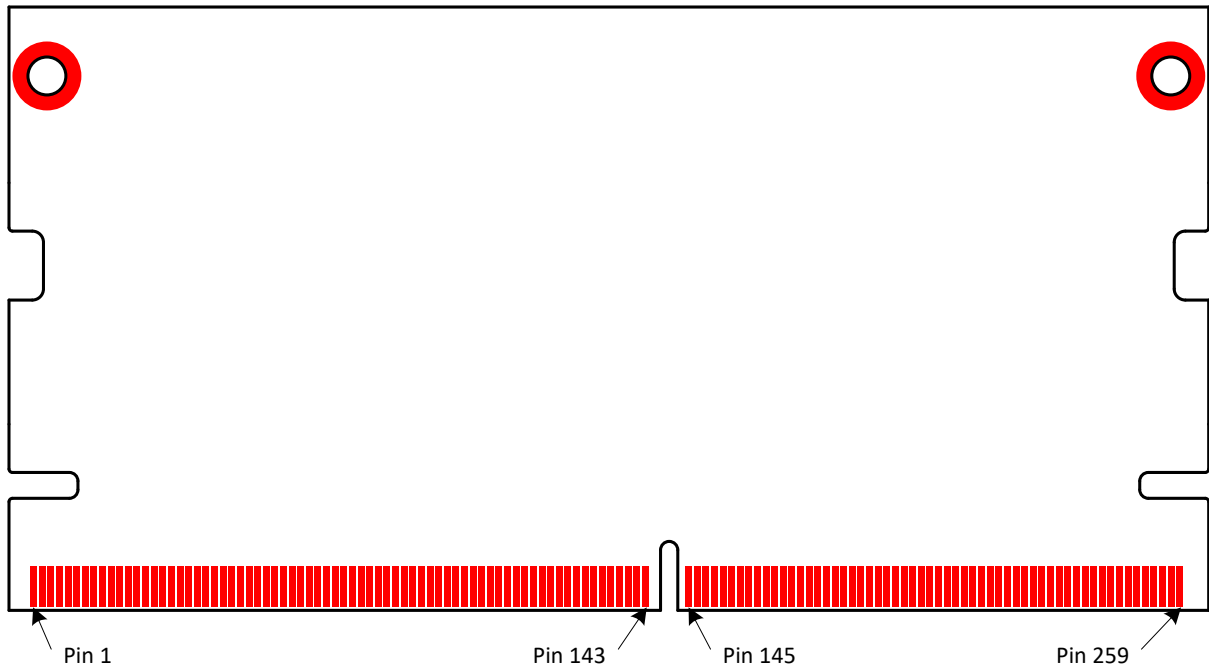


Figure 8: Pin numbering schema on the top side of the module (top view)

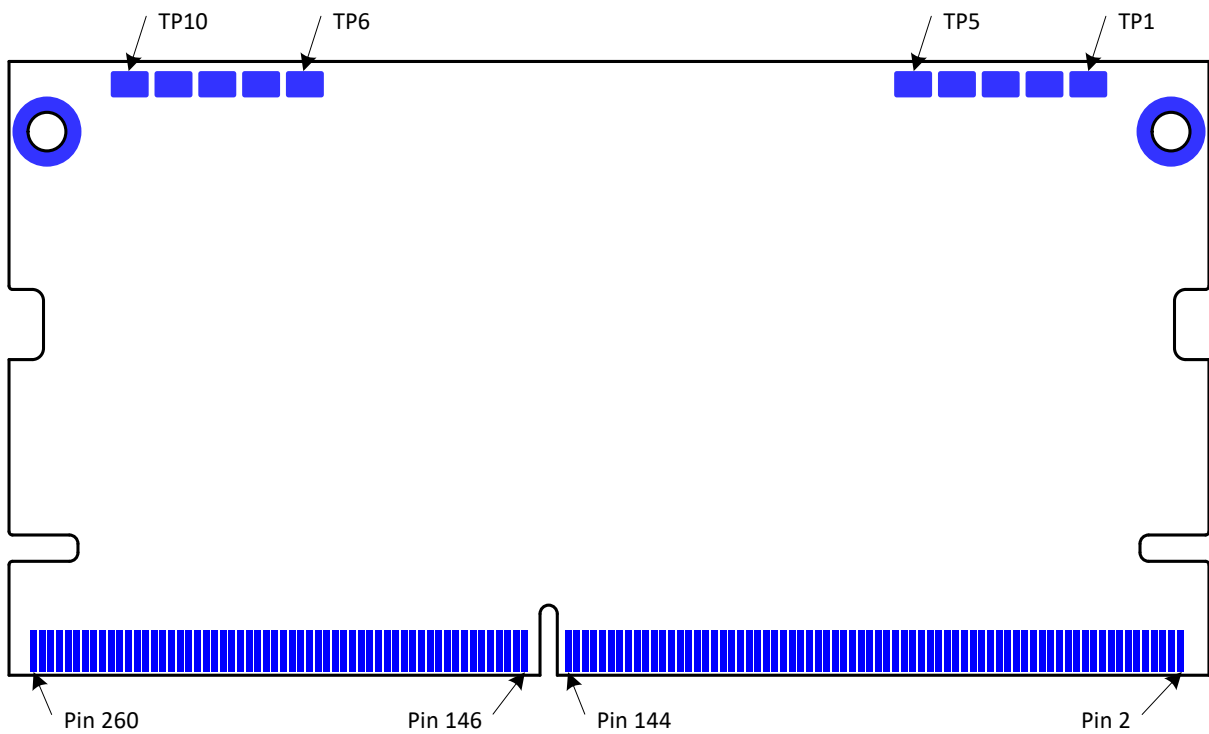


Figure 9: Pin numbering schema on the bottom side of the module (bottom view)

4.5.1 Generic Test Point Interfaces

Every Verdin module provides 10 test points on the module PCB's bottom side, as shown in Figure 10. The test points are split into groups of 5 pads. Each set is symmetrical about the centered Y-axis (the Y plane is orthogonal to the connector edge).

The test points are "Module-specific" pins. The signals connected to these test points are defined for each Verdin module for factory testing purposes. Customer carrier boards shall leave these pads unconnected.

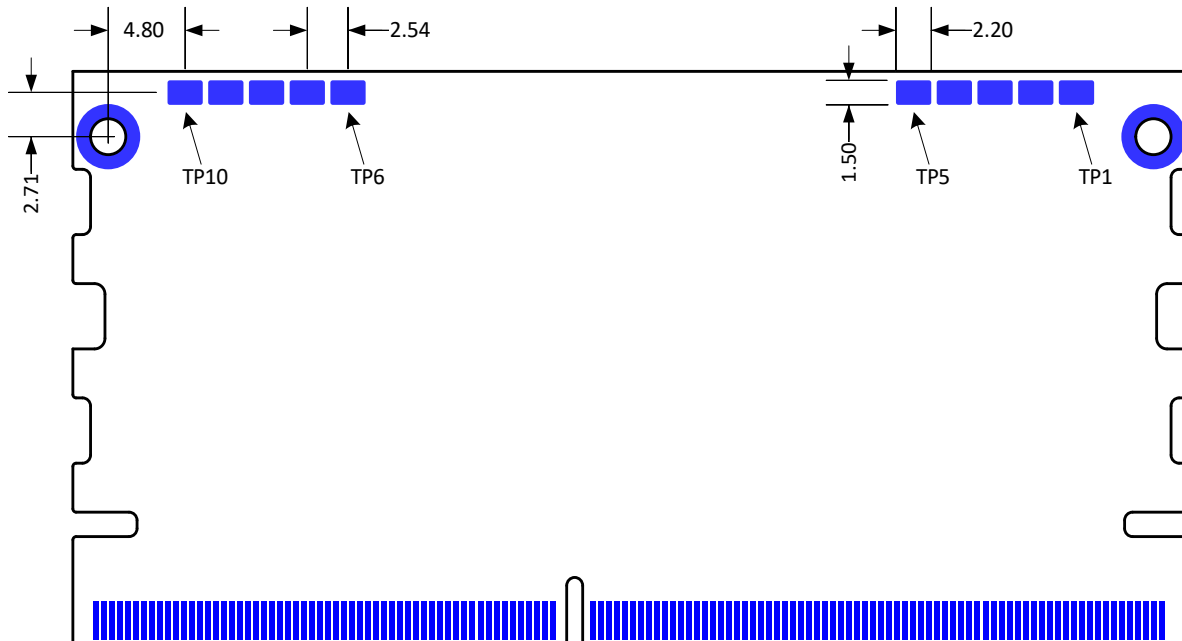


Figure 10: Bottom side of module illustrating test points and relative positions (bottom view)

4.6 Thermal Solutions

There will be two off-the-shelf thermal solutions available for the Verdin module. A clip-on solution allows convenient handling of the module since the heatsink is solely attached to the module. The Verdin module features an extra notch for mounting the clip-on heatsink.

The second thermal solution will use the two Verdin module mounting screw holes in conjunction with two additional holes on the carrier board for a reliable and vibration-proof heatsink. This is the preferred solution for final products in harsh environments.

More information on both thermal solutions will be available soon.

5. Electrical Specifications

5.1 Power Supplies

All Verdin modules are powered by a single voltage VCC and an optional low-current backup power supply for purposes such as Real Time Clock (RTC) support. The main power supply offers a wide input voltage range of 3.135V to 5.5V (absolute). This allows for supplying the module with 3.3V $\pm 5\%$, 5V $\pm 10\%$, or even from a single-cell lithium battery. For simple applications, the module can run directly from a USB power port.

The Verdin form factor targets a thermal design power of up to 5W (module). The maximum continuous current draw from VCC is 2.5 amps.

Most of the GPIO capable I/O pins run on 1.8V logic level. The Verdin module provides a reference 1.8V output for the I/O rails (PWR_1V8_MOCI). The module provides up to 250mA on this pin. Carrier boards may use this module output rail directly as the only 1.8V supply for their peripherals. This saves complexity and cost on the carrier board. The carrier board needs to ensure that the maximum amount of current drawn from the PWR_1V8_MOCI output pin does not exceed 250mA. Drawing a higher current can lead to instability and damages to the module power supply.

Further carrier board power supply requirements (power rating, isolation and decoupling, bulk capacitance, and characteristics such as ramp-up rate, etc.) are detailed in a separate carrier board design guide application note.

5.2 Power Supply and Power Management Signals

VCC is the only power supply required to be present for the module to become operational. Once VCC is present and is within specification, the module powers up and starts normal operation automatically.

VCC_BACKUP is not required for the module to start normal operation. However, it is mandatory if the application requires features that rely on this supply being always on, such as the Real-Time Clock (RTC).

Besides power supply pins, the Verdin module form factor supports several power-management signals. The signals are not mandatory to be used with carrier boards. However, they allow different power management schemes to be implemented on carrier boards: from a very simple approach to an advanced one with extra power-saving features and even systems operating from single-cell lithium batteries.

For power management purposes, all Verdin modules feature the following system control signals:

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
258	CTRL_RESET_MOCI#	O	OD	3.3V Tolerant	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# does not get asserted. The output is an open-drain type without a pull-up resistor on the module. The signal is 3.3V tolerant. The carrier board can pull the signal up to 1.8V or 3.3V. This signal can be left floating on carrier boards.
254	CTRL_PWR_EN_MOCI	O	CMOS	1.8V	Enable signal for the power rails of the carrier board peripherals. This output remains high during sleep modes.
256	CTRL_SLEEP_MOCI#	O	CMOS	1.8V	Enable signal for the power rails on the carrier board peripherals needs to be turned off during sleep mode. It is only high during the running mode. The signal is standard GPIO with an on-module 10k pull-down resistors. The signal is defined during the power-up sequence. The signal can be left floating on the carrier board.
260	CTRL_RESET_MICO#	I	OD	1.8V	Open-drain input, which resets the module if shorted to ground on carrier board. There is a 100k on-module pull-up to the 1.8V RTC rail present. This means that this signal can be left floating on carrier boards.
248	CTRL_PWR_BTN_MICO#	I	OD	1.8V	Long pulling down (>5s*) is shutting down the module. Short pulling down is turning on module from off-state. A more detailed function description can be found in section 5.3 Open-drain input with 100k pull-up resistor to the 1.8V RTC rail is on the module. This signal can be left floating on carrier boards. (* the actual minimum duration depends on the Verdin module)
246	CTRL_RECOVERY_MICO#	I	OD	1.8V	Shorting to the ground during power-up is setting the module into recovery mode. There is a 10k pull-up on the module. This signal can be left floating on carrier boards.
252	CTRL_WAKE1_MICO#	I	CMOS	1.8V	Wake capable pin, which allows resuming from sleep mode. There are no pull resistors on the carrier board. This signal can be left floating on carrier boards if the wake feature is disabled in the software.
250	CTRL_FORCE_OFF_MOCI#	O	OD	5V Tolerant	Output for forcing the turning-off of the main power rail. This signal needs to be blanked (ignored) for the first 400ms during the power-up sequence. The output is an open-drain type without a pull-up resistor on the module. The signal is 5V tolerant. The carrier board can pull the signal up to 1.8V, 3.3V, or 5V. This signal can be left floating on carrier boards.

Figure 11: System Control Signals

To make the direction of the power management signals clear, the ending MICO or MOCI are appended to the signal names. MICO is the abbreviation for “Module Input, Carrier board Output,” while MOCI stands for “Module Output, Carrier board Input”.

In general, every Verdin module shall start booting if the main power rail is applied. Most of the system control signals are optional to be used on the carrier board. The power management features of Verdin modules provide great flexibility and may support different carrier board power scenarios.

Detailed information on the possible carrier board power management schemes, power management states, and power up and down sequences can be found in the carrier board design guide.

5.3 Module Power Management States

Verdin modules support different power states. The following table describes what the various states mean. Depending on the carrier board power supply use case, some of the states may not be available.

Name	Description
No VCC	The main VCC power rail is not applied to the module. The VCC_BACKUP is maybe available for keeping the RTC running. The CTRL_PWR_EN_MOCI and CTRL_SLEEP_MOCI# are both low to make sure no peripheral rails on the carrier board are enabled. CTRL_RESET_MOCI# and CTRL_FORCE_OFF_MOCI# are undefined. They can be high-z or driven low in this state.
Running	The module is running. Some unused module or carrier board peripherals maybe are switched off.
Reset	The module and the peripheral devices are in the reset state. The preferred reset mode is a "cold reset". This means the PMIC shuts down all the rails on the module and drives the CTRL_PWR_EN_MOCI and CTRL_SLEEP_MOCI# low to turn off also the carrier board rails. Some modules may implement a "warm reset" instead. In this reset state, the rails on the module, including CTRL_PWR_EN_MOCI, are kept up and running while only the reset signals are asserted. The Verdin module datasheet contains information on which type of reset is implemented by the module If the CTRL_RESET_MICO# is low, the module is kept in the reset mode. This allows the carrier board to prolong the reset cycle
Sleep	The CPU is in a low power suspend state. The peripherals on the module are either turned off or are put in a sleep state. The CTRL_SLEEP_MOCI# is driven low, allowing to turn off the power rails of peripherals that do not need to be powered in the sleep mode. The module can be woken up by an RTC event, a wake capable on-module peripherals, the CTRL_PWR_BTN_MICO# (power button), the CTRL_WAKE1_MICO#, or a wake-enabled GPIO (depending on the module).
Module OFF	The PMIC on the module has shut down all the power rails, but the VCC is still applied to the module. CTRL_PWR_EN_MOCI, CTRL_SLEEP_MOCI#, and CTRL_RESET_MOCI# are all set low to turn off peripheral power rails on the carrier board. The CTRL_FORCE_OFF_MOCI# output is also low. It depends on the carrier board power supply scheme whether this causes the module to stay in the "Module OFF" state or the VCC is removed, which means the module goes into "No VCC" mode. The power consumption of the module in this state is very low. The VCC rail is only used for keeping the power management circuits and the RTC on. The actual consumption can be found in the datasheet of the Verdin module.

Table 2: Available Apalis power states

The module automatically transitions to the running mode when the VCC main power rail is applied to the module. In other words, all Verdin modules are ramping up the power rails and boot the system whenever the VCC is applied.

The CTRL_PWR_BTN_MICO# allows implementing a power button behavior like the ones used on regular personal computers and smartphones. Short pressing the power button is powering up the system from the "Module OFF" state or wakes the system from the sleep state. If the module is running, short pressing the power button generates a software interrupt. Depending on the operating system settings, this starts a software shut down or opens a menu that lets the customer decide what to do. Pressing the power button longer than 5 seconds shuts down the system immediately (without software interaction).

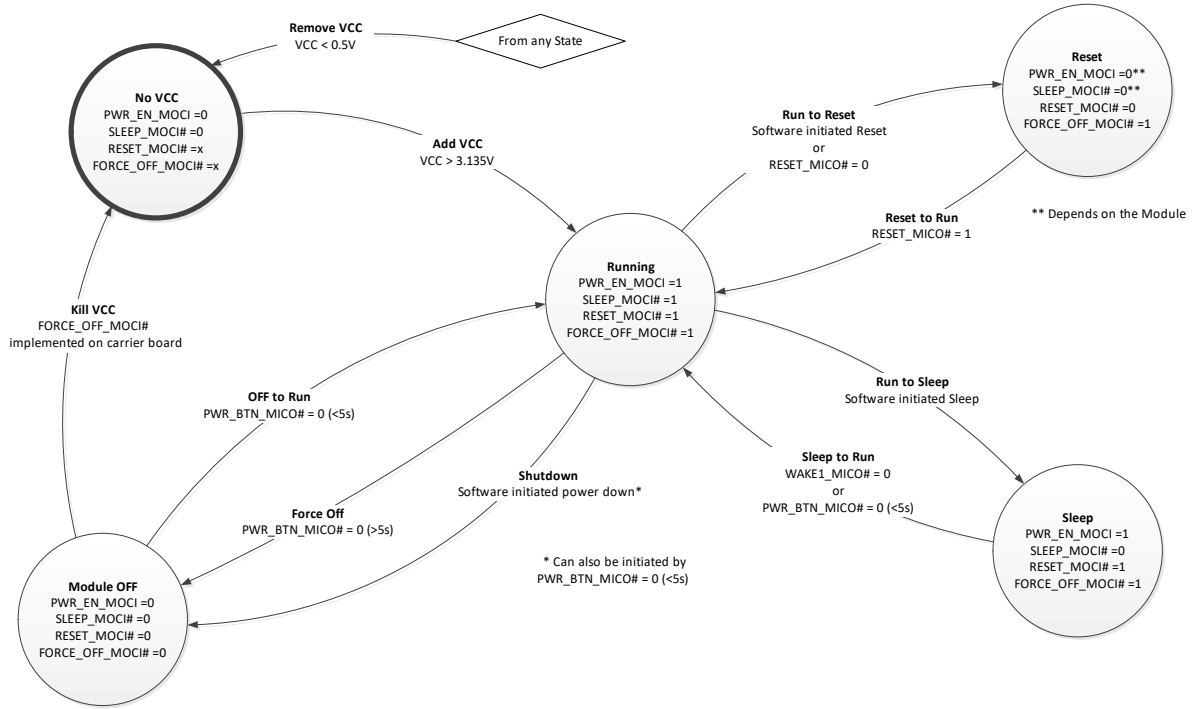


Figure 12: Module Power States and Transitions

6. Appendix A – Module Top Side Signal Definition

Pin Number	Signal Group	Signal Name	Signal Type	Voltage Domain	Feature Group
1	JTAG	JTAG_1_TDI	Input	JTAG_1_VREF	“Reserved”
3		JTAG_1_TRST#	Input	JTAG_1_VREF	“Reserved”
5		JTAG_1_TDO	Output	JTAG_1_VREF	“Reserved”
7		JTAG_1_VREF	Reference Output	JTAG_1_VREF	“Reserved”
9		JTAG_1_TCK	Input	JTAG_1_VREF	“Reserved”
11		GND			
13		JTAG_1_TMS	Input	JTAG_1_VREF	“Reserved”
15	PWM	PWM_1	Output	1.8V	“Always Compatible”
17	DSI	GPIO_9_DSI	Bidirectional	1.8V	“Reserved”
19		PWM_3_DSI	Output	1.8V	“Reserved”
21		GPIO_10_DSI	Bidirectional	1.8V	“Reserved”
23		DSI_1_D3_N	Differential Pair Output		“Reserved”
25		DSI_1_D3_P	Differential Pair Output		“Reserved”
27		GND			
29		DSI_1_D2_N	Differential Pair Output		“Reserved”
31		DSI_1_D2_P	Differential Pair Output		“Reserved”
33		GND			
35		DSI_1_CLK_N	Differential Pair Output		“Reserved”
37		DSI_1_CLK_P	Differential Pair Output		“Reserved”
39		GND			
41		DSI_1_D1_N	Differential Pair Output		“Reserved”
43		DSI_1_D1_P	Differential Pair Output		“Reserved”
45		GND			
47		DSI_1_D0_N	Differential Pair Bidirectional		“Reserved”
49		DSI_1_D0_P	Differential Pair Bidirectional		“Reserved”
51		GND			
53		I2C_2_DSI_SDA	Open-Drain	1.8V	“Reserved”
55		I2C_2_DSI_SCL	Open-Drain	1.8V	“Reserved”
57	HDMI	I2C_3_HDMI_SDA	Open-Drain	1.8V	“Reserved”
59		I2C_3_HDMI_SCL	Open-Drain	1.8V	“Reserved”
61		HDMI_1_HPDP	Input	1.8V	“Reserved”
63		HDMI_1_CEC	Bidirectional	1.8V	“Reserved”
65		GND			
67		HDMI_1_TXC_N	Differential Pair Output		“Reserved”

69		HDMI_1_TXC_P	Differential Pair Output		"Reserved"
71		GND			
73		HDMI_1_TXD0_N	Differential Pair Output		"Reserved"
75		HDMI_1_TXD0_P	Differential Pair Output		"Reserved"
77		GND			
79		HDMI_1_TXD1_N	Differential Pair Output		"Reserved"
81		HDMI_1_TXD1_P	Differential Pair Output		"Reserved"
83		GND			
85		HDMI_1_TXD2_N	Differential Pair Output		"Reserved"
87		HDMI_1_TXD2_P	Differential Pair Output		"Reserved"
89		GND			
91		CSI_1_MCLK	Output	1.8V	"Reserved"
93		I2C_4_CSI_SDA	Open-Drain	1.8V	"Reserved"
95		I2C_4_CSI_SCL	Open-Drain	1.8V	"Reserved"
97		GND			
99		CSI_1_D3_P	Differential Pair Input		"Reserved"
101		CSI_1_D3_N	Differential Pair Input		"Reserved"
103		GND			
105		CSI_1_D2_P	Differential Pair Input		"Reserved"
107		CSI_1_D2_N	Differential Pair Input		"Reserved"
109	CSI	GND			
111		CSI_1_CLK_P	Differential Pair Input		"Reserved"
113		CSI_1_CLK_N	Differential Pair Input		"Reserved"
115		GND			
117		CSI_1_D1_P	Differential Pair Input		"Reserved"
119		CSI_1_D1_N	Differential Pair Input		"Reserved"
121		GND			
123		CSI_1_D0_P	Differential Pair Bidirectional		"Reserved"
125		CSI_1_D0_N	Differential Pair Bidirectional		"Reserved"
127		GND			
129		UART_1_RXD	Input	1.8V	"Always Compatible"
131	UART	UART_1_TXD	Output	1.8V	"Always Compatible"
133		UART_1_RTS	Output	1.8V	"Reserved"
135		UART_1_CTS	Input	1.8V	"Reserved"

137		UART_2_RXD	Input	1.8V	"Always Compatible"
139		UART_2_TXD	Output	1.8V	"Always Compatible"
141		UART_2_RTS	Output	1.8V	"Reserved"
143		UART_2_CTS	Input	1.8V	"Reserved"
Notch					
145	DEBUG UART	GND			
147		UART_3_RXD	Input	1.8V	"Always Compatible"
149		UART_3_TXD	Output	1.8V	"Always Compatible"
151		UART_4_RXD	Input	1.8V	"Reserved"
153		UART_4_TXD	Output	1.8V	"Reserved"
155	USB	USB_1_EN	Output	1.8V	"Always Compatible"
157		USB_1_OC#	Input	1.8V	"Always Compatible"
159		USB_1_VBUS	Input	5V Tolerant	"Always Compatible"
161		USB_1_ID	Input	1.8V	"Always Compatible"
163		USB_1_D_N	Differential Pair Bidirectional		"Always Compatible"
165		USB_1_D_P	Differential Pair Bidirectional		"Always Compatible"
167		GND			
169		USB_2_SSTX_N	Differential Pair Output		"Reserved"
171		USB_2_SSTX_P	Differential Pair Output		"Reserved"
173		GND			
175		USB_2_SSRX_N	Differential Pair Input		"Reserved"
177		USB_2_SSRX_P	Differential Pair Input		"Reserved"
179		GND			
181		USB_2_D_N	Differential Pair Bidirectional		"Always Compatible"
183		USB_2_D_P	Differential Pair Bidirectional		"Always Compatible"
185		USB_2_EN	Output	1.8V	"Always Compatible"
187		USB_2_OC#	Input	1.8V	"Always Compatible"
189		RGMII	ETH_2_RGMII_INT#	Input	1.8V
191	ETH_2_RGMII_MDIO		Bidirectional	1.8V	"Reserved"
193	ETH_2_RGMII_MDC		Output	1.8V	"Reserved"
195	GND				
197	ETH_2_RGMII_RXC		Input	1.8V	"Reserved"
199	ETH_2_RGMII_RX_CTL		Input	1.8V	"Reserved"
201	ETH_2_RGMII_RXD_0		Input	1.8V	"Reserved"
203	ETH_2_RGMII_RXD_1		Input	1.8V	"Reserved"
205	ETH_2_RGMII_RXD_2		Input	1.8V	"Reserved"
207	ETH_2_RGMII_RXD_3		Input	1.8V	"Reserved"
209	GND				
211	ETH_2_RGMII_TX_CTL		Output	1.8V	"Reserved"

213		ETH_2_RGMII_TXC	Output	1.8V	"Reserved"	
215		ETH_2_RGMII_TXD_3	Output	1.8V	"Reserved"	
217		ETH_2_RGMII_TXD_2	Output	1.8V	"Reserved"	
219		ETH_2_RGMII_TXD_1	Output	1.8V	"Reserved"	
221		ETH_2_RGMII_TXD_0	Output	1.8V	"Reserved"	
223		GND				
225		ETH_1_MDIO_P	Differential Pair Bidirectional		"Always Compatible"	
227		ETH_1_MDIO_N	Differential Pair Bidirectional		"Always Compatible"	
229		GND				
231		ETH_1_MD11_N	Differential Pair Bidirectional		"Always Compatible"	
233		ETH_1_MD11_P	Differential Pair Bidirectional		"Always Compatible"	
235	Gigabit Ethernet	ETH_1_LINK	Open-Drain Output	3.3V Tolerant	"Always Compatible"	
237		ETH_1_ACT	Open-Drain Output	3.3V Tolerant	"Always Compatible"	
239		ETH_1_MD12_P	Differential Pair Bidirectional		"Always Compatible"	
241		ETH_1_MD12_N	Differential Pair Bidirectional		"Always Compatible"	
243		GND				
245		ETH_1_MD13_N	Differential Pair Bidirectional		"Always Compatible"	
247		ETH_1_MD13_P	Differential Pair Bidirectional		"Always Compatible"	
249		Power	VCC_BACKUP	Power Input	3.6V Max	"Always Compatible"
251			VCC	Power Input	3.135 – 5.5V	"Always Compatible"
253			VCC	Power Input	3.135 – 5.5V	"Always Compatible"
255	VCC		Power Input	3.135 – 5.5V	"Always Compatible"	
257	VCC		Power Input	3.135 – 5.5V	"Always Compatible"	
259	VCC		Power Input	3.135 – 5.5V	"Always Compatible"	

7. Appendix B - Module Bottom Side Signal Definition

Pin Number	Signal Group	Signal Name	Signal Type	Voltage Domain	Feature Group	
2	ADC	ADC_1	Analog Input	1.8V	"Reserved"	
4		ADC_2	Analog Input	1.8V	"Reserved"	
6		ADC_3	Analog Input	1.8V	"Reserved"	
8		ADC_4	Analog Input	1.8V	"Reserved"	
10		GND				
12	I2C	I2C_1_SDA	Open-Drain	1.8V	"Always Compatible"	
14		I2C_1_SCL	Open-Drain	1.8V	"Always Compatible"	
16	PWM	PWM_2	Output	1.8V	"Reserved"	
18	CAN	GND				
20		CAN_1_TX	Output	1.8V	"Reserved"	
22		CAN_1_RX	Input	1.8V	"Reserved"	
24		CAN_2_TX	Output	1.8V	"Reserved"	
26		CAN_2_RX	Input	1.8V	"Reserved"	
28	I2S	GND				
30		I2S_1_BCLK	Bidirectional	1.8V	"Reserved"	
32		I2S_1_SYNC	Bidirectional	1.8V	"Reserved"	
34		I2S_1_D_OUT	Output	1.8V	"Reserved"	
36		I2S_1_D_IN	Input	1.8V	"Reserved"	
38		I2S_1_MCLK	Output	1.8V	"Reserved"	
40		GND				
42		I2S_2_BCLK	Bidirectional	1.8V	"Reserved"	
44		I2S_2_SYNC	Bidirectional	1.8V	"Reserved"	
46		I2S_2_D_OUT	Output	1.8V	"Reserved"	
48	I2S_2_D_IN	Input	1.8V	"Reserved"		
50	QSPI	GND				
52		QSPI_1_CLK	Output	1.8V	"Reserved"	
54		QSPI_1_CS#	Output	1.8V	"Reserved"	
56		QSPI_1_IO0	Bidirectional	1.8V	"Reserved"	
58		QSPI_1_IO1	Bidirectional	1.8V	"Reserved"	

60		QSPI_1_IO2	Bidirectional	1.8V	“Reserved”
62		QSPI_1_IO3	Bidirectional	1.8V	“Reserved”
64		QSPI_1_CS2#	Output	1.8V	“Reserved”
66		QSPI_1_DQS	Output	1.8V	“Reserved”
68	SDIO	GND			
70		SD_1_D2	Bidirectional	3.3V/1.8V	“Always Compatible”
72		SD_1_D3	Bidirectional	3.3V/1.8V	“Always Compatible”
74		SD_1_CMD	Bidirectional	3.3V/1.8V	“Always Compatible”
76		SD_1_PWR_EN*	Output	3.3V/1.8V	“Always Compatible”
78		SD_1_CLK	Output	3.3V/1.8V	“Always Compatible”
80		SD_1_D0	Bidirectional	3.3V/1.8V	“Always Compatible”
82		SD_1_D1	Bidirectional	3.3V/1.8V	“Always Compatible”
84		SD_1_CD#*	Input	3.3V/1.8V	“Always Compatible”
86		“Module-specific”	GND		
88	MSP_1		Differential Pair/ Single Ended		“Module-specific”
90	MSP_2		Differential Pair/ Single Ended		“Module-specific”
92	MSP_3		GND/ Low Speed/ Single Ended		“Module-specific”
94	MSP_4		Differential Pair/ Single Ended		“Module-specific”
96	MSP_5		Differential Pair/ Single Ended		“Module-specific”
98	GND				
100	MSP_6		Differential Pair/ Single Ended		“Module-specific”
102	MSP_7		Differential Pair/ Single Ended		“Module-specific”
104	MSP_8		GND/ Low Speed/ Single Ended		“Module-specific”
106	MSP_9		Differential Pair/ Single Ended		“Module-specific”
108	MSP_10		Differential Pair/ Single Ended		“Module-specific”
110	GND				
112	MSP_11		Differential Pair/ Single Ended		“Module-specific”
114	MSP_12	Differential Pair/ Single Ended		“Module-specific”	
116	MSP_13	GND/ Low Speed/ Single Ended		“Module-specific”	
118	MSP_14	Differential Pair/ Single Ended		“Module-specific”	

120		MSP_15	Differential Pair/ Single Ended		"Module-specific"
122		GND			
124		MSP_16	Differential Pair/ Single Ended		"Module-specific"
126		MSP_17	Differential Pair/ Single Ended		"Module-specific"
128		MSP_18	GND/ Low Speed/ Single Ended		"Module-specific"
130		MSP_19	Differential Pair/ Single Ended		"Module-specific"
132		MSP_20	Differential Pair/ Single Ended		"Module-specific"
134		GND			
136		MSP_21	Differential Pair/ Single Ended		"Module-specific"
138		MSP_22	Differential Pair/ Single Ended		"Module-specific"
140		MSP_23	GND/ Low Speed/ Single Ended		"Module-specific"
142		MSP_24	Differential Pair/ Single Ended		"Module-specific"
144		MSP_25	Differential Pair/ Single Ended		"Module-specific"
Notch					
146		GND			
148		MSP_26	Differential Pair/ Single Ended		"Module-specific"
150		MSP_27	Differential Pair/ Single Ended		"Module-specific"
152		MSP_28	GND/ Low Speed/ Single Ended		"Module-specific"
154		MSP_29	Differential Pair/ Single Ended		"Module-specific"
156		MSP_30	Differential Pair/ Single Ended		"Module-specific"
158		GND			
160	"Module-specific"	MSP_31	Differential Pair/ Single Ended		"Module-specific"
162		MSP_32	Differential Pair/ Single Ended		"Module-specific"
164		MSP_33	GND/ Low Speed/ Single Ended		"Module-specific"
166		MSP_34	Differential Pair/ Single Ended		"Module-specific"
168		MSP_35	Differential Pair/ Single Ended		"Module-specific"
170		GND			
172		MSP_36	Differential Pair/ Single Ended		"Module-specific"
174		MSP_37	Differential Pair/ Single Ended		"Module-specific"

176		MSP_38	GND/ Low Speed/ Single Ended		“Module-specific”
178		MSP_39	Differential Pair/ Single Ended		“Module-specific”
180		MSP_40	Differential Pair/ Single Ended		“Module-specific”
182		GND			
184		MSP_41	Differential Pair/ Single Ended		“Module-specific”
186		MSP_42	Differential Pair/ Single Ended		“Module-specific”
188		MSP_43	GND/ Low Speed/ Single Ended		“Module-specific”
190		MSP_44	Differential Pair/ Single Ended		“Module-specific”
192		MSP_45	Differential Pair/ Single Ended		“Module-specific”
194		GND			
196	SPI	SPI_1_CLK	Output	1.8V	“Always Compatible”
198		SPI_1_MISO	Input	1.8V	“Always Compatible”
200		SPI_1_MOSI	Output	1.8V	“Always Compatible”
202		SPI_1_CS	Output	1.8V	“Always Compatible”
204		GND			
206	GPIO	GPIO_1	Bidirectional	1.8V	“Always Compatible”
208		GPIO_2	Bidirectional	1.8V	“Always Compatible”
210		GPIO_3	Bidirectional	1.8V	“Always Compatible”
212		GPIO_4	Bidirectional	1.8V	“Always Compatible”
214		PWR_1V8_MOCI	Output 250mA max.	1.8V	“Always Compatible”
216		GPIO_5_CSI	Bidirectional	1.8V	“Always Compatible”
218		GPIO_6_CSI	Bidirectional	1.8V	“Always Compatible”
220		GPIO_7_CSI	Bidirectional	1.8V	“Always Compatible”
222		GPIO_8_CSI	Bidirectional	1.8V	“Always Compatible”
224			GND		
226	PCIe	PCIE_1_CLK_N	Differential Pair Output		“Reserved”
228		PCIE_1_CLK_P	Differential Pair Output		“Reserved”
230		GND			
232		PCIE_1_L0_RX_N	Differential Pair Input		“Reserved”
234		PCIE_1_L0_RX_P	Differential Pair Input		“Reserved”

236		GND			
238		PCIE_1_L0_TX_N	Differential Pair Output		“Reserved”
240		PCIE_1_L0_TX_P	Differential Pair Output		“Reserved”
242		GND			
244		PCIE_1_RESET#	Output	1.8V	“Reserved”
246	System Control	CTRL_RECOVERY_MICO#	Open Drain Input	1.8V	“Always Compatible”
248		CTRL_PWR_BTN_MICO#	Open Drain Input	1.8V	“Always Compatible”
250		CTRL_FORCE_OFF_MOCI#	Open-Drain Output, 5V Tolerant		“Always Compatible”
252		CTRL_WAKE1_MICO#	Input	1.8V	“Always Compatible”
254		CTRL_PWR_EN_MOCI	Output	1.8V	“Always Compatible”
256		CTRL_SLEEP_MOCI#	Output	1.8V	“Always Compatible”
258		CTRL_RESET_MOCI#	Open-Drain Output, 3.3V Tolerant		“Always Compatible”
260		CTRL_RESET_MICO#	Open Drain Input	1.8V	“Always Compatible”

* The voltage domain may differ from the related interface signal domain. This depends on the architecture of the various SoCs. Please refer to Verdin module datasheets for details.

8. Appendix C - Physical Pin Definition and Location

Signal Group	Module Top Side	MXM3 Pins		Module Bottom Side	Signal Group
JTAG	JTAG_1_TDI	1	2	ADC_1	ADC
	JTAG_1_TRST#	3	4	ADC_2	
	JTAG_1_TDO	5	6	ADC_3	
	JTAG_1_VREF	7	8	ADC_4	
	JTAG_1_TCK	9	10	GND	
	GND	11	12	I2C_1_SDA	I2C
	JTAG_1_TMS	13	14	I2C_1_SCL	
PWM	PWM_1	15	16	PWM_2	PWM
DSI	GPIO_9_DSI	17	18	GND	CAN
	PWM_3_DSI	19	20	CAN_1_TX	
	GPIO_10_DSI	21	22	CAN_1_RX	
	DSI_1_D3_N	23	24	CAN_2_TX	
	DSI_1_D3_P	25	26	CAN_2_RX	
	GND	27	28	GND	I2S
	DSI_1_D2_N	29	30	I2S_1_BCLK	
	DSI_1_D2_P	31	32	I2S_1_SYNC	
	GND	33	34	I2S_1_D_OUT	
	DSI_1_CLK_N	35	36	I2S_1_D_IN	
	DSI_1_CLK_P	37	38	I2S_1_MCLK	
	GND	39	40	GND	
	DSI_1_D1_N	41	42	I2S_2_BCLK	
	DSI_1_D1_P	43	44	I2S_2_SYNC	
	GND	45	46	I2S_2_D_OUT	
	DSI_1_D0_N	47	48	I2S_2_D_IN	QSPI
	DSI_1_D0_P	49	50	GND	
	GND	51	52	QSPI_1_CLK	
	I2C_2_DSI_SDA	53	54	QSPI_1_CS#	
	I2C_2_DSI_SCL	55	56	QSPI_1_IO0	
I2C_3_HDMI_SDA	57	58	QSPI_1_IO1		
I2C_3_HDMI_SCL	59	60	QSPI_1_IO2	SDIO	
HDMI_1_HPD	61	62	QSPI_1_IO3		
HDMI_1_CEC	63	64	QSPI_1_CS2#		
GND	65	66	QSPI_1_DQS		
HDMI_1_TXC_N	67	68	GND		
HDMI_1_TXC_P	69	70	SD_1_D2		
GND	71	72	SD_1_D3		
HDMI_1_TXD0_N	73	74	SD_1_CMD		
HDMI_1_TXD0_P	75	76	SD_1_PWR_EN		
GND	77	78	SD_1_CLK		
HDMI_1_TXD1_N	79	80	SD_1_D0	SDIO	
HDMI_1_TXD1_P	81	82	SD_1_D1		

	GND	83	84	SD_1_CD#	
	HDMI_1_TXD2_N	85	86	GND	"Module-specific"
	HDMI_1_TXD2_P	87	88	MSP_1	
CSI	GND	89	90	MSP_2	
	CSI_1_MCLK	91	92	MSP_3	
	I2C_4_CSI_SDA	93	94	MSP_4	
	I2C_4_CSI_SCL	95	96	MSP_5	
	GND	97	98	GND	
	CSI_1_D3_P	99	100	MSP_6	
	CSI_1_D3_N	101	102	MSP_7	
	GND	103	104	MSP_8	
	CSI_1_D2_P	105	106	MSP_9	
	CSI_1_D2_N	107	108	MSP_10	
	GND	109	110	GND	
	CSI_1_CLK_P	111	112	MSP_11	
	CSI_1_CLK_N	113	114	MSP_12	
	GND	115	116	MSP_13	
	CSI_1_D1_P	117	118	MSP_14	
	CSI_1_D1_N	119	120	MSP_15	
	GND	121	122	GND	
	CSI_1_D0_P	123	124	MSP_16	
CSI_1_D0_N	125	126	MSP_17		
GND	127	128	MSP_18		
UART	UART_1_RXD	129	130	MSP_19	
	UART_1_TXD	131	132	MSP_20	
	UART_1_RTS	133	134	GND	
	UART_1_CTS	135	136	MSP_21	
	UART_2_RXD	137	138	MSP_22	
	UART_2_TXD	139	140	MSP_23	
	UART_2_RTS	141	142	MSP_24	
	UART_2_CTS	143	144	MSP_25	
Notch					
DEBUG UART	GND	145	146	GND	"Module-specific"
	UART_3_RXD	147	148	MSP_26	
	UART_3_TXD	149	150	MSP_27	
	UART_4_RXD	151	152	MSP_28	
	UART_4_TXD	153	154	MSP_29	
USB	USB_1_EN	155	156	MSP_30	
	USB_1_OC#	157	158	GND	
	USB_1_VBUS	159	160	MSP_31	
	USB_1_ID	161	162	MSP_32	
	USB_1_D_N	163	164	MSP_33	
	USB_1_D_P	165	166	MSP_34	
GND	167	168	MSP_35		

	USB_2_SSTX_N	169	170	GND	
	USB_2_SSTX_P	171	172	MSP_36	
	GND	173	174	MSP_37	
	USB_2_SSRX_N	175	176	MSP_38	
	USB_2_SSRX_P	177	178	MSP_39	
	GND	179	180	MSP_40	
	USB_2_D_N	181	182	GND	
	USB_2_D_P	183	184	MSP_41	
	USB_2_EN	185	186	MSP_42	
	USB_2_OC#	187	188	MSP_43	
RGMII	ETH_2_RGMII_INT#	189	190	MSP_44	SPI
	ETH_2_RGMII_MDIO	191	192	MSP_45	
	ETH_2_RGMII_MDC	193	194	GND	
	GND	195	196	SPI_1_CLK	
	ETH_2_RGMII_RXC	197	198	SPI_1_MISO	
	ETH_2_RGMII_RX_CTL	199	200	SPI_1_MOSI	
	ETH_2_RGMII_RXD_0	201	202	SPI_1_CS	
	ETH_2_RGMII_RXD_1	203	204	GND	GPIO
	ETH_2_RGMII_RXD_2	205	206	GPIO_1	
	ETH_2_RGMII_RXD_3	207	208	GPIO_2	
	GND	209	210	GPIO_3	
	ETH_2_RGMII_TX_CTL	211	212	GPIO_4	
	ETH_2_RGMII_TXC	213	214	PWR_1V8_MOCI	
	ETH_2_RGMII_TXD_3	215	216	GPIO_5_CSI	
	ETH_2_RGMII_TXD_2	217	218	GPIO_6_CSI	
	ETH_2_RGMII_TXD_1	219	220	GPIO_7_CSI	
	ETH_2_RGMII_TXD_0	221	222	GPIO_8_CSI	
Gigabit Ethernet	GND	223	224	GND	PCIe
	ETH_1_MDI0_P	225	226	PCIE_1_CLK_N	
	ETH_1_MDI0_N	227	228	PCIE_1_CLK_P	
	GND	229	230	GND	
	ETH_1_MDI1_N	231	232	PCIE_1_L0_RX_N	
	ETH_1_MDI1_P	233	234	PCIE_1_L0_RX_P	
	ETH_1_LINK	235	236	GND	
	ETH_1_ACT	237	238	PCIE_1_L0_TX_N	
	ETH_1_MDI2_P	239	240	PCIE_1_L0_TX_P	
	ETH_1_MDI2_N	241	242	GND	
	GND	243	244	PCIE_1_RESET#	
	ETH_1_MDI3_N	245	246	CTRL_RECOVERY_MICO#	
	ETH_1_MDI3_P	247	248	CTRL_PWR_BTN_MICO#	
Power	VCC_BACKUP	249	250	CTRL_FORCE_OFF_MOCI#	System Control
	VCC	251	252	CTRL_WAKE1_MICO#	
	VCC	253	254	CTRL_PWR_EN_MOCI	
	VCC	255	256	CTRL_SLEEP_MOCI#	

	VCC	257	258	CTRL_RESET_MOCI#	
	VCC	259	260	CTRL_RESET_MICO#	

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