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Apalis iMX8

Errata Document

Document Revision History

Date	Doc. Rev.	Notes
2020-07-09	Rev. 1.0	Initial Release
2020-07-17	Rev. 1.1	Errata #2: added to the document
2021-05-17	Rev. 1.2	Errata #3: added to the document
2021-09-13	Rev. 1.3	Errata #4: added to the document
2022-01-07	Rev. 1.4	Errata #5: added to the document

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Errata #1: HAR-4399 – Instability Issue on the LVDS Interface

Affected Version:	**Apalis iMX8QM 4GB WB IT V1.1B (and older)** **Apalis iMX8QM 4GB IT V1.1B (and older)** **Apalis iMX8QP 2GB WB V1.1B (and older)** **Apalis iMX8QP 2GB V1.1B (and older)**
Fixed in:	**Upcoming version**

Customer Impact

If the display interface (LVDS) is used, it may be unstable. This errata does not impact customers not utilizing this interface.

Description

On 07.07.2020, we were informed about an LVDS instability issue (flickering) on the new version of NXP® i.MX 8QM/i.MX 8QP, which is used in our prototype Apalis iMX8 products until version 1.1B.

NXP stated that "This failure causes information to be displayed blurry or with the wrong color on the screen. Potentially the screen may be observed to go black, which the driver can perceive as the screen not working." More details about the problem can be found on the following website: https://components.arrow.com/pcnattachment/pcn-attachment.jsp?Reg=EU&pcnId=344908

We are working with NXP to fix the products as soon as possible. It will be fixed in the next product release.

Errata #2: HAR-4106 – Power on after SW shut-down not possible

Affected Version:	**Apalis iMX8QM 4GB WB IT V1.1A (and older)** **Apalis iMX8QM 4GB IT V1.1A (and older)** **Apalis iMX8QP 2GB WB V1.1A (and older)** **Apalis iMX8QP 2GB V1.1A (and older)**
Fixed in:	**Apalis iMX8QM 4GB WB IT V1.1B** **Apalis iMX8QM 4GB IT V1.1B** **Apalis iMX8QP 2GB WB V1.1B** **Apalis iMX8QP 2GB V1.1B**

Customer Impact

If the RTC battery is present, it is not possible to turn on the module after shutting down the PMIC in the software.

Description

The module can be shut down by simply removing the main power rail or software command. In case of a software initiated shut-down, the power state machine of the SoC is set to power off. This state is backed up with the RTC battery. A module-internal power button signal is required to get it out of the power-off state. There is a circuit on the module that generates a pulse signal for the internal power button signal. This pulse is generated if the main power rail (VCC pins) is power-cycled or the RESET_MICO# is pressed.

Unfortunately, the power button pulse that is generated is too short. The SoC does not get out of the power-off state, and therefore the PMIC is not turned on. The module does not start if the RTC rail is retained during the main voltage power cycle (VCC). The module can also not be started by pressing the reset button (RESET_MICO#). The only way to start the module after the PMIC is put to power-off is to remove the RTC rail together with the main module rail.

Shutting down the module by removing the main module rail is not affected by this issue. This means, if the power is removed without doing a software shut down, the module is booting normally after turning on the main module rail.

Workaround

Option 1: Do not use the software initiated PMIC shut down. It is possible to shut down the software to ensure the system is in a safe state for removing the power. But the command to the PMIC for shutting down should not be sent. Leave the PMIC running and just remove the main input voltage from the module (remove VCC).

Option 2: Assemble C267 for making the power button signal pulse long enough. The capacitor C267 is not assembled on Apalis iMX8 modules with version 1.1A or older. By assembling C267 with a 10µF 6.3V capacitor with the 0603 size. The power button signal pulse gets its required duration. This means the module can be turned on either by power cycling VCC or by pressing the RESET_MICO# button

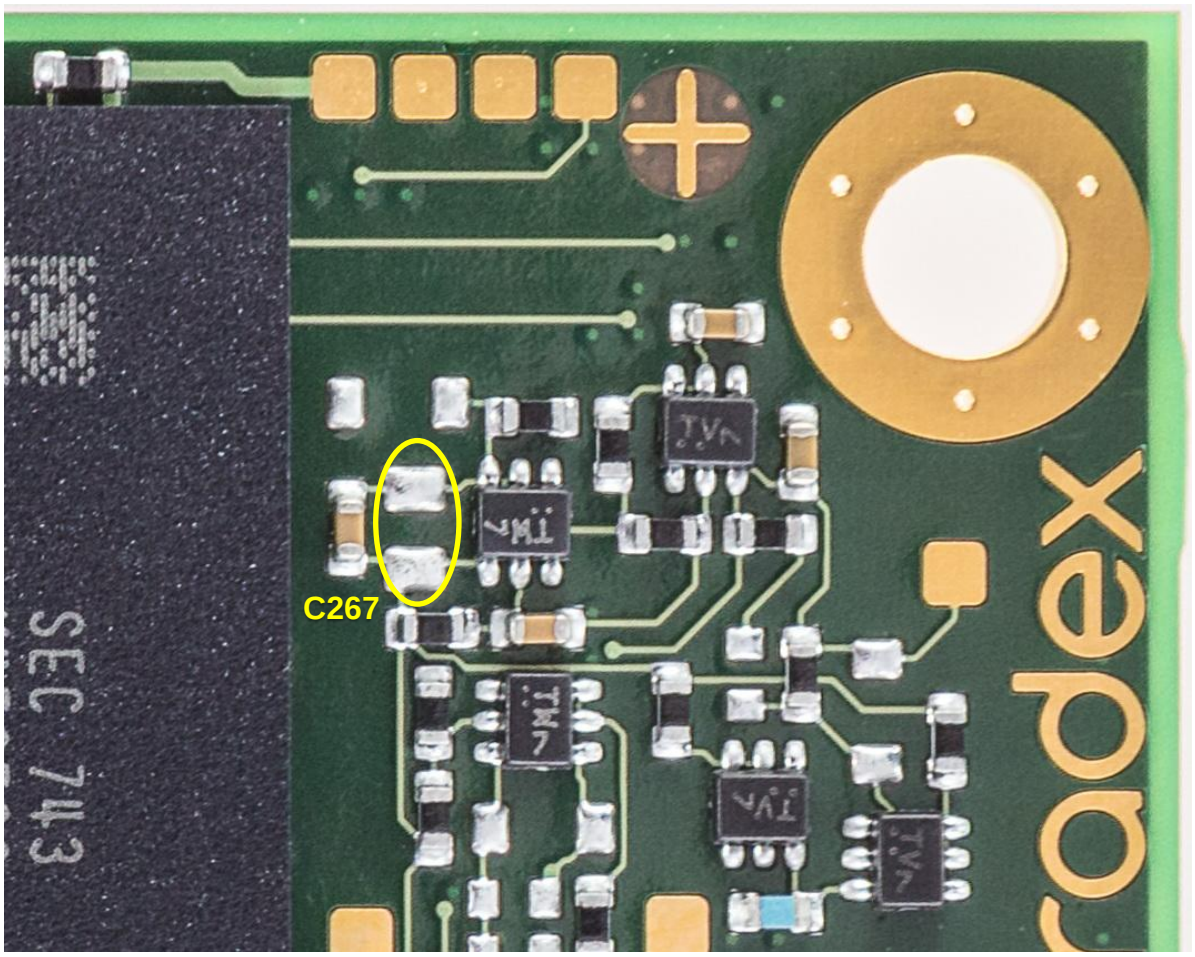

Figure 1. Location of C267 (top side, top view)

Errata #3: HAR-6830 – Different Reset State of SoC Pins

Affected Version: **Apalis iMX8QM 4GB WB IT (all versions)**
Apalis iMX8QM 4GB IT (all versions)
Apalis iMX8QP 2GB WB (all versions)
Apalis iMX8QP 2GB (all versions)
Fixed in: **Not scheduled**

Customer Impact

In the case of some GPIO-capable pins, the reset states are different from those documented in the previous versions of the module datasheet. The USBO1_EN and the USBH_EN signals are high during the reset state. Therefore, the USB power rails can get unintentionally enabled. Depending on the carrier board, other affected pins may have an impact on the behavior of the carrier board. It is advised to carefully check the updated reset state documentation in the module datasheet.

Description

The pin configuration registers of the i.MX8 SoC have reset states. These reset states have been stated in the Toradex Apalis iMX8 datasheet (document revision 1.1 and earlier) as reset states in section 4.4.

However, the i.MX 8 SoC features a System Controller Unit (SCU) that handles all pin configurations. The SCU comes with firmware (SCFW) that has its own default pin configurations. By the time of the release of the RESET_MOCI# signal, the SCU already overrides the pin configurations. Therefore, the SCU default settings are the relevant reset states for the pins. In the case of some of the GPIO-capable pins, the SCFW reset states are different from the register reset states. The Apalis iMX8 datasheet (document revision 1.2 and newer) has been updated with the reset values dictated by the SCFW. A comparison list can be found in this article: https://developer.toradex.com/knowledge-base/reset-state-of-the-imx8-soc-pins.

Despite the original intention, the USBO1_EN and the USBH_EN have pull-up resistors enabled instead of being pulled down during reset. This means that the USB power rails can get unintentionally enabled in the reset state of the module.

Depending on the carrier board, the different reset states of the SoC pins can result in unintended behavior. For example, on the Ixora carrier board V1.2A, the MMC1_D5 (pin 152) and MMC1_D6 (pin 156) are used for driving LEDs. These two pins have pull-up resistors enabled instead of the pull-down by default. Therefore, the LEDs are lit during the reset cycle.

Workaround

The values of the internal pull-up and pull-down resistors of the SoC are between 15kΩ and 50kΩ. These pull resistors can be disabled in the bootloader or during kernel boot. The issue caused by the unintentional pull-resistor states persists in time between the release of the reset signal and the bootloader configuring the IO pins in the intended state. In that case, an external pull-resistor on the carrier board can resolve the issue. According to measurements, adding a 10k pull-down resistor to a GPIO-capable pin with an internal pull-up resistor enabled results in a voltage level of around 0.6V. With an external 1k pull-down, the level goes below 100mV. However, these are just typical values at room temperature.

For the USBO1_EN and the USBH_EN signals, it is recommended to add a 10k pull-down resistor (or replace the existing weak pull-down resistor). This keeps the power enable signal level below the maximum input low threshold of the USB power switch IC during the reset cycle.

Errata #4: HAR-8448 – Triggering Recovery Mode on the Apalis iMX8 takes long, or the SoM does not go into Recovery Mode

Affected Version: **All versions of Apalis iMX8**
Fixed in: **Currently not planned**

Customer Impact

Triggering Recovery Mode on the SoM takes long, or the SoM does not go into Recovery Mode.

Description

In some cases, the recovery button of carrier boards needs to be pressed for 6-10s after powering up the SoM to get it into Recovery Mode. In other cases, the SoM does not go into recovery mode at all, even after the 6-10s period has elapsed.

The issue is caused by the combination of the NXP i.MX8 SoC's boot ROM code and the behavior of the USB interface of the host computer the USB OTG port of the carrier board is connected to. On the SoC side, a boot monitor timer is initialized at power-up. During USB enumeration in serial download mode, the host side may enumerate multiple times until enumeration succeeds. The enumeration retries take time and result in a delayed entry into Recovery Mode.

In some other cases, the maximum number of enumeration retries may get exceeded, which results in an enumeration failure. Under corner conditions, the ROM code may not be able to refresh the boot monitor timer due to the behavior of the USB host, causing a device system reset.

Workaround

In general, changing to a different host is the most effective way to avoid the issues. NXP may potentially fix this issue in the future.

Errata #5: HAR-8522 – The Audio Codec Does Not Reset Correctly with Low-Impedance Headphones Plugged in

Affected Version: **Apalis iMX8QM 4GB WB IT (all versions)**
Apalis iMX8QM 4GB IT (all versions)
Apalis iMX8QP 2GB WB (all versions)
Apalis iMX8QP 2GB (all versions)
Fixed in: **Not scheduled**

Customer Impact

After a software-initiated reset cycle (software reboot), the SGTL5000 audio codec may not work anymore.

Description

The headphone output signals of the SGTL5000 audio codec (SODIMM pin 316: AAP1_HP_L and SODIMM pin 318: AAP1_HP_R) have a DC offset of around 1.65V. Series capacitors must be placed between the SoM edge connector pins and the headphones to block this offset voltage. The Toradex reference design uses values between 47µF and 100µF for this purpose.

With headphones plugged in, these series capacitors get charged with 1.65V. In a software-initiated reset cycle (software reboot), all power rails of the SoM are turned off. After a delay of 5ms, the rails get re-enabled, and the SoM starts booting. The SGTL5000 can only be reset by power cycling it, as the codec does not have a dedicated reset input.

If headphones are plugged in during a software reboot, the voltage at the series capacitors is backfeeding to the power rails of the audio codec. The series capacitors are not fully discharged since the power rails are turned off only for around 5ms. The voltage at the 3.3V analog rail of the audio codec remains at about 1.5V. The residual voltage can cause the audio codec not to reset properly. This reset issue can prevent the audio codec from functioning properly. Power cycling the SoM resolves the problem.

The issue only occurs during software reboots. Regular power cycles are not affected. The issue mainly appears when low-impedance headphones are used. Occurrences are less frequent with high-impedance headphones (devices with smaller drivers).

When using the headphone output as a high-impedance line output signal, the resulting backfeeding current is low enough not to cause an issue. Without headphones plugged in, the circuit is open, and therefore no backfeeding occurs. This means that there is no residual voltage, and consequently, the software reset works properly.

Workaround

A locked-up audio codec can be recovered by power cycling the SoM.

Using high-impedance headphones instead of low-impedance ones reduces the backfeeding current (and therefore, the risk of having this issue manifest itself). Using the headphone output as a line-out signal with an external amplifier further helps to reduce the backfeeding.

In case only high-impedance headphones are used (or the interface is used as a line-out signal), the series capacitors' values can be reduced without sacrificing the signal quality at low frequencies. Series capacitors with lower capacity discharge faster and reduce the residual voltage during a software reboot.

If the audio codec needs to be reliably reset when used in combination with low-impedance headphones, an additional discharge circuit can be added to the carrier board. The idea behind this circuit is to discharge the series capacitors while the RESET_MOCI# signal is low. A resistor value of 47R is a good choice for series capacitors with values between 47µF and 100µF.

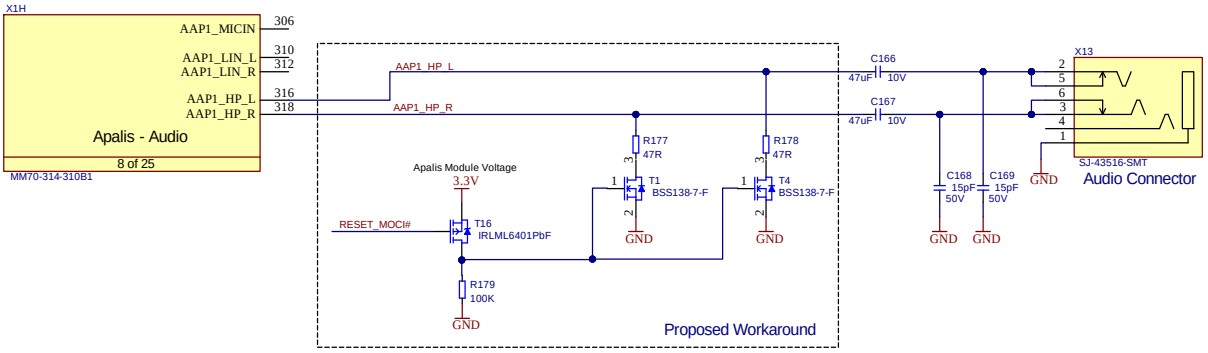

Figure 2. Proposed headphone capacitor discharge circuit