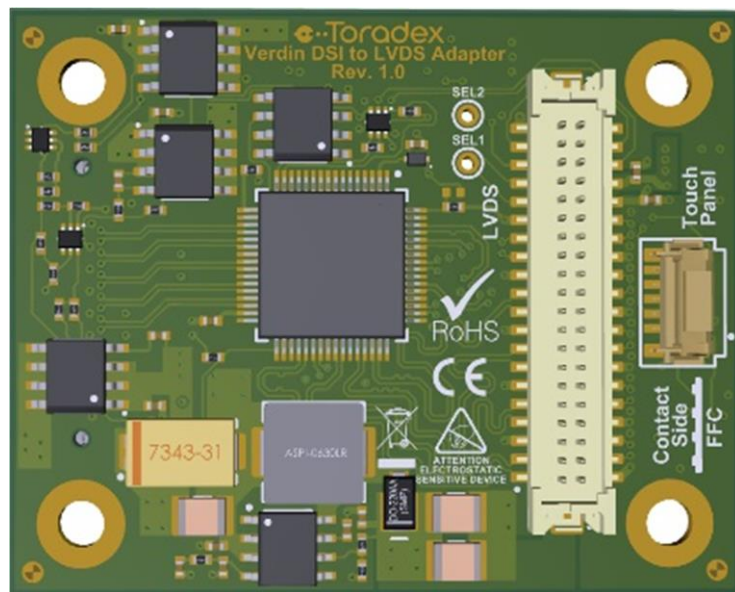


Verdin DSI to LVDS Adapter



Revision History

Date	Doc. Rev.	Board Version	Changes
20-November-19	Rev. 0.90	V1.0	Initial document release
24-March-20	Rev. 0.91	V1.0	Renaming net names according to the net naming convention Changing table fonts
31-March-20	Rev. 0.92	V1.0	Section 4. has been updated with additional details
6-April-20	Rev. 0.93	V1.0	Various cosmetic improvements

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1. Introduction

The Verdin DSI to LVDS Adapter is an add-on board for the Verdin Development Board which uses a MIPI-DSI Interface to provide an LVDS data output.

The Verdin DSI to LVDS Adapter uses Texas Instruments SN65DSI84-Q1 DSI to Single/Dual-Channel LVDS Bridge. It features a Single-Channel MIPI[®] D-PHY receiver front-end configuration with 4 data lanes per channel operating at 1Gbps per data lane and a maximum input bandwidth of 4Gbps.

The bridge decodes MIPI[®] DSI 18-bpp RGB666 and 24-bpp RGB888 packets and converts the formatted video data-stream to an LVDS output operating at pixel clocks range from 25 MHz to 154 MHz, offering a Dual-Channel LVDS or Single-Channel LVDS with four data lanes per channel. It is well suited for WUXGA (1920 x 1080) at 60 frames per second (fps) with up to 24 bits-per-pixel (bpp).

The Verdin DSI to LVDS Adapter can be connected to the MIPI[®] DSI connector (X43) on the Verdin Development Board.

1.1. Reference Documents

For detailed technical information on the suitable computer modules and other reference documents, please refer the following sections:

1.1.1 Verdin iMX8M Mini Computer Module Datasheet

The Verdin iMX8M Mini SoM datasheet can be downloaded here:

https://docs.toradex.com/107207-verdin_imx8m_mini_datasheet.pdf

1.1.2 Toradex Developer Website

<http://developer.toradex.com/>

1.1.3 SN65DSI84-Q1 MIPI[®] DSI to Dual-Link LVDS Bridge Product Datasheet

<http://www.ti.com/lit/ds/symlink/sn65dsi84-q1.pdf>

2. Features

2.1. One-Channel MIPI[®] DSI Receiver

- Implements MIPI D-PHY version 1.00.00 Physical Layer Front-end and DSI version 1.02.00
- Single-Channel DSI Receiver configurable for one, two, three, or four D-PHY data lanes per channel operating up to 1 Gbps per lane
- Supports 18-bpp and 24-bpp DSI Video Packets with RGB666 and RGB888 Formats

2.2. LVDS Transmitter

- Suitable for 60-fps WUXGA 1920 x 1200 resolution at 18-bpp and 24-bpp color (Dual-Channel LVDS), and 60-fps 1366 x 768 resolution at 18-bpp and 24-bpp (Single-Channel LVDS)
- Output Configurable for Single-Channel or Dual-Channel LVDS
- Supports Single-Channel DSI to Dual-Channel LVDS operating mode
- LVDS Output-Clock Range of 25 MHz to 154 MHz in Dual-Channel or Single-Channel mode
- LVDS Channel SWAP, LVDS PIN Order Reverse feature for ease of PCB routing

2.3. Hardware Architecture Block Diagram

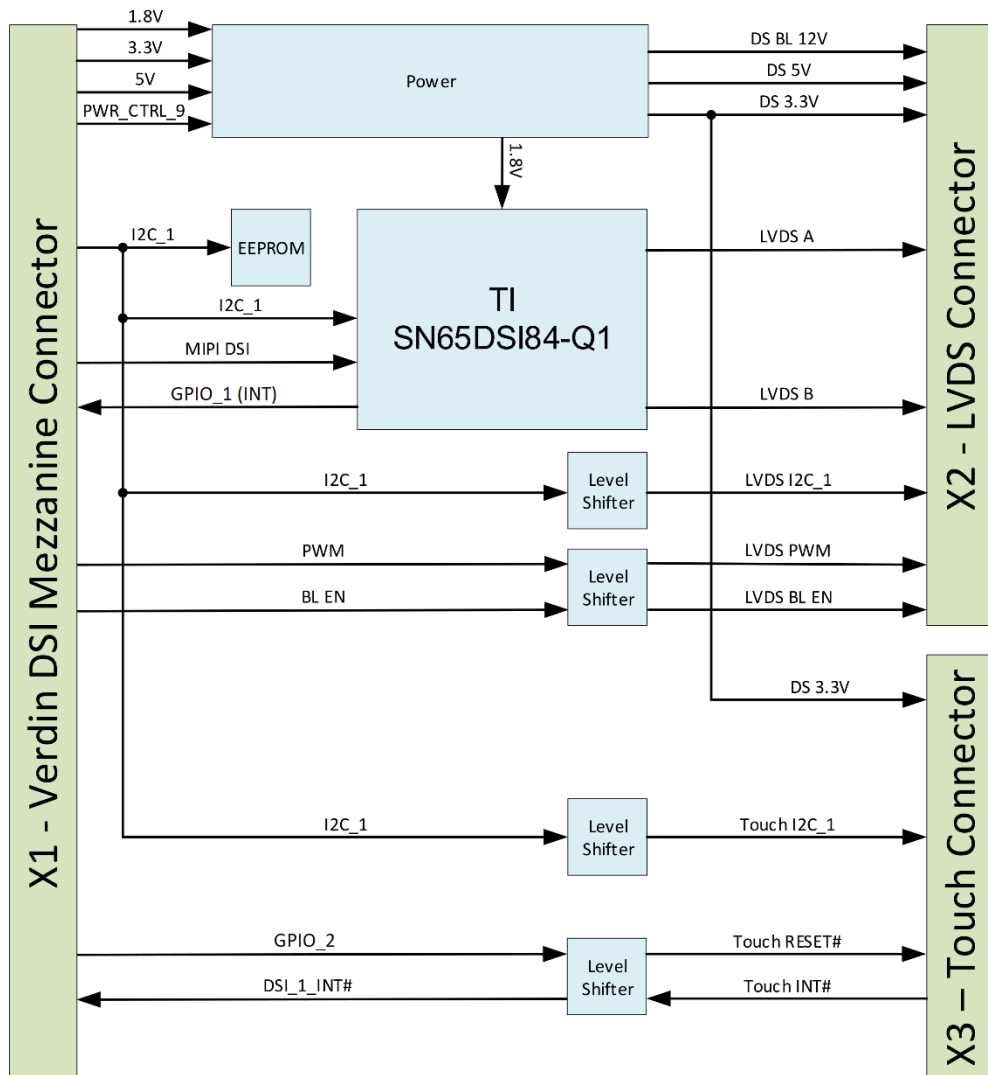


Fig.1 Verdin DSI to LVDS Adapter Hardware Architecture

2.4. Physical Drawings

2.4.1 Top Side Connector

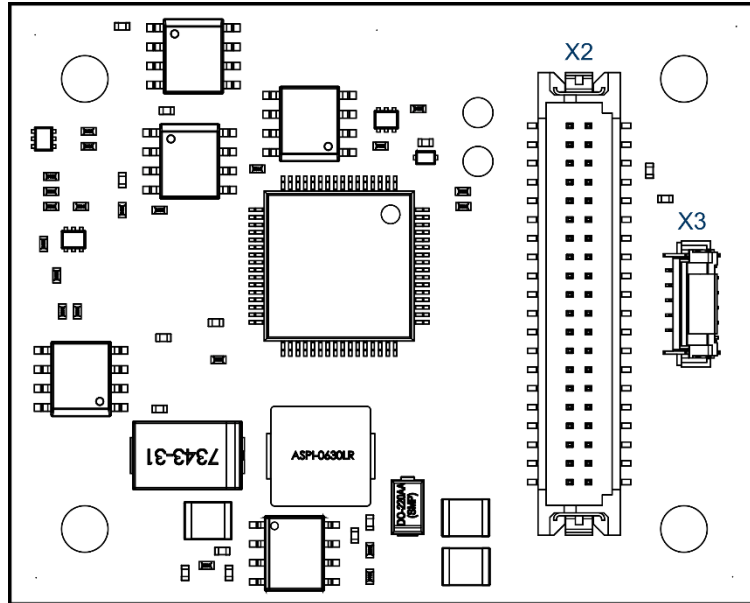


Fig.2 Verdin DSI to LVDS Adapter – Top Side

2.4.2 Bottom Side Connector

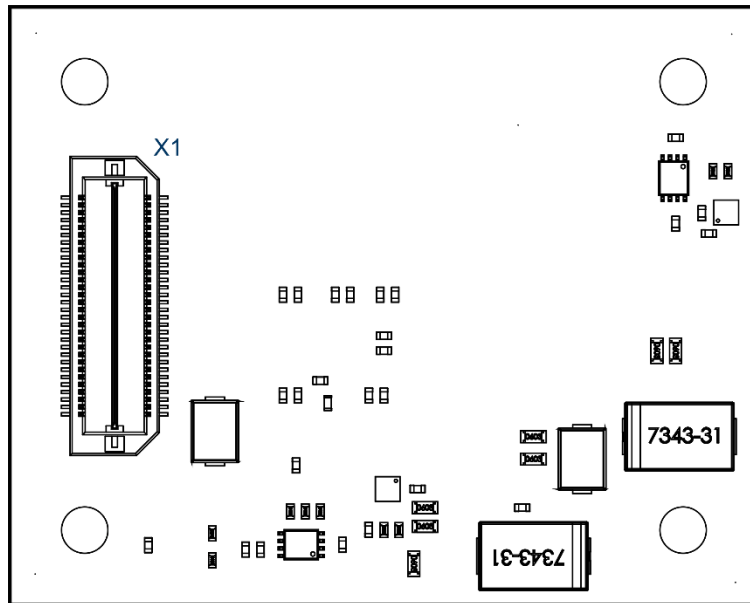


Fig.3 Verdin DSI to LVDS Adapter – Bottom Side

Ref	Description	Remarks
X1	MIPI® DSI Interface Connector	
X2	LVDS Connector	
X3	Capacitive Touch Panel Connector	

2.4.3 MIPI® DSI Interface with Verdin Development Board

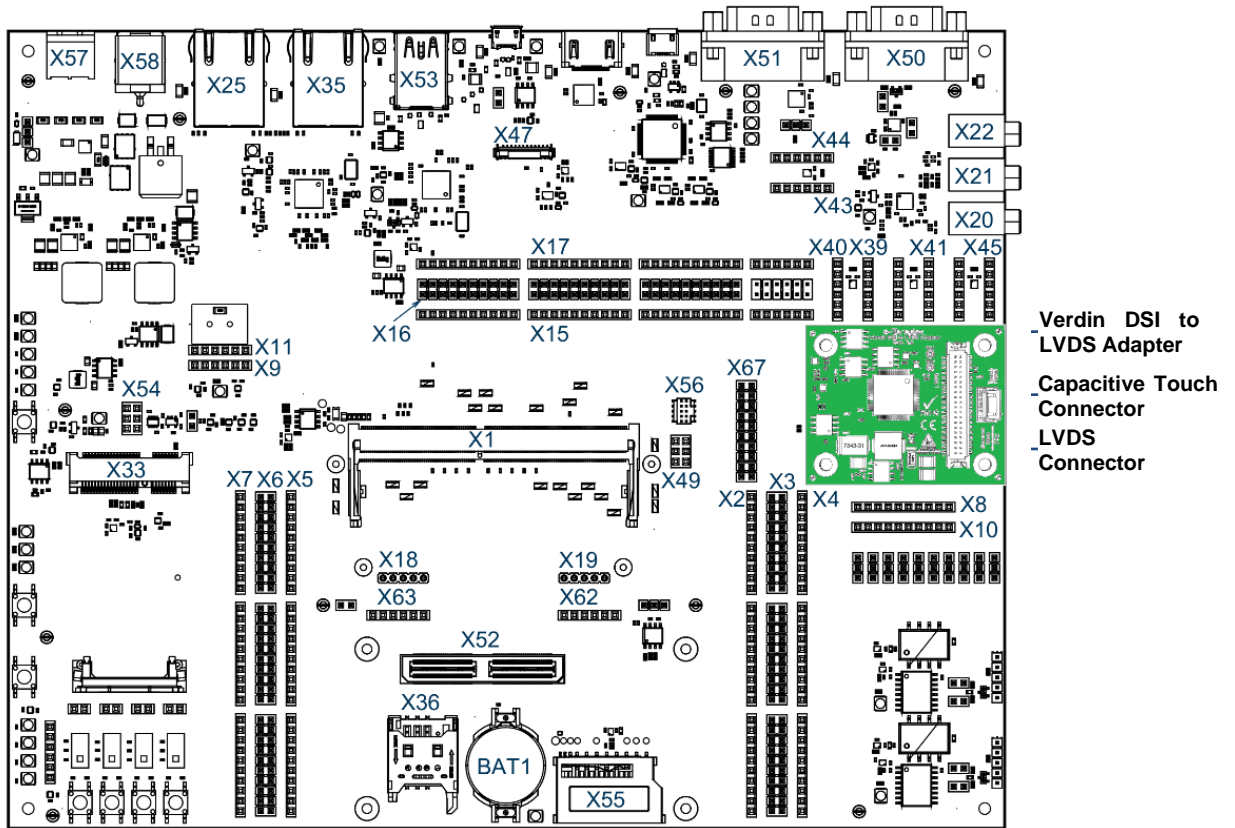


Fig.4 Verdin DSI to LVDS Adapter installed on Verdin Development Board

3. Interface Description

3.1. Mezzanine Connector (X1)

Manufacturer: Samtec - QTH-030-02-L-D-A

Type: High-Speed Ground Plane Socket

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down
1	GPIO_1	I/O	+1.8V	
2	GPIO_2	I/O	+1.8V	
3	I2C_1_SDA	I/O	+1.8V	1.8k to +1.8V on DB
4	GND	PWR		
5	I2C_1_SCL	O	+1.8V	1.8k to +1.8V on DB
6	NC			
7	DSI_1_INT#	I	+1.8V	
8	+V_SUPPLY_FILT_SW	PWR	+6 - 27V	
9	GND	PWR		
10	+V_SUPPLY_FILT_SW	PWR	+6 - 27V	
11	DSI_1_D0_P			
12	+V_SUPPLY_FILT_SW	PWR	+6 - 27V	
13	DSI_1_D0_N			
14	+V_SUPPLY_FILT_SW	PWR	+6 - 27V	
15	GND	PWR		
16	+V_SUPPLY_FILT_SW	PWR	+6 - 27V	
17	DSI_1_D1_P			
18	NC			
19	DSI_1_D1_N			
20	+V5_SW	PWR	+5V	
21	GND	PWR		
22	+V5_SW	PWR	+5V	
23	DSI_1_CLK_P			
24	+V5_SW	PWR	+5V	
25	DSI_1_CLK_N			
26	+V5_SW	PWR	+5V	
27	GND	PWR		
28	+V5_SW	PWR	+5V	
29	DSI_1_D2_P			
30	NC			
31	DSI_1_D2_N			
32	+V3.3_SW	PWR		
33	GND	PWR		
34	+V3.3_SW	PWR	+3.3V	
35	DSI_1_D3_P			
36	+V3.3_SW	PWR	+3.3V	
37	DSI_1_D3_N			
38	+V3.3_SW	PWR	+3.3V	
39	GND	PWR		
40	+V3.3_SW	PWR	+3.3V	
41	NC			
42	NC			
43	NC			
44	+V1.8_SW	PWR	+1.8V	
45	NC			

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down
46	+V1.8_SW	PWR	+1.8V	
47	NC			
48	+V1.8_SW	PWR	+1.8V	
49	GND	PWR		
50	+V1.8_SW	PWR	+1.8V	
51	NC			
52	+V1.8_SW	PWR	+1.8V	
53	NC			
54	NC			
55	DSI_1_BKL_EN	O	+1.8V	
56	GND	PWR		
57	DSI_PWM_3	O	+1.8V	
58	NC			
59	GND	PWR		
60	PWR_CTRL_9	O	+1.8V	
61	GND	PWR		

3.2. LVDS Connector (X2)

Manufacturer: Hirose - DF13E-40DP-1.25V(76)

Type: Header connector

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down
1	LVDS_1_A_TX3_P			
2	GND	PWR		
3	LVDS_1_A_TX3_N			
4	LVDS_1_B_CLK_N			
5	GND	PWR		
6	LVDS_1_B_CLK_P			
7	LVDS_1_A_TX2_P			
8	GND	PWR		
9	LVDS_1_A_TX2_N			
10	LVDS_1_B_TX0_N			
11	GND	PWR		
12	LVDS_1_B_TX0_P			
13	LVDS_1_A_TX1_P			
14	GND	PWR		
15	LVDS_1_A_TX1_N			
16	LVDS_1_B_TX1_N			
17	GND	PWR		
18	LVDS_1_B_TX1_P			
19	LVDS_1_A_TX0_P			
20	GND	PWR		
21	LVDS_1_A_TX0_N			
22	LVDS_1_B_TX2_N			
23	GND	PWR		
24	LVDS_1_B_TX2_P			
25	LVDS_1_A_CLK_P			
26	GND	PWR		
27	LVDS_1_A_CLK_N			
28	LVDS_1_B_TX3_N			
29	GND	PWR		
30	LVDS_1_B_TX3_P			
31	RESERVED (SEL1)	PWR		
32	+V3.3_LVDS	PWR	+3.3V	
33	RESERVED (SEL2)	PWR		
34	+V5_LVDS	PWR	+5V	
35	DSI_PWM_3_LVDS	O	+3.3V	
36	I2C_1_LVDS_SDA	IO	+3.3V	4.7k to +3.3V
37	DSI_1_BKL_EN_LVDS	O	+3.3V	
38	I2C_1_LVDS_SCL	O	+3.3V	4.7k to +3.3V
39	+V12_BL	PWR	+12V	
40	+V12_BL	PWR	+12V	

3.3. Capacitive Touch Connector (X3)

Manufacturer: Hirose - FH12-10S-0.5SVA(54)

Type: Receptacle FPC/FFC connector

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down
1	I2C_1_CTL_SDA	IO	+3.3V	4.7k to +3.3V
2	I2C_1_CTL_SCL	O	+3.3V	4.7k to +3.3V
3	GND	PWR		
4	TOUCH_INT#	I	+3.3V	
5	TOUCH_RESET#	O	+3.3V	
6	+V3.3_LVDS	PWR	+3.3V	
7	NC			
8	NC			
9	NC			
10	NC			

4. Electrical Characteristics

4.1. Power Supply Characteristics

4.1.1 Supply Voltage

Parameter	Min.	Typ.	Max.	Unit
+V1.8_SW Supply Voltage	1.65	1.8	1.95	V
+V3.3_SW Supply Voltage	3.0	3.3	3.5	V
+V5_SW Supply Voltage (not used)		-		V
+V_SUPPLY_FILT_SW Supply Voltage (not used)		-		V

4.1.2 Current Consumption

Parameter	Conditions	Typ. Supply Current ^{1,2}	Unit
+V1.8_SW Supply Voltage	SN65DSI84: SINGLE Channel DSI to DUAL Channel LVDS, 1440 x 900	108	mA
+V3.3_SW Supply Voltage		6	mA

1: Excluding display consumption

2: T_{amb} = 25 °C

5. Operating Conditions

5.1. Operating Temperature Range

- 35 to +85 °C

6. Mechanical Data

6.1. Verdin DSI to LVDS Adapter Dimensions - Top Side

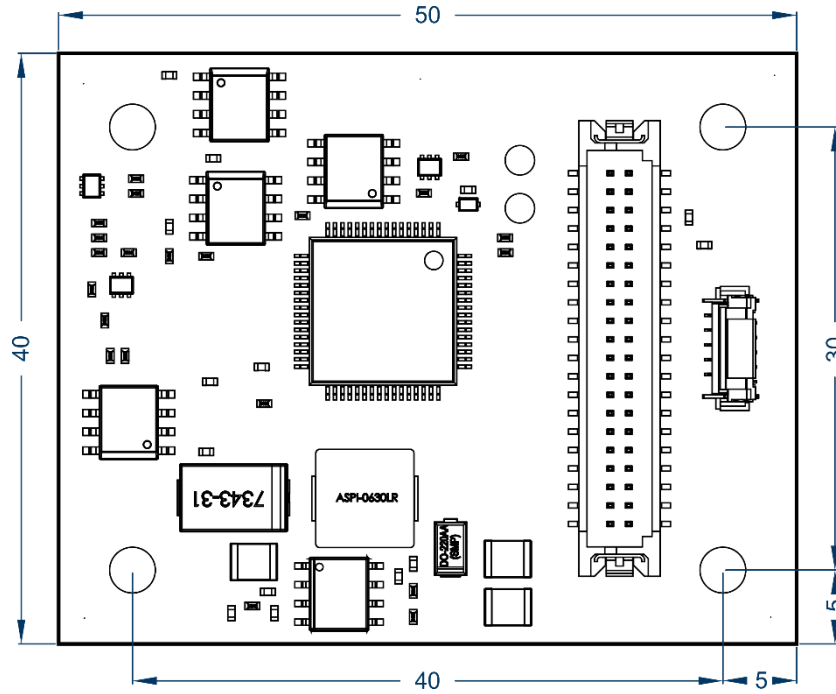


Fig.5 Verdin DSI to LVDS Adapter Dimensions(mm) - Top view

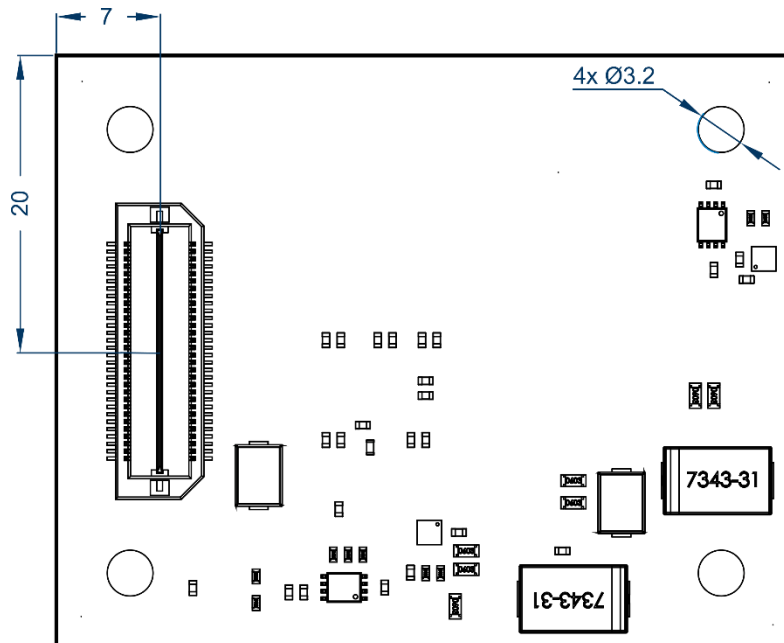


Fig.6 Verdin DSI to LVDS Adapter Dimensions (mm) - Bottom view

7. Design Data

The design data for the Toradex carrier boards and adapter boards are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the board design data, please use the link below:

<http://developer.toradex.com/carrier-board-design/reference-designs>

8. Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: <http://www.toradex.com/support/product-compliance>

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