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Verdin Development Board

Errata Document

Document Revision History

Date	Doc. Rev.	Notes
2020-03-24	Rev. 0.90	Initial Release
2020-03-31	Rev. 0.91	Errata #2: Title and content updated
2020-04-14	Rev. 0.92	Minor cosmetic improvements
2020-09-10	Rev. 0.93	Fix versions updated Errata #4: Added
2021-02-08	Rev. 0.94	Errata #5: Added

Overview

Errata #1: HAR-3274 – Inconsistency concerning the position of general-purpose LEDs and the order of related signals on connector X38

Affected Version: **Verdin Development Board V1.0B**
Fixed in: **Verdin Development Board V1.1A**

1.1. Customer Impact

This error might create confusion while using this product feature.

1.2. Description

The position of LED21, LED22, LED23, LED24 in the general-purpose LEDs and Switches area is not consistent with the order of related signals available on the connector X38.
This might create confusion when using this product feature.

1.3. Workaround

The table below shows the connections between the X38 connector and the related LEDs. This table should be used to avoid confusion when using this product feature.

X38 pin	Signal	Linked LED
1	+V1.8_SW	-
2	LED_1	LED21
3	LED_2	LED22
4	LED_3	LED23
5	LED_4	LED24
6	GND	-

Errata #2: HAR-3252 – SDIO evaluation kits failing when used in HS400 mode

Affected Version: **Verdin Development Board V1.0B**
Fixed in: **Verdin Development Board V1.1A**

2.1. Customer Impact

SDIO evaluation kits connected to the SDIO interface of the product may not work correctly at HS400 mode due to signal integrity issues. Regular SD cards are working fine as expected.

2.2. Description

SDIO interface is failing when SDIO evaluation kits are used in HS400 mode.
By default, the software initiates communication in HS400 mode, which uses a 200MHz clock on the SD_1_CLK signal; this results in a failed tuning test.
If a mode with lower frequencies is forced, the cards are working fine.
This is caused by a signal integrity issue concerning the clock signal of the SDIO interface.

2.3. Workaround

There is no fix for this issue at the moment. SDIO evaluation kits might need to be used at lower frequency modes.

Errata #3: HAR-3379 – Missing a pull-up resistor on the WAKE1_MICO# signal

Affected Version: **Verdin Development Board V1.0B**
Fixed in: **Verdin Development Board V1.1A**

3.1. Customer Impact

The absence of a pull-up resistor may lead to an ambiguous signal state.

3.2. Description

The WAKE1_MICO# signal is an open drain signal driven low by a PCI Express Mini Card wake event. This pin should be pulled up to keep the signal inactive. The absence of the pull-up may lead to inconsistent signal behavior.

3.3. Workaround

It is recommended to enable the SoM's internal pull-up of the pin connected to this signal.

Errata #4: HAR-3935 – CTRL_FORCE_OFF_MOCI# is pulled-up to wrong voltage rail

Affected Version: **Verdin Development Board V1.0B**
Fixed in: **Verdin Development Board V1.1A**

4.1. Customer Impact

The main power gets killed as soon as the CTRL_PWR_EN_MOCI# goes low and the +V1.8_SW rail is turned off. This means the main power is killed during a reset cycle, and the power-down sequence is not graceful.

4.2. Description

According to the Verdin specifications, the CTRL_FORCE_OFF_MOCI# is an open-drain output of the module, which is 5V tolerant and requires a pull-up resistor on the carrier board. On the Verdin Development Board V1.0B, the CTRL_FORCE_OFF_MOCI# is pulled up to the +V1.8_SW rail. Unfortunately, this rail is switched by the CTRL_PWR_EN_MOCI# signal. During a reset cycle (software or button initiated), the CTRL_PWR_EN_MOCI# signal can go low for power cycling the peripherals on the carrier board. This is also disabling the +V1.8_SW, which means the CTRL_FORCE_OFF_MOCI# goes low and triggers the kill input of IC16. The IC16 will then kill the main power of the module. This means resetting the module can cause an unintentional power-off of the system.

During a regular power-down cycle, the CTRL_FORCE_OFF_MOCI# signal is supposed to go low as the last step after all the module and carrier board peripheral rails are shut down in the correct order. Due to the incorrectly pulled up CTRL_FORCE_OFF_MOCI# signal, the main power gets killed in a too early state. This means the power rails are not shut down in the intended graceful sequence. Even with this non-graceful shutdown, damages on the module or carrier board are not expected.

4.3. Workaround

Removing R80 disables the CTRL_FORCE_OFF_MOCI# signal on the Verdin Development Board. However, this disables the “kill-feature” entirely. Therefore, after a shutdown, the supplies are not turned off, which prevents the system from being turned on by using the power button. For turning on the system, either power cycle the whole board or turn off the main 3.3V rail on the carrier board by pressing the power button for >3s. Besides this inconvenience, the modification is compatible with all Verdin module versions.

An alternate workaround is removing R95 and adding a 100kΩ pull-up resistor from CTRL_FORCE_OFF_MOCI# to +V5_STB. This makes the circuit fully compatible with the new Verdin modules. The kill-feature would work with this modification as intended with the new Verdin modules. However, for the older Verdin iMX8M Mini V1.0B module, the CTRL_FORCE_OFF_MOCI# is not 5V tolerant and the CTRL_FORCE_OFF_MOCI# signal gets also asserted during the reset cycle. This means after the modification, the development board is not compatible anymore with the Verdin iMX8M Mini V1.0B. Read Errata #13 and Errata #5 of the Verdin iMX8M Mini V1.0B module for more information. The following picture shows one potential implementation of the alternate workaround patch:

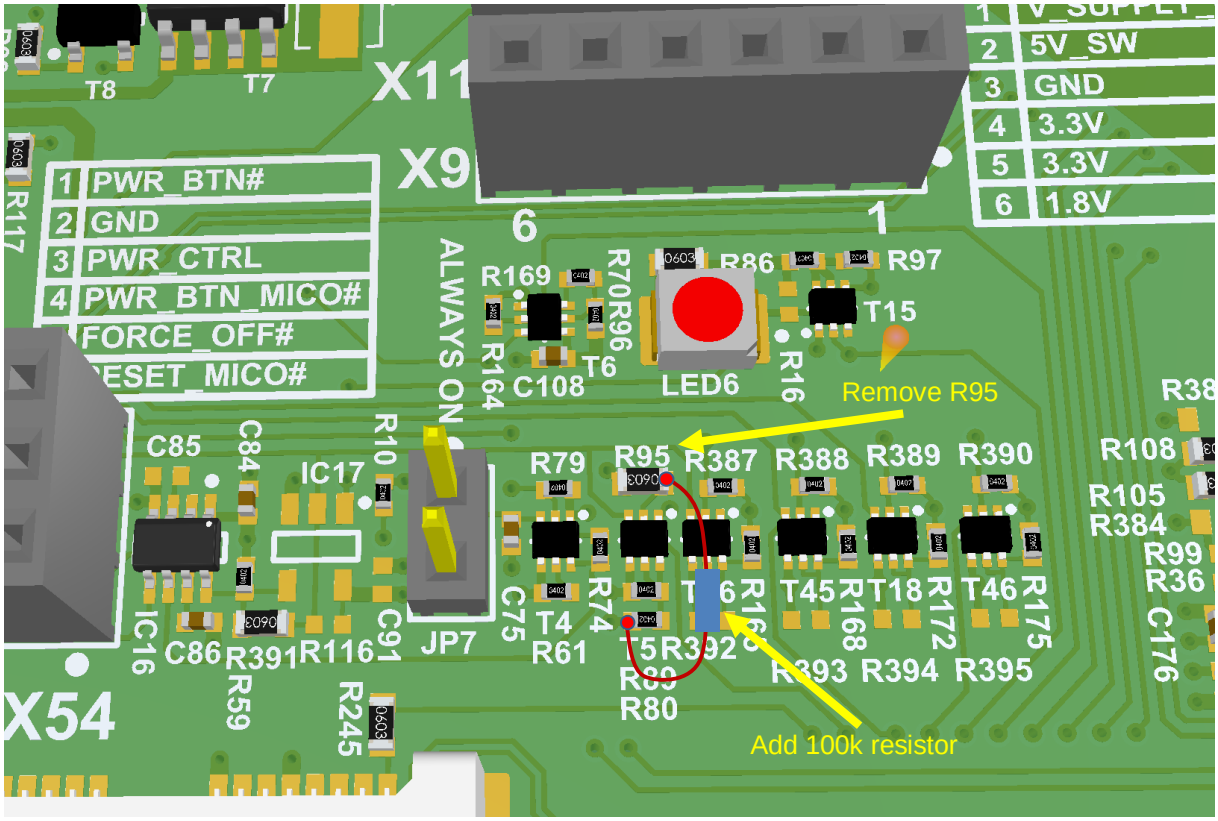

Figure 1 Verdin Development Board CTRL_FORCE_OFF_MOCI# pull-up patch (Top Side)

Errata #5: HAR-6600 – Ethernet PHY address strapping resistor for configuring PHYAD2 missing

Affected Version: **Verdin Development Board V1.0B**
Fixed in: **Verdin Development Board V1.1A**

5.1. Customer Impact

In combination with the Verdin iMX8M Plus, the Ethernet PHY on the carrier board (which is connected to the RGMII interface of the SoM) gets strapped to address 0b00011 rather than the intended 0b00111. This address is not compatible with the default address configuration used in applicable Toradex software, causing the 2nd Ethernet interface of the carrier board to be non-functional. The strapped value and the resulting PHY address - in combination with future Verdin modules - may be different.

5.2. Description

The last three bits of the PHY address are strapped by the PHYAD0, PHYAD1, and PHYAD2 pin. PHYAD0 and PHYAD1 are located on the LED output signals, which are strapped correctly. PHYAD2 is located on the RXC pin of the PHY (ETH_2_RGMII_RXC signal). The strapping resistors R188 and R189 are both missing in the BOM. Intended by design is to strap the signal high by assembling R188. Since both strapping resistors are missing, the strapping value is dictated by the module's behavior of the ETH_2_RGMII_RXC signal during the enabling of the Ethernet power rails. The Ethernet power rails are enabled on the carrier board by the PWR_CTRL_4 signal.

The Verdin iMX8M Plus has a weak pull-down enabled on the ETH_2_RGMII_RXC by default. Therefore, the PHY address gets strapped to 0b00011 rather than the intended 0b00111. In this case, the module can only communicate over the MDIO interface with the PHY if the driver changes the address to 0b00011.

5.3. Workaround

The best workaround is to populate R188 with a 10kΩ resistor. The resistor is a 0603 type.

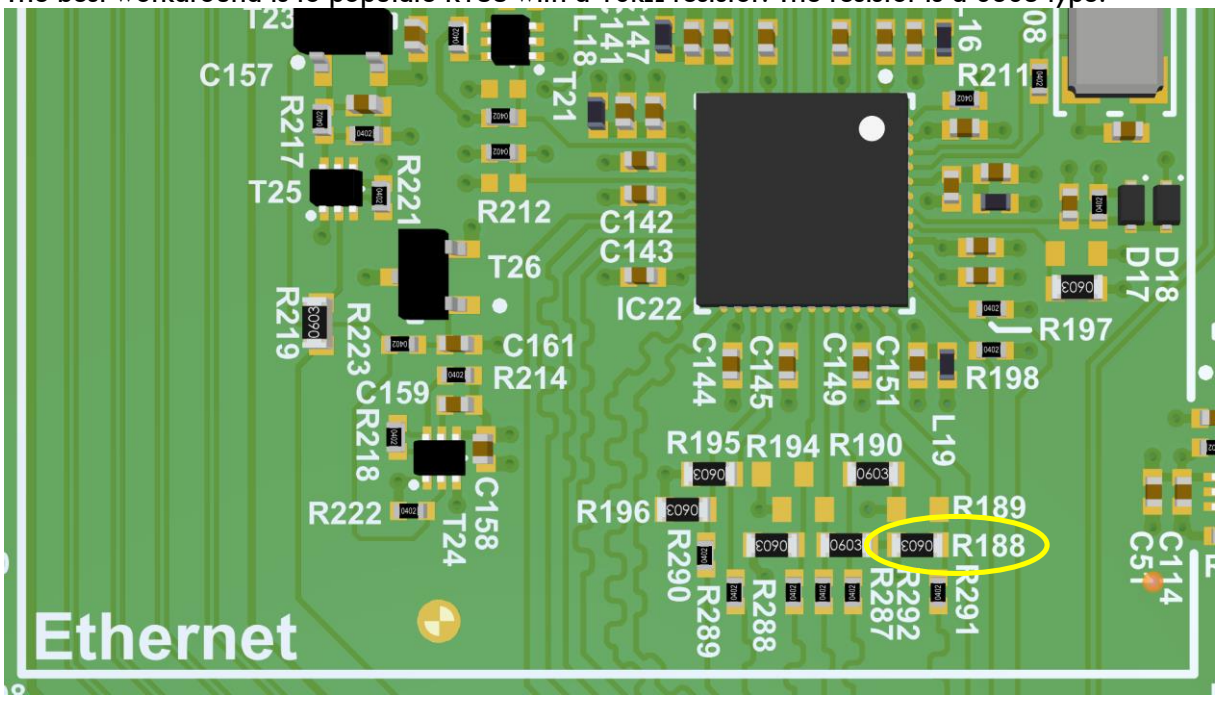

Figure 2 Verdin Development Board – location of R188 (Top Side)

An alternate workaround is changing the PHY address to 0b00011 in software. However, this causes the software to not be compatible with newer versions of the Verdin Development Board and the other Verdin carrier boards following the same PHY address recommendation/convention.