

Verdin Development Board

Errata Document





Document Revision History

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2020-03-24	Rev. 0.90	Initial Release
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2020-04-14	Rev. 0.92	Minor cosmetic improvements
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2021-04-28	Rev. 0.95	Errata #6: Added
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2023-04-06	Rev. 1.7	Errata #14: Fixed inaccurate description of issue and changed workaround.



Overview

Errata #1:	HAR-3274 – Inconsistency concerning the position of general-purpose LEDs and the
	order of related signals on connector X384
Errata #2:	HAR-3252 – SDIO evaluation kits failing when used in HS400 mode5
Errata #3:	HAR-3379 – Missing a pull-up resistor on the WAKE1_MICO# signal6
Errata #4:	HAR-3935 – CTRL_FORCE_OFF_MOCI# is pulled-up to wrong voltage rail7
Errata #5:	HAR-6600 – Ethernet PHY address strapping resistor for configuring PHYAD2 missing9
Errata #6:	HAR-7206 – Series capacitor values are too small for the audio codec's speaker output to
	be used in a stereo setup10
Errata #7:	HAR-8016 – CSI_1_MCLK Voltage Level is not 3.3V12
Errata #8:	HAR-8290 - The LED status signals of the on-module Ethernet PHY are swapped13
Errata #9:	HAR-8342 – Stitching Capacitors Influence Verdin iMX8M Plus Bluetooth Config
	Strapping14
Errata #10:	HAR-8426 – Signal distortion on the audio codec's "Line In" input16
Errata #11:	HAR-8833 – The carrier board turns off or resets when a cable is connected to the USB-C
	FTDI debug connector
Errata #12:	HAR-8934 – The RC element on the PCIe reset signal contributes to violating the PCIe
	specification19
Errata #13:	HAR-8976 – The silkscreen of X53 power indication LEDs is not correct21
Errata #14:	HAR-9004 – Overvoltage protection triggered when hot plugin Verdin Development Board
	V1.1A



Errata #1: HAR-3274 – Inconsistency concerning the position of general-purpose LEDs and the order of related signals on connector X38

Affected Version:	Verdin Development Board V1.0B
Fixed in:	Verdin Development Board V1.1A

1.1 Customer Impact

This error might create confusion while using this product feature.

1.2 Description

The position of LED21, LED22, LED23, LED24 in the general-purpose LEDs and Switches area is not consistent with the order of related signals available on the connector X38. This might create confusion when using this product feature.

1.3 Workaround

The table below shows the connections between the X38 connector and the related LEDs. This table should be used to avoid confusion when using this product feature.

X38 pin	Signal	Linked LED
1	+V1.8_SW	-
2	LED_1	LED21
3	LED_2	LED22
4	LED_3	LED23
5	LED_4	LED24
6	GND	-



Errata #2: HAR-3252 – SDIO evaluation kits failing when used in HS400 mode

Affected Version:	Verdin Development Board V1.0B
Fixed in:	Verdin Development Board V1.1A

2.1 Customer Impact

SDIO evaluation kits connected to the SDIO interface of the product may not work correctly at HS400 mode due to signal integrity issues. Regular SD cards are working fine as expected.

2.2 Description

SDIO interface is failing when SDIO evaluation kits are used in HS400 mode. By default, the software initiates communication in HS400 mode, which uses a 200MHz clock on the SD_1_CLK signal; this results in a failed tuning test.

If a mode with lower frequencies is forced, the cards are working fine. This is caused by a signal integrity issue concerning the clock signal of the SDIO interface.

2.3 Workaround

There is no fix for this issue at the moment. SDIO evaluation kits might need to be used at lower frequency modes.



Errata #3: HAR-3379 – Missing a pull-up resistor on the WAKE1_MICO# signal

Affected Version:	Verdin Development Board V1.0B
Fixed in:	Verdin Development Board V1.1A

3.1 Customer Impact

The absence of a pull-up resistor may lead to an ambiguous signal state.

3.2 Description

The WAKE1_MICO# signal is an open drain signal driven low by a PCI Express Mini Card wake event. This pin should be pulled up to keep the signal inactive. The absence of the pull-up may lead to inconsistent signal behavior.

3.3 Workaround

It is recommended to enable the SoM's internal pull-up of the pin connected to this signal.



Errata #4: HAR-3935 – CTRL_FORCE_OFF_MOCI# is pulled-up to wrong voltage rail

Affected Version:	Verdin Development Board V1.0B
Fixed in:	Verdin Development Board V1.1A

4.1 Customer Impact

The main power gets killed when the CTRL_PWR_EN_MOCI# goes low and the +V1.8_SW rail is turned off. This means the main power is killed during a reset cycle, and the power-down sequence is not graceful.

4.2 Description

According to the Verdin specifications, the CTRL_FORCE_OFF_MOCI# is an open-drain output of the module, which is 5V tolerant and requires a pull-up resistor on the carrier board. On the Verdin Development Board V1.0B, the CTRL_FORCE_OFF_MOCI# is pulled up to the +V1.8_SW rail. Unfortunately, this rail is switched by the CTRL_PWR_EN_MOCI# signal. During a reset cycle (software or button initiated), the CTRL_PWR_EN_MOCI# signal can go low for power cycling the peripherals on the carrier board. This is also disabling the +V1.8_SW, which means the CTRL_FORCE_OFF_MOCI# goes low and triggers the kill input of IC16. The IC16 then kills the main power of the module. This means resetting the module can cause an unintentional power-off of the system.

During a regular power-down cycle, the CTRL_FORCE_OFF_MOCI# signal is supposed to go low as the last step after all the module and carrier board peripheral rails are shut down in the correct order. Due to the incorrectly pulled up CTRL_FORCE_OFF_MOCI# signal, the main power gets killed in a too early state. This means the power rails are not shut down in the intended graceful sequence. Even with this non-graceful shutdown, damages on the module or carrier board are not expected.

4.3 Workaround

Removing R80 disables the CTRL_FORCE_OFF_MOCI# signal on the Verdin Development Board. However, this disables the "kill-feature" entirely. Therefore, the supplies are not turned off after a shutdown, which prevents the system from being turned on by using the power button. For turning on the system, either power cycle the whole board or turn off the main 3.3V rail on the carrier board by pressing the power button for >3s. Besides this inconvenience, the modification is compatible with all Verdin module versions.

An alternate workaround is removing R95 and adding a 100kΩ pull-up resistor from CTRL_FORCE_OFF_MOCI# to +V5_STB. This makes the circuit fully compatible with the new Verdin modules. The kill-feature would work with this modification as intended with the new Verdin modules. However, for the older Verdin iMX8M Mini V1.0B module, the CTRL_FORCE_OFF_MOCI# is not 5V tolerant, and the CTRL_FORCE_OFF_MOCI# signal gets also asserted during the reset cycle. After the modification, the development board is no longer compatible with the Verdin iMX8M Mini V1.0B. Read Errata #13 and Errata #5 of the Verdin iMX8M Mini V1.0B module for more information. The following picture shows one potential implementation of the alternate workaround patch:





Figure 1. Verdin Development Board CTRL_FORCE_OFF_MOCI# pull-up patch (Top Side)



Errata #5: HAR-6600 – Ethernet PHY address strapping resistor for configuring PHYAD2 missing

Affected Version:	Verdin Development Board V1.0B
Fixed in:	Verdin Development Board V1.1A

5.1 Customer Impact

In combination with the Verdin iMX8M Plus, the Ethernet PHY on the carrier board (which is connected to the RGMII interface of the SoM) gets strapped to address 0b00011 rather than the intended 0b00111. This address is not compatible with the default address configuration used in applicable Toradex software, causing the 2nd Ethernet interface of the carrier board to be non-functional. The strapped value and the resulting PHY address may be different in combination with future Verdin modules.

5.2 Description

The last three bits of the PHY address are strapped by the PHYAD0, PHYAD1, and PHYAD2 pin. PHYAD0 and PHYAD1 are located on the LED output signals, which are strapped correctly. PHYAD2 is located on the RXC pin of the PHY (ETH_2_RGMII_RXC signal). The strapping resistors R188 and R189 are both missing in the BOM. Intended by design is to strap the signal high by assembling R188. Since both strapping resistors are missing, the strapping value is dictated by the module's behavior of the ETH_2_RGMII_RXC signal during the enabling of the Ethernet power rails. The Ethernet power rails are enabled on the carrier board by the PWR_CTRL_4 signal.

The Verdin iMX8M Plus has a weak pull-down enabled on the ETH_2_RGMII_RXC by default. Therefore, the PHY address gets strapped to 0b00011 rather than the intended 0b00111. In this case, the module can only communicate over the MDIO interface with the PHY if the driver changes the address to 0b00011.

5.3 Workaround

The best workaround is to populate R188 with a $10k\Omega$ resistor. The resistor is a 0603 type.



Figure 2. Verdin Development Board - location of R188 (Top Side)



Errata #6: HAR-7206 – Series capacitor values are too small for the audio codec's speaker output to be used in a stereo setup

Affected Version:	Verdin Development Board V1.1A
Fixed in:	To be scheduled

6.1 Customer Impact

The audio output is significantly attenuated or not audible at all when the audio codec's speaker output is used in combination with external speakers connected in a stereo setup.

The issue does not affect the speaker output when the external speakers are connected in a mono setup.

6.2 Description

The audio codec featured on the Verdin Development Board V1.1 includes an integrated speaker driver.

The Verdin Development Board V1.1 provides two audio codec speaker output operating modes: mono and stereo. In a mono setup, one or two external speakers are connected as a Bridge Tied Load (BTL) to the connectors X28 or X29. In this setup, the speaker output should work fine.

In a stereo setup, two external speakers are connected to the connector X13. In this case, one end of each speaker's coil is connected to the common ground pin (GND), the other ends are connected to the audio codec IC through the capacitors C182 or C183, respectively.

The capacitors C182 (1uF) and C183 (1uF), in conjunction with the speaker's impedance (80hm), form high-pass filters. The cut-off frequency of the high-pass filters is around 20 kHz.

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi * 80hm * 1uF} \approx 20kHz$$

This frequency is at the upper edge of the audible frequency range, and lower frequencies are attenuated/filtered out by the aforementioned high-pass filter.

6.3 Workaround

A partial workaround has already been applied to the Verdin Development Board V1.1A: 00hm resistors have assembled instead of the capacitors C182 and C183. To complete the workaround, external capacitors connected in series with the external speakers are required (see Figure 3).

The exact values of the capacitors depend on the desired cut-off frequency and the impedance of the speakers. Some applications may not require the complete audible frequency range of approx. 20Hz – 20Hz to be available. The low-frequency limit is 100Hz for many low-power speakers, so going below this cut-off frequency may be unnecessary.

For 80hm speakers, we recommend using either 220uF series capacitors for a cut-off frequency of approximately 90Hz or 470uF for 42Hz respectively (minimum 6.3V rated in both cases).





Figure 3. Verdin Development Board – connection of the external speakers in a stereo setup, with external series capacitors



Errata #7: HAR-8016 – CSI_1_MCLK Voltage Level is not 3.3V

Affected Version:	Verdin Development Board V1.0B
	Verdin Development Board V1.1A

Fixed in: TBD

7.1 Customer impact

If a MIPI CSI-2 camera requires the CSI_1_MCLK signal (pin #12 of X47), and if it requires this signal to be at 3.3V level, then the current voltage level of the signal won't be compatible with the camera.

7.2 Description

On the MIPI CSI-2 interface used on the Verdin Development Board V1.1A, all single-ended signals are at 3.3V level, except for the CSI_1_MCLK signal (pin #12 of X47), which is at 1.8V level.

7.3 Workaround

In case a MIPI CSI-2 camera requires the CSI_1_MCLK signal (pin #12 of X47), and in case it requires this signal to be at 3.3V level, it could be level shifted on custom carrier boards.



Errata #8:	HAR-8290 – The LED status signals of the on-module Ethernet PHY are swapped	
Affected Versio	on:	Verdin Development Board V1.0B Verdin Development Board V1.1A

Fixed in: TBD

8.1 Customer impact

The roles of the Ethernet link and activity LEDs are swapped (the wrong Ethernet LED is turned on or is blinking).

8.2 Description

The KSZ9131 Ethernet PHY on the Verdin modules has two LED outputs (ETH_1_LED_1 and ETH_1_LED_2) used to indicate the link and activity statuses on the bus. These LEDs are available on pin 235 and 237 of the module edge connector, respectively. ETH_1_LED_1 (pin 235) is intended to indicate the activity status, while ETH_1_LED_2 (pin 237) is intended to indicate the link status.

On the PCB versions 1.0 and 1.1, these two signals are swapped. In the next revision of the carrier board PCB, the connections will be corrected. In the Verdin Development Board datasheet, the corrected connections are shown.

8.3 Workaround

For custom carrier board designs, the correct LED connections should be implemented. A potential workaround could be flipping the roles and behavior of the LED outputs of the onmodule Ethernet PHY in software. However, this is not supported by the related driver.



Errata #9:	HAR-8342 – Stitching Capacitors Influence Verdin iMX8M Plus
	Bluetooth Config Strapping

Affected Version:	Verdin Development Board V1.0B Verdin Development Board V1.1A
Fixed in:	Verdin Development Board V1.1B

9.1 Customer impact

The Bluetooth solution of the Wi-Fi/Bluetooth-equipped Verdin iMX8M Plus SoM is not accessible by the system as the host interface strapping signal of the Bluetooth solution is unintentionally influenced by two stitching capacitors on the carrier board. This leaves the Bluetooth solution in the UART interface mode instead of SDIO.

9.2 Description

The signal used for strapping the HCI (Host Controller Interface) configuration of the Bluetooth solution at the time of powering up a Verdin iMX8M Plus SoM is also available on the Module-specific pin MSP_8 (#104) of the SoM edge connector. Module-specific pins feature stitching capacitors for providing current return paths for cases when those pins are being used for accommodating high-speed signals.

The Verdin Development Board V1.1A features two such capacitors (C250, C313) on the MSP_8 signal. During powering up the system, the stitching capacitors delay the transition of the related signal to the intended state and thus result in a wrong configuration being strapped. Instead of SDIO mode, the host interface of the Bluetooth solution gets configured to UART mode. As a result, the Bluetooth solution is not accessible by the system.

The strapping of the Wi-Fi/Bluetooth module of the Verdin iMX8M Mini SoM is not affected by the stitching capacitors on MSP_8. The Verdin iMX8M Mini provides the strapping pin on the MSP_25, which does not feature strapping capacitors.

9.3 Workaround

Remove the stitching capacitors C250 and C313 from the carrier board. This makes the Bluetooth interface work in case the carrier board is connected to a Verdin iMX8M Plus SoM with a hardware version of V1.0C or newer.





Figure 4. Location of C250 and C313 (top side)

If the carrier board is connected to a Verdin iMX8M Plus V1.0B, another stitching capacitor needs to be removed from the SoM. For more information, please refer to HAR-8341 in the Verdin iMX8M Plus errata. The issue will be resolved in future HW versions of these products.



Errata #10: HAR-8426 – Signal distortion on the audio codec's "Line In" input

Affected Version:	Verdin Development Board V1.0B
Fixed in:	Verdin Development Board V1.1A

10.1 Customer impact

The audio signals from the "Line In" input (connector X21) are distorted and the amplitudes of the signals are smaller than intended. There is crosstalk from the "Line In" input (connector X21) to the "Mic In" input (connector X22).

10.2 Description

The 10k pull-down resistors R135 and R138 connected to the pins 26 and 24 of the audio codec (IC28) affect the functionality of the device's internal multiplexers and signal amplifiers. The analog input pins of the audio codec shift the input DC offset to their internal virtual ground VMID. The external pull-down resistors are affecting this DC offset, causing the opening of the internal multiplexer's analog signal switches and the saturation of the amplifier's outputs. This leads to the distortion of the "Line In" signals (only the positive polarity parts of the input signals are recorded) and crosstalk from the "Line In" input to the "Mic In" input.

10.3 Workaround

Remove the pull-down resistors R135 and R138 from the carrier board. This makes the audio codec's "Line In" and "Mic In" inputs work properly.



Figure 5. Location of R135 and R138 (top side)



Errata #11: HAR-8833 – The carrier board turns off or resets when a cable is connected to the USB-C FTDI debug connector

Affected Version:	Verdin Development Board V1.0B Verdin Development Board V1.1A Verdin Development Board V1.1B
Fixed in:	Verdin Development Board V1.1C

11.1 Customer impact

The module may reset or turn off, or the carrier board may turn off when a cable is being connected to the USB-C connector of the FTDI debug port while the board is turned on.

11.2 Description

Due to a race condition between the pull-up voltage at the gates of the transistor level shifters, the DBG_PWR_BTN#, DBG_FORCE_OFF#, DBG_RESET#, DBG_RECOVERY#, and the FTDI_JTAG_TRST# signals can get unintentionally triggered when connecting a cable to the USB-C connector of the FTDI debug port. This may reset or shut down the module or shut down the power rails of the carrier board.

11.3 Workaround

Connect the cable to the USB-C connector of the FTDI debug port before powering on the carrier board.

As an alternative solution, the resistors R165, R168, R172, R175, and R319 can be replaced with resistors having a resistance of 1MOhm. This slows down the transistor level shifter circuits and makes sure that the power control signals are not triggered when connecting the cable to the USB-C connector of the FTDI debug port. The same improvement is going to be implemented in future versions of the product.





Figure 6. Location of R165, R168, R172, and R175 (top side)



Figure 7. Location of R319 (top side)



Errata #12: HAR-8934 – The RC element on the PCIe reset signal contributes to violating the PCIe specification

Affected Version:	Verdin Development Board V1.0B Verdin Development Board V1.1A Verdin Development Board V1.1B
Fixed in:	Verdin Development Board V1.1C

12.1 Customer impact

PCIe devices connected to the PCIe interface of the carrier board may not get detected properly or malfunction.

12.2 Description

According to the PCIe specifications, software needs to wait a minimum of 100ms before sending a configuration request to a PCIe device after enabling the power and the clock.

The Verdin specification provides a dedicated reset signal for the PCIe interface (PCIE_1_RESET#). The Verdin Development Board features an RC delay circuit on this signal. This circuit consists of a 10uF capacitor and a 10kOhm pull-up resistor, resulting in a time constant of 100ms. The actual time it takes for the device to get out of the reset state is influenced by the threshold level of the device's reset input and component tolerances as well.

These factors together make the timing unpredictable. Consequently, a PCIe device may still be in the reset state when the driver is sending the first configuration requests. The issue does not necessarily manifest in the case of all potential PCIe devices and can be temperature-dependent as well.

12.3 Workaround

By eliminating the RC delay circuit from the reset signal, the module's reset timing can be fully controlled by the PCI_1_RESET# signal. To achieve that, remove the 10uF capacitor C173. The change prevents the described issue from happening. The change is going to be implemented in future versions of the product.

Alternatively, the delay between releasing the reset and initiating the configuration requests can be increased in the driver. However, this is not the preferred method as this requires modifications to be done to the standard drivers.





Figure 8. Location of C173 (top side)



Errata #13: HAR-8976 – The silkscreen of X53 power indication LEDs is not correct

Affected Version: Verdin Development Board V1.1A Verdin Development Board V1.1B Verdin Development Board V1.1C Verdin Development Board V1.1D

Fixed in: Verdin Development Board V1.1E

13.1 Customer impact

One needs to pay attention when checking the power status LEDs (LED4, LED5) of the upper and lower ports of the dual stacked USB host connector (X53) as the silkscreen indication is misleading.

13.2 Description

For the dual stacked USB host connector (X53), the assignments of the upper and lower ports and the related power status indication LEDs are swapped. LED5 is indicating the power status of the lower port, while LED4 is indicating the power status of the upper port. The silkscreen is going to be updated in a future product version.

13.3 Workaround

There is no workaround to the issue.



Errata #14: HAR-9004 – Overvoltage protection triggered when hot plugin Verdin Development Board V1.1A

Affected Version:	Verdin Development Board V1.1A Verdin Development Board V1.1B
Fixed in:	Verdin Development Board V1.1C Verdin Development Board V1.1F

14.1 Customer impact

Hot plugging a 26.4V power supply to the carrier board may trigger the protection IC (IC25) and prevent the product from powering up.

14.2 Description

The carrier board features a protection IC (IC25) that protects the product from various powerrelated error scenarios, namely: overvoltage, overcurrent, undervoltage, reverse polarity. In case a power supply providing a voltage near the high threshold of the input voltage range (26.4V) gets hot-plugged to the carrier board, ringing may form at the input of the protection device. The energy is bouncing between the low-ESR capacitors C98 and the capacitors on the switched side (C106, C107, C174). This may trigger the overcurrent protection, causing the board to not power up. In this case, the protection IC's fault indication LED (LED17) is going to blink to indicate the fault condition.

14.3 Workaround

Unsoldering the capacitor C98 will improve the power hot-plug capability of the product. The issue is going to be resolved in newer versions of the product.



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