Preliminary – Subject to Change

Toradex
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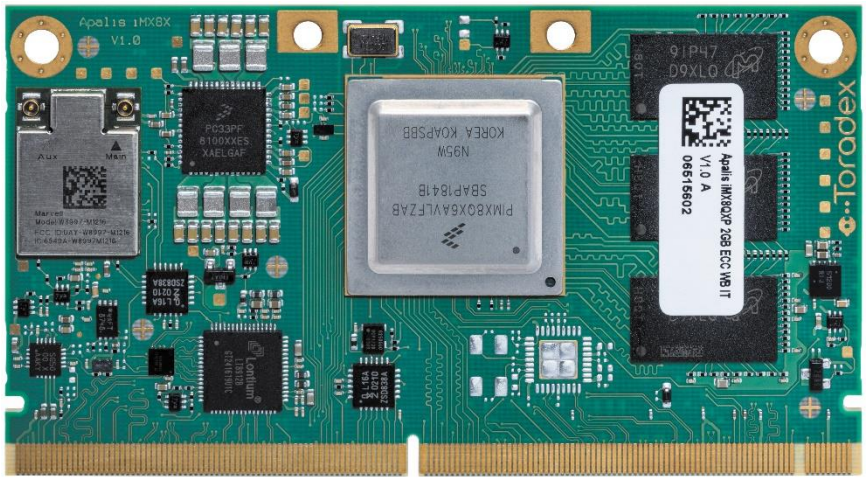
Apalis iMX8X

Datasheet



Revision History

Date	Doc. Rev.	Apalis iMX8X Version	Changes
11-Oct-2019	Rev. 0.9	V1.0	Initial Release
19-Dec-2019	Rev. 1.0	V1.1	Section 5.4: Add USB VBUS information Minor changes
07-Jan-2020	Rev. 1.1	V1.1	Section 5.4: Correction of USB VBUS information Section 8.6: Update temperature range of non-IT modules
12-Mar-2020	Rev. 1.2	V1.1	Section 1.2.1: Update SoC part numbers Section 8.6: Clarification and correction of thermal specifications Minor changes
23-Apr-2020	Rev 1.3	V1.1	Minor cosmetic improvements
07-Jul-2020	Rev. 1.4	V1.1	Sections 1.1 and 1.2.1: HiFi 4 DSP functionality has been removed from the document as it will not be supported anymore by this product
30-Sep-2020	Rev. 1.5	V1.1	Section 8.5.1: Update the MXM3 connector
19-Jan-2021	Rev. 1.6	V1.1	Section 5.22: Change ADC input resistor from 10kΩ to 1kΩ
25-Jan-2021	Rev. 1.7	V1.1	Section 1.2.1: Update SoC part number Section 1.2.1: Correction of maximum M4 core frequency Section 1.2.2: Update eMMC Flash size Update Figure 5 and Figure 6 Minor changes
18-May-2021	Rev. 1.8	V1.1	Section 4.3: Clarify reset state Section 4.4: Update reset state of pin 209 and 262 Section 5.3: Update default IO voltage of RGMII signals Section 5.25: Add support for CAN-FD Section 8.3: Rename Section and clarify module power consumption Minor changes

Contents

1. Introduction

1.1 Hardware

The Apalis iMX8X is a computer module based on the NXP® i.MX 8X family of embedded System on Chips (SoCs). The i.MX 8X family consists of the i.MX 8QuadXPlus, i.MX 8DualXPlus, and i.MX 8DualX. The top-tier i.MX 8QuadXPlus (i.MX 8QXP) features four Cortex-A35 cores as the central processor cluster. The Cortex-A35 is currently Arm's most efficient Armv8 core. They provide full 64-bit Armv8-A support while maintaining seamless backward compatibility with 32-bit Armv7-A software. The main cores run with up to 1.2 GHz.

In addition to the main CPU complex, the i.MX 8QXP features a Cortex-M4F processor, which peaks up to 266 MHz. This processor is independent of the main complex and features its dedicated interfaces while it can also access the regular interfaces. This heterogeneous multicore system allows for running additional real-time operating systems on the M4 cores for time- and security-critical tasks. The i.MX 8QXP features a System Controller Unit (SCU), which runs on an additional independent Cortex-M4 processor. A primary task of this controller is resource management with proper access and permission control to make sure the M4 core and main CPU complex are isolated from each other. This massively increases the safety of the heterogeneous multicore system in comparison with older SoCs.

The Apalis iMX8X has a strong focus on safety. The module is available with error-correcting code memory (ECC memory) based on a 40-bit wide DDR3L SDRAM interface.

The i.MX 8QXP features a powerful GC7000Lite Graphics Processing Unit (GPU) from Vivante®. The GPU provides 16 Vega shader cores with tessellation, geometry, and compute shaders. The GPU can peak with up to 64 GFLOPS and supports OpenGL® 3.0, OpenGL® ES3.1, DirectX® 11, and Vulkan.

The Apalis iMX8X incorporates DVFS (Dynamic Voltage and Frequency Switching) and thermal throttling, enabling the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption.

The Apalis iMX8X is also available as a version with a Dual-Band (2.4/5 GHz) Wi-Fi ac/a/b/g/n and Bluetooth 5/BLE interface. The Wi-Fi module features MHF4 compatible connectors for external antennas. The module is pre-certified for FCC (US), CE (Europa), and IC (Canada).

The module targets a wide range of applications, including audio, voice, video, and safety-critical; automotive: infotainment, instrument cluster, head unit, heads-up display (HUD), rear-seat entertainment and full digital electronic cockpit (eCockpit); home/building automation; Digital Signage; Industrial Automation, Data Acquisition, Thin Clients, Robotics, and much more.

It offers a wide range of interfaces from simple GPIOs, industry-standard I2C, SPI, CAN, and UART buses to SuperSpeed USB 3.1 Gen 1 and PCI Express interfaces. The Apalis iMX8X module features a Gigabit Ethernet PHY with IEEE1588 support on the module. Additionally, the module allows connecting an additional (Gigabit) Ethernet PHY on the customer carrier board using the RGMII or RMII interface.

The Apalis iMX8X module encapsulates the complexity of the modern-day electronic design, such as high-speed impedance-controlled layouts with high component density utilizing blind and buried via technology. This allows the customer to create a carrier board that implements the application-specific electronics, which is generally much less complicated. The Apalis iMX8X module takes this one step further and implements an interface pinout which allows direct connection of real-world I/O ports without needing to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move

toward high-speed, serial technologies that use impedance-controlled differential pairs. It allows them to easily route such interfaces to standard connectors in a simple, robust fashion.

1.2 Main Features

1.2.1 CPU

	Apalis iMX8DXP 1GB	Apalis iMX8QXP 2GB ECC IT	Apalis iMX8QXP 2GB WB IT
i.MX 8X Family SoC	MIMX8DX5CVLFZAx	MIMX8QX5CVLFZAx	MIMX8QX5CVLFZAx
Arm Cortex-A35 CPU Cores	2	4	4
Arm Cortex-M4F CPU Cores	1	1	1
L1 Instruction Cache (each core)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)
L1 Data Cache (each core)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)
L2 Cache (shared by all A35 cores)	512 KByte (A35)	512 KByte (A35)	512 KByte (A35)
Tightly-Coupled Memory	256 KByte (M4)	256 KByte (M4)	256 KByte (M4)
Maximum CPU frequency	1.2 GHz (A35) 264 MHz (M4)	1.2 GHz (A35) 264 MHz (M4)	1.2 GHz (A35) 264 MHz (M4)
NEON MPE	✓	✓	✓
Arm TrustZone	✓	✓	✓
Advanced High Assurance Boot	✓	✓	✓
Cryptographic Acceleration and Assurance Module	✓	✓	✓
Secure Real-Time Clock	✓	✓	✓
Secure JTAG Controller	✓	✓	✓
Secure Non-Volatile Storage	✓	✓	✓

1.2.2 Memory

	Apalis iMX8DXP 1GB	Apalis iMX8QXP 2GB ECC IT	Apalis iMX8QXP 2GB WB IT
DDR3L RAM Size	1 GByte	2 GByte	2 GByte
DDR3L RAM Speed	1866 MT/s	1866 MT/s	1866 MT/s
DDR3L ECC	-	✓	-
DDR3L RAM Memory Width	1x32-bit	1x40 bit (8-bit ECC)	1x32 bit
eMMC NAND Flash (8-bit)* V5.0	8 GByte	16 GByte	16 GByte

*eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear-leveling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.2.3 Interfaces

	Apalis iMX8DXP 1GB	Apalis iMX8QXP 2GB ECC IT	Apalis iMX8QXP 2GB WB IT
Wi-Fi IEEE 802.11 ac/a/b/g/n Dual-Band (2.4/5 GHz)	-	-	1
Bluetooth 5/BLE	-	-	1
LCD RGB (720p60)	1 (up to 18-bit)	1 (up to 18-bit)	1 (up to 18-bit)
LVDS (2x single channel 85 Mpxiel/s or 1x dual channel 165 Mpixel/s)	1	1	1
HDMI 1.4 (max 1080p60)	1	-	1
VGA Analog Video	-	-	-
MIPI DSI	2x 4 Data Lanes*	2x 4 Data Lanes*	2x 4 Data Lanes*
Resistive Touch Screen	4 Wire	4 Wire	4 Wire
Analogue Audio Headphone out	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Line in	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Mic-in	1 (Mono)	1 (Mono)	1 (Mono)
Medium Quality Sound (MQS)	1* (Stereo)	1* (Stereo)	1* (Stereo)
SAI (AC97/I^2S)	1+2* (2x only input)	1+2* (2x only input)	1+2* (2x only input)
ESAI (AC97/I^2S)	1*	1*	1*
S/PDIF	1* in / 1* out	1* in / 1* out	1* in / 1* out
Parallel Camera Interface	1	1	1
MIPI CSI-2	1x 4 data lanes*	1x 4 data lanes*	1x 4 data lanes*
I^2C	3+5*	3+5*	3+5*
SPI	2+2*	2+2*	2+2*
QSPI	2*	2*	2*
UART	4+1*	4+1*	4+1*
SD/SDIO/MMC	1	1	1
GPIO	8+83*	8+83*	8+83*
USB 2.0 OTG (host/device)	1	1	1
USB 3.1 Gen 1 host [1)]	1	1+3*	1+2*

USB 2.0 host	3+1*	3+1*	3
PCIe (Gen 3.0)	1	1	1
Serial ATA	-	-	-
10/100/1000 MBit/s Ethernet	1	1	1
RGMII/RMII/MII interface for 2nd Ethernet PHY on Baseboard	1*	1*	1*
PWM	2+9*	2+9*	2+9*
Analog Inputs	4	4	4
CAN/CAN-FD	2+1*	2+1*	2+1*

*These interfaces are available on pins that are not defined as standard interfaces in the Apalis architecture. The pins are either located in the type-specific area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints.
[1)] The USB3.1 Gen 1 host column indicates only the additional SuperSpeed signals required for a USB3.1 Gen 1 interface. Each USB3.1 Gen 1 port also requires the signals of the USB2.0 host ports. Therefore, the maximum available USB host ports are determined by the available USB2.0 host ports.

1.2.4 Graphics Processing Unit

	Apalis iMX8DXP 1GB	Apalis iMX8QXP 2GB ECC IT	Apalis iMX8QXP 2GB WB IT
Vivante GC7000Lite GPU Units	1	1	1
Vega Shaders (per unit)	16	16	16
OpenGL® ES 3.2	-	-	-
OpenGL® ES 3.1, 3.0	✓	✓	✓
OpenGL 3.0, 2.1	✓	✓	✓
DirectX 11	✓	✓	✓
OpenVG 1.1	✓	✓	✓
DirectFB 1.4+	✓	✓	✓
GDI (Direct Draw)	✓	✓	✓
Vulkan 1.0 support	✓	✓	✓

1.2.5 HD Video Decode

- ✓ H.265 HEVC Main Profile 2160p30 Level 5.0
- ✓ H.264 AVC Constrained Baseline, Main and High profile 1080p60
- ✓ H.264 MVC
- ✓ WMV9/VC-1 Simple, Main, and Advanced Profile
- ✓ MPEG 1 and 2 Main Profile at High Level
- ✓ AVS Jizhun Profile (JP)
- ✓ MJPEG4.2 ASP, H263, Sorenson Spark
- ✓ Divx 3.11, with Global Motion Compensation (GMC)
- ✓ ON2/Google VP6/VP8
- ✓ RealVideo 8/9/10
- ✓ JPEG and MJPEG A/B Baseline

1.2.6 HD Video Encode

- ✓ H.264 (Baseline, Main, High Profile) 1080p30

1.2.7 Supported Operating Systems

- ✓ Embedded Linux
- ✓ For other operating systems, please contact Toradex

1.3 Interface Overview

The table in Figure 1 shows the interfaces supported on the Apalis® iMX8X module and whether an interface is provided on standard or type-specific pins. The CAN interface is an example of an interface that uses standard and alternate function pins. Two CAN interfaces are provided as part of the standard interface pinout. An additional CAN is available as an alternate function of the UART 2 RTS CTS signals. These functions on alternate pins can only be used if the primary function of the pin is not used. Check section 4.4 for a list of all alternate functions of the MXM3 pins. The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis iMX8X Module. The tool allows comparing the interfaces of different Apalis modules. More information on this tool can be found here: http://developer.toradex.com/knowledge-base/pinout-designer

Feature	Total	Standard	Type-Specific	Alternate Function
4 Wire Resistive Touch	4	4		
Analog Inputs	4	4		
Analog Audio (Line in/out, Mic in)	1	1		
Medium Quality Sound (MQS)	1			1
CAN/CAN-FD	3	2		1
CSI Ports	1		1	
DSI Ports	2			2
Single-Channel LVDS Display	2	2		
Dual-Channel LVDS Display (shared with the single-channel)	1	1		
Gigabit Ethernet	1	1		
RGMII/RMII (2nd Ethernet	1			1
GPIO	91	8		83
SAI (I^2S)	3	1		2
ESAI	1			1
HDMI (Video source shared with DSI/LVDS)	1*	1*		
eDP/DP				
I^2C	8	3		5
Parallel Camera	1	1		
Parallel LCD (max. 18-bit)	1	1		
PCI-Express (lane count)	1	1		
PWM	11	2		9
SATA				
SD/SDIO/MMC	1			
S/PDIF In	1			1
S/PDIF Out	1			1
SPI	4	2		2
QSPI	2			2
UART	5	4		1

USB 2.0 OTG (host/device)	1	1		
USB 3.1 Gen 1 host	4*	1	2*	1
USB 2.0 host	4*	3	1*	
VGA				

Figure 1: Apalis® iMX8X Module Interfaces

*These interfaces are not available on all the Apalis iMX8X module versions. Please compare the available interfaces in section 1.2.3 or use the Toradex Pinout Designer.

1.4 Reference Documents

1.4.1 NXP i.MX 8X

You will find the details about i.MX 8 SoC in the Datasheet and Reference Manual provided by NXP.
https://www.nxp.com/products/audio/smart-haptic-driver/i.mx-8x-family-arm-cortex-a35-3d-graphics-4k-video-dsp-error-correcting-code-on-ddr:i.MX8X

1.4.2 Ethernet Transceiver

Apalis iMX8X uses the Micrel KSZ9131RNX Gigabit Ethernet Transceiver (PHY).
https://www.microchip.com/wwwproducts/en/KSZ9131

1.4.3 Audio Codec

Apalis iMX8X uses the NXP SGTL5000 Audio Codec.
http://www.nxp.com/products/interface-and-connectivity/interface-and-system-management/switch-monitoring-ics/ultra-low-power-audio-codec:SGTL5000

1.4.4 Touch Screen Controller

Apalis iMX8X uses the Analog Device AD7879-1 Touchscreen Controller.
http://www.analog.com/en/products/analog-to-digital-converters/integrated-special-purpose-converters/capacitive-to-digital-and-touch-screen-controllers/ad7879.html

1.4.5 USB Hub

The Apalis iMX8X features the Microchip USB5744 USB 3.1 Gen 1 Hub.
https://www.microchip.com/wwwproducts/en/USB5744

1.4.6 HDMI Bridge

The Apalis iMX8X features Lontium Semiconductor LT8912B MIPI DSI to HDMI Bridge.
http://www.lontiumsemi.com/product/View_86.html

1.4.7 Wi-Fi and Bluetooth Module

Some of the Apalis iMX8X use the Azurewave AW-CM276NF wireless module. The AW-CM276NF datasheet is available under NDA from Toradex. Please contact your local sales team for more information.
https://developer.toradex.com/knowledge-base/azurewave-aw-cm276nf-wi-fi-bluetooth-module

1.4.8 Apalis Carrier Board Design Guide

This document provides additional information about the Apalis form factor. A custom carrier board should follow the Apalis Carrier Board Design Guide to make the board compatible within

the Apalis module family. Please study this document in detail before starting your carrier board design.
http://docs.toradex.com/101123-apalis-arm-carrier-board-design-guide.pdf

1.4.9 Layout Design Guide

This document contains information about high-speed layout design and additional information to get the carrier board layout the first time right.
http://docs.toradex.com/102492-layout-design-guide.pdf

1.4.10 Toradex Developer Center

You can find a lot of additional information in the Toradex Developer Center, which is updated with the latest product support information regularly.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Apalis iMX8.
http://www.developer.toradex.com

1.4.11 Apalis Carrier Board Schematics

We provide the completed schematics plus the Altium project file, including library symbols and IPC-7351 compliant footprints for the Apalis Evaluation Board and other carrier boards free of charge. This is of great help when designing your carrier board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.4.12 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparing the interfaces of different modules.
http://developer.toradex.com/knowledge-base/pinout-designer

1.5 Naming Conventions

The naming of i.MX 8X based products can be confusing. In this document, a consistent naming convention is used. The punctuation and spaces in the names are important to be noticed.

i.MX 8 Series	A series of different SoC families which consist of the i.MX 8, i.MX 8M, iMX 8M Mini, i.MX 8M Nano, as well as the i.MX 8X families. This document only contains information on the Apalis module, which uses an i.MX 8X family SoC. For information on other i.MX 8 Series based modules, please visit the Toradex website.
i.MX 8X	The NXP i.MX 8X SoC family, which consists of the i.MX 8QXP, i.MX 8DXP, and i.MX 8DX. Whenever this document uses the term i.MX 8X, all versions of the i.MX 8X SoC family is meant.
i.MX 8QuadXPlus	The top-tier SoC of the i.MX 8X family. It features a quad-core Cortex-A35 main CPU
i.MX 8QXP	Short name for the i.MX 8QuadXPlus
i.MX 8DualXPlus	Dual-core SoC of the iMX 8X family
i.MX 8DXP	Short name for the i.MX 8DualXPlus
i.MX 8DualX	Dual-core SoC of the iMX 8X family with a reduced feature set compared to the i.MX 8DXP
i.MX 8DX	Short name for the i.MX 8DualX

Apalis iMX8X	Apalis module based on the i.MX 8X family SoC. Whenever this document uses the term Apalis iMX8X, all versions of the Apalis iMX8X are meant. Please do not confuse it with the Apalis iMX8, a module based on the i.MX 8 Family processors (e.g., i.MX 8QM).
Apalis iMX8QXP	Apalis module based on the i.MX 8QXP processor. This term means both SKUs, the Apalis iMX8QXP 2GB ECC IT as well as the Apalis iMX8QXP 2GB WB IT
Apalis iMX8QXP 2GB ECC IT	Apalis module based on the i.MX 8QXP processor with 2GB ECC memory and IT temperature range
Apalis iMX8QXP 2GB WB IT	Apalis module based on the i.MX 8QXP processor with 2GB non-ECC memory, Wi-Fi/Bluetooth, and IT temperature range
Apalis iMX8DXP	Apalis module based on the i.MX 8DXP processor. This term means the Apalis iMX8DXP 1GB module
Apalis iMX8DXP 1GB	Apalis module based on the i.MX 8DXP processor with 1GB non-ECC memory and commercial temperature range

1.6 Build to Order Options

The Apalis iMX8X module is available in different variants (see section 1.2). Besides these stock-keeping units (SKU), it is possible to get customized versions of the module. These versions are built to order (BTO). This means the lead time is higher since they are not on stock. Additional setup costs may apply for such versions. Please get in touch with your local Toradex sales team to discuss a BTO version of the Apalis iMX8X module. The following customization options are available for the Apalis iMX8X:

- Different SoC: i.MX8QXP, i.MX8DXP, i.MX8DX
- RAM size (with or without ECC)
- eMMC size
- Industrial or commercial temperature range
- With or without Wi-Fi and Bluetooth module
- Without on-module audio codec.
    - The I2S interface can be routed to the analog audio interface pins on the edge connector (Pin 310, 312, 316, and 318)
    - The I2S interface can be routed to the Bluetooth module for Bluetooth audio.
- Without the resistive touch controller
- Without the on-module Ethernet PHY. The RGMII interface signals can be made available on the type-specific pins of the module edge connector. This allows having both RGMII interfaces available on the module edge connector for dual Ethernet PHYs on the carrier board.
- Without DSI to HDMI bridge
- PF8200 PMIC as a replacement of the PF8100 for additional safety features
- Making the PMIC FSOB (safety output) signal available on module edge connector pin 216 (VGA1_VSYNC)
- Additional secondary PCAL6416A 16-bit I²C GPIO expander. This allows having GPIO function (for backward compatibility with other modules) on the pins 176, 178, 180, 184, 186, 188, 190, 249, 251, 253, 263, 269, 271, 287, 289, and 291.
- Additional on-module I²C EEPROM

- USB Configurations
  - No USB hub: Only possible on modules without Wi-Fi, 1x OTG + 1x USB 3.1 Gen 1Host available
  - USB 2.0 Hub: For modules with Wi-Fi, the maximum throughput is reduced due to the USB 2.0 connection to the Wi-Fi module.
  - USB 3.1 Gen 1 Hub: Up to four USB 3.1 Gen 1 host interfaces available on the module edge connector

2. Architecture Overview

2.1 Apalis iMX8QXP 2GB WB IT Block Diagram

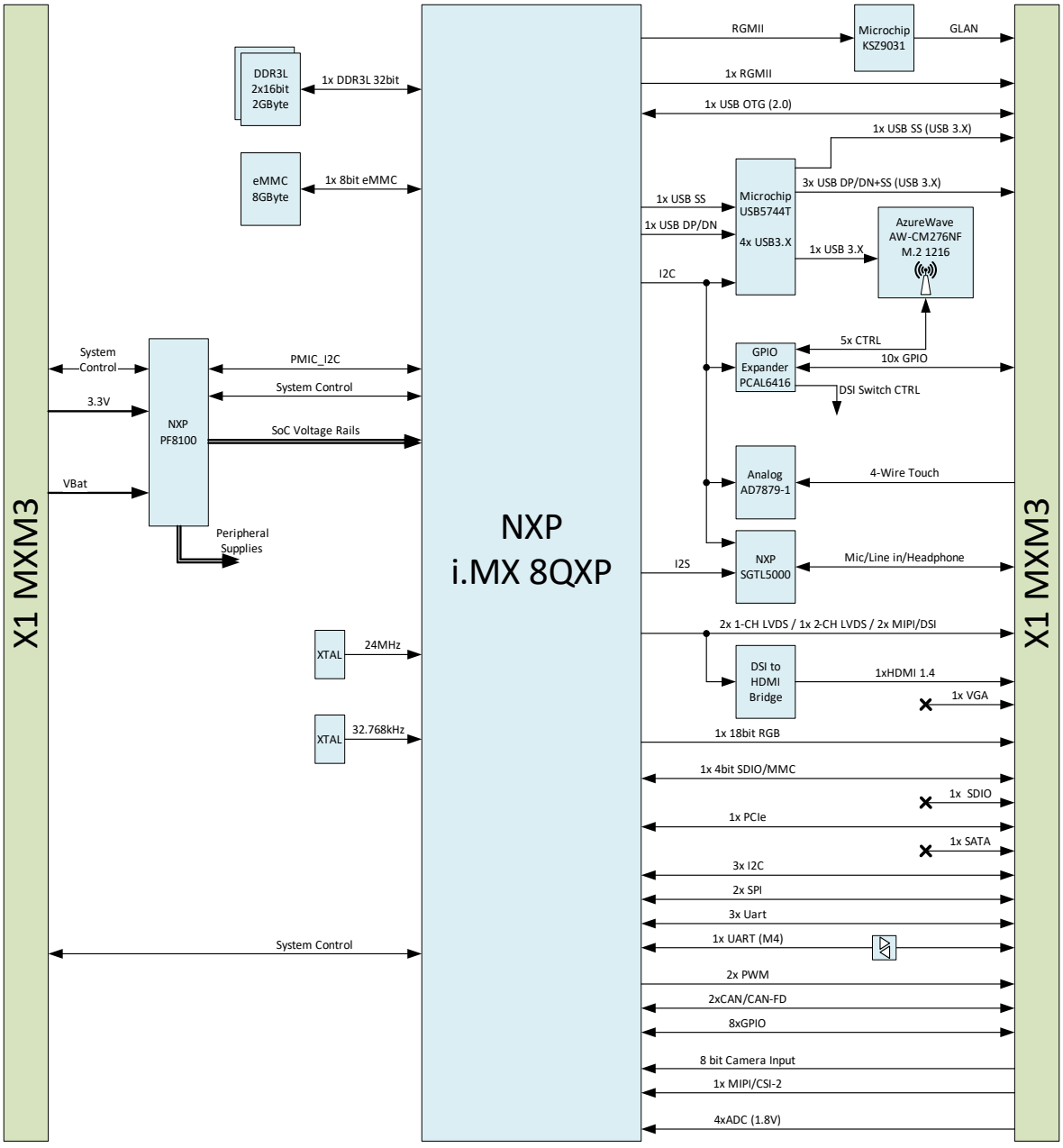


Figure 2 Apalis iMX8QXP 2GB WB IT Block Diagram

2.2 Apalis iMX8QXP 2GB ECC IT Block Diagram

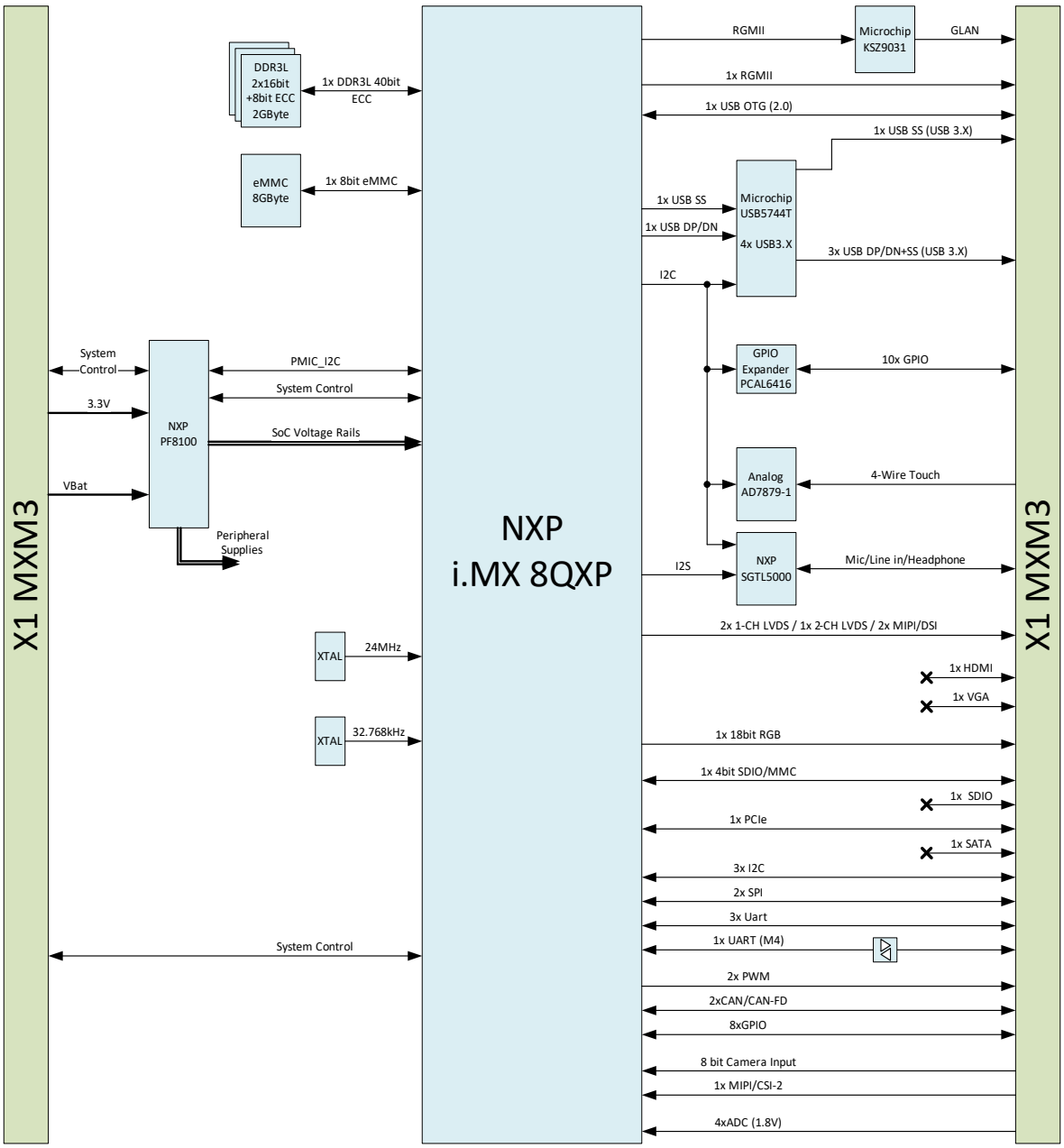


Figure 3 Apalis iMX8QXP 2GB ECC IT Block Diagram

2.3 Apalis iMX8DXP 1GB Block Diagram

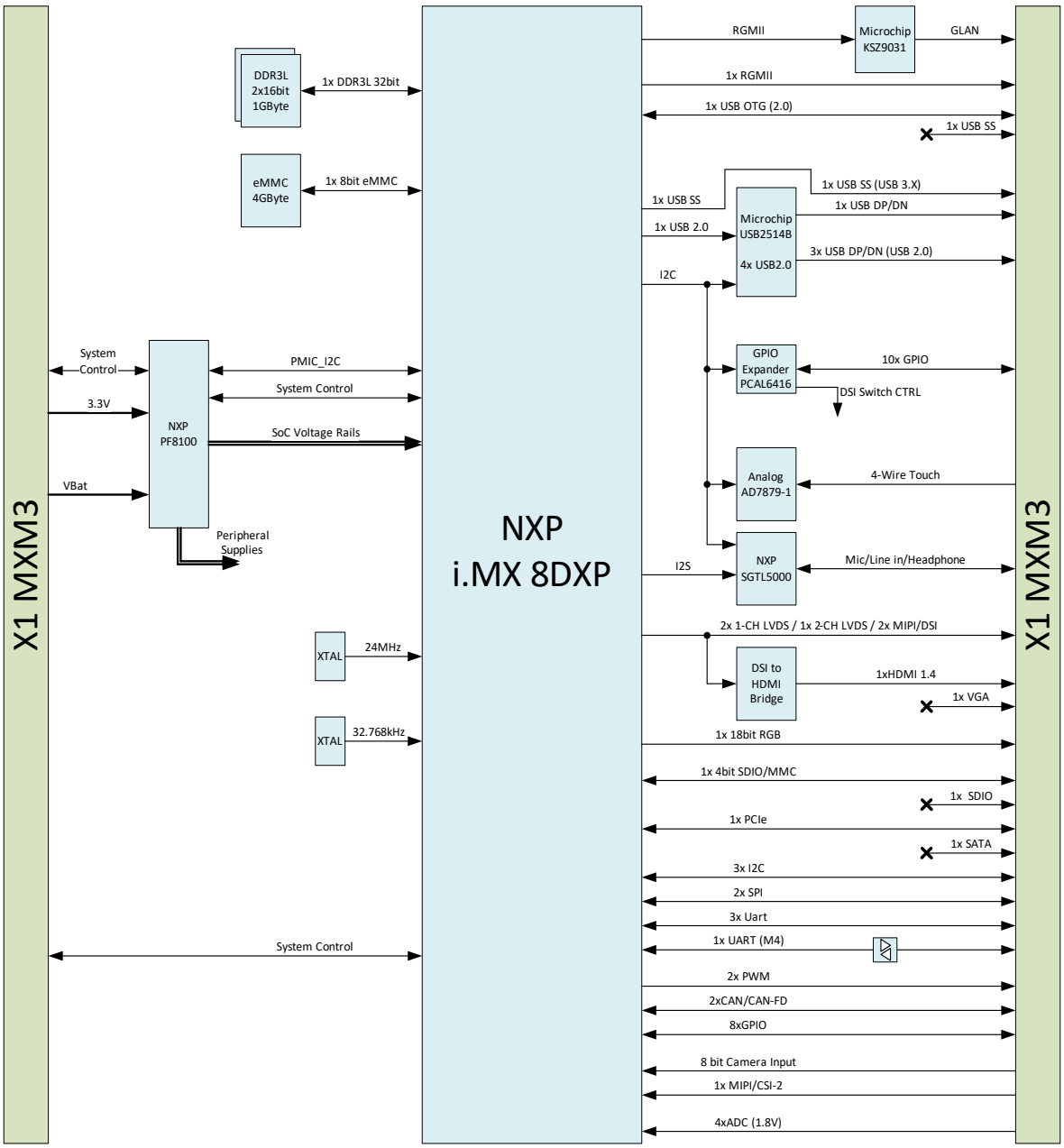


Figure 4 Apalis iMX8DXP 1GB Block Diagram

3. Apalis iMX8X Connector

3.1 Pin Numbering

The diagrams in Figure 5 and Figure 6 show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema. Pins on the top side of the module have even numbers, and pins on the bottom side have odd numbers.

The pin number increases linearly as a multiple of the pitch – that is, pins that are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins that do not exist due to the connector notch are also accounted for (pins 166 through 172).

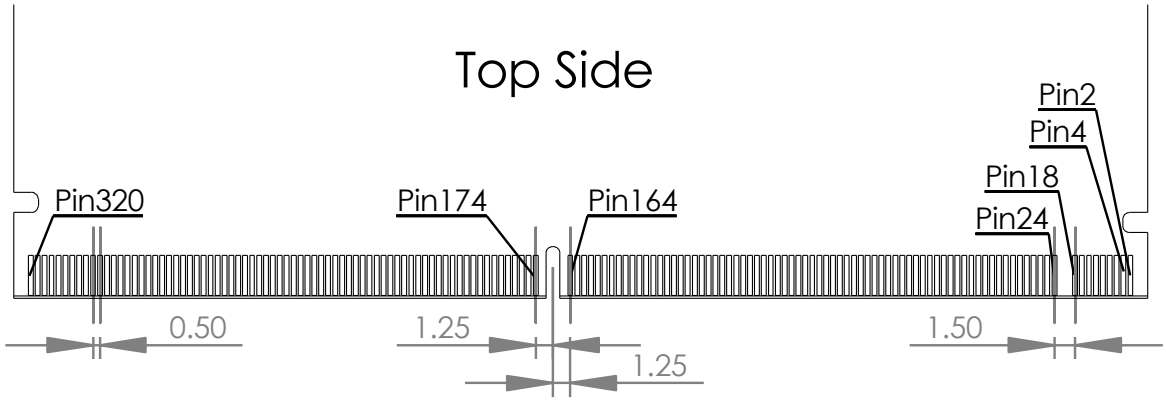


Figure 5: Pin numbering schema on the top side of the module

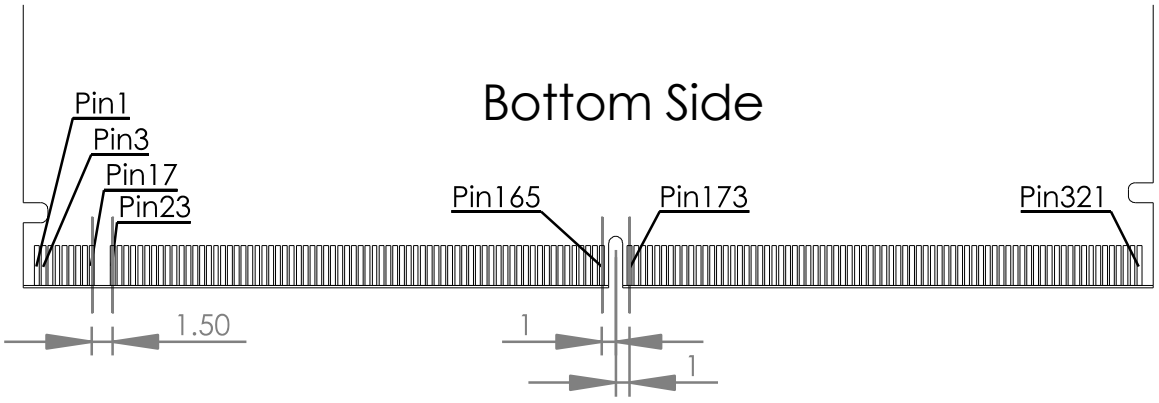


Figure 6: Pin numbering schema on the bottom side of the module

3.2 Assignment

The following table describes the MXM3 connector pinout. Some pins are shaded dark grey as type-specific interfaces. These pins might not be compatible with other modules in the Apalis family. Please be aware that you might lose compatibility with other Apalis modules on your carrier board if you make use of these interfaces. It should be noted that type-specific interfaces will be kept common across modules that share such interfaces wherever possible. For example, if both modules A and module B have a four-lane MIPI CSI-2 interface available in the same configurations as a type-specific interface, they shall be assigned to the same pins in the type-

specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type-specific interface.

- X1: Pin number on the MXM3 module edge connector (X1).
- Apalis Signal Name: The name of the signal according to the Apalis form factor definition. This name corresponds to the default usage of the pin. Some of the pins also have an alternate function, but to be compatible with other Apalis modules, only the default function should be used, and the carrier board should be implemented according to the Apalis Carrier Board Design Guide.
- iMX8X Ball Name: The name of the pin of the i.MX 8X SoC.

Table 3-1 X1 Connector

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
1	GPIO1	QSPI0B_DATA3		
3	GPIO2	QSPI0B_DQS		
5	GPIO3	QSPI0B_SS0_B		
7	GPIO4	QSPI0B_SS1_B		
9	GND		GND	
11	GPIO5	QSPI0B_SCLK		
13	GPIO6	QSPI0B_DATA0		
15	GPIO7	QSPI0B_DATA1		
17	GPIO8	QSPI0B_DATA2		
23	GND		GND	
25	SATA1_RX+			no connection
27	SATA1_RX-			no connection
29	GND		GND	
31	SATA1_TX-			no connection
33	SATA1_TX+			no connection
35	SATA1_ACT#	MIPI_DSI0_I2C0_SCL		
37	WAKE1_MICO	MIPI_DSI0_I2C0_SDA		
39	GND		GND	
41	PCIE1_RX-	PCIE0_RX0_N		
43	PCIE1_RX+	PCIE0_RX0_P		
45	GND		GND	
47	PCIE1_TX-	PCIE0_TX0_N		
49	PCIE1_TX+	PCIE0_TX0_P		
51	GND		GND	
53	PCIE1_CLK-	PCIE_REFCLK100M_N		50Ω termination on the module
55	PCIE1_CLK+	PCIE_REFCLK100M_P		50Ω termination on the module
57	GND		GND	
59	TS_DIFF1-	ENET0_MDIO		Signal is shared with internal Ethernet PHY
61	TS_DIFF1+	ENET0_MDC		Signal is shared with internal Ethernet PHY
63	TS_1		Recovery circuit	Can be kept floating for regular boot
65	TS_DIFF2-			no connection
67	TS_DIFF2+			no connection
69	GND		GND	

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
71	TS_DIFF3-			no connection
73	TS_DIFF3+			no connection
75	GND		GND	
77	TS_DIFF4-			no connection
79	TS_DIFF4+			no connection
81	GND		GND	
83	TS_DIFF5-		USB5744 USBRXM_DN2	**Not Available on Apalis iMX8DXP 1GB**
85	TS_DIFF5+		USB5744 USBRXP_DN2	
87	TS_2		CONFIG_HOST[0]	AW-CM276NF Pin 8, **Only on module with Wi-Fi, Maximum voltage 1.8V**, leave unconnected
89	TS_DIFF6-		USB5744 USBTXM_DN2	**Not Available on Apalis iMX8DXP 1GB**
91	TS_DIFF6+		USB5744 USBTXP_DN2	
93	GND		GND	
95	TS_DIFF7-		USB5744 USBRXM_DN1 [2]	**Only available on Apalis iMX8QXP 2GB ECC IT**
97	TS_DIFF7+		USB5744 USBRXP_DN1 [2]	
99	TS_3		CONFIG_HOST[1]	AW-CM276NF Pin 8, **Only on module with Wi-Fi, Maximum voltage 1.8V,** leave unconnected
101	TS_DIFF8-		USB5744 USBTXM_DN1 [2]	**Only available on Apalis iMX8QXP 2GB ECC IT**
103	TS_DIFF8+		USB5744 USBTXP_DN1 [2]	
105	GND		GND	
107	TS_DIFF9-		USB5744 USBDM_DN1 [2] [4]	**Not available on Apalis iMX8QXP 2GB WB IT**
109	TS_DIFF9+		USB5744 USBDP_DN1 [2] [4]	
111	GND		GND	
113	TS_DIFF10-			no connection
115	TS_DIFF10+			no connection
117	GND		GND	
119	TS_DIFF11-			no connection
121	TS_DIFF11+			no connection
123	TS_4		GPIO[8]/ UART_SOUT	AW-CM276NF Pin 55, **Only on module with Wi-Fi**
125	TS_DIFF12-			no connection
127	TS_DIFF12+			no connection
129	GND		GND	
131	TS_DIFF13-			no connection
133	TS_DIFF13+		GPIO[9]/ UART_SIN	AW-CM276NF Pin 56, **Only on module with Wi-Fi**
135	TS_5		GPIO[2]/ WLAN_LED	AW-CM276NF Pin 64, **Only on module with Wi-Fi**
137	TS_DIFF14-	MIPI_CSI0_DATA3_N		
139	TS_DIFF14+	MIPI_CSI0_DATA3_P		
141	GND		GND	
143	TS_DIFF15-	MIPI_CSI0_DATA2_N		
145	TS_DIFF15+	MIPI_CSI0_DATA2_P		
147	GND			
149	TS_DIFF16-	MIPI_CSI0_DATA1_N		
151	TS_DIFF16+	MIPI_CSI0_DATA1_P		

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
153	GND		GND	
155	TS_DIFF17-	MIPI_CSI0_DATA0_N		
157	TS_DIFF17+	MIPI_CSI0_DATA0_P		
159	TS_6		GPIO[3]/ BT_LED	AW-CM276NF Pin 65, **Only on module with Wi-Fi**
161	TS_DIFF18-	MIPI_CSI0_CLK_N		
163	TS_DIFF18+	MIPI_CSI0_CLK_P		
165	GND		GND	
173	CAM1_D7	CSI_D07		
175	CAM1_D6	CSI_D06		
177	CAM1_D5	CSI_D05		
179	CAM1_D4	CSI_D04		
181	CAM1_D3	CSI_D03		
183	CAM1_D2	CSI_D02		
185	CAM1_D1	CSI_D01		
187	CAM1_D0	CSI_D00		
189	GND		GND	
191	CAM1_PCLK	CSI_PCLK		
193	CAM1_MCLK	CSI_MCLK		
195	CAM1_VSYNC	CSI_VSYNC		
197	CAM1_HSYNC	CSI_HSYNC		
199	GND		GND	
201	I2C3_SDA (CAM)	CSI_RESET		
203	I2C3_SCL (CAM)	CSI_EN		
205	I2C2_SDA (DDC)	MIPI_DSI1_I2C0_SDA		
207	I2C2_SCL (DDC)	MIPI_DSI1_I2C0_SCL		
209	I2C1_SDA	USB_SS3_TC3		
211	I2C1_SCL	USB_SS3_TC0		
213	GND		GND	
215	SPDIF1_OUT		PCAL6416 (Addr 0x20) P0_2	GPIO expander, No SPDIF function
217	SPDIF1_IN		PCAL6416 (Addr 0x20) P0_1	GPIO expander, No SPDIF function
219	GND		GND	
221	SPI1_CLK	SPI0_SCK		
223	SPI1_MISO	SPI0_SDI		
225	SPI1_MOSI	SPI0_SDO		
227	SPI1_CS	SPI0_CS0		
229	SPI2_MISO	SPI2_SDI		
231	SPI2_MOSI	SPI2_SDO		
233	SPI2_CS	SPI2_CS0		
235	SPI2_CLK	SPI2_SCK		
237	GND		GND	
239	BKL1_PWM	MIPI_DSI1_GPIO0_00		
241	GND		GND	
243	LCD1_PCLK	MCLK_OUT0		
245	LCD1_VSYNC	MCLK_IN0		

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
247	LCD1_HSYNC	SPI3_CS0		
249	LCD1_DE	MCLK_IN1		No GPIO function on SoC Pin
251	LCD1_R0		1k pull-down resistor	
253	LCD1_R1		1k pull-down resistor	
255	LCD1_R2	SPDIF0_EXT_CLK [3)]		Configurable RGMII voltage
257	LCD1_R3	SPI3_SCK		
259	LCD1_R4	SPI3_SDO		
261	LCD1_R5	SPI3_SDI		
263	LCD1_R6	SPI3_CS1		No GPIO function on SoC Pin
265	LCD1_R7	UART1_CTS_B		
267	GND		GND	
269	LCD1_G0		1k pull-down resistor	
271	LCD1_G1		1k pull-down resistor	
273	LCD1_G2	ESAI0_TX2_RX3 [3)]		Configurable RGMII voltage
275	LCD1_G3	ESAI0_TX3_RX2 [3)]		Configurable RGMII voltage
277	LCD1_G4	ESAI0_TX4_RX1 [3)]		Configurable RGMII voltage
279	LCD1_G5	ESAI0_TX5_RX0 [3)]		Configurable RGMII voltage
281	LCD1_G6	SPDIF0_RX [3)]		Configurable RGMII voltage
283	LCD1_G7	SPDIF0_TX [3)]		Configurable RGMII voltage
285	GND		GND	
287	LCD1_B0		1k pull-down resistor	
289	LCD1_B1		1k pull-down resistor	
291	LCD1_B2	ESAI0_FSR [3)]		No GPIO function on SoC Pin
293	LCD1_B3	ESAI0_FST [3)]		Configurable RGMII voltage
295	LCD1_B4	ESAI0_SCKR [3)]		Configurable RGMII voltage
297	LCD1_B5	ESAI0_SCKT [3)]		Configurable RGMII voltage
299	LCD1_B6	ESAI0_TX0 [3)]		Configurable RGMII voltage
301	LCD1_B7	ESAI0_TX1 [3)]		Configurable RGMII voltage
303	AGND		AGND	
305	AN1_ADC0	ADC_IN0		**1.8V max**
307	AN1_ADC1	ADC_IN1		**1.8V max**
309	AN1_ADC2	ADC_IN4		**1.8V max**
311	AN1_TSWIP_ADC3	ADC_IN5		**1.8V max**
313	AGND		AGND	
315	AN1_TSPX		TSPX	AD7819 Ball A3 **(1.8V Level)**
317	AN1_TSMX		TSMX	AD7819 Ball C3 **(1.8V Level)**
319	AN1_TSPY		TSPY	AD7819 Ball B3 **(1.8V Level)**
321	AN1_TSMY		TSMY	AD7819 Ball D3 **(1.8V Level)**
2	PWM1	UART1_RTS_B	PCAL6416 (Addr 0x20) P1_0	Multiplexed (two pins), GPIO Expander
4	PWM2	MIPI_DSI0_GPIO0_00		
6	PWM3	MIPI_DSI0_GPIO0_01		No PWM function available
8	PWM4	MIPI_DSI1_GPIO0_01		No PWM function available
10	VCC		VCC	

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
12	CAN1_RX	FLEXCAN1_RX		
14	CAN1_TX	FLEXCAN1_TX		
16	CAN2_RX	FLEXCAN2_RX		
18	CAN2_TX	FLEXCAN2_TX		
24	POWER_ENABLE_MOCI		Power Management	
26	RESET_MOCI#		Power Management	Open Drain Signal
28	RESET_MICO#		Power Management	Open Drain Signal
30	VCC		VCC	
32	ETH1_MDI2+		TXRXP_C	KSZ9131 Pin 7
34	ETH1_MDI2-		TXRXM_C	KSZ9131 Pin 8
36	VCC		VCC	
38	ETH1_MDI3+		TXRXP_D	KSZ9131 Pin 10
40	ETH1_MDI3-		TXRXM_D	KSZ9131 Pin 11
42	ETH1_ACT		LED1	KSZ9131Pin17 (buffered)
44	ETH1_LINK		LED2	KSZ9131Pin15 (buffered)
46	ETH1_CTREF			no connection
48	ETH1_MDI0-		TXRXM_A	KSZ9131 Pin 3
50	ETH1_MDI0+		TXRXP_A	KSZ9131 Pin 2
52	VCC		VCC	
54	ETH1_MDI1-		TXRXM_B	KSZ9131 Pin6
56	ETH1_MDI1+		TXRXP_B	KSZ9131 Pin5
58	VCC		VCC	
60	USBO1_VBUS	USB_OTG1_VBUS		
62	USBO1_SSRX+		USB5744 USBRXP_DN3	SuperSpeed signals of USBH3 Port, not USBO1. **Not Available on Apalis iMX8DXP 1GB**
64	USBO1_SSRX-		USB5744 USBRXM_DN3	
66	VCC		VCC	
68	USBO1_SSTX+		USB5744 USBTXP_DN3	SuperSpeed signals of USBH3 Port, not USBO1. **Not Available on Apalis iMX8DXP 1GB**
70	USBO1_SSTX-		USB5744 USBTXM_DN3	
72	USBO1_ID	USB_OTG1_ID		
74	USBO1_D+	USB_OTG1_DP		
76	USBO1_D-	USB_OTG1_DN		
78	VCC		VCC	
80	USBH2_D+		USB5744 USBDP_DN2 [4]	
82	USBH2_D-		USB5744 USBDM_DN2 [4]	
84	USBH_EN	USB_SS3_TC1		
86	USBH3_D+		USB5744 USBDP_DN3 [4]	
88	USBH3_D-		USB5744 USBDM_DN3 [4]	
90	VCC		VCC	
92	USBH4_SSRX-		USB5744 USBRXM_DN4 [5]	
94	USBH4_SSRX+		USB5744 USBRXP_DN4 [5]	

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
96	USBH_OC#	QSPI0A_DATA0		
98	USBH4_D+		USB5744 USBDP_DN4 [4]	
100	USBH4_D-		USB5744 USBDM_DN4 [4]	
102	VCC		VCC	
104	USBH4_SSTX-		USB5744 USBTXM_DN4 [5]	
106	USBH4_SSTX+		USB5744 USBTXP_DN4 [5]	
108	VCC		VCC	
110	UART1_DTR		PCAL6416 (Addr 0x20) P0_7	GPIO Expander, No UART function on this pin
112	UART1_TXD	UART1_TX		
114	UART1_RTS	QSPI0A_DATA2		
116	UART1_CTS	QSPI0A_DATA3		
118	UART1_RXD	UART1_RX		
120	UART1_DSR		PCAL6416 (Addr 0x20) P0_6	GPIO Expander, No UART function on this pin
122	UART1_RI		PCAL6416 (Addr 0x20) P0_5	GPIO Expander, No UART function on this pin
124	UART1_DCD		PCAL6416 (Addr 0x20) P0_4	GPIO Expander, No UART function on this pin
126	UART2_TXD	UART0_TX		
128	UART2_RTS	FLEXCAN0_RX		
130	UART2_CTS	FLEXCAN0_TX		
132	UART2_RXD	UART0_RX		
134	UART3_TXD	UART2_TX		
136	UART3_RXD	UART2_RX		
138	UART4_TXD	SCU_GPIO0_01	PCAL6416 (Addr 0x20) P0_3	Bidirectional level shifter, GPIO Expander, No UART function on this pin
140	UART4_RXD	SCU_GPIO0_00		Bidirectional level shifter
142	GND		GND	
144	MMC1_D2	USDHC1_DATA2 [1]		Switchable output voltage
146	MMC1_D3	USDHC1_DATA3 [1]		Switchable output voltage
148	MMC1_D4	QSPI0A_DATA1		No MMC data signal available on this pin
150	MMC1_CMD	USDHC1_CMD [1]		Switchable output voltage
152	MMC1_D5	USDHC1_RESET_B		No MMC data signal available on this pin
154	MMC1_CLK	USDHC1_CLK [1]		Switchable output voltage
156	MMC1_D6	USDHC1_WP		No MMC data signal available on this pin
158	MMC1_D7	QSPI0A_SS0_B		No MMC data signal available on this pin
160	MMC1_D0	USDHC1_DATA0 [1]		Switchable output voltage
162	MMC1_D1	USDHC1_DATA1 [1]		Switchable output voltage
164	MMC1_CD#	USDHC1_CD_B		
174	VCC_BACKUP		RTC Battery input	
176	SD1_D2			no connection
178	SD1_D3			no connection
180	SD1_CMD			no connection
182	GND		GND	

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
184	SD1_CLK			no connection
186	SD1_D0			no connection
188	SD1_D1			no connection
190	SD1_CD#			no connection
192	GND		GND	
194	DAP1_MCLK	ADC_IN3		Output level shifter, Clock shared with on-module Audio Codec
196	DAP1_D_OUT	SAI0_TXD		
198	DAP1_RESET#	QSPI0A_SS1_B		
200	DAP1_BIT_CLK	SAI0_TXC		
202	DAP1_D_IN	SAI0_RXD		
204	DAP1_SYNC	SAI0_TXFS		
206	GND		GND	
208	VGA1_R			no connection
210	VGA1_G			no connection
212	VGA1_B			no connection
214	VGA1_HSYNC			no connection
216	VGA1_VSYNC			no connection
218	GND		GND	
220	HDMI1_CEC		PCAL6416 (Addr 0x20) P0_0	GPIO Expander, No CEC function on this pin
222	HDMI1_TXD2+		LT8912B HDMITX2_DP	Display source shared with LVDS1_B
224	HDMI1_TXD2-		LT8912B HDMITX2_DN	
226	GND		GND	
228	HDMI1_TXD1+		LT8912B HDMITX1_DP	Display source shared with LVDS1_B
230	HDMI1_TXD1-		LT8912B HDMITX1_DN	
232	HDMI1_HPD		LT8912B HPD / PCAL6416 (Addr 0x20) P1_7	Multiplexed (two pins), GPIO Expander
234	HDMI1_TXD0+		LT8912B HDMITX0_DP	Display source shared with LVDS1_B
236	HDMI1_TXD0-		LT8912B HDMITX0_DN	
238	GND		GND	
240	HDMI1_TXC+		LT8912B HDMITX_CKP	Display source shared with LVDS1_B
242	HDMI1_TXC-		LT8912B HDMITX_CKN	
244	GND		GND	
246	LVDS1_A_CLK-	MIPI_DSI0_CLK_N		
248	LVDS1_A_CLK+	MIPI_DSI0_CLK_P		
250	GND		GND	
252	LVDS1_A_TX0-	MIPI_DSI0_DATA0_N		
254	LVDS1_A_TX0+	MIPI_DSI0_DATA0_P		
256	GND		GND	
258	LVDS1_A_TX1-	MIPI_DSI0_DATA1_N		
260	LVDS1_A_TX1+	MIPI_DSI0_DATA1_P		
262	USBO1_OC#	USB_SS3_TC2		
264	LVDS1_A_TX2-	MIPI_DSI0_DATA2_N		
266	LVDS1_A_TX2+	MIPI_DSI0_DATA2_P		
268	GND		GND	

X1 Pin	Apalis Signal Name	i.MX 8X Ball Name	Non i.MX 8X Ball	Note
270	LVDS1_A_TX3-	MIPI_DSI0_DATA3_N		
272	LVDS1_A_TX3+	MIPI_DSI0_DATA3_P		
274	USBO1_EN	QSPI0A_SCLK		
276	LVDS1_B_CLK-	MIPI_DSI1_CLK_N		Display source shared with HDMI1
278	LVDS1_B_CLK+	MIPI_DSI1_CLK_P		
280	GND		GND	
282	LVDS1_B_TX0-	MIPI_DSI1_DATA0_N		Display source shared with HDMI1
284	LVDS1_B_TX0+	MIPI_DSI1_DATA0_P		
286	BKL1_ON	QSPI0A_DQS		
288	LVDS1_B_TX1-	MIPI_DSI1_DATA1_N		Display source shared with HDMI1
290	LVDS1_B_TX1+	MIPI_DSI1_DATA1_P		
292	GND		GND	
294	LVDS1_B_TX2-	MIPI_DSI1_DATA2_N		Display source shared with HDMI1
296	LVDS1_B_TX2+	MIPI_DSI1_DATA2_P		
298	GND		GND	
300	LVDS1_B_TX3-	MIPI_DSI1_DATA3_N		Display source shared with HDMI1
302	LVDS1_B_TX3+	MIPI_DSI1_DATA3_P		
304	AGND		AGND	
306	AAP1_MICIN		MIC_IN	SGTL5000 Pin 10
308	AGND		AGND	
310	AAP1_LIN_L		LINEIN_L	SGTL5000 Pin 9
312	AAP1_LIN_R		LINEIN_R	SGTL5000 Pin 8
314	AVCC		AVCC	
316	AAP1_HP_L		HEADPHONE_L	SGTL5000 Pin 4
318	AAP1_HP_R		HEADPHONE_R	SGTL5000 Pin 1
320	AVCC		AVCC	

[1] It is possible to change the IO voltage of the main SD interface from 3.3V (default) to 1.8V to support SD UHS-I speeds. Please note that the voltage can only be changed for all the pins simultaneously and not individually. Therefore, use these pins with care.
[2] This SoC pin is not available on modules with Wi-Fi and Bluetooth.
[3] The RGMII interface signals' IO voltage can be set to 1.8V, 2.5V, or 3.3V to comply with the NXP requirements for RGMII. Please note that the voltage can only be changed for all the pins simultaneously and not individually. During power-on, the IO voltage of these pins is turned off. The software needs to switch on the rail accordingly. Use these pins with care.
[4] The Apalis iMX8DXP 1GB features the USB2514B USB 2.0 hub instead of USB5744T USB 3.1 Gen 1hub. Therefore, the hub pins are different on this SKU
[5] The Apalis iMX8DXP 1GB bypasses the USB 3.1 Gen 1 SuperSpeed signals of the SoC to the module edge connector. More information can be found in section 0.

4. I/O Pins

4.1 Function Multiplexing

The NXP i.MX 8X SoC (low-speed) I/O pins can be configured for any of the (and up to) five alternate functions. Most of the pins can also be used as GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). For example, the i.MX 8X signal pin on the MXM3 finger pin 118 has the primary function UART1.RX (Apalis standard function UART1_RXD). Besides this UART function, the pin can also be configured as PWM1.OUT (PWM output), GPT0.COMPARE (timer compare input), GPT1.CLK (timer clock), and GPIO0.IO22 (GPIO)

The default setting for this pin is the primary function UART1.RX. It is strongly recommended to, whenever possible, use a pin for a function that is compatible with all Apalis modules. This guarantees the best compatibility with the standard software and with the other modules in the Apalis family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the table listed in chapter 4.4, you will find a list of all pins with alternate functions. There you can see which alternate functions are available for each pin.

Special care has to be taken with the MXM3 pins that multiple signals connected. When using one of these pins, make sure that the unused pin of each multiplexed pair is tri-stated or configured as an input to avoid undesired behavior and hardware damage. The following table lists all MXM3 pins that have more than one signal pin connected:

Table 4-1 Multiplexed Pins

X1 Pin #	Signal 1	Signal 2	Remarks
2	UART1_RTS_B	PCAL6416 (Addr 0x20) P1_0	
138	SCU_GPIO0_01	PCAL6416 (Addr 0x20) P0_3	SoC signal features bidirectional level shifter since the SoC pin is only 1.8V capable
232	LT8912B HPD	PCAL6416 (Addr 0x20) P1_7	Signal 1 is the hotplug-detect input of the DSI to HDMI bridge LT8912B

A few signals are shared between the on-module peripherals and the module edge connector. For these signals, the alternate functions are not possible to use. Special care must be taken with these signals.

Table 4-2 Shared Signals

X1 Pin #	SoC Function	On-Module Peripheral	Remarks
59	ENET0_MDIO	Ethernet PHY MDIO	The MDIO/MDC interface is a multi-user bus. Make sure the external PHY uses a different address as the on-module Ethernet PHY.
61	ENET0_MDC	Ethernet PHY MDC	
194	MCLK_OUT0	Audio Codec Master Clock	The signal features an output level shifter since the internal Audio codec runs with 1.8V IO voltage. If both codecs are in use, the external codec needs to run with the same frequency as the on-module codec.

4.2 Pin Control

The alternate function of each pin can be changed independently. On previous i.MX-based SoCs (e.g., i.MX 6 or i.MX 7), the multiplexing and pad control has been changed by directly writing to the IOMUX registers. On the i.MX 8X based SoC, this is no longer possible. The IOMUX registers can only be controlled by the System Controller Unit (SCU). This allows the SCU to do proper resource management of the peripherals. The SCU makes sure only the cores with permission to the according domain are allowed to make changes in the pin configuration.

To change the multiplexing and configuration of the SoC pins, a System Controller API is provided. Please see the System Controller API Reference Guide from NXP for more information. With the help of this API, the following settings can be set individually for every pin:

- Selecting the alternate function for this pin
- Configuring as input, open drain, open-drain input, or regular push-pull output
- Low power behavior such as latching
- Wakeup masking
- Wakeup control which includes falling and rising edge as well as high and low level
- Pull up and down resistor enabling
- Drive strength control
- Locking mechanism for muxing and pad control

4.3 Pin Reset Status

The interface pins of the i.MX 8X are configured by the system controller unit (SCU). After a reset, the SCU firmware (SCFW) configures the pins to a default state. Most of them are configured as input with a pull-down enabled. A few are tri-stated or pulled-up. Please check the table in chapter 4.4 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

Please be aware that during the power-up sequence, the pins enter into the reset states indicated when the related IO bank voltages are enabled on the module and the SCFW has configured the pins (while the RESET_MOCI# signal is active). The states of the pins are undefined before those conditions are met. After the reset has been released (the RESET_MOCI# signal is inactive), the states of the pins may be reconfigured by software components being involved in the boot process (e.g., U-Boot, Kernel).

Reset Status Description

PD:	Pull-Down (Input)
PU:	Pull-Up (Input)
Z:	Tristate (Input)

4.4 SoC Functions List

Below is a list of all the i.MX 8X pins that are available on the MXM3 connector. It shows the alternate functions that are available for each pin. The GPIO functionality is always defined as the ALT4 function. The alternate functions used to provide the primary interfaces to ensure the best compatibility with other Apalis modules are highlighted.

Function Short Forms

ACM:	Audio Clock Mux
ADC:	Analog-Digital Convert input
ADMA:	Audio DMA Subsystem
CI_PI:	Parallel Capture Interface
CONN:	Connectivity Subsystem
CSI:	Camera Serial Interface
DMA:	Direct Memory Access
DSI:	Display Serial Interface
ENET:	Ethernet MAC interface
ESAI:	Enhanced Serial Audio Interface
FLEXCAN:	Flexible Controller Area Network (Flexible CAN)
FTM:	FlexTimer Module
GPIO:	General Purpose Input Output
GPT:	General Purpose Timer
I2C:	Inter-Integrated Circuit
KPP:	Keypad Port
LSIO:	Low-Speed I/O
LCD:	Liquid Crystal Display Interface
LVDS:	Low Voltage Differential Signalling (also known as FPD-Link or FlatLink)
M40:	Cortex M4 Processor complex (dedicated interface for the M4 processor)
MIPI_CSI:	MIPI CSI Subsystem
MIPI_DSI:	MIPI DSI/LVDS Subsystem
MLB:	Media Local Bus (MediaLB)
MQS:	Medium Quality Sound
NAND:	Interface for NAND Flash
PCIE:	PCI Express
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
SAI:	Serial Interface for Audio (I2S and AC97)
SCU:	System Controller Unit
SNVS:	Secure Non-Volatile Storage
SPI:	Serial Peripheral Interface Bus
TAMPER:	Tamper detection
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)
WDOG:	Watchdog

X1 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Default Mode	Reset State	Power Block
1	QSPI0B_DATA3	AM8	LSIO.QSPI0B.DATA3	LSIO.QSPI1A.DATA3	LSIO.KPP0.ROW0		LSIO.GPIO3.IO21	ALT0	PD	VDD_QSPI0B_1P8_3P3
3	QSPI0B_DQS	AK10	LSIO.QSPI0B.DQS	LSIO.QSPI1A.DQS	LSIO.KPP0.ROW1		LSIO.GPIO3.IO22	ALT0	PD	VDD_QSPI0B_1P8_3P3
5	QSPI0B_SS0_B	AH10	LSIO.QSPI0B.SS0_B	LSIO.QSPI1A.SS0_B	LSIO.KPP0.ROW2		LSIO.GPIO3.IO23	ALT4	PU	VDD_QSPI0B_1P8_3P3
7	QSPI0B_SS1_B	AJ9	LSIO.QSPI0B.SS1_B	LSIO.QSPI1A.SS1_B	LSIO.KPP0.ROW3		LSIO.GPIO3.IO24	ALT4	PU	VDD_QSPI0B_1P8_3P3
11	QSPI0B_SCLK	AR11	LSIO.QSPI0B.SCLK	LSIO.QSPI1A.SCLK	LSIO.KPP0.COL0		LSIO.GPIO3.IO17	ALT4	PD	VDD_QSPI0B_1P8_3P3
13	QSPI0B_DATA0	AM10	LSIO.QSPI0B.DATA0	LSIO.QSPI1A.DATA0	LSIO.KPP0.COL1		LSIO.GPIO3.IO18	ALT0	PD	VDD_QSPI0B_1P8_3P3
15	QSPI0B_DATA1	AL9	LSIO.QSPI0B.DATA1	LSIO.QSPI1A.DATA1	LSIO.KPP0.COL2		LSIO.GPIO3.IO19	ALT0	PD	VDD_QSPI0B_1P8_3P3
17	QSPI0B_DATA2	AJ11	LSIO.QSPI0B.DATA2	LSIO.QSPI1A.DATA2	LSIO.KPP0.COL3		LSIO.GPIO3.IO20	ALT0	PD	VDD_QSPI0B_1P8_3P3
35	MIPI_DSI0_I2C0_SCL	AC31	MIPI_DSI0.I2C0.SCL	MIPI_DSI1.GPIO0.IO02			LSIO.GPIO1.IO25	ALT0	PU	VDD_MIPI_DSI_DIG_1P8_3P3
37	MIPI_DSI0_I2C0_SDA	AB28	MIPI_DSI0.I2C0.SDA	MIPI_DSI1.GPIO0.IO03			LSIO.GPIO1.IO26	ALT0	PU	VDD_MIPI_DSI_DIG_1P8_3P3
41	PCIE0_RX0_N	B12	HSIO.PCIE0.RX0_N							VDD_PCIE_LDO_1P0_CAP
43	PCIE0_RX0_P	A13	HSIO.PCIE0.RX0_P							VDD_PCIE_LDO_1P0_CAP
47	PCIE0_TX0_N	A9	HSIO.PCIE0.TX0_N							VDD_PCIE_LDO_1P0_CAP
49	PCIE0_TX0_P	B10	HSIO.PCIE0.TX0_P							VDD_PCIE_LDO_1P0_CAP
53	PCIE_REFCLK100M_N	D12	HSIO.PCIE_IOB.EXT_REFCLK100M_N							VDD_PCIE_1P8
55	PCIE_REFCLK100M_P	E11	HSIO.PCIE_IOB.EXT_REFCLK100M_P							VDD_PCIE_1P8
59	ENET0_MDIO [2)]	B32	CONN.ENET0.MDIO	~~ADMA.I2C3.SDA~~	~~CONN.ENET1.MDIO~~		~~LSIO.GPIO5.IO10~~	ALT0	PU	VDD_ENET_MDIO_1P8_3P3
61	ENET0_MDC [2)]	D30	CONN.ENET0.MDC	~~ADMA.I2C3.SCL~~	~~CONN.ENET1.MDC~~		~~LSIO.GPIO5.IO11~~	ALT4	PD	VDD_ENET_MDIO_1P8_3P3
137	MIPI_CSI0_DATA3_N	AN19	MIPI_CSI0.DN3							VDD_MIPI_CSI0_1P8
139	MIPI_CSI0_DATA3_P	AR19	MIPI_CSI0.DP3							VDD_MIPI_CSI0_1P8
143	MIPI_CSI0_DATA2_N	AN23	MIPI_CSI0.DN2							VDD_MIPI_CSI0_1P8
145	MIPI_CSI0_DATA2_P	AR23	MIPI_CSI0.DP2							VDD_MIPI_CSI0_1P8
149	MIPI_CSI0_DATA1_N	AM20	MIPI_CSI0.DN1							VDD_MIPI_CSI0_1P8
151	MIPI_CSI0_DATA1_P	AP20	MIPI_CSI0.DP1							VDD_MIPI_CSI0_1P8
155	MIPI_CSI0_DATA0_N	AM22	MIPI_CSI0.DN0							VDD_MIPI_CSI0_1P8
157	MIPI_CSI0_DATA0_P	AP22	MIPI_CSI0.DP0							VDD_MIPI_CSI0_1P8
161	MIPI_CSI0_CLK_N	AN21	MIPI_CSI0.CKN							VDD_MIPI_CSI0_1P8
163	MIPI_CSI0_CLK_P	AR21	MIPI_CSI0.CKP							VDD_MIPI_CSI0_1P8
173	CSI_D07	AM28	CI_PI.CSI_D09		ADMA.SAI3.RXD	SNVS.TAMPER_IN2		ALT0	PD	VDD_CSI_1P8_3P3
175	CSI_D06	AJ25	CI_PI.CSI_D08		ADMA.SAI3.RXC	SNVS.TAMPER_IN1		ALT0	PD	VDD_CSI_1P8_3P3
177	CSI_D05	AM30	CI_PI.CSI_D07		ADMA.SAI2.RXFS	SNVS.TAMPER_IN0		ALT0	PD	VDD_CSI_1P8_3P3
179	CSI_D04	AN29	CI_PI.CSI_D06		ADMA.SAI2.RXD	SNVS.TAMPER_OUT4		ALT0	PD	VDD_CSI_1P8_3P3
181	CSI_D03	AJ27	CI_PI.CSI_D05		ADMA.SAI2.RXC	SNVS.TAMPER_OUT3		ALT0	PD	VDD_CSI_1P8_3P3
183	CSI_D02	AP30	CI_PI.CSI_D04		ADMA.SAI0.RXFS	SNVS.TAMPER_OUT2		ALT0	PD	VDD_CSI_1P8_3P3
185	CSI_D01	AL29	CI_PI.CSI_D03		ADMA.SAI0.RXD	SNVS.TAMPER_OUT1		ALT0	PD	VDD_CSI_1P8_3P3
187	CSI_D00	AK28	CI_PI.CSI_D02		ADMA.SAI0.RXC	SNVS.TAMPER_OUT0		ALT0	PD	VDD_CSI_1P8_3P3
191	CSI_PCLK	AK26	CI_PI.CSI_PCLK	MIPI_CSI0.I2C0.SCL		ADMA.SPI1.SCK	LSIO.GPIO3.IO00	ALT0	PD	VDD_CSI_1P8_3P3
193	CSI_MCLK	AM26	CI_PI.CSI_MCLK	MIPI_CSI0.I2C0.SDA		ADMA.SPI1.SDO	LSIO.GPIO3.IO01	ALT4	PD	VDD_CSI_1P8_3P3
195	CSI_VSYNC	AL27	CI_PI.CSI_VSYNC	CI_PI.CSI_D01		SNVS.TAMPER_IN4		ALT0	PD	VDD_CSI_1P8_3P3
197	CSI_HSYNC	AR29	CI_PI.CSI_HSYNC	CI_PI.CSI_D00	ADMA.SAI3.RXFS	SNVS.TAMPER_IN3		ALT0	PD	VDD_CSI_1P8_3P3
201	CSI_RESET	AR27	CI_PI.CSI_RESET	CI_PI.CSI_I2C.SDA	ADMA.I2C3.SDA	ADMA.SPI1.CS0	LSIO.GPIO3.IO03	ALT0	PD	VDD_CSI_1P8_3P3
203	CSI_EN	AP28	CI_PI.CSI_EN	CI_PI.CSI_I2C.SCL	ADMA.I2C3.SCL	ADMA.SPI1.SDI	LSIO.GPIO3.IO02	ALT0	PD	VDD_CSI_1P8_3P3
205	MIPI_DSI1_I2C0_SDA	AC29	MIPI_DSI1.I2C0.SDA	MIPI_DSI0.GPIO0.IO03			LSIO.GPIO1.IO30	ALT0	PU	VDD_MIPI_DSI_DIG_1P8_3P3
207	MIPI_DSI1_I2C0_SCL	AE33	MIPI_DSI1.I2C0.SCL	MIPI_DSI0.GPIO0.IO02			LSIO.GPIO1.IO29	ALT0	PU	VDD_MIPI_DSI_DIG_1P8_3P3
209	USB_SS3_TC3	C15	ADMA.I2C1.SDA	CONN.USB_OTG2.OC			LSIO.GPIO4.IO06	ALT0	PD	VDD_USB_3P3
211	USB_SS3_TC0	F14	ADMA.I2C1.SCL	CONN.USB_OTG1.PWR	CONN.USB_OTG2.PWR		LSIO.GPIO4.IO03	ALT0	PD	VDD_USB_3P3
221	SPI0_SCK	P30	ADMA.SPI0.SCK	ADMA.SAI0.TXC	M40.I2C0.SCL	M40.GPIO0.IO00	LSIO.GPIO1.IO04	ALT0	PD	VDD_SPI_SAI_1P8_3P3
223	SPI0_SDI	P34	ADMA.SPI0.SDI	ADMA.SAI0.TXD	M40.TPM0.CH0	M40.GPIO0.IO02	LSIO.GPIO1.IO05	ALT0	PD	VDD_SPI_SAI_1P8_3P3
225	SPI0_SDO	R31	ADMA.SPI0.SDO	ADMA.SAI0.TXFS	M40.I2C0.SDA	M40.GPIO0.IO01	LSIO.GPIO1.IO06	ALT4	PD	VDD_SPI_SAI_1P8_3P3
227	SPI0_CS0	R33	ADMA.SPI0.CS0	ADMA.SAI0.RXD	M40.TPM0.CH1	M40.GPIO0.IO03	LSIO.GPIO1.IO08	ALT0	PD	VDD_SPI_SAI_1P8_3P3
229	SPI2_SCK	R29	ADMA.SPI2.SCK				LSIO.GPIO1.IO03	ALT0	PD	VDD_SPI_SAI_1P8_3P3
231	SPI2_SDI	N31	ADMA.SPI2.SDI				LSIO.GPIO1.IO02	ALT0	PD	VDD_SPI_SAI_1P8_3P3

X1 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Default Mode	Reset State	Power Block
233	SPI2_SDO	P32	ADMA.SPI2.SDO				LSIO.GPIO1.IO01	ALT4	PD	VDD_SPI_SAI_1P8_3P3
235	SPI2_CS0	P28	ADMA.SPI2.CS0				LSIO.GPIO1.IO00	ALT0	PD	VDD_SPI_SAI_1P8_3P3
239	MIPI_DSI1_GPIO0_00	AD30	MIPI_DSI1.GPIO0.IO00	ADMA.I2C2.SCL	MIPI_DSI1.PWM0.OUT		LSIO.GPIO1.IO31	ALT0	PD	VDD_MIPI_DSI_DIG_1P8_3P3
243	MCLK_OUT0	L29	ADMA.ACM.MCLK_OUT0	ADMA.ESAI0.TX_HF_CLK	ADMA.LCD_CLK	ADMA.SPI2.SDO	LSIO.GPIO0.IO20	ALT4	PD	VDD_SPI_MCLK_UART_1P8_3P3
245	MCLK_IN0	G35	ADMA.ACM.MCLK_IN0	ADMA.ESAI0.RX_HF_CLK	ADMA.LCD_VSYNC	ADMA.SPI2.SDI	LSIO.GPIO0.IO19	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
247	SPI3_CS0	J31	ADMA.SPI3.CS0	ADMA.ACM.MCLK_OUT1	ADMA.LCD_HSYNC		LSIO.GPIO0.IO16	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
249	MCLK_IN1	M28	ADMA.ACM.MCLK_IN1	ADMA.I2C3.SDA	ADMA.LCD_EN	ADMA.SPI2.SCK	ADMA.LCD_D17	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
255	SPDIF0_EXT_CLK	E35	ADMA.SPDIF0.EXT_CLK		ADMA.LCD_D12	CONN.ENET1.REFCLK_125M_25M	LSIO.GPIO0.IO12	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
257	SPI3_SCK	H32	ADMA.SPI3.SCK		ADMA.LCD_D13		LSIO.GPIO0.IO13	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
259	SPI3_SDO	F34	ADMA.SPI3.SDO		ADMA.LCD_D14		LSIO.GPIO0.IO14	ALT4	PD	VDD_SPI_MCLK_UART_1P8_3P3
261	SPI3_SDI	G33	ADMA.SPI3.SDI		ADMA.LCD_D15		LSIO.GPIO0.IO15	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
263	SPI3_CS1	K30	ADMA.SPI3.CS1	ADMA.I2C3.SCL	ADMA.LCD_RESET	ADMA.SPI2.CS0	ADMA.LCD_D16	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
265	UART1_CTS_B	K32	ADMA.UART1.CTS_B	LSIO.PWM3.OUT	ADMA.LCD_D17	LSIO.GPT1.COMPARE	LSIO.GPIO0.IO24	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
273	ESAI0_TX2_RX3	K28	ADMA.ESAI0.TX2_RX3	CONN.ENET1.RMII_RX_ER	ADMA.LCD_D06	CONN.ENET1.RGMII_RXD2	LSIO.GPIO0.IO06	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
275	ESAI0_TX3_RX2	C33	ADMA.ESAI0.TX3_RX2		ADMA.LCD_D07	CONN.ENET1.RGMII_RXD1	LSIO.GPIO0.IO07	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
277	ESAI0_TX4_RX1	F32	ADMA.ESAI0.TX4_RX1		ADMA.LCD_D08	CONN.ENET1.RGMII_TXD0	LSIO.GPIO0.IO08	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
279	ESAI0_TX5_RX0	J29	ADMA.ESAI0.TX5_RX0		ADMA.LCD_D09	CONN.ENET1.RGMII_TXD1	LSIO.GPIO0.IO09	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
281	SPDIF0_RX	G31	ADMA.SPDIF0.RX	ADMA.MQS.R	ADMA.LCD_D10	CONN.ENET1.RGMII_RXD0	LSIO.GPIO0.IO10	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
283	SPDIF0_TX	D34	ADMA.SPDIF0.TX	ADMA.MQS.L	ADMA.LCD_D11	CONN.ENET1.RGMII_RX_CTL	LSIO.GPIO0.IO11	ALT4	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
291	ESAI0_FSR	F30	ADMA.ESAI0.FSR	CONN.ENET1.RCLK50M_OUT	ADMA.LCD_D00	CONN.ENET1.RGMII_TXC	CONN.ENET1.RCLK50M_IN	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
293	ESAI0_FST	G29	ADMA.ESAI0.FST	CONN.MLB.CLK	ADMA.LCD_D01	CONN.ENET1.RGMII_TXD2	LSIO.GPIO0.IO01	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
295	ESAI0_SCKR	H28	ADMA.ESAI0.SCKR		ADMA.LCD_D02	CONN.ENET1.RGMII_TX_CTL	LSIO.GPIO0.IO02	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
297	ESAI0_SCKT	E31	ADMA.ESAI0.SCKT	CONN.MLB.SIG	ADMA.LCD_D03	CONN.ENET1.RGMII_TXD3	LSIO.GPIO0.IO03	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
299	ESAI0_TX0	D32	ADMA.ESAI0.TX0	CONN.MLB.DATA	ADMA.LCD_D04	CONN.ENET1.RGMII_RXC	LSIO.GPIO0.IO04	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
301	ESAI0_TX1	B34	ADMA.ESAI0.TX1		ADMA.LCD_D05	CONN.ENET1.RGMII_RXD3	LSIO.GPIO0.IO05	ALT0	PD	VDD_ESAI_SPDIF_1P8_2P5_3P3
305	ADC_IN0	U35	ADMA.ADC.IN0	M40.I2C0.SCL	M40.GPIO0.IO00		LSIO.GPIO1.IO10	ALT0	PD	VDD_ADC_DIG_1P8
307	ADC_IN1	U33	ADMA.ADC.IN1	M40.I2C0.SDA	M40.GPIO0.IO01		LSIO.GPIO1.IO09	ALT0	PD	VDD_ADC_DIG_1P8
309	ADC_IN4	W29	ADMA.ADC.IN4	M40.TPM0.CH0	M40.GPIO0.IO04		LSIO.GPIO1.IO14	ALT0	PD	VDD_ADC_DIG_1P8
311	ADC_IN5	V34	ADMA.ADC.IN5	M40.TPM0.CH1	M40.GPIO0.IO05		LSIO.GPIO1.IO13	ALT0	PD	VDD_ADC_DIG_1P8
2	UART1_RTS_B	N29	ADMA.UART1.RTS_B	LSIO.PWM2.OUT	ADMA.LCD_D16	LSIO.GPT1.CAPTURE	LSIO.GPT0.CLK	ALT4	PD	VDD_SPI_MCLK_UART_1P8_3P3
4	MIPI_DSI0_GPIO0_00	AD32	MIPI_DSI0.GPIO0.IO00	ADMA.I2C1.SCL	MIPI_DSI0.PWM0.OUT		LSIO.GPIO1.IO27	ALT0	PD	VDD_MIPI_DSI_DIG_1P8_3P3
6	MIPI_DSI0_GPIO0_01	AE35	MIPI_DSI0.GPIO0.IO01	ADMA.I2C1.SDA			LSIO.GPIO1.IO28	ALT0	PD	VDD_MIPI_DSI_DIG_1P8_3P3
8	MIPI_DSI1_GPIO0_01	AF34	MIPI_DSI1.GPIO0.IO01	ADMA.I2C2.SDA			LSIO.GPIO2.IO00	ALT0	PD	VDD_MIPI_DSI_DIG_1P8_3P3
12	FLEXCAN1_RX	AA33	ADMA.FLEXCAN1.RX	ADMA.SAI2.RXFS	ADMA.FTM.CH2	ADMA.SAI1.TXD	LSIO.GPIO1.IO17	ALT0	PD	VDD_CAN_UART_1P8_3P3

X1 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Default Mode	Reset State	Power Block
14	FLEXCAN1_TX	AA35	ADMA.FLEXCAN1.TX	ADMA.SAI3.RXC	ADMA.DMA0.REQ_IN0	ADMA.SAI1.RXD	LSIO.GPIO1.IO18	ALT4	PD	VDD_CAN_UART_1P8_3P3
16	FLEXCAN2_RX	AB34	ADMA.FLEXCAN2.RX	ADMA.SAI3.RXD	ADMA.UART3.RX	ADMA.SAI1.RXFS	LSIO.GPIO1.IO19	ALT0	PD	VDD_CAN_UART_1P8_3P3
18	FLEXCAN2_TX	AA31	ADMA.FLEXCAN2.TX	ADMA.SAI3.RXFS	ADMA.UART3.TX	ADMA.SAI1.RXC	LSIO.GPIO1.IO20	ALT4	PD	VDD_CAN_UART_1P8_3P3
60	USB_OTG1_VBUS	H18	CONN.USB_OTG1.VBUS							
72	USB_OTG1_ID	G17	CONN.USB_OTG1.ID							VDD_USB_3P3
74	USB_OTG1_DP	D18	CONN.USB_OTG1.DP							VDD_USB_3P3
76	USB_OTG1_DN	E19	CONN.USB_OTG1.DN							VDD_USB_3P3
84	USB_SS3_TC1	H14	ADMA.I2C1.SCL	CONN.USB_OTG2.PWR			LSIO.GPIO4.IO04	ALT0	PD	VDD_USB_3P3
96	QSPI0A_DATA0	AK14	LSIO.QSPI0A.DATA0				LSIO.GPIO3.IO09	ALT0	PD	VDD_QSPI0A_1P8_3P3
112	UART1_TX	H34	ADMA.UART1.TX	LSIO.PWM0.OUT	LSIO.GPT0.CAPTURE		LSIO.GPIO0.IO21	ALT4	PD	VDD_SPI_MCLK_UART_1P8_3P3
114	QSPI0A_DATA2	AJ13	LSIO.QSPI0A.DATA2				LSIO.GPIO3.IO11	ALT0	PD	VDD_QSPI0A_1P8_3P3
116	QSPI0A_DATA3	AH12	LSIO.QSPI0A.DATA3				LSIO.GPIO3.IO12	ALT0	PD	VDD_QSPI0A_1P8_3P3
118	UART1_RX	L31	ADMA.UART1.RX	LSIO.PWM1.OUT	LSIO.GPT0.COMPARE	LSIO.GPT1.CLK	LSIO.GPIO0.IO22	ALT0	PD	VDD_SPI_MCLK_UART_1P8_3P3
126	UART0_TX	AA29	ADMA.UART0.TX	ADMA.MQS.L	ADMA.FLEXCAN0.TX	SCU.UART0.TX	LSIO.GPIO1.IO22	ALT4	PD	VDD_CAN_UART_1P8_3P3
128	FLEXCAN0_RX	Y34	ADMA.FLEXCAN0.RX	ADMA.SAI2.RXC	ADMA.UART0.RTS_B	ADMA.SAI1.TXC	LSIO.GPIO1.IO15	ALT0	PD	VDD_CAN_UART_1P8_3P3
130	FLEXCAN0_TX	Y32	ADMA.FLEXCAN0.TX	ADMA.SAI2.RXD	ADMA.UART0.CTS_B	ADMA.SAI1.TXFS	LSIO.GPIO1.IO16	ALT4	PD	VDD_CAN_UART_1P8_3P3
132	UART0_RX	AB32	ADMA.UART0.RX	ADMA.MQS.R	ADMA.FLEXCAN0.RX	SCU.UART0.RX	LSIO.GPIO1.IO21	ALT0	PD	VDD_CAN_UART_1P8_3P3
134	UART2_TX	AC35	ADMA.UART2.TX	ADMA.FTM.CH1	ADMA.FLEXCAN1.TX		LSIO.GPIO1.IO23	ALT4	PD	VDD_CAN_UART_1P8_3P3
136	UART2_RX	AD34	ADMA.UART2.RX	ADMA.FTM.CH0	ADMA.FLEXCAN1.RX		LSIO.GPIO1.IO24	ALT0	PD	VDD_CAN_UART_1P8_3P3
138	SCU_GPIO0_01 [1]	AH30	SCU.GPIO0.IO01	SCU.UART0.TX	M40.UART0.TX	ADMA.UART3.TX	SCU.WDOG0.WDOG_OUT	ALT0	PU	VDD_ANA1_1P8
140	SCU_GPIO0_00 [1]	AF28	SCU.GPIO0.IO00	SCU.UART0.RX	M40.UART0.RX	ADMA.UART3.RX	LSIO.GPIO2.IO03	ALT0	PD	VDD_ANA1_1P8
144	USDHC1_DATA2	D26	CONN.USDHC1.DATA2	CONN.NAND.WE_B	ADMA.UART3.CTS_B		LSIO.GPIO4.IO27	ALT0	PU	VDD_USDHC1_1P8_3P3
146	USDHC1_DATA3	E25	CONN.USDHC1.DATA3	CONN.NAND.ALE	ADMA.UART3.RTS_B		LSIO.GPIO4.IO28	ALT0	PU	VDD_USDHC1_1P8_3P3
148	QSPI0A_DATA1	AR13	LSIO.QSPI0A.DATA1				LSIO.GPIO3.IO10	ALT0	PD	VDD_QSPI0A_1P8_3P3
150	USDHC1_CMD	C25	CONN.USDHC1.CMD	CONN.NAND.CE0_B	ADMA.MQS.R		LSIO.GPIO4.IO24	ALT0	PU	VDD_USDHC1_1P8_3P3
152	USDHC1_RESET_B	B24	CONN.USDHC1.RESET_B	CONN.NAND.RE_N	ADMA.SPI2.SCK		LSIO.GPIO4.IO19	ALT4	PU	VDD_USDHC1_VSELECT_1P8_3P3
154	USDHC1_CLK	G23	CONN.USDHC1.CLK		ADMA.UART3.RX		LSIO.GPIO4.IO23	ALT4	PD	VDD_USDHC1_1P8_3P3
156	USDHC1_WP	D24	CONN.USDHC1.WP	CONN.NAND.DQS_N	ADMA.SPI2.SDI		LSIO.GPIO4.IO21	ALT0	PD	VDD_USDHC1_VSELECT_1P8_3P3
158	QSPI0A_SS0_B	AM12	LSIO.QSPI0A.SS0_B				LSIO.GPIO3.IO14	ALT4	PU	VDD_QSPI0A_1P8_3P3
160	USDHC1_DATA0	A27	CONN.USDHC1.DATA0	CONN.NAND.CE1_B	ADMA.MQS.L		LSIO.GPIO4.IO25	ALT0	PU	VDD_USDHC1_1P8_3P3
162	USDHC1_DATA1	B26	CONN.USDHC1.DATA1	CONN.NAND.RE_B	ADMA.UART3.TX		LSIO.GPIO4.IO26	ALT0	PU	VDD_USDHC1_1P8_3P3
164	USDHC1_CD_B	E23	CONN.USDHC1.CD_B	CONN.NAND.DQS_P	ADMA.SPI2.CS0	CONN.NAND.DQS	LSIO.GPIO4.IO22	ALT0	PU	VDD_USDHC1_VSELECT_1P8_3P3
194	ADC_IN3 [3]	V30	~~ADMA.ADC.IN3~~	~~M40.UART0.TX~~	~~M40.GPIO0.IO03~~	ADMA.ACM.MCLK_OUT0	~~LSIO.GPIO1.IO11~~	ALT0	PD	VDD_ADC_DIG_1P8
196	SAI0_TXD	K34	ADMA.SAI0.TXD	ADMA.SAI1.RXC	ADMA.SPI1.SDO	ADMA.LCD_D18	LSIO.GPIO0.IO25	ALT0	PD	VDD_SPI_SAI_1P8_3P3
198	QSPI0A_SS1_B	AK12	LSIO.QSPI0A.SS1_B				LSIO.GPIO3.IO15	ALT4	PU	VDD_QSPI0A_1P8_3P3
200	SAI0_TXC	J35	ADMA.SAI0.TXC	ADMA.SAI1.TXD	ADMA.SPI1.SDI	ADMA.LCD_D19	LSIO.GPIO0.IO26	ALT0	PD	VDD_SPI_SAI_1P8_3P3
202	SAI0_RXD	M34	ADMA.SAI0.RXD	ADMA.SAI1.RXFS	ADMA.SPI1.CS0	ADMA.LCD_D20	LSIO.GPIO0.IO27	ALT0	PD	VDD_SPI_SAI_1P8_3P3
204	SAI0_TXFS	L33	ADMA.SAI0.TXFS	ADMA.SPI2.CS1	ADMA.SPI1.SCK		LSIO.GPIO0.IO28	ALT0	PD	VDD_SPI_SAI_1P8_3P3
246	MIPI_DSI0_CLK_N	AJ19	MIPI_DSI0.CKN							VDD_MIPI_DSI0_1P8
248	MIPI_DSI0_CLK_P	AK20	MIPI_DSI0.CKP							VDD_MIPI_DSI0_1P8
252	MIPI_DSI0_DATA0_N	AJ21	MIPI_DSI0.DN0							VDD_MIPI_DSI0_1P8
254	MIPI_DSI0_DATA0_P	AK22	MIPI_DSI0.DP0							VDD_MIPI_DSI0_1P8
258	MIPI_DSI0_DATA1_N	AJ17	MIPI_DSI0.DN1							VDD_MIPI_DSI0_1P8
260	MIPI_DSI0_DATA1_P	AK18	MIPI_DSI0.DP1							VDD_MIPI_DSI0_1P8
262	USB_SS3_TC2	G15	ADMA.I2C1.SDA	CONN.USB_OTG1.OC	CONN.USB_OTG2.OC		LSIO.GPIO4.IO05	ALT0	PD	VDD_USB_3P3
264	MIPI_DSI0_DATA2_N	AJ23	MIPI_DSI0.DN2							VDD_MIPI_DSI0_1P8
266	MIPI_DSI0_DATA2_P	AK24	MIPI_DSI0.DP2							VDD_MIPI_DSI0_1P8
270	MIPI_DSI0_DATA3_N	AJ15	MIPI_DSI0.DN3							VDD_MIPI_DSI0_1P8
272	MIPI_DSI0_DATA3_P	AK16	MIPI_DSI0.DP3							VDD_MIPI_DSI0_1P8
274	QSPI0A_SCLK	AP12	LSIO.QSPI0A.SCLK				LSIO.GPIO3.IO16	ALT4	PD	VDD_QSPI0A_1P8_3P3
276	MIPI_DSI1_CLK_N	AM16	MIPI_DSI1.CKN							VDD_MIPI_DSI1_1P8

X1 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Default Mode	Reset State	Power Block
278	MIPI_DSI1_CLK_P	AP16	MIPI_DSI1.CKP							VDD_MIPI_DSI1_1P8
282	MIPI_DSI1_DATA0_N	AN15	MIPI_DSI1.DN0							VDD_MIPI_DSI1_1P8
284	MIPI_DSI1_DATA0_P	AR15	MIPI_DSI1.DP0							VDD_MIPI_DSI1_1P8
286	QSPI0A_DQS	AL11	LSIO.QSPI0A.DQS				LSIO.GPIO3.IO13	ALT0	PD	VDD_QSPI0A_1P8_3P3
288	MIPI_DSI1_DATA1_N	AN17	MIPI_DSI1.DN1							VDD_MIPI_DSI1_1P8
290	MIPI_DSI1_DATA1_P	AR17	MIPI_DSI1.DP1							VDD_MIPI_DSI1_1P8
294	MIPI_DSI1_DATA2_N	AM14	MIPI_DSI1.DN2							VDD_MIPI_DSI1_1P8
296	MIPI_DSI1_DATA2_P	AP14	MIPI_DSI1.DP2							VDD_MIPI_DSI1_1P8
300	MIPI_DSI1_DATA3_N	AM18	MIPI_DSI1.DN3							VDD_MIPI_DSI1_1P8
302	MIPI_DSI1_DATA3_P	AP18	MIPI_DSI1.DP3							VDD_MIPI_DSI1_1P8

[1] This signal is shared with the on-module Audio codec and features an output level shifter. Therefore, only the clock output feature is available
[2] Since the on-module Ethernet PHY shares these pins, only MDIO/MDC function is possible
[3] Bi-directional level shifter on this pin. Interface speed and pin control is limited

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
10, 30, 36, 52, 58, 66, 78, 90, 102, 108	VCC	I	3.3V main power supply	Use decoupling capacitors on all pins.
9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298	GND	I	Digital Ground	
174	VCC_BACKUP	I/O	RTC Power supply can be connected to a backup battery.	It can be left unconnected if the internal RTC is not used.

5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
314, 320	AVCC	I	3.3V Analogue supply	Connect this pin to a 3.3V supply. For better audio accuracy, we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the VCC 3.3V input supply.
303, 313, 304, 308	AGND	I	Analogue Ground	Connect this pin to GND. For better audio accuracy, we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Apalis iMX8.

5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
28	RESET_MICO#	I	Reset Input	This pin is low active and resets the Apalis module. This pin is connected to the power manager IC. There is a 100k pull-up resistor on the module.
26	RESET_MOCI#	O	Reset Output	This pin is active low. This pin is driven low at boot up. This is an open-drain signal with a 10k pull-up resistor on the module.
24	POWER_ENABLE_MOCI	O	Signal for the carrier board to enable the peripheral voltage rails	More information about the required power management on the carrier board can be found in the Apalis Carrier Board Design Guide

The Apalis iMX8X features the NXP PF8100 power management IC (PMIC). Besides managing the power up and down sequence, this IC also controls the voltage level of certain power rails. When applying the Apalis module's main power, the PMIC will ramp up all rails and, in the end, releases the RSETBMCU signal. This reset is used for the SoC, some of the on-module peripherals, and is available as a buffered output on pin 26 of the SODIMM module edge connector. To meet the reset timing requirements of PCI Express, the external reset output RESET_MOCI# needs to be delayed. Figure 7 shows the circuit that is used for delaying the RESET_MOCI# signal. The transistor holds down the external reset signal until the bootloader releases the signal by driving the LSIO.GPIO4.IO01 (ball PCIE_CTRL0_CLKREQ_B) low.

The Apalis iMX8X allows the external reset input on pin 28 of the module edge connector to initiate a warm reset cycle. This input signal directly drives the RESETBMCU signal down, which resets the SoC, the on-module peripherals, and generates a reset cycle on pin 26. For proper power-up sequencing, the external reset input on pin 28 is not required to be driven by the carrier board. The pin 28 reset input can be left unconnected if there is no need for initiating the module reset externally.

The RESET_MICO# signal on pin 28 is also routed to a power button circuit on the module. This circuit generates a button signal on the falling edge of the external reset signal. This button signal is routed to the ON_OFF_BUTTON input of the SoC and allows you to wake up the system after power-down. The power button circuit generates this button signal also when the main input voltage is reapplied. More information about the module's power sequencing can be found in the Apalis Carrier Board Design Guide.

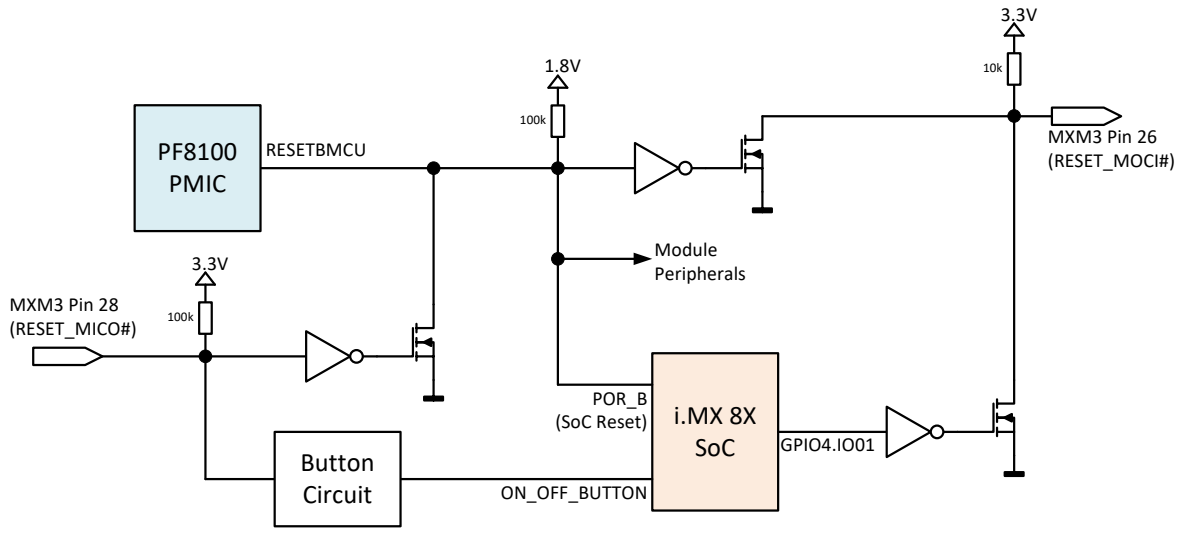


Figure 7 RESET_MOCI# circuit

5.2 GPIOs

The Apalis form factor features eight dedicated general-purpose input-output (GPIO) pins. Besides these 8 GPIOs, several pins can be used as GPIO if their primary function is not used. For compatibility reasons, it is recommended to use the eight dedicated GPIOs first.

Table 5-4 Dedicated GPIO signals

X1 Pin#	Apalis Standard Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
1	GPIO1	QSPI0B_DATA3	LSIO.GPIO3.IO21	I/O	
3	GPIO2	QSPI0B_DQS	LSIO.GPIO3.IO22	I/O	
5	GPIO3	QSPI0B_SS0_B	LSIO.GPIO3.IO23	I/O	
7	GPIO4	QSPI0B_SS1_B	LSIO.GPIO3.IO24	I/O	
11	GPIO5	QSPI0B_SCLK	LSIO.GPIO3.IO17	I/O	
13	GPIO6	QSPI0B_DATA0	LSIO.GPIO3.IO18	I/O	
15	GPIO7	QSPI0B_DATA1	LSIO.GPIO3.IO19	I/O	
17	GPIO8	QSPI0B_DATA2	LSIO.GPIO3.IO20	I/O	

Besides the regular GPIOs that can be accessed by the primary Cortex A35 cores and the Cortex M4F core, a few GPIOs are tightly coupled to the real-time capable M4F core. These GPIOs are all located as alternate functions. Some of these pins are the ADC pins which are only rated for 1.8V.

Table 5-5 Tightly Coupled M4F GPIO signals

X1 Pin#	Apalis Standard Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
221	SPI1_CLK	SPI0_SCK	M40.GPIO0.IO00	I/O	
305	AN1_ADC0	ADC_IN0			**Maximum voltage 1.8V**
225	SPI1_MOSI	SPI0_SDO	M40.GPIO0.IO01	I/O	
307	AN1_ADC1	ADC_IN1			**Maximum voltage 1.8V**
223	SPI1_MISO	SPI0_SDI	M40.GPIO0.IO02	I/O	
227	SPI1_CS	SPI0_CS0	M40.GPIO0.IO03	I/O	
309	AN1_ADC2	ADC_IN4	M40.GPIO0.IO04	I/O	**Maximum voltage 1.8V**
311	AN1_TSWIP_ADC3	ADC_IN5	M40.GPIO0.IO05	I/O	**Maximum voltage 1.8V**

Also, the System Controller Unit (SCU) M4 core features dedicated tightly coupled GPIOs. The two GPIOs are available as alternate functions of the UART4 interface. Please note that there are bidirectional level shifters on both of these signals. This means the configurable pull-up and down resistors are not available.

Table 5-6 Tightly Coupled SCU GPIO signals

X1 Pin#	Apalis Standard Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
138	UART4_TXD	SCU_GPIO0_01	SCU.GPIO0.IO01	I/O	Bidirectional level shifter
140	UART4_RXD	SCU_GPIO0_00	SCU.GPIO0.IO00	I/O	Bidirectional level shifter

The i.MX 8X SoC does not feature enough GPIO for fulfilling all the needs of the module. Therefore, the module is equipped with up to two 16-bit GPIO expanders. The NXP PCAL6416A I²C is used. These expanders allow for every I/O individual settings for directions, output drive strength, internal pull up or down resistors, and interrupt masking. By default, all pins are set to high impedance inputs. It is recommended to enable pull-up or pull-down resistors for unused pins. The two expanders are located on the on-module I²C interface (I2C0 interface) that is also used for communicating with the audio codec, resistive touch controller, DSI to HDMI bridge, as well as the USB hub. The first expander is on the I²C address 0x20 and uses the GPIO4.IO02 as an interrupt for the SoC. The second expander is using the address 0x21 and uses GPIO4.IO00 for the interrupt. Some of the GPIO expander signals are used for on-module peripherals. The standard SKUs of the Apalis iMX8X feature only the first GPIO expander. The second expander (on address 0x21) is not assembled and is only available on request (BTO).

Table 5-7 GPIO Expander 1 (I²C Address 0x20)

X1 Pin#	Apalis Standard Function	PCAL6416 Pin Name	PCAL6416 Function	I/O	Description
220	HDMI1_CEC	P0_0	Port 0, I/O 0	I/O	
217	SPDIF1_IN	P0_1	Port 0, I/O 1	I/O	
215	SPDIF1_OUT	P0_2	Port 0, I/O 2	I/O	
138	UART4_TXD	P0_3	Port 0, I/O 3	I/O	The pin is multiplexed with an SoC interface
124	UART1_DCD	P0_4	Port 0, I/O 4	I/O	
122	UART1_RI	P0_5	Port 0, I/O 5	I/O	
120	UART1_DSR	P0_6	Port 0, I/O 6	I/O	
110	UART1_DTR	P0_7	Port 0, I/O 7	I/O	
2	PWM1	P1_0	Port 1, I/O 0	I/O	The pin is multiplexed with an SoC interface
		P1_1	Port 1, I/O 1	O	Wi-Fi wakeup (host to Wi-Fi)
		P1_2	Port 1, I/O 2	O	Wi-Fi/Bluetooth disable radio
		P1_3	Port 1, I/O 3	O	Bluetooth wakeup (host to Bluetooth)
		P1_4	Port 1, I/O 4	O	Wi-Fi/Bluetooth power enable
		P1_5	Port 1, I/O 5	I	Wi-Fi wakeup (Wi-Fi to host)
		P1_6	Port 1, I/O 6	O	DSI switch select
232	HDMI1_HPD	P1_7	Port 1, I/O 7	I/O	The pin is multiplexed with the HP input of the LT8912B DSI to HDMI bridge

Table 5-8 GPIO Expander 2 (I²C Address 0x21), not available on standard SKU

X1 Pin#	Apalis Standard Function	PCAL6416 Pin Name	PCAL6416 Function	I/O	Description
190	SD1_CD#	P0_0	Port 0, I/O 0	I/O	
188	SD1_D1	P0_1	Port 0, I/O 1	I/O	
186	SD1_D0	P0_2	Port 0, I/O 2	I/O	
184	SD1_CLK	P0_3	Port 0, I/O 3	I/O	
180	SD1_CMD	P0_4	Port 0, I/O 4	I/O	
178	SD1_D3	P0_5	Port 0, I/O 5	I/O	
176	SD1_D2	P0_6	Port 0, I/O 6	I/O	
251	LCD1_R0	P0_7	Port 0, I/O 7	I/O	
253	LCD1_R1	P1_0	Port 1, I/O 0	I/O	
269	LCD1_G0	P1_1	Port 1, I/O 1	I/O	
271	LCD1_G1	P1_2	Port 1, I/O 2	I/O	
249	LCD1_DE	P1_3	Port 1, I/O 3	I/O	The pin is multiplexed with an SoC interface
263	LCD1_R6	P1_4	Port 1, I/O 4	I/O	The pin is multiplexed with an SoC interface
287	LCD1_B0	P1_5	Port 1, I/O 5	I/O	
291	LCD1_B2	P1_6	Port 1, I/O 6	I/O	The pin is multiplexed with an SoC interface
289	LCD1_B1	P1_7	Port 1, I/O 7	I/O	

5.2.1 Wakeup Source

In principle, all GPIOs can be used to wake up the Apalis module from a suspended state. In the Apalis module standard, pin 37 is the default wakeup source. Only this pin is guaranteed to be wake-up-compatible with other Apalis modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Apalis modules. The wake signal of the Ethernet PHY is connected to GPIO1.IO12.

Table 5-9 Apalis Wakeup Source

X1 Pin#	Apalis Standard Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
37	WAKE1_MICO	MIPI_DSI0_I2C0_SDA	LSIO.GPIO1.IO26	I/O	Standard external wake signal
		ADC_IN2	LSIO.GPIO1.IO12	I/O	Internal Ethernet PHY wake signal

5.3 Ethernet

The Apalis Module features a 10/100/1000 Mbit Ethernet interface. The MAC is integrated into the i.MX 8X SoC and connected to a separate PHY located on the module. Therefore only the magnetics are required on the carrier board. The Micrel KSZ9131 Gigabit Ethernet Transceiver chip is connected via RGMII to the NXP i.MX 8X.

The Gigabit Ethernet MAC in the SoC integrates an accurate IEEE 1588 compliant timer for clock synchronization for distributed control nodes used in industrial automation applications. The Ethernet interface supports Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN).

Table 5-10 Ethernet Pins

X1 Pin #	Apalis Signal Name	KSZ9131 Signal Name	I/O	Description	Remarks
50	ETH1_MDI0+	TXRXP_A	I/O	Media Dependent Interface	100BASE-TX: Transmit +
48	ETH1_MDI0-	TXRXM_A	I/O	Media Dependent Interface	100BASE-TX: Transmit -
56	ETH1_MDI1+	TXRXP_B	I/O	Media Dependent Interface	100BASE-TX: Receive +
54	ETH1_MDI1-	TXRXM_B	I/O	Media Dependent Interface	100BASE-TX: Receive -
32	ETH1_MDI2+	TXRXP_C	I/O	Media Dependent Interface	100BASE-TX: Unused
34	ETH1_MDI2-	TXRXM_C	I/O	Media Dependent Interface	100BASE-TX: Unused
38	ETH1_MDI3+	TXRXP_D	I/O	Media Dependent Interface	100BASE-TX: Unused
40	ETH1_MDI3-	TXRXM_D	I/O	Media Dependent Interface	100BASE-TX: Unused
46	ETH+_CTREF	NC	O	Center tap supply	KSZ9131 does not need a center tap supply
42	ETH1_ACT	LED1	O	LED indication output	Toggles during RX/TX activity
44	ETH1_LINK	LED2	O	LED indication output	Is low if a link (any speed) is established

The Micrel KSZ9131 does not require a center tap supply on the magnetics. Nevertheless, follow the Apalis Carrier Board Design Guide and connect the magnetics center tap to pin 46 of the Apalis module. This guarantees full compatibility with other Apalis modules, which require a center tap supply.

If only fast Ethernet is required, 10/100Mbit magnetics with only two lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

The Apalis iMX8X features a second Ethernet port. This port requires an Ethernet PHY on the carrier board. The second MAC in the SoC provides two different interface standards for the connection with the PHY:

- RGMII: Reduced Gigabit Media Independent Interface. This interface allows connecting a Gigabit Ethernet PHY such as a secondary KSZ9131.
- RMII: Reduced Media Independent Interface. This is the preferred mode for interfacing a 10/100 Mbit/s Ethernet PHY, such as the KSZ8041.

The MDIO configuration port signals are shared between the on-module and external Ethernet PHY. It is crucial to make sure that the two PHYs are not strapped to the same address. The MDIO interface of the Ethernet PHY on the module is using the address 00100. We recommend using the address 00111 for the external PHY. Since the MDIO signals are shared, the on-module Ethernet PHY's power rail cannot be turned off if an external Ethernet PHY is used.

The secondary RGMII/RMII Ethernet interface is not part of the Apalis standard. Therefore, the signals are not compatible with other Apalis modules. Most of the signals are located on the module edge connector pins, initially reserved as a parallel RGB LCD interface.

The secondary RGMII/RMII Ethernet interface needs special attention regarding the supply voltage level. The RGMII/RMII voltage is switchable through LDO3OUT of the PMIC PF8100. The voltage level must be defined by software configuration. During the power-up sequence, the IO voltage is set to 3.3V by default. All the RGMII/RMII signals are configured as GPIO inputs with enabled pull-down resistors. If the interface is used with 1.8V IO voltage, it is important to configure first the LDO3OUT voltage and then change the alternate function to RGMII/RMII. This ensures full compatibility with 1.8V RGMII signal levels.

If the secondary Ethernet interface is used as RGMII, the output voltages are limited to 1.8V and 2.5V. For RMII and other alternate functions (e.g., GPIO) of these pins, also 3.3V logic level is

suitable. Please note that the ENET1_MDC and ENET1_MDIO are always set to 3.3V, independent of the RGMII/RMII signals' output voltage settings.

Table 5-11 RGMII signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
283	LCD1_G7	SPDIF0_TX	CONN.ENET1.RGMII_RX_CTL	I	RGMII_RX_CTL
299	LCD1_B6	ESAI0_TX0	CONN.ENET1.RGMII_RXC	I	RGMII_RXC
281	LCD1_G6	SPDIF0_RX	CONN.ENET1.RGMII_RXD0	I	RGMII_RXD0
275	LCD1_G3	ESAI0_TX3_RX2	CONN.ENET1.RGMII_RXD1	I	RGMII_RXD1
273	LCD1_G2	ESAI0_TX2_RX3	CONN.ENET1.RGMII_RXD2	I	RGMII_RXD2
301	LCD1_B7	ESAI0_TX1	CONN.ENET1.RGMII_RXD3	I	RGMII_RXD3
295	LCD1_B4	ESAI0_SCKR	CONN.ENET1.RGMII_TX_CTL	O	RGMII_TX_CTL
291	LCD1_B2	ESAI0_FSR	CONN.ENET1.RGMII_TXC	O	RGMII_TXC
277	LCD1_G4	ESAI0_TX4_RX1	CONN.ENET1.RGMII_TXD0	O	RGMII_TXD0
279	LCD1_G5	ESAI0_TX5_RX0	CONN.ENET1.RGMII_TXD1	O	RGMII_TXD1
293	LCD1_B3	ESAI0_FST	CONN.ENET1.RGMII_TXD2	O	RGMII_TXD2
297	LCD1_B5	ESAI0_SCKT	CONN.ENET1.RGMII_TXD3	O	RGMII_TXD3
61	TS_DIFF1+	ENET0_MDC	CONN.ENET1.MDC	O	RGMII_MDC **shared with PHY on the module**
59	TS_DIFF1-	ENET0_MDIO	CONN.ENET1.MDIO	I/O	RGMII_MDIO **shared with PHY on the module**
255	LCD1_R2	SPDIF0_EXT_CLK	CONN.ENET1.REFCLK_125M_25M	I	Optional 125MHz reference clock input

Table 5-12 RMII signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
281	LCD1_G6	SPDIF0_RX	CONN.ENET1.RGMII_RXD0	I	RMII_RXD0
275	LCD1_G3	ESAI0_TX3_RX2	CONN.ENET1.RGMII_RXD1	I	RMII_RXD1
273	LCD1_G2	ESAI0_TX2_RX3	CONN.ENET1.RMII_RX_ER	I	RMII_RXER
277	LCD1_G4	ESAI0_TX4_RX1	CONN.ENET1.RGMII_TXD0	O	RMII_TXD0
279	LCD1_G5	ESAI0_TX5_RX0	CONN.ENET1.RGMII_TXD1	O	RMII_TXD1
295	LCD1_B4	ESAI0_SCKR	CONN.ENET1.RGMII_TX_CTL	O	RMII_TXEN
283	LCD1_G7	SPDIF0_TX	CONN.ENET1.RGMII_RX_CTL	I	RMII_CRS_DV
61	TS_DIFF1+	ENET0_MDC	CONN.ENET1.MDC	O	RMII_MDC **shared with PHY on the module**
59	TS_DIFF1-	ENET0_MDIO	CONN.ENET1.MDIO	I/O	RMII_MDIO **shared with PHY on the module**
291	LCD1_B2	ESAI0_FSR	CONN.ENET1.RCLK50M_OUT	O	50MHz Reference clock that is provided from the MAC to the PHY
291	LCD1_B2	ESAI0_FSR	CONN.ENET1.RCLK50M_IN	I	50MHz Reference clock that is provided from the PHY to the MAC

5.4 Wi-Fi and Bluetooth

The Apalis iMX8X is available as a version with on-module Wi-Fi and Bluetooth interfaces. The additional "WB" in the product name indicates that this version features Wi-Fi and Bluetooth. These Apalis module versions are making use of the AW-CM276NF Dual-Band Wi-Fi and Bluetooth module from Azurewave.

Features:

- Wi-Fi 802.11a/b/g/n/ac
- Dual-Band 5 GHz and 2.4GHz
- Up to 866.7 Mbps
- 20/40/80 MHz channel bandwidth
- Station/Client Mode, Access Point Mode, Wi-Fi- Direct Mode, and Simultaneous Station and Access point mode
- Bluetooth 5.0 (BR/EDR), BLE
- Murata HSC (MXHP32) connector for the dual external antenna in 2x2 configuration, compatible to IPX/IPEX connector MHF4 series
- Pre-certified for CE (Europe), FCC (United States), IC (Canada), TELEC (Japan), and WPC (India). See https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products

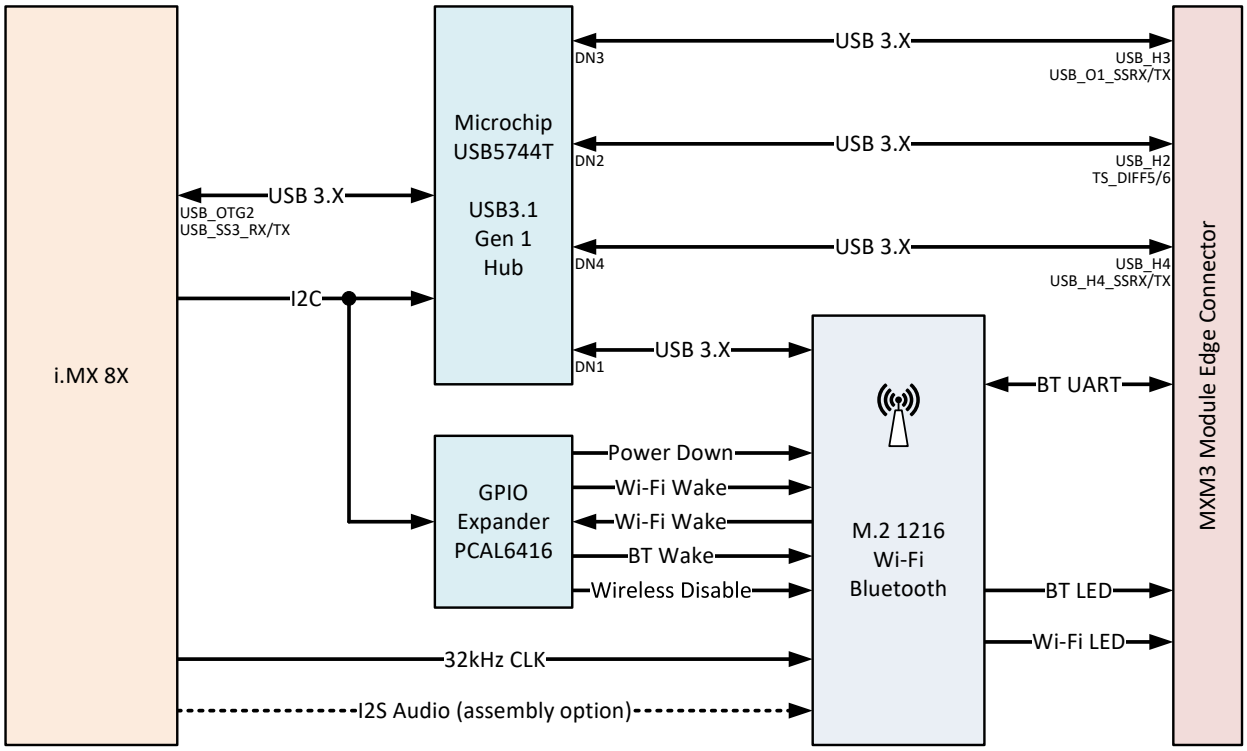


Figure 8: Wi-Fi and Bluetooth block diagram

The Wi-Fi module is connected over a USB 3.1 Gen 1 SuperSpeed interface with the i.MX 8X SoC. Since the SoC does not feature enough USB ports, there is an on-module USB 3.1 Gen 1 Hub. The control signals are connected to an I²C GPIO expander since the SoC has a limited number of GPIO-capable pins.

The AW-CM276NF features four wake signals, of which three are connected to the GPIO expander. Two are input signals (one for the Wi-Fi and one for Bluetooth), allowing for waking up the radio. Only the output signal of the AW-CM276NF, which the Wi-Fi receiver uses to wake up the system (SoC), is available on the expander. The wake output of the Bluetooth is not available on the Apalis iMX8X.

The Wi-Fi and Bluetooth module features a power-down signal. With this signal, the wireless module can be shut down completely. After re-enabling the module, the firmware for the AW-CM276NF has to be downloaded again.

Table 5-13 Control Signals from GPIO Expander

PCAL6416 Port	Signal	AW-CM276NF Pin Name	I/O	Description
P1_1	Wi-Fi_WKUP_WLAN	GPIO[15]/ TMS/ Host Wake WLAN	I	HOST_WKUP_WLAN: SoC to AW-CM276NF Wi-Fi Wakeup, the signal is also available on SODIMM
P1_2	Wi-Fi_W_DISABLE	GPIO[22]/ PCIE_W_DISABLEn	I	PCIe Wireless Disable Input (active low), the signal is also available on SODIMM
P1_3	Wi-Fi_WKUP_BT	GPIO[12]/ UART Host Wake BT	I	HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup, the signal is also available on SODIMM
P1_4	Wi-Fi_PDn	PDn	I	Power Down of complete Wi-Fi/BT module (active low). Firmware needs to be re-downloaded.
P1_5	Wi-Fi_WKUP_HOST	GPIO[14]/TCK/ WLAN Wake Host	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output

The AW-CM276NF features a USB VBUS signal input on its GPIO[0] port. This signal is used for notifying the Wi-Fi and Bluetooth module that a USB connection has been established and the USB enumeration process can start. A general-purpose output pin is connected to this input of the Azurewave module to emulate a USB connection cycle.

Table 5-14 Control Signals from SoC

SoC GPIO	Signal	AW-CM276NF Pin Name	I/O	Description
GPIO4.IO00	Wi-Fi_USB_VBUS_ON	GPIO[1]	I	Presence signalization of USB interface

Some interface pins of the Wi-Fi and Bluetooth module are available on the module edge connector in the type-specific pin area. It is not guaranteed that these pins are compatible with other Apalis modules.

Table 5-15 MXM3 Signal Pins of the AW-CM276NF

X1 Pin#	Apalis Std Function	AW-CM276NF Pin Name	I/O	Description
123	TS_4	GPIO[8]/UART_SOUT	O	BT UART mode: TX data
133	TS_DIFF13+	GPIO[9]/UART_SIN	I	BT UART mode: RX data
135	TS_5	GPIO[2]/WLAN_LED	O	Wi-Fi activity LED
159	TS_6	GPIO3/BT_LED	O	Bluetooth activity LED

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. Please contact Toradex about certifying the Apalis iMX8QXP 2GB WB IT: Contact your local sales office or support@toradex.com.

5.5 USB

The Apalis module form factor features up to four USB interfaces, two USB 3.1 Gen 1 SuperSpeed (previously called USB 3.0, backward compatible with USB 2.0), and two USB 2.0 High-Speed interfaces. The i.MX 8 SoC, on the other hand, features only two USB ports. One USB 3.1 Gen 1 port with SuperSpeed signals and one with USB 2.0 High-Speed only. Depending on the Apalis iMX8X module version, there is a USB 3.1 Gen 1 USB (Microchip USB5744T) or USB 2.0 (Microchip USB2514B) hub on the module to serve all the standard USB interfaces of the Apalis module form factor.

Even though both USB ports of the i.MX 8X SoC are OTG capable, only the port that is not connected to the on-module USB hub can be used as USB OTG (host and client). This USB_O1 port is also used for the serial mode (recovery mode).

The offered USB interfaces are dependent on the different versions of the Apalis iMX8X module. Please carefully check the compatibility between the Apalis iMX8X modules and other Apalis modules. The Toradex Pinout Designer can be a helpful tool for checking compatibility. If only one USB port with USB 3.1 Gen 1 SuperSpeed capability is required, the USB_H4 port should be considered to maximize compatibility with other Apalis modules.

5.5.1 USB Configuration on Apalis iMX8QXP 2GB WB IT

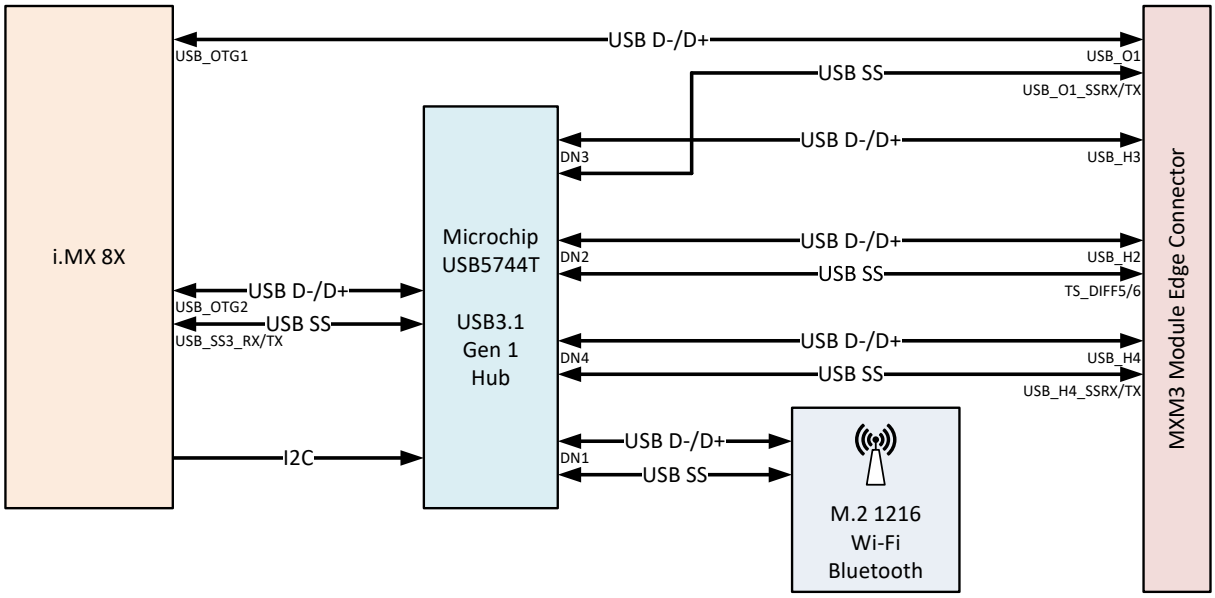


Figure 9: USB block diagram of Apalis iMX8QXP 2GB WB IT

Even though the SuperSpeed signals of the USB_H3 interface are made available on the USB_O1 SuperSpeed module edge connector pins, they are meant to be used with the USB_H3 interface, not the USB_O1. The SuperSpeed signals of the USB_H2 port are available on the type-specific area. This means they are not compatible with other Apalis modules.

Table 5-16 USBO1 Data Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
74	USBO1_D+	USB_OTG1_DP	CONN.USB_OTG1.DP	I/O	Positive Differential USB Signal, OTG capable
76	USBO1_D-	USB_OTG1_DN	CONN.USB_OTG1.DN	I/O	Negative Differential USB Signal, OTG capable

Table 5-17 USBH2 Data Pins

X1 Pin#	Apalis Std Function	USB5744T Ball Name	I/O	Description
80	USBH2_D+	USBDP_DN2	I/O	Positive Differential USB Signal
82	USBH2_D-	USBDM_DN2	I/O	Negative Differential USB Signal
85	TS_DIFF5+	USBRXP_DN2	I	Positive differential receiving host signal for USB SuperSpeed
83	TS_DIFF5-	USBRXM_DN2	I	Negative differential receiving host signal for USB SuperSpeed
91	TS_DIFF6+	USBTXP_DN2	O	Positive differential transmission host signal for USB SuperSpeed
89	TS_DIFF6-	USBTXM_DN2	O	Negative differential transmission host signal for USB SuperSpeed

Table 5-18 USBH3 Data Pins

X1 Pin#	Apalis Std Function	USB5744T Ball Name	I/O	Description
86	USBH3_D+	USBDP_DN3	I/O	Positive Differential USB Signal
88	USBH3_D-	USBDM_DN3	I/O	Negative Differential USB Signal
62	USBO1_SSRX+	USBRXP_DN3	I	Positive differential receiving host signal for USB SuperSpeed
64	USBO1_SSRX-	USBRXM_DN3	I	Negative differential receiving host signal for USB SuperSpeed
68	USBO1_SSTX+	USBTXP_DN3	O	Positive differential transmission host signal for USB SuperSpeed
70	USBO1_SSTX-	USBTXM_DN3	O	Negative differential transmission host signal for USB SuperSpeed

Table 5-19 USBH4 Data Pins

X1 Pin#	Apalis Std Function	USB5744T Ball Name	I/O	Description
98	USBH4_D+	USBDP_DN4	I/O	Positive Differential USB Signal
100	USBH4_D-	USBDM_DN4	I/O	Negative Differential USB Signal
94	USBH4_SSRX+	USBRXP_DN4	I	Positive differential receiving host signal for USB SuperSpeed
92	USBH4_SSRX-	USBRXM_DN4	I	Negative differential receiving host signal for USB SuperSpeed
106	USBH4_SSTX+	USBTXP_DN4	O	Positive differential transmission host signal for USB SuperSpeed
104	USBH4_SSTX-	USBTXM_DN4	O	Negative differential transmission host signal for USB SuperSpeed

5.5.2 USB Configuration on Apalis iMX8QXP 2GB ECC IT

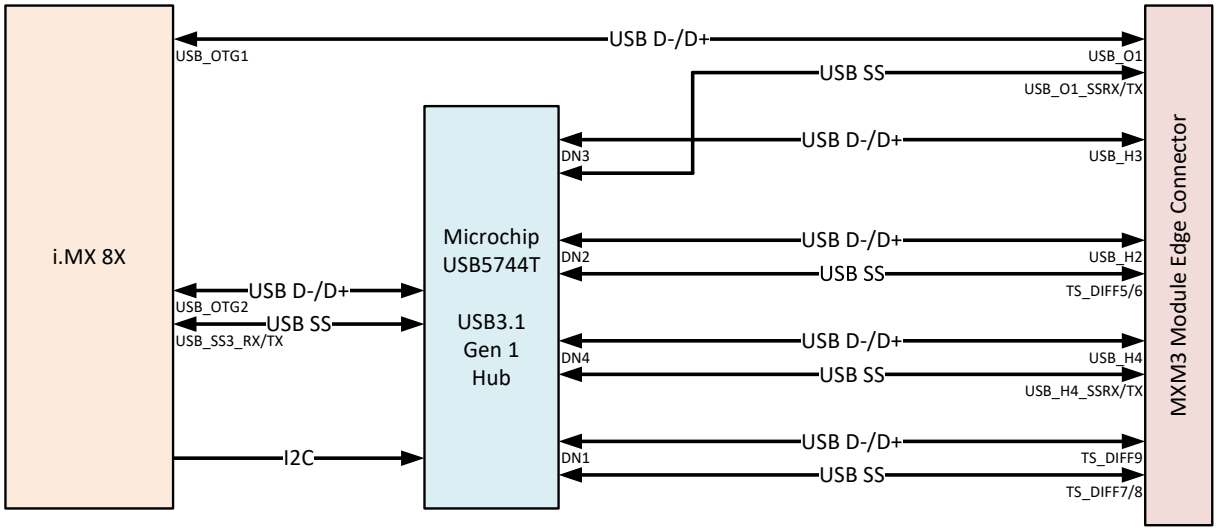


Figure 10: USB block diagram of Apalis iMX8QXP 2GB ECC IT

The USB configuration of the Apalis iMX8QXP 2GB ECC IT is very similar to the Apalis iMX8QXP 2GB WB IT. It only adds a fifth USB port to the type-specific area. This USB port is used on the module with the wireless feature for the Wi-Fi and Bluetooth module. The port is compatible with the fifth USB 2.0 port of the Apalis iMX6 modules.

Table 5-20 USBO1 Data Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
74	USBO1_D+	USB_OTG1_DP	CONN.USB_OTG1.DP	I/O	Positive Differential USB Signal, OTG capable
76	USBO1_D-	USB_OTG1_DN	CONN.USB_OTG1.DN	I/O	Negative Differential USB Signal, OTG capable

Table 5-21 USBH2 Data Pins

X1 Pin#	Apalis Std Function	USB5744T Ball Name	I/O	Description
80	USBH2_D+	USBDP_DN2	I/O	Positive Differential USB Signal
82	USBH2_D-	USBDM_DN2	I/O	Negative Differential USB Signal
85	TS_DIFF5+	USBRXP_DN2	I	Positive differential receiving host signal for USB SuperSpeed
83	TS_DIFF5-	USBRXM_DN2	I	Negative differential receiving host signal for USB SuperSpeed
91	TS_DIFF6+	USBTXP_DN2	O	Positive differential transmission host signal for USB SuperSpeed
89	TS_DIFF6-	USBTXM_DN2	O	Negative differential transmission host signal for USB SuperSpeed

Table 5-22 USBH3 Data Pins

X1 Pin#	Apalis Std Function	USB5744T Ball Name	I/O	Description
86	USBH3_D+	USBDP_DN3	I/O	Positive Differential USB Signal
88	USBH3_D-	USBDM_DN3	I/O	Negative Differential USB Signal
62	USBO1_SSRX+	USBRXP_DN3	I	Positive differential receiving host signal for USB SuperSpeed
64	USBO1_SSRX-	USBRXM_DN3	I	Negative differential receiving host signal for USB SuperSpeed
68	USBO1_SSTX+	USBTXP_DN3	O	Positive differential transmission host signal for USB SuperSpeed
70	USBO1_SSTX-	USBTXM_DN3	O	Negative differential transmission host signal for USB SuperSpeed

Table 5-23 USBH4 Data Pins

X1 Pin#	Apalis Std Function	USB5744T Ball Name	I/O	Description
98	USBH4_D+	USBDP_DN4	I/O	Positive Differential USB Signal
100	USBH4_D-	USBDM_DN4	I/O	Negative Differential USB Signal
94	USBH4_SSRX+	USBRXP_DN4	I	Positive differential receiving host signal for USB SuperSpeed
92	USBH4_SSRX-	USBRXM_DN4	I	Negative differential receiving host signal for USB SuperSpeed
106	USBH4_SSTX+	USBTXP_DN4	O	Positive differential transmission host signal for USB SuperSpeed
104	USBH4_SSTX-	USBTXM_DN4	O	Negative differential transmission host signal for USB SuperSpeed

Table 5-24 USBH5 Data Pins

X1 Pin#	Apalis Std Function	USB5744T Ball Name	I/O	Description
109	TS_DIFF9+	USBDP_DN1	I/O	Positive Differential USB Signal
107	TS_DIFF9-	USBDM_DN1	I/O	Negative Differential USB Signal
97	TS_DIFF7+	USBRXP_DN1	I	Positive differential receiving host signal for USB SuperSpeed
95	TS_DIFF7-	USBRXM_DN1	I	Negative differential receiving host signal for USB SuperSpeed
103	TS_DIFF8+	USBTXP_DN1	O	Positive differential transmission host signal for USB SuperSpeed
101	TS_DIFF8-	USBTXM_DN1	O	Negative differential transmission host signal for USB SuperSpeed

5.5.3 USB Configuration on Apalis iMX8DXP 1GB

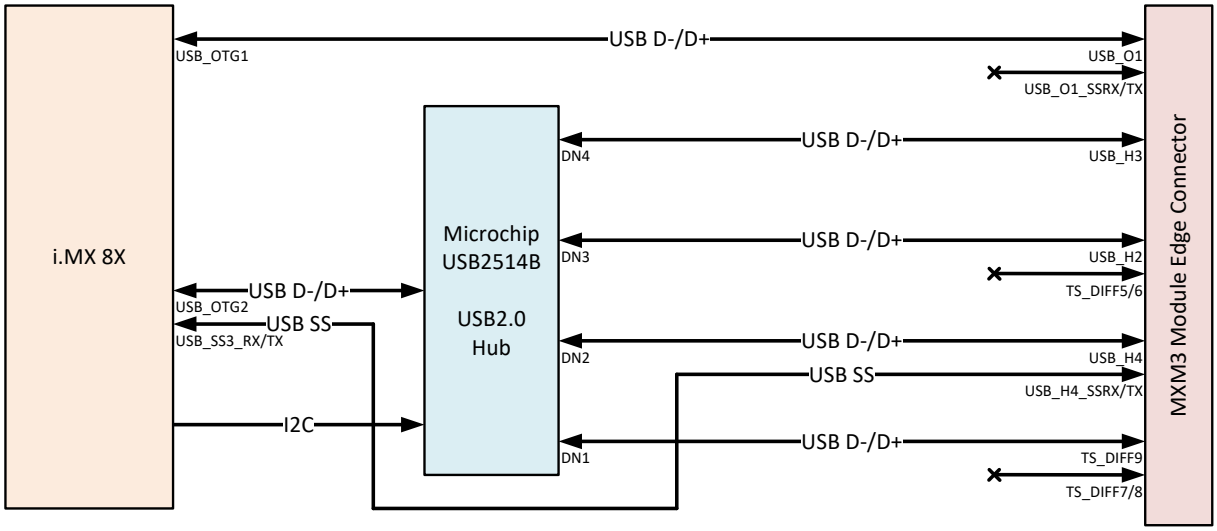


Figure 11: USB block diagram of Apalis iMX8DXP 1GB

The Apalis iMX8DXP 1GB features only a USB 2.0 hub. The SuperSpeed signals of the i.MX 8X SoC are routed directly to the USB_H4 port. This port can be used as a full USB 3.1 Gen 1 interface, while all the other USB ports of the module only feature High-Speed USB 2.0. The fifth port is located in the type-specific area and is compatible with the Apalis iMX6 modules.

Table 5-25 USBO1 Data Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
74	USBO1_D+	USB_OTG1_DP	CONN.USB_OTG1.DP	I/O	Positive Differential USB Signal, OTG capable
76	USBO1_D-	USB_OTG1_DN	CONN.USB_OTG1.DN	I/O	Negative Differential USB Signal, OTG capable

Table 5-26 USBH2 Data Pins

X1 Pin#	Apalis Std Function	USB2514B Ball Name	I/O	Description
80	USBH2_D+	USBDN3_DP	I/O	Positive Differential USB Signal
82	USBH2_D-	USBDN3_DM	I/O	Negative Differential USB Signal

Table 5-27 USBH3 Data Pins

X1 Pin#	Apalis Std Function	USB2514B Ball Name	I/O	Description
86	USBH3_D+	USBDN4_DP	I/O	Positive Differential USB Signal
88	USBH3_D-	USBDN4_DM	I/O	Negative Differential USB Signal

Table 5-28 USBH4 Data Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	USB2514B Ball Name	I/O	Description
98	USBH4_D+		USBDN2_DP	I/O	Positive Differential USB Signal
100	USBH4_D-		USBDN2_DM	I/O	Negative Differential USB Signal
94	USBH4_SSRX+	USB_SS3_RX_P		I	Positive differential receiving host signal for USB3.0
92	USBH4_SSRX-	USB_SS3_RX_N		I	Negative differential receiving host signal for USB3.0
106	USBH4_SSTX+	USB_SS3_TX_P		O	Positive differential transmission host signal for USB3.0
104	USBH4_SSTX-	USB_SS3_TX_N		O	Negative differential transmission host signal for USB3.0

Table 5-29 USBH5 Data Pins

X1 Pin#	Apalis Std Function	USB2514B Ball Name	I/O	Description
109	TS_DIFF9+	USBDN1_DP	I/O	Positive Differential USB Signal
107	TS_DIFF9-	USBDN1_DM	I/O	Negative Differential USB Signal

5.5.4 USB Control Signals

All different Apalis iMX8X modules versions feature the same USB control signals.

Table 5-30 USB OTG Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
72	USBO1_ID	USB_OTG1_ID	CONN.USB_OTG1.ID	I	Use this pin to detect the ID pin if you use USB OTG.
60	USBO1_VBUS	USB_OTG1_VBUS	CONN.USB_OTG1.VBUS	I	Use this pin to detect if VBUS is present.

If you use the USB Host function, you need to provide the 5V USB supply voltage on your carrier board for the interfaces. The Apalis iMX8X provides additional signals for controlling the USB supply. We recommend using the following pins to guarantee the best possible compatibility. The USBH2, USBH3, and USBH4 interfaces share the bus power control signals, whereas USBO1 has its dedicated control signals.

Table 5-31 USB Power Control Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
274	USBO1_EN	QSPI0A_SCLK	LSIO.GPIO3.IO16	O	This pin enables the external USB voltage supply for the USBO1 interface. Regular GPIO, not a dedicated USB function.
262	USBO1_OC#	USB_SS3_TC2	CONN.USB_OTG1.OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBO1 interface.
84	USBH_EN	USB_SS3_TC1	CONN.USB_OTG2.PWR	O	This pin enables the external USB voltage supply for the USBH2, USBH3, and USBH4 interfaces.
96	USBH_OC#	QSPI0A_DATA0	LSIO.GPIO3.IO09	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBH2, USBH3, and USBH4 interfaces. Regular GPIO, not a dedicated USB function.

5.6 Display

The i.MX 8X SoC features a single display controller. The display controller has two outputs that can be routed internally to the two LVDS/DSI PHYs, the parallel RGB interface, and the internal imaging subsystem. The two LVDS/DSI PHYs can individually be used as MIPI DSI or single-channel LVDS interface. The two PHYs can be combined for using them as dual-channel LVDS.

Depending on the Apalis iMX8X module version, there is a DSI to HDMI bridge on the module. An analog switch alternates the DSI signals either to the HDMI bridge or the module edge connector. Therefore, the HDMI interface cannot be used if the secondary LVDS channel/DSI port or a dual-channel LVDS is in use.

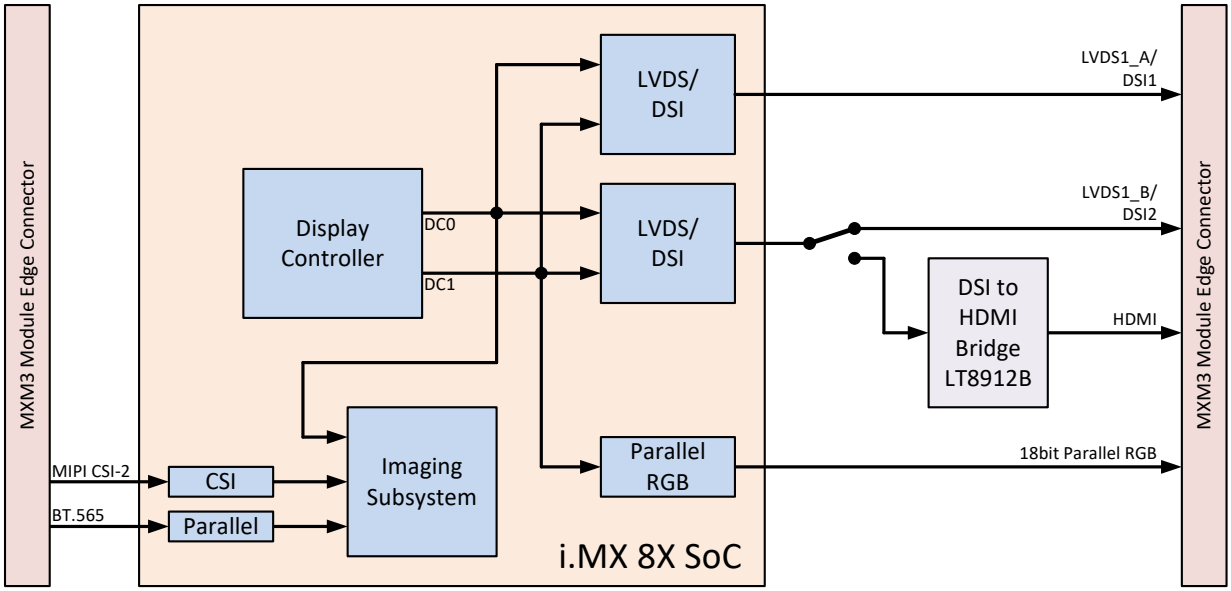


Figure 12: Display and Imaging Block Diagram

5.6.1 Parallel RGB LCD interface

The Apalis iMX8X provides one parallel LCD interface on the SODIMM connector. The i.MX 8X SoC would support up to 24-bit color per pixel. However, only 18-bit is possible since some of the data pins are not available on the module edge connector. The 18-bit signals are mapped to the edge connector in an order that is compatible with the standard 24-bit mapping used in the Apalis form factor. The missing low significant bits of each color have 1kΩ pull-down resistors on the module, ensuring the signals are not floating. Set the LCD interface controller into the 18-bit color mapping mode if a 24-bit or 18-bit display is used. This allows compatibility with other Apalis modules that feature a parallel RGB LCD interface.

Features:

- Up to 720p60 (720 x 1280 @ 60 Hz)
- 18-bit color (Apalis 24-bit compatible color mapping)
- Supports parallel TTL displays and smart displays
- Digital video interface output supported with ITU-R BT.656 format
- Max pixel clock 85MHz

Table 5-32 Standard Parallel RGB LCD Interface Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	24-bit RGB Interface*	18-bit RGB Interface	16-bit RGB Interface
287	LCD1_B0	No connection to SoC, 1kΩ pull down		O	B0		
289	LCD1_B1	No connection to SoC, 1kΩ pull down		O	B1		
291	LCD1_B2	ESAI0_FSR	ADMA.LCD_D00	O	B2	B0	B0
293	LCD1_B3	ESAI0_FST	ADMA.LCD_D01	O	B3	B1	B1
295	LCD1_B4	ESAI0_SCKR	ADMA.LCD_D02	O	B4	B2	B2
297	LCD1_B5	ESAI0_SCKT	ADMA.LCD_D03	O	B5	B3	B3
299	LCD1_B6	ESAI0_TX0	ADMA.LCD_D04	O	B6	B4	B4
301	LCD1_B7	ESAI0_TX1	ADMA.LCD_D05	O	B7	B5	G0
269	LCD1_G0	No connection to SoC, 1kΩ pull down		O	G0		
271	LCD1_G1	No connection to SoC, 1kΩ pull down		O	G1		
273	LCD1_G2	ESAI0_TX2_RX3	ADMA.LCD_D06	O	G2	G0	G1
275	LCD1_G3	ESAI0_TX3_RX2	ADMA.LCD_D07	O	G3	G1	G2
277	LCD1_G4	ESAI0_TX4_RX1	ADMA.LCD_D08	O	G4	G2	G3
279	LCD1_G5	ESAI0_TX5_RX0	ADMA.LCD_D09	O	G5	G3	G4
281	LCD1_G6	SPDIF0_RX	ADMA.LCD_D10	O	G6	G4	G5
283	LCD1_G7	SPDIF0_TX	ADMA.LCD_D11	O	G7	G5	R0
251	LCD1_R0	No connection to SoC, 1kΩ pull down		O	R0		
253	LCD1_R1	No connection to SoC, 1kΩ pull down		O	R1		
255	LCD1_R2	SPDIF0_EXT_CLK	ADMA.LCD_D12	O	R2	R0	R1
257	LCD1_R3	SPI3_SCK	ADMA.LCD_D13	O	R3	R1	R2
259	LCD1_R4	SPI3_SDO	ADMA.LCD_D14	O	R4	R2	R3
261	LCD1_R5	SPI3_SDI	ADMA.LCD_D15	O	R5	R3	R4
263	LCD1_R6	SPI3_CS1	ADMA.LCD_D16	O	R6	R4	
265	LCD1_R7	UART1_CTS_B	ADMA.LCD_D17	O	R7	R5	
249	LCD1_DE	MCLK_IN1	ADMA.LCD_EN	O	Data Enable (other names: Output Enable, L_BIAS)		
247	LCD1_HSYNC	SPI3_CS0	ADMA.LCD_HSYNC	O	Horizontal Sync (other names: Line Clock, L_LCKL)		
245	LCD1_VSYNC	MCLK_IN0	ADMA.LCD_VSYNC	O	Vertical Sync (other names: Frame Clock, L_FCLK)		
243	LCD1_PCLK	MCLK_OUT0	ADMA.LCD_CLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)		

*This is the compatible mapping of a 24-bit display. The RGB LCD interface needs to be set to 18-bit. The lower significant bits are set all to 0 by 1kΩ pull-down resistors.

Table 5-33 Additional Parallel RGB LCD Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
239	BKL1_PWM	MIPI_DSI1_GPIO0_00	MIPI_DSI1.PWM0.OUT	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	QSPI0A_DQS	LSIO.GPIO3.IO13	O	Enable signal for the backlight.
205	I2C2_SDA (DDC)	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL (DDC)	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL	O	

5.6.2 LVDS

The official name for the LVDS interface is actually FPD-Link or FlatLink, which uses the low voltage differential signaling (LVDS) technology. However, very often, this interface is simply called LVDS.

The LVDS interface serializes the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to Seven parallel signals. For an 18-bit RGB interface, including the control signals (Display Enable, Vertical, and Horizontal Sync), each FPD_Link/FlatLink channel requires three LVDS data pairs. The additional color bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two color-mapping standards for the 24-bit interface. The less common “24-bit / 18-bit compatible” (JEIDA format, Intel 24.0 LVDS data format) standard packs the two low significant bits of each color into the fourth LVDS pair. This standard is backward compatible with the 18-bit mode. It is possible to connect an 18-bit display to a 24-bit interface or vice versa. The more common 24-bit color mapping standard (VESA format, Intel 24.1 LVDS data format) serializes the two most significant bits of each color into the fourth LVDS pair. This mode is not backward-compatible. Therefore, only 24-bit displays can be connected to a 24-bit host with this color mapping. The LVDS interfaces of Apalis iMX8 are configurable to support different color mappings and depths. This ensures compatibility with 18-bit and 24-bit displays with both kinds of color mappings.

Figure 13 shows the LVDS output signals for the “24-bit /18-bit Compatible Color Mapping” (JEIDA format, Intel 24.0 LVDS data format)

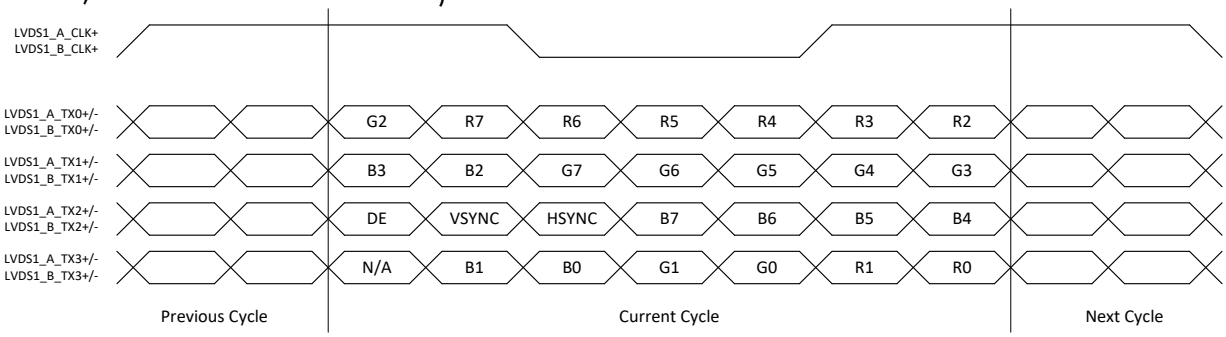


Figure 13: 24-bit / 18-bit Compatible Color Mapping (Intel 24.0 LVDS Data Format)

Figure 14 shows the LVDS output signals for the common 24-bit color mapping (VESA format, Intel 24.1 LVDS data format).

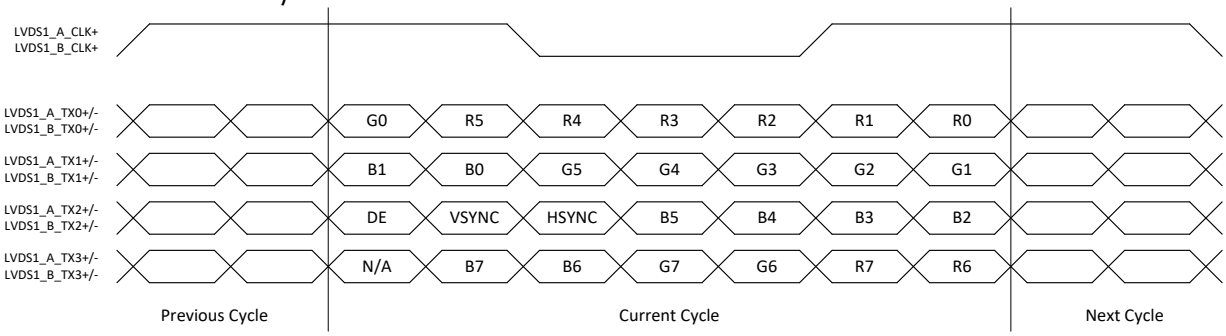


Figure 14: Common 24-bit VESA Color Mapping (Intel 24.1 LVDS Data Format)

Figure 15 shows the LVDS output signals for the 18-bit interface.

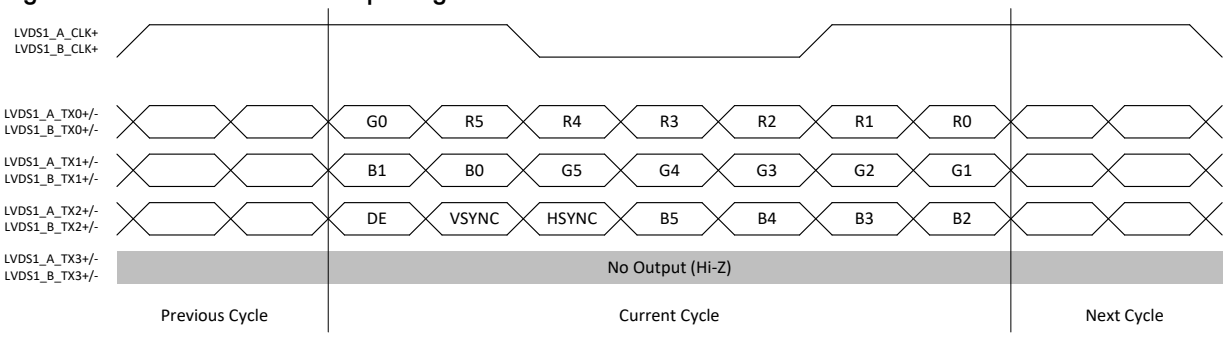


Figure 15: 18-bit Mode

A single channel LVDS interface can support resolutions up to 1366x768 pixels @60 frames per second (85MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual-channel configuration, the odd bits are transmitted in the first channel, and the even bits are sent in the second channel. The dual-channel LVDS interface can support resolutions up to 1920x1200 @60fps (170MHz pixel clock maximum).

The i.MX 8X features two single-channel LVDS ports. It is possible to combine these two LVDS ports to a dual-channel interface for higher resolution displays. Figure 16 shows the possible LVDS display configurations.

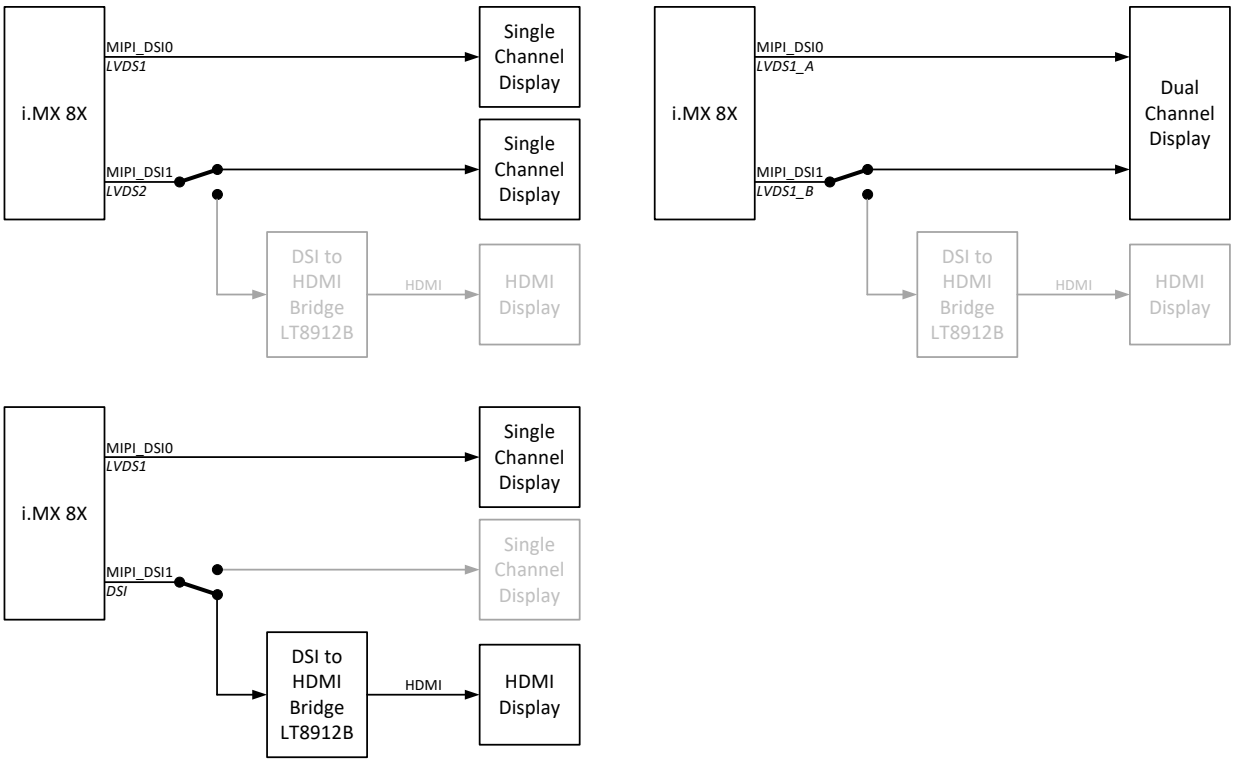


Figure 16: Possible LVDS Display configurations

The LVDS display interface on the i.MX 8X shares the interface pins with the MIPI DSI interface. The secondary channel features an analog switch that routes the DSI signals to the HDMI bridge. See also Figure 12 for the video output block diagram.

Table 5-34 LVDS interface signals (Apalis standard)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	I/O	Description
248	LVDS1_A_CLK+	MIPI_DSI0_CLK_P	O	LVDS Clock out for channel A (odd pixels/single channel)
246	LVDS1_A_CLK-	MIPI_DSI0_CLK_N	O	
254	LVDS1_A_TX0+	MIPI_DSI0_DATA0_P	O	LVDS data lane 0 for channel A (odd pixels/single channel)
252	LVDS1_A_TX0-	MIPI_DSI0_DATA0_N	O	
260	LVDS1_A_TX1+	MIPI_DSI0_DATA1_P	O	LVDS data lane 1 for channel A (odd pixels/single channel)
258	LVDS1_A_TX1-	MIPI_DSI0_DATA1_N	O	
266	LVDS1_A_TX2+	MIPI_DSI0_DATA2_P	O	LVDS data lane 2 for channel A (odd pixels/single channel)
264	LVDS1_A_TX2-	MIPI_DSI0_DATA2_N	O	
272	LVDS1_A_TX3+	MIPI_DSI0_DATA3_P	O	LVDS data lane 3 for channel A (odd pixels/single channel; unused for 18-bit)
270	LVDS1_A_TX3-	MIPI_DSI0_DATA3_N	O	
278	LVDS1_B_CLK+	MIPI_DSI1_CLK_P	O	LVDS Clock out for channel B (even pixels/unused for the single-channel)
276	LVDS1_B_CLK-	MIPI_DSI1_CLK_N	O	
284	LVDS1_B_TX0+	MIPI_DSI1_DATA0_P	O	LVDS data lane 0 for channel B (odd pixels/unused for the single-channel)
282	LVDS1_B_TX0-	MIPI_DSI1_DATA0_N	O	
290	LVDS1_B_TX1+	MIPI_DSI1_DATA1_P	O	LVDS data lane 1 for channel B (odd pixels/unused for the single-channel)
288	LVDS1_B_TX1-	MIPI_DSI1_DATA1_N	O	
296	LVDS1_B_TX2+	MIPI_DSI1_DATA2_P	O	LVDS data lane 2 for channel B (odd pixels/unused for the single-channel)
294	LVDS1_B_TX2-	MIPI_DSI1_DATA2_N	O	

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	I/O	Description
302	LVDS1_B_TX3+	MIPI_DSI1_DATA3_P	O	LVDS data lane 3 for channel B (odd pixels/unused for the single-channel; unused for 18-bit)
300	LVDS1_B_TX3-	MIPI_DSI1_DATA3_N	O	

Table 5-35 LVDS Display Control Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
239	BKL1_PWM	MIPI_DSI1_GPIO0_00	MIPI_DSI1.PWM0.OUT	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	QSPI0A_DQS	LSIO.GPIO3.IO13	O	Enable signal for the backlight.
205	I2C2_SDA (DDC)	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA	I/O	I²C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL (DDC)	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL	O	

Table 5-36 Additional LVDS Display Control Signals (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
4	PWM2	MIPI_DSI0_GPIO0_00	MIPI_DSI0.GPIO0.IO00		Dedicated GPIO functions for the first DSI/LVDS port. These pins also feature regular GPIO functionality on ALT4
6	PWM3	MIPI_DSI0_GPIO0_01	MIPI_DSI0.GPIO0.IO01		
207	I2C2_SCL (DDC)	MIPI_DSI1_I2C0_SCL	MIPI_DSI0.GPIO0.IO02		
205	I2C2_SDA (DDC)	MIPI_DSI1_I2C0_SDA	MIPI_DSI0.GPIO0.IO03		
35	SATA1_ACT#	MIPI_DSI0_I2C0_SCL	MIPI_DSI0.I2C0.SCL		Dedicated I²C the first DSI/LVDS port.
37	WAKE1_MICO	MIPI_DSI0_I2C0_SDA	MIPI_DSI0.I2C0.SDA		
4	PWM2	MIPI_DSI0_GPIO0_00	MIPI_DSI0.PWM0.OUT		Dedicated backlight PWM the first DSI/LVDS port.
239	BKL1_PWM	MIPI_DSI1_GPIO0_00	MIPI_DSI1.GPIO0.IO00		Dedicated GPIO functions for the second DSI/LVDS port. These pins also feature regular GPIO functionality on ALT4
8	PWM4	MIPI_DSI1_GPIO0_01	MIPI_DSI1.GPIO0.IO01		
35	SATA1_ACT#	MIPI_DSI0_I2C0_SCL	MIPI_DSI1.GPIO0.IO02		
37	WAKE1_MICO	MIPI_DSI0_I2C0_SDA	MIPI_DSI1.GPIO0.IO03		

5.6.3 HDMI

The i.MX 8X SoC does not feature a native HDMI interface. However, depending on the version of the Apalis iMX8X, there is an on-module MIPI DSI to HDMI bridge available, the Lontium Semiconductor LT8912B. The bridge is controlled over the on-module I²C interface (I2C0 interface), which is also used for the audio codec, resistive touch controller, GPIO expander, and USB Hub. The LT8912B occupies the addresses 0x48, 0x49, 0x4a, and 0x4b of the I²C interface. The bridge has an interrupt output that is connected to the GPIO GPIO3.IO06 of the SoC.

The DSI signals are shared over an analog switch with the secondary DSI/LVDS interface. The analog switch is controlled by the GPIO expander (port 1, I/O 6). If this GPIO is set low, the DSI signals are routed to the module edge connector. For using the HDMI interface, the GPIO must be set high to route the DSI signals to the bridge.

The HDMI interface on the Apalis iMX8X does not support audio stream. Consumer electronic control (CEC) and High-bandwidth Content Protection (HDCP) are both not available.

HDMI Features

- HDMI 1.4 standard
- Up to 1080p60 (1920x1080@60Hz)
- 8-bit per color channel

Table 5-37 HDMI Interface Signals

X1 Pin#	Apalis Std Function	LT8912B Ball Name	I/O	Description
240	HDMI1_TXC+	HDMITX_CKP	O	HDMI Differential Clock
242	HDMI1_TXC-	HDMITX_CKN	O	
234	HDMI1_TXD0+	HDMITX0_DP	O	HDMI Differential Data 0
236	HDMI1_TXD0-	HDMITX0_DN	O	
228	HDMI1_TXD1+	HDMITX1_DP	O	HDMI Differential Data 1
230	HDMI1_TXD1-	HDMITX1_DN	O	
222	HDMI1_TXD2+	HDMITX2_DN	O	HDMI Differential Data 2
224	HDMI1_TXD2-	HDMITX2_DP	O	

Table 5-38 Additional Display Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
220	HDMI1_CEC			I/O	CEC not available.
232	HDMI1_HPD	GPIO Expander Port 1, I/O 7/ LT8912B HPD (level-shifted)		I	Hot Plug Detect, connected to GPIO expander as well as HPD input of bridge
205	I2C2_SDA (DDC)	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA	I/O	Display Data Channel, shared with the other display interfaces
207	I2C2_SCL (DDC)	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL	O	

5.6.4 Analog VGA

The Apalis iMX8X does not feature an analog VGA interface. The pins on the module edge connector are left unconnected.

5.6.5 Display Serial Interface (DSI)

The i.MX 8X SoC provides up to two MIPI/DSI interfaces to connect compatible displays. The DSI subsystem is combined with LVDS. This means the two LVDS channels can be configured as two MIPI/DSI interfaces with up to 4 data lanes. The lanes are capable of up to 1.05GHz data. The interface is bidirectional (high-speed out, low power/speed in from display). The interface uses the MIPI D-PHY for the physical layer. Each of the interfaces allows the programming of the display resolution from 160x120 (QQVGA) to 1920x1200 (WUXGA) with 60Hz and 24-bit.

Since the DSI signals are shared with the LVDS interface, the DSI ports are not available on the type-specific pins. They are available on the LVDS pins. Therefore, the DSI port is not compatible with other Apalis modules.

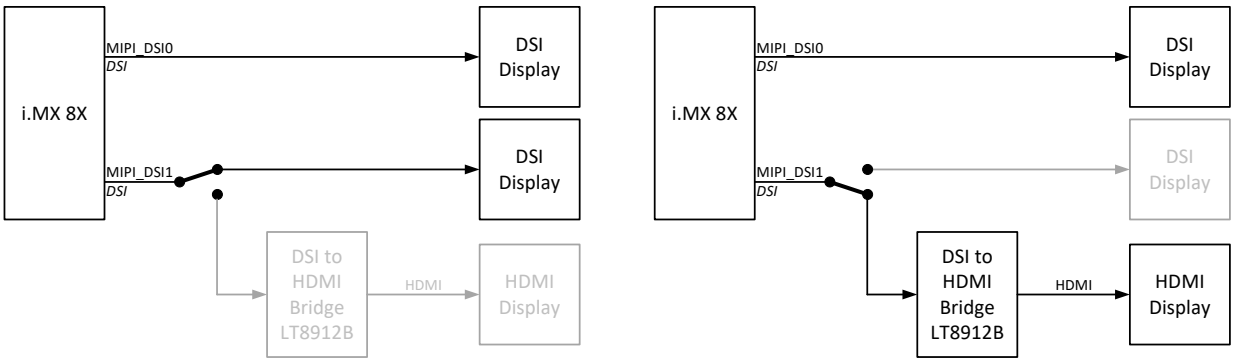


Figure 17: Possible DSI Display configurations

Table 5-39 DSI interface signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
248	LVDS1_A_CLK+	MIPI_DSI0_CLK_P	MIPI_DSI0.CKP	O	DSI Interface 1 clock
246	LVDS1_A_CLK-	MIPI_DSI0_CLK_N	MIPI_DSI0.CKN		
254	LVDS1_A_TX0+	MIPI_DSI0_DATA0_P	MIPI_DSI0.DP0	I/O	DSI Interface 1 data lane 1
252	LVDS1_A_TX0-	MIPI_DSI0_DATA0_N	MIPI_DSI0.DN0		
260	LVDS1_A_TX1+	MIPI_DSI0_DATA1_P	MIPI_DSI0.DP1	O	DSI Interface 1 data lane 2
258	LVDS1_A_TX1-	MIPI_DSI0_DATA1_N	MIPI_DSI0.DN1		
266	LVDS1_A_TX2+	MIPI_DSI0_DATA2_P	MIPI_DSI0.DP2	O	DSI Interface 1 data lane 3
264	LVDS1_A_TX2-	MIPI_DSI0_DATA2_N	MIPI_DSI0.DN2		
272	LVDS1_A_TX3+	MIPI_DSI0_DATA3_P	MIPI_DSI0.DP3	O	DSI Interface 1 data lane 4
270	LVDS1_A_TX3-	MIPI_DSI0_DATA3_N	MIPI_DSI0.DN3		
278	LVDS1_B_CLK+	MIPI_DSI1_CLK_P	MIPI_DSI1.CKP	O	DSI Interface 2 clock
276	LVDS1_B_CLK-	MIPI_DSI1_CLK_N	MIPI_DSI1.CKN		
284	LVDS1_B_TX0+	MIPI_DSI1_DATA0_P	MIPI_DSI1.DP0	I/O	DSI Interface 2 data lane 1
282	LVDS1_B_TX0-	MIPI_DSI1_DATA0_N	MIPI_DSI1.DN0		
290	LVDS1_B_TX1+	MIPI_DSI1_DATA1_P	MIPI_DSI1.DP1	O	DSI Interface 2 data lane 2
288	LVDS1_B_TX1-	MIPI_DSI1_DATA1_N	MIPI_DSI1.DN1		
296	LVDS1_B_TX2+	MIPI_DSI1_DATA2_P	MIPI_DSI1.DP2	O	DSI Interface 2 data lane 3
294	LVDS1_B_TX2-	MIPI_DSI1_DATA2_N	MIPI_DSI1.DN2		
302	LVDS1_B_TX3+	MIPI_DSI1_DATA3_P	MIPI_DSI1.DP3	O	DSI Interface 2 data lane 4
300	LVDS1_B_TX3-	MIPI_DSI1_DATA3_N	MIPI_DSI1.DN3		

5.7 Camera Interface

The i.MX 8X SoC features a single Imagining Subsystem with three input sources and stores streams into the memory. The subsystem consists of the Imaging Sensor Interface (ISI), MJPEG Encoder, and Decoder. The three input sources are the MIPI CSI-2, the parallel camera input port, and an internal link from the Display Controller.

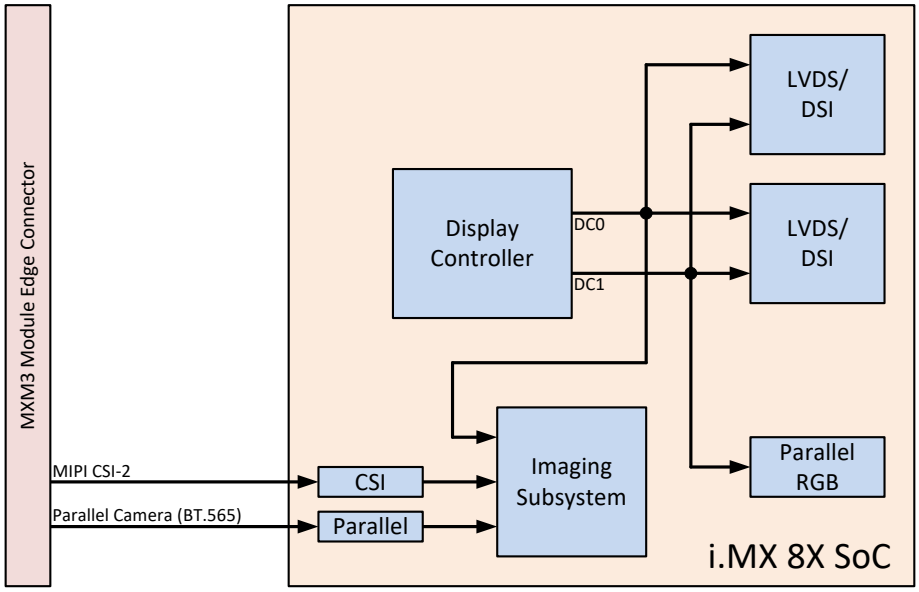


Figure 18: Display and Imaging Block Diagram

5.7.1 Parallel Camera Interface

The i.MX 8X SoC itself features one parallel camera interface called Parallel Capture Interface (PI_CI). In some parts of the NXP documentation, the term CMOS sensor interface (CSI) is used. It is important not to confuse this name with the interface standard MIPI/CSI-2, a serial camera interface.

The camera interface on the i.MX 8X SoC features up to 10 data bits. However, only 8-bit BT.656 is compatible with other Apalis modules. The remaining two bits are located as an alternate function of the camera sync signals.

Features:

- Raw (Bayer), RGB, YUV, YCbCr input
- Support for CCIR656 (BT.656)
- Maximum pixel clock frequency 150 MHz
- 8/10-bit parallel video interface
- Dedicated synchronization signals (VSYNC, HSYNC) or embedded in the data stream (BT.656)

Table 5-40 Parallel Camera Interface Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
187	CAM1_D0	CSI_D00	CI_PI.CSI_D02	I	Camera pixel data
185	CAM1_D1	CSI_D01	CI_PI.CSI_D03	I	Camera pixel data
183	CAM1_D2	CSI_D02	CI_PI.CSI_D04	I	Camera pixel data
181	CAM1_D3	CSI_D03	CI_PI.CSI_D05	I	Camera pixel data
179	CAM1_D4	CSI_D04	CI_PI.CSI_D06	I	Camera pixel data
177	CAM1_D5	CSI_D05	CI_PI.CSI_D07	I	Camera pixel data
175	CAM1_D6	CSI_D06	CI_PI.CSI_D08	I	Camera pixel data
173	CAM1_D7	CSI_D07	CI_PI.CSI_D09	I	Camera pixel data
191	CAM1_PCLK	CSI_PCLK	CI_PI.CSI_PCLK	I	Camera pixel clock
197	CAM1_HSYNC	CSI_HSYNC	CI_PI.CSI_HSYNC	I	Camera horizontal sync
195	CAM1_VSYNC	CSI_VSYNC	CI_PI.CSI_VSYNC	I	Camera vertical sync
193	CAM1_MCLK	CSI_MCLK	CI_PI.CSI_MCLK	O	Camera reference clock output

Table 5-41 Additional Parallel Camera Interface Pins (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
197	CAM1_HSYNC	CSI_HSYNC	CI_PI.CSI_D00	I	Additional camera pixel data for 10-bit
195	CAM1_VSYNC	CSI_VSYNC	CI_PI.CSI_D01	I	Additional camera pixel data for 10-bit
203	I2C3_SCL (CAM)	CSI_EN	CI_PI.CSI_EN	O	Camera enable
201	I2C3_SDA (CAM)	CSI_RESET	CI_PI.CSI_RESET	O	Camera reset
203	I2C3_SCL (CAM)	CSI_EN	CI_PI.CSI_I2C.SCL	I/O	Dedicated I^2C interface for the parallel camera
201	I2C3_SDA (CAM)	CSI_RESET	CI_PI.CSI_I2C.SDA	I/O	

Table 5-42 Camera Interface Color Pin Mapping

i.MX 8X Port Name	Bayer 10-bit Generic	BT.656/ YUV 8-bit/ CCIR656	RGB888 8-bit 3 cycle	YCbCr 8-bit 2 cycle
CSI_D00	D0			
CSI_D01	D1			
CSI_D02	D2	Y/C0	R/G/B0	Y/C0
CSI_D03	D3	Y/C1	R/G/B1	Y/C1
CSI_D04	D4	Y/C2	R/G/B2	Y/C2
CSI_D05	D5	Y/C3	R/G/B3	Y/C3
CSI_D06	D6	Y/C4	R/G/B4	Y/C4
CSI_D07	D7	Y/C5	R/G/B5	Y/C5
CSI_D08	D8	Y/C6	R/G/B6	Y/C6
CSI_D09	D9	Y/C7	R/G/B7	Y/C7

5.7.2 Camera Serial Interface (MIPI CSI-2)

The NXP i.MX 8X supports one quad lane MIPI CSI-2 interface for connecting compatible cameras. The interface is compatible with single and dual lane CSI cameras. The interface uses MIPI D-PHY as the physical layer. The interface supports RGB, YUV, and RAW color space definitions. 24-bit down to 6-bit per pixel are supported.

The MIPI CSI-2 signals are located in the type-specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules will be compatible with this interface. If you plan to use the CSI interface, please be aware that other modules may not be compatible with your carrier board.

Features

- Scalable data lane support, 1 to 4 Data Lanes
- Up to 1.5Gbps per lane, providing 4K30 capability for the 4 lanes
- Supports 10Mbps data rate in low power modes
- Implements all three CSI-2 MIPI layers (pixel to byte backing, low-level protocol, and lane management)
- Unidirectional master operation supported

As the CSI is a high-speed interface, some additional layout requirements need to be followed on the carrier board. These requirements are not defined in the Apalis Carrier Board Design Guide as this interface is type-specific. Please find the related information in the table below.

Table 5-43 CSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	750MHz (1.5GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-Pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-44 CSI interface signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	CSI Signal Name	I/O	Description
163	TS_DIFF18+	MIPI_CSI0_CLK_P	CSI1_CLK+	I	CSI interface 1 clock
161	TS_DIFF18-	MIPI_CSI0_CLK_N	CSI1_CLK-	I	
157	TS_DIFF17+	MIPI_CSI0_DATA0_P	CSI1_D1+	I/O	CSI interface 1 data lane 1
155	TS_DIFF17-	MIPI_CSI0_DATA0_N	CSI1_D1-	I/O	
151	TS_DIFF16+	MIPI_CSI0_DATA1_P	CSI1_D2+	I	CSI interface 1 data lane 2
149	TS_DIFF16-	MIPI_CSI0_DATA1_N	CSI1_D2-	I	
145	TS_DIFF15+	MIPI_CSI0_DATA2_P	CSI1_D3+	I	CSI interface 1 data lane 3
143	TS_DIFF15-	MIPI_CSI0_DATA2_N	CSI1_D3-	I	
139	TS_DIFF14+	MIPI_CSI0_DATA3_P	CSI1_D4+	I	CSI interface 1 data lane 4
137	TS_DIFF14-	MIPI_CSI0_DATA3_N	CSI1_D4-	I	

Table 5-45 Additional Camera Interface Signals (Apalis Standard)

X1 Pin#	Apalis Signal Name	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
201	I2C3_SDA (CAM)	CSI_RESET	ADMA.I2C3.SDA	I/O	Camera control I^2C
203	I2C3_SCL (CAM)	CSI_EN	ADMA.I2C3.SCL	O	Camera control I^2C

5.8 PCI Express

The NXP i.MX 8X SoC features a single-lane PCI Express (PCIe) interface. The PCIe interface is compliant with the PCIe 3.0 specification and supports an 8Gb/s data rate. It is backward-compatible with the PCIe 2.0 and 1.1 standards which support 5Gb/s and 2.5Gb/s.

PCIe is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 5-46 PCIe Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
55	PCIE1_CLK+	PCIE_REFCLK100M_P	HSIO.PCIE_IOB.EXT_REFCLK100M_P	O	100MHz Reference clock differential pair. Sourced by a reference clock oscillator
53	PCIE1_CLK-	PCIE_REFCLK100M_N	HSIO.PCIE_IOB.EXT_REFCLK100M_N		
49	PCIE1_TX+	PCIE0_TX0_P	HSIO.PCIE0.TX0_P	O	Apalis standard PCIe interface Transmit data lane 0
47	PCIE1_TX-	PCIE0_TX0_N	HSIO.PCIE0.TX0_N		
43	PCIE1_RX+	PCIE0_RX0_P	HSIO.PCIE0.RX0_P	I	Apalis standard PCIe interface Receive data lane 0
41	PCIE1_RX-	PCIE0_RX0_N	HSIO.PCIE0.RX0_N		

Table 5-47 Additional PCIe Control Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
37	WAKE1_MICO	MIPI_DSI0_I2C0_SDA	LSIO.GPIO1.IO26	I	General-purpose wake signal
26	RESET_MOCI#			O	General reset output
209	I2C1_SDA	USB_SS3_TC3	ADMA.I2C1.SDA	I/O	Some PCIe devices need the SMB interface for special configurations. I2C1 should be used if the interface is necessary
211	I2C1_SCL	USB_SS3_TC0	ADMA.I2C1.SCL	O	

5.9 SATA

The Apalis iMX8X does not feature a SATA interface. The pins on the module edge connector are left unconnected.

5.10 I²C

The i.MX 8X SoC features a total number of ten I²C controllers. Not all of these interfaces are available externally. Some of them are dedicated interfaces with limited function.

- General-purpose I²C with DMA support
  - 4x general-purpose I²C. Three of them are available on the module edge connector (two as standard Apalis I²C, one as an alternate function). The fourth port is used on the module for the audio codec, the GPIO expander, HDMI bridge, and USB hub.
  - 1x I²C interface that is tightly coupled with the Cortex-M4 core. It is available as an alternate function.
- Low-speed I²C without DMA support for a dedicated purpose. It could also be used as general-purpose but require the associated PHY (for example, MIPI) to be powered on
  - 2x master I²C for LVDS and MIPI/DSI. One available as standard Apalis I²C, the other one as an alternate function.
  - 1x master I²C for MIPI/CSI-2, available externally as an alternate function.
  - 1x master I²C for parallel camera input, available externally as an alternate function.
- I²C tightly coupled with SCU
  - 1x Dedicated for PMIC, cannot be used externally

The Apalis module standard features only three I²C interfaces. The rest of the available interfaces are alternate functions of other interface pins. These additional interfaces are not compatible with other Apalis modules. Therefore, it is highly recommended to use the three standard I2C interfaces primarily.

General-purpose I²C ports features:

- Supports standard and fast mode of operation (0-400KHz), Fm+ (1Mbit/s), and high-speed mode (3.2 MHz).
- System Management Bus (SMBus) compliant specifications
- Master and slave mode (slave mode may not be supported in regular BSP)
- Multi-master support
- Clock stretching support
- 7-bit or 10-bit addressing
- DMA support

Table 5-48 Apalis standard I²C Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I2C Port	Description
209	I2C1_SDA	USB_SS3_TC3	ADMA.I2C1.SDA	I2C1	Generic I²C
211	I2C1_SCL	USB_SS3_TC0	ADMA.I2C1.SCL		
205	I2C2_SDA (DDC)	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA	MIPI_DSI1	I²C port for the DDC interface. It is a low-speed I²C that can also be used for general purpose
207	I2C2_SCL (DDC)	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL		
201	I2C3_SDA (CAM)	CSI_RESET	ADMA.I2C3.SDA	I2C3	I²C port for the camera interface, can also be used for other purposes
203	I2C3_SCL (CAM)	CSI_EN	ADMA.I2C3.SCL		

Some of the I²C ports used as Apalis standard I²C interfaces are also available on alternate pins. Use them only if there is a conflict with the compatible pins.

Table 5-49 Alternate Pins for Standard I²C Signals (not compatible with other Apalis family modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I2C Port	Description
262	USBO1_OC#	USB_SS3_TC2	ADMA.I2C1.SDA	I2C1	Alternate pins for the generic I²C
6	PWM3	MIPI_DSI0_GPIO0_01			
84	USBH_EN	USB_SS3_TC1	ADMA.I2C1.SCL		
4	PWM2	MIPI_DSI0_GPIO0_00			
249	LCD1_DE	MCLK_IN1	ADMA.I2C3.SDA	I2C3	Alternate pins for the camera interface I²C
263	LCD1_R6	SPI3_CS1	ADMA.I2C3.SCL		

Table 5-50 Additional General Purpose I²C Signals (not compatible with other Apalis family modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I2C Port	Description
8	PWM4	MIPI_DSI1_GPIO0_01	ADMA.I2C2.SDA	I2C2	General-purpose I²C
239	BKL1_PWM	MIPI_DSI1_GPIO0_00	ADMA.I2C2.SCL		

Table 5-51 Tightly coupled M4 I²C Signals (not compatible with other Apalis family modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	Description
225	SPI1_MOSI	SPI0_SDO	M40.I2C0.SDA	Dedicated I²C port for the M4 core.
307	AN1_ADC1	ADC_IN1		Dedicated I²C port for the M4 core. 1.8V signal!
221	SPI1_CLK	SPI0_SCK	M40.I2C0.SCL	Dedicated I²C port for the M4 core.
305	AN1_ADC0	ADC_IN0		Dedicated I²C port for the M4 core. 1.8V signal!

Table 5-52 Dedicated low-speed I²C Signals (not compatible with other Apalis family modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	Description
193	CAM1_MCLK	CSI_MCLK	MIPI_CSI0.I2C0.SDA	Dedicated I²C port for the CSI camera
191	CAM1_PCLK	CSI_PCLK	MIPI_CSI0.I2C0.SCL	
37	WAKE1_MICO	MIPI_DSI0_I2C0_SDA	MIPI_DSI0.I2C0.SDA	Dedicated I²C port for the LVDS/DSI port
35	SATA1_ACT#	MIPI_DSI0_I2C0_SCL	MIPI_DSI0.I2C0.SCL	
201	I2C3_SDA (CAM)	CSI_RESET	CI_PI.CSI_I2C.SDA	Dedicated I²C port for the parallel Camera input
203	I2C3_SCL (CAM)	CSI_EN	CI_PI.CSI_I2C.SCL	

5.10.1 Real-Team Clock (RTC) recommendation

The Apalis module features an RTC circuit that is located inside the SoC. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for time-keeping. As long as the main power supply is provided to the module, the RTC is sourced from this rail. If the RTC needs to be retained even without the module's main voltage, a coin cell needs to be applied to the VCC_BACKUP (pin 174) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section **Error! Reference source not found.**). Therefore, a standard l ithium coin cell battery can drain faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the

carrier board instead. In this case, add the external RTC to the I2C1 (pin 209/211) interface of the module and leave the VCC_BACKUP pin unconnected. A suitable reference schematic can be found in the schematic diagram of the Apalis evaluation board.

5.11 UART

The i.MX 8X SoC features a total number of six UARTs. Four regular UARTs are available on the standard Apalis module edge connector pins and therefore are compatible with other Apalis modules. Additional to the regular UARTs, the SoC features one UART, tightly coupled with the Cortex-M4 core. The last UART is tightly coupled to the System Controller Unit. It is used for the debugging messages of the SCU.

The Apalis UART1 is, according to the Apalis specification, a full-featured UART. The i.MX 8X does not feature the DTR, DSR, DCD, and RI signals. The CTS and RTS signals of this port are only available as alternate functions of the PWM and parallel LCD interface. Therefore, the UART1 on the Apalis iMX8X only features RX and TX. There are no other hardware control signals on their standard location. The UART1 is used as a standard debug interface for the Toradex Linux operating systems. Therefore, it is desirable to keep this port accessible for system debugging.

General-purpose UART Features

- Full-duplex, standard non-return-to-zero (NRZ format)
- Programmable baud rates
- Interrupt, DMA, or polled operation.
- Hardware parity generation and checking
- Character length 7- to 10-bit
- Programmable 1-bit or 2-bit stop bits
- Idle line, address mark, and receive data match wakeup method
- Automatic address matching to reduce ISR overhead
- IrDA 1.4 support

Table 5-53 UART1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
118	UART1_RXD	UART1_RX	ADMA.UART1.RX	I	Received Data
112	UART1_TXD	UART1_TX	ADMA.UART1.TX	O	Transmitted Data

Table 5-54 UART2 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
132	UART2_RXD	UART0_RX	ADMA.UART0.RX	I	Received Data
126	UART2_TXD	UART0_TX	ADMA.UART0.TX	O	Transmitted Data
128	UART2_RTS	FLEXCAN0_RX	ADMA.UART0.RTS_B	O	Request to Send
130	UART2_CTS	FLEXCAN0_TX	ADMA.UART0.CTS_B	I	Clear to Send

Table 5-55 UART3 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
136	UART3_RXD	UART2_RX	ADMA.UART2.RX	I	Received Data
134	UART3_TXD	UART2_TX	ADMA.UART2.TX	O	Transmitted Data

Since the UART4 is located on SoC pins that are only 1.8V, there is a bidirectional level shifter on the module for these pins. Be aware of the limited performance of these signal pins.

Table 5-56 UART4 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
140	UART4_RXD	SCU_GPIO0_00	ADMA.UART3.RX	I	Received Data, bidirectional level shifter on the module
138	UART4_TXD	SCU_GPIO0_01	ADMA.UART3.TX	O	Transmitted Data, bidirectional level shifter on the module

For the UART1 and UART4, there are additional hardware flow signals available. The signals are not compatible with other Apalis modules.

Table 5-57 Additional UART1 and UART 4 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
2	PWM1	UART1_RTS_B	ADMA.UART1.RTS_B	O	Additional Request to Send for UART 1
265	LCD1_R7	UART1_CTS_B	ADMA.UART1.CTS_B	I	Additional Clear to Send UART 1
146	MMC1_D3	USDHC1_DATA3	ADMA.UART3.RTS_B	O	Additional Request to Send for UART 4
144	MMC1_D2	USDHC1_DATA2	ADMA.UART3.CTS_B	I	Additional Clear to Send UART 4

For the UART3, there are alternate pins available. However, for compatibility purposes, it is recommended to use the standard Apalis pins instead.

Table 5-58 Alternate UART4 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
154	MMC1_CLK	USDHC1_CLK	ADMA.UART3.RX	I	Alternate Received Data for UART 4
16	CAN2_RX	FLEXCAN2_RX			
162	MMC1_D1	USDHC1_DATA1	ADMA.UART3.TX	O	Alternate Transmitted Data for UART 4
18	CAN2_TX	FLEXCAN2_TX			

For the M4 core, there is a tightly coupled UART available. The pins are located on the RX and TX signals of the Apalis standard UART4. Since these pins feature a bidirectional level shifter on the module, the performance is limited.

Table 5-59 Tightly Coupled M4 UART Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
140	UART4_RXD	SCU_GPIO0_00	M40.UART0.RX	I	Received Data tightly coupled with M4, bidirectional level shifter on the module
138	UART4_TXD	SCU_GPIO0_01	M40.UART0.TX	O	Transmitted Data tightly coupled with M4, bidirectional level shifter on the module

The System Controller Unit (SCU) has its own tightly coupled UART interface. The interface is used as a debug port for the SCU. The interface cannot be used as a general-purpose UART. The pins are only available on to different alternate function sets. Please be aware that the alternate function set on pin 138/140 features a bidirectional level shifter.

Table 5-60 Tightly Coupled SCU UART Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
132	UART2_RXD	UART0_RX	SCU.UART0.RX	I	Received Data, debug interface of system controller unit, bidirectional level shifter on pin 140
140	UART4_RXD	SCU_GPIO0_00			
126	UART2_TXD	UART0_TX	SCU.UART0.TX	O	Transmitted Data, debug interface of system controller unit, bidirectional level shifter on pin 138
138	UART4_TXD	SCU_GPIO0_01			

5.12 SPI

The i.MX 8X SoC features a total of four SPI interfaces. Two of them are available on the Apalis module standard pins. The other two ports are also available. They are located on alternate functions of other interfaces

The SPI ports operate at up to 60MHz in master mode and up to 40MHz in slave mode. However, there are exceptions. Some of the additional SPI interface pins are limited to 40MHz in master mode and 20MHz in slave mode. Check the NXP datasheet for more information.

Features:

- Up to 60 Mbps in master mode
- Up to 40 Mbps in slave mode
- 32-bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable
- Simultaneous receive and transmit (1-bit mode)
- Wakeup function on receiving data match

Each SPI channel supports four different modes of the SPI protocol:

Table 5-61 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock is positive polarity, and the data is latched on the positive edge of the SCK
1	0	1	The clock is positive polarity, and the data is latched on the negative edge of the SCK
2	1	0	The clock is negative polarity, and the data is latched on the positive edge of the SCK
3	1	1	The clock is negative polarity, and the data is latched on the negative edge of the SCK

Pay attention to the data direction of the signals in master respectively slave mode. The following table describes the data direction of the signals at the module side.

Table 5-62 SPI Signal Direction in Master and Slave Mode

i.MX 8X Port Name	Master Mode		Slave Mode	
	I/O	Description	I/O	Description
SPIx_SDO	O	Master Output, Slave Input	O	Master Input, Slave Output
SPIx_SDI	I	Master Input, Slave Output	I	Master Output, Slave Input
SPIx_CS0	O	Slave Select	I	Slave Select
SPIx_SCK	O	Serial Clock	I	Serial Clock

In the Apalis module standard, only the SPI master mode is specified. Therefore, the slave mode might not be compatible with other modules. The signal direction in the following tables corresponds to the SPI master mode.

Table 5-63 Apalis SPI Port 1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
225	SPI1_MOSI	SPI0_SDO	ADMA.SPI0.SDO	O	Master Output, Slave Input
223	SPI1_MISO	SPI0_SDI	ADMA.SPI0.SDI	I	Master Input, Slave Output
227	SPI1_CS	SPI0_CS0	ADMA.SPI0.CS0	I/O	Slave Select
221	SPI1_CLK	SPI0_SCK	ADMA.SPI0.SCK	I/O	Serial Clock

Table 5-64 Apalis SPI Port 2 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
231	SPI2_MOSI	SPI2_SDO	ADMA.SPI2.SDO	O	Master Output, Slave Input
229	SPI2_MISO	SPI2_SDI	ADMA.SPI2.SDI	I	Master Input, Slave Output
233	SPI2_CS	SPI2_CS0	ADMA.SPI2.CS0	I/O	Slave Select
235	SPI2_CLK	SPI2_SCK	ADMA.SPI2.SCK	I/O	Serial Clock

Table 5-65 Additional Signals for Apalis SPI Port 2 (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
243	LCD1_PCLK	MCLK_OUT0	ADMA.SPI2.SDO	O	Alternate pin for Master Output, Slave Input
156	MMC1_D6	USDHC1_WP	ADMA.SPI2.SDI	I	Alternate pin for Master Input, Slave Output
245	LCD1_VSYNC	MCLK_IN0			
164	MMC1_CD#	USDHC1_CD_B	ADMA.SPI2.CS0	I/O	Alternate pin for Slave Select
263	LCD1_R6	SPI3_CS1			
204	DAP1_SYNC	SAI0_TXFS	ADMA.SPI2.CS1	O	Secondary Slave Select
152	MMC1_D5	USDHC1_RESET_B	ADMA.SPI2.SCK	I/O	Alternate pin for Serial Clock
249	LCD1_DE	MCLK_IN1			

Table 5-66 Additional SPI ports, incompatible with other modules

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
259	LCD1_R4	SPI3_SDO	ADMA.SPI3.SDO	O	Master Output, Slave Input
261	LCD1_R5	SPI3_SDI	ADMA.SPI3.SDI	I	Master Input, Slave Output
247	LCD1_HSYNC	SPI3_CS0	ADMA.SPI3.CS0	I/O	Slave Select
263	LCD1_R6	SPI3_CS1	ADMA.SPI3.CS1	O	Slave Select
257	LCD1_R3	SPI3_SCK	ADMA.SPI3.SCK	I/O	Serial Clock
193	CAM1_MCLK	CSI_MCLK	ADMA.SPI1.SDO	O	Master Output, Slave Input
196	DAP1_D_OUT	SAI0_TXD			
200	DAP1_BIT_CLK	SAI0_TXC	ADMA.SPI1.SDI	I	Master Input, Slave Output
203	I2C3_SCL (CAM)	CSI_EN			
201	I2C3_SDA (CAM)	CSI_RESET	ADMA.SPI1.CS0	I/O	Slave Select
202	DAP1_D_IN	SAI0_RXD			
191	CAM1_PCLK	CSI_PCLK	ADMA.SPI1.SCK	I/O	Serial Clock
204	DAP1_SYNC	SAI0_TXFS			

5.13 PWM (Pulse Width Modulation)

The i.MX 8X features a four-channel general-purpose Pulse Width Modulator (PWM). It has a 16-bit counter and is optimized to generate simple sound samples and generate tones. It has a 16-bit resolution, and there is a 4-level deep FIFO available to minimize the interrupt overhead. There is a 12-bit prescaler available for dividing the clock. Due to the SoC's multiplexing limitations, only one of the four general-purpose PWM signals is available on the module edge connector as Apalis standard PWM signal. The rest of the general-purpose PWM signals are available as an alternate function.

Additional to the general-purpose PWM, the i.MX 8X features dedicated PWM generators for the parallel LCD and the LVDS and MIPI/DSI interfaces. One of the DSI PWMs is available as the second Apalis standard PWM while the other is available as an alternate function. The dedicated PWM of the parallel LCD interface is not available on the module edge connector.

The third and fourth Apalis standard PWM outputs (pin 6 and 8) on the Apalis iMX8X module are only served with standard GPIOs. There is no dedicated PWM function available on these pins. This means on these two module edge pins, only GPIO bit-banged PWM is possible.

Table 5-67 General Purpose PWM Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
2	PWM1	UART1_RTS_B	LSIO.PWM2.OUT	O	PWM Output 1 (general purpose PWM)
4	PWM2	MIPI_DSI0_GPIO0_00	MIPI_DSI0.PWM0.OUT	O	PWM Output 2 (dedicated DSI PWM)
6	PWM3	MIPI_DSI0_GPIO0_01	LSIO.GPIO1.IO28	O	These pins are **only GPIOs**. There is no PWM function available. It is only possible to bit-bang the GPIO for a simple PWM application.
8	PWM4	MIPI_DSI1_GPIO0_01	LSIO.GPIO2.IO00	O	
239	BKL1_PWM	MIPI_DSI1_GPIO0_00	MIPI_DSI1.PWM0.OUT	O	Apalis standard backlight PWM output. Use this output for the DSI/LVDS, and LCD RGB interface, compatible with other Apalis modules

Table 5-68 Locations of additional PWM Interface Signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
112	UART1_TXD	UART1_TX	LSIO.PWM0.OUT	O	General Purpose GPIO
118	UART1_RXD	UART1_RX	LSIO.PWM1.OUT	O	General Purpose GPIO
265	LCD1_R7	UART1_CTS_B	LSIO.PWM3.OUT	O	General Purpose GPIO

Besides the standard PWM interfaces, the i.MX 8X features a Timer PWM Modules (TPM), tightly coupled to the Cortex M4 core. The TPM is based on a simple timer known for many years from the HCS08 8-bit microcontrollers. Besides generating PWM signals, it can also be used for input-capture and output-compare functions. The TPM is dedicated to the M4 core. However, there is a FlexTimer (FTM) module for the main cores. The FTM builds upon the TPM, but enhances it by additional dead time insertion hardware, fault control input, signed up counter function, enhancing the triggering functionality, and allowing the polarity and initialization to be controlled. The FTM, as well as the TPM for the M4 core, are available on the module edge connector as alternate functions.

Table 5-69 TPM and FTM Interface Signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
223	SPI1_MISO	SPI0_SDI	M40.TPM0.CH0	I/O	Timer PWM Module output tightly coupled with the Cortex M4 core. **Pin 309 and 311 are only 1.8V!**
309	AN1_ADC2	ADC_IN4			
227	SPI1_CS	SPI0_CS0	M40.TPM0.CH1	I/O	
311	AN1_TSWIP_ADC3	ADC_IN5			
136	UART3_RXD	UART2_RX	ADMA.FTM.CH0	I/O	Flex Timer Module channel signals. It can be used with all the CPU cores
134	UART3_TXD	UART2_TX	ADMA.FTM.CH1	I/O	
12	CAN1_RX	FLEXCAN1_RX	ADMA.FTM.CH2	I/O	

5.14 OWR (One-Wire)

The Apalis iMX8X does not feature a One-Wire interface. However, it is possible to implement a bit-banging One Wire driver.

5.15 SD/MMC

The i.MX 8X SoC provides two SDIO interfaces; one is used internally for the eMMC Flash. The other is available on the module edge connector Pins as Apalis standard MMC (4-bit) interface. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, and eMMC devices.

Since the SoC does not feature a third SDIO interface, the second Apalis port cannot be served. This means the signals of the Apalis SD card interface are left unconnected on the Apalis iMX8X.

i.MX 8X SDIO interface	Max Bus Width	Description
USDHC0 / EMMC0	8-bit	Connected to the internal eMMC boot device. Not available at the module edge connector
USDHC1	4-bit	Apalis Standard MMC1 interface
Not available on Apalis iMX8X		Apalis Standard SD1 interface

Features:

- Supports SD Memory Card Specification 2.0 and 3.0
- Supports SDIO Card Specification Version 2.0 and 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, 4.41, 5.0, and 5.1
- Supports addressing larger capacity SD 3.0 or SDXC cards up to 2 TByte
- Supports SPI mode
- Supports SD UHS-I mode (up to 208MHz) with a 1.8V IO voltage level.
- 3.3V and 1.8V IO voltage mode supported (Apalis standard is only 3.3V)

According to the Apalis module specification, the SD/MMC interface's IO voltage level supports only a 3.3V logic level. Therefore, the SD interfaces are limited to default or high-speed mode; UHS-I modes are not supported in the Apalis standard. Nevertheless, the MMC1 interface (i.MX 8X USDHC1) can switch to the 1.8V IO level. This allows using the interface in UHS-I mode with higher speed. Please note that this IO voltage level is not mandatory in the Apalis module specification, and therefore other modules might not support this mode. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interfaces are used in the 1.8V mode, it is recommended to remove the pull-up resistors on the carrier board. The i.MX 8X features internal pull-up resistors that can be used instead.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MByte/s	3.3V	Apalis Standard
High Speed	50 MHz	25 MByte/s	3.3V	
SDR12	25 MHz	12.5 MByte/s	1.8V	UHS-I May not compatible with other modules
SDR25	50 MHz	25 MByte/s	1.8V	
DDR50	50 MHz	50 MByte/s	1.8V	
SDR50	100 MHz	50 MByte/s	1.8V	
SDR104	208 MHz	104 MByte/s	1.8V	

The I/O voltage of the SDIO power block can be changed independently from the other I/O blocks, but all SDIO block signals change their voltages together. The I/O voltage of the Apalis MMC1 interface (i.MX 8X USDHC1) is provided by the LDO2OUT output of the power management IC (PMIC). The voltages are changed by controlling the VSELECT input of the PMIC.

Table 5-70 Apalis MMC1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
150	MMC1_CMD	USDHC1_CMD	CONN.USDHC1.CMD	I/O	Command
160	MMC1_D0	USDHC1_DATA0	CONN.USDHC1.DATA0	I/O	Serial Data 0
162	MMC1_D1	USDHC1_DATA1	CONN.USDHC1.DATA1	I/O	Serial Data 1
144	MMC1_D2	USDHC1_DATA2	CONN.USDHC1.DATA2	I/O	Serial Data 2
146	MMC1_D3	USDHC1_DATA3	CONN.USDHC1.DATA3	I/O	Serial Data 3
154	MMC1_CLK	USDHC1_CLK	CONN.USDHC1.CLK	O	Serial Clock
164	MMC1_CD#	USDHC1_CD_B	CONN.USDHC1.CD_B	I	Card Detect

There are a few extra interface signals available for the MMC1 interface. These pins are not required for regular usage of the interface. The signals are available as alternate functions and therefore are not compatible with other Apalis modules.

Table 5-71 Additional MMC1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
152	MMC1_D5	USDHC1_RESET_B	CONN.USDHC1.RESET_B	I	Card reset signal
156	MMC1_D6	USDHC1_WP	CONN.USDHC1.WP	I	Card write protect

5.16 Analog Audio

The Apalis iMX8X offers analog audio input and output channels. On the module, an NXP SGTL5000 chip handles the analog audio interface. The SGTL5000 is connected over I²S (SAI1) with the i.MX 8X SoC. Please consult the NXP SGTL5000 datasheet for more information.

Table 5-72 Analogue Audio Interface Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Pin on the SGTL5000 (20pin QFN)
306	AAP1_MICIN	Analogue Input	Microphone input	10
310	AAP1_LIN_L	Analogue Input	Left Line Input	9
312	AAP1_LIN_R	Analogue Input	Right Line Input	8
316	AAP1_HP_L	Analogue Output	Headphone Left Output	4
318	AAP1_HP_R	Analogue Output	Headphone Right Output	1

5.17 Synchronous Audio Interface (SAI)

The i.MX 8X SoC features four Synchronous Audio Interfaces (SAI). Two of them can transmit and receive audio streams, while the other two interfaces can only receive. The Apalis form factor features one audio codec interface as standard SAI0 is connected to this interface. Besides this standard audio interface, the remaining three digital audio interfaces are also available on the module edge connector as an alternate function. However, one full-featured interface (SAI1) is used for the on-module SGTL5000 audio codec. The interface is still available on the external module edge pin connector but can only be used if the internal codec is not in use.

Table 5-73 SAI Instance Configuration

SAI Instance	Tx/Rx Data Lines (stereo)	Tx/Rx FIFO Depth	Use Case
SAI0	1/1	64/64	Apalis standard digital audio interface
SAI1	1/1	64/64	On-module audio codec. Also available externally but can only be used if the internal codec is not in use. It is also connected internally to the MQS subsystem
SAI2	0/1	-/64	Input only, Available on module edge connector as an alternate function, not compatible with other modules
SAI3	0/1	-/64	Input only, Available on module edge connector as an alternate function, not compatible with other modules
SAI4	1/1	64/64	Audio Mixer interface, SoC internal connection
SAI5	0/1	-/64	Audio Mixer interface, SoC internal connection

The SAI interfaces can be used as Intel® Audio Codec '97 (also known as AC'97 or AC97) or as I2S (also known as Inter-IC Sound, Integrated Interchip Sound, or IIS). The interfaces can be used to connect an additional external audio codec. Please be aware that some Apalis modules may

provide different codec standards such as HD Audio or just a subset of AC97 and I2S on this interface. The SAI on the Apalis iMX8X cannot be used as an HD Audio interface.

Table 5-74 Standard Digital Audio Port Signals (compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
202	DAP1_D_IN	SAI0_RXD	ADMA.SAI0.RXD	I	Data Input to i.MX 8X
196	DAP1_D_OUT	SAI0_TXD	ADMA.SAI0.TXD	O	Data Output from i.MX 8X
204	DAP1_SYNC	SAI0_TXFS	ADMA.SAI0.TXFS	I/O	Field Select (Transmit Frame Sync)
200	DAP1_BIT_CLK	SAI0_TXC	ADMA.SAI0.TXC	I/O	Serial Clock (Transmit Bit Clock)
198	DAP1_RESET	QSPI0A_SS1_B	LSIO.GPIO3.IO15	O	Audio codec reset (regular GPO)
194	DAP1_MCLK	ADC_IN3	ADMA.ACM.MCLK_OUT0	O	Master clock output. Shared with internal codec. Level shifted.

For controlling the I²S codec, an additional I²C interface is required, and the generic I²C interface I2C1is recommended for this purpose. Some codecs need an external master reference clock. According to the Apalis standard, the module edge connector pin number 194 should be used as the master clock. The Apalis iMX8X features a master clock output on pin 194. However, the SoC pin is shared with the internal codec and is level-shifted. Therefore, the clock frequency must be the same as long as the internal codec is also in use. There is a second audio codec master clock available, but only as an alternate function that is not pin-compatible with other Apalis modules.

Table 5-75 Alternate Master Clock Pins (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
247	LCD1_HSYNC	SPI3_CS0	ADMA.ACM.MCLK_OUT1	O	Master clock output. Independent from on-module codec master clock.
243	LCD1_PCLK	MCLK_OUT0	ADMA.ACM.MCLK_OUT0	O	Master clock output. Same clock source as on-module codec master clock.
245	LCD1_VSYNC	MCLK_IN0	ADMA.ACM.MCLK_IN0	I	Master clock input
249	LCD1_DE	MCLK_IN1	ADMA.ACM.MCLK_IN1	I	Master clock input

Table 5-76 Additional Signals for Standard Digital Audio Port (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
185	CAM1_D1	CSI_D01	ADMA.SAI0.RXD	I	Alternate Data Input to i.MX 8X
227	SPI1_CS	SPI0_CS0			
183	CAM1_D2	CSI_D02	ADMA.SAI0.RXFS	I/O	Field Select (Receive Frame Sync)
187	CAM1_D0	CSI_D00	ADMA.SAI0.RXC	I/O	Serial Clock (Receive Bit Clock)
223	SPI1_MISO	SPI0_SDI	ADMA.SAI0.TXD	O	Alternate Data Output from i.MX 8X
225	SPI1_MOSI	SPI0_SDO	ADMA.SAI0.TXFS	I/O	Alternate Field Select (Transmit Frame Sync)
221	SPI1_CLK	SPI0_SCK	ADMA.SAI0.TXC	I/O	Alternate Serial Clock (Transmit Bit Clock)

The SAI1 is the second full-featured SAI interface of the i.MX 8X. Since this interface is used for the on-module codec, the digital audio interface can only be used if the on-module codec is not used. The SAI1 interface is also shared with the MQS interface inside the SoC.

Table 5-77 SAI1 Signals (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
14	CAN1_TX	FLEXCAN1_TX	ADMA.SAI1.RXD	I	Data Input to i.MX 8X
16	CAN2_RX	FLEXCAN2_RX	ADMA.SAI1.RXFS	I/O	Field Select (Receive Frame Sync)
202	DAP1_D_IN	SAI0_RXD			
18	CAN2_TX	FLEXCAN2_TX	ADMA.SAI1.RXC	I/O	Serial Clock (Receive Bit Clock)
196	DAP1_D_OUT	SAI0_TXD			
12	CAN1_RX	FLEXCAN1_RX	ADMA.SAI1.TXD	O	Data Output from i.MX 8X
200	DAP1_BIT_CLK	SAI0_TXC			
130	UART2_CTS	FLEXCAN0_TX	ADMA.SAI1.TXFS	I/O	Field Select (Transmit Frame Sync)
128	UART2_RTS	FLEXCAN0_RX	ADMA.SAI1.TXC	I/O	Serial Clock (Transmit Bit Clock)

Table 5-78 SAI2 Signals (input only, not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
130	UART2_CTS	FLEXCAN0_TX	ADMA.SAI2.RXD	I	Data Input to i.MX 8X
179	CAM1_D4	CSI_D04			
12	CAN1_RX	FLEXCAN1_RX	ADMA.SAI2.RXFS	I/O	Field Select (Receive Frame Sync)
177	CAM1_D5	CSI_D05			
128	UART2_RTS	FLEXCAN0_RX	ADMA.SAI2.RXC	I/O	Serial Clock (Receive Bit Clock)
181	CAM1_D3	CSI_D03			

Table 5-79 SAI3 Signals (input only, not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
16	CAN2_RX	FLEXCAN2_RX	ADMA.SAI3.RXD	I	Data Input to i.MX 8X
173	CAM1_D7	CSI_D07			
18	CAN2_TX	FLEXCAN2_TX	ADMA.SAI3.RXFS	I/O	Field Select (Receive Frame Sync)
197	CAM1_HSYNC	CSI_HSYNC			
14	CAN1_TX	FLEXCAN1_TX	ADMA.SAI3.RXC	I/O	Serial Clock (Receive Bit Clock)
175	CAM1_D6	CSI_D06			

5.17.1 Synchronous Audio Interface used as I²S

The SAI can be used as I²S interfaces with the following features:

- Master or Slave
- Asynchronous 64x32-bit FIFO for each transmitter and receiver
- Word size from 8-bit to 32-bit

The following signals are used for the I²S interface:

Table 5-80 Synchronous Audio Interface used as Maser I2S

i.MX 8X Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx_TXD	SDIN	O	Serial Data Output from i.MX 8X
SAIx_RXD	SDOUT	I	Serial Data Input to i.MX 8X
SAIx_TXFS	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx_TXC	SCK	I/O	Serial Continuous Clock

Table 5-81 Synchronous Audio Interface used as Slave I²S

i.MX 8X Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx_RXD	SDOUT	I	Serial Data Input to i.MX 8X
SAIx_TXD	SDIN	O	Serial Data Output from i.MX 8X
SAIx_TXFS	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx_TXC	SCK	I/O	Serial Continuous Clock

5.17.2 Synchronous Audio Interface used as AC'97

The SAI interface can be configured as AC'97 compatible interface. The AC'97 Audio interface does not need an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97Audio codec does require a master reference clock, but instead, a separate crystal/oscillator can be used. Please take care of the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host and not to the signal direction.

Table 5-82 Synchronous Audio Interface used as AC'97

i.MX 8X Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx_RXD	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 8X
SAIx_TXD	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 8X
SAIx_TXFS	SYNC	O	AC'97 Audio Sync
SAIx_TXC	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

5.18 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for communication with various serial audio devices, including industry-standard codecs, S/PDIF transceivers, and other DSPs. The interface is only available as an alternate function as it is not part of the Apalis module standard.

Features

- Independent (asynchronous) mode or shared (synchronous) mode of the transmitter and receiver
- Master or slave mode
- Up to 6 transmitters and up to 4 receivers

- Programmable data interface modes (I2S, LSB aligned, MSB aligned)
- Programmable word length (8, 12, 16, 20, or 24-bit)
- AC97 support
- 128word FIFO shared by all transmitters
- 128word FIFO shared by all receivers

Table 5-83 ESAI Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
297	LCD1_B5	ESAI0_SCKT	ADMA.ESAI0.SCKT	I/O	TX serial bit clock
293	LCD1_B3	ESAI0_FST	ADMA.ESAI0.FST	I/O	Frame sync for transmitters and receivers in the synchronous mode and the transmitters only in asynchronous mode
243	LCD1_PCLK	MCLK_OUT0	ADMA.ESAI0.TX_HF_CLK	I/O	TX high-frequency clock
299	LCD1_B6	ESAI0_TX0	ADMA.ESAI0.TX0	I/O	TX data 0
301	LCD1_B7	ESAI0_TX1	ADMA.ESAI0.TX1	I/O	TX data 1
273	LCD1_G2	ESAI0_TX2_RX3	ADMA.ESAI0.TX2_RX3	I/O	TX data 2 or RX data 3
275	LCD1_G3	ESAI0_TX3_RX2	ADMA.ESAI0.TX3_RX2	I/O	TX data 3 or RX data 2
277	LCD1_G4	ESAI0_TX4_RX1	ADMA.ESAI0.TX4_RX1	I/O	TX data 4 or RX data 1
279	LCD1_G5	ESAI0_TX5_RX0	ADMA.ESAI0.TX5_RX0	I/O	TX data 5 or RX data 0
295	LCD1_B4	ESAI0_SCKR	ADMA.ESAI0.SCKR	I/O	RX serial bit clock
291	LCD1_B2	ESAI0_FSR	ADMA.ESAI0.FSR	I/O	RX frame sync signal in asynchronous mode
245	LCD1_VSYNC	MCLK_IN0	ADMA.ESAI0.RX_HF_CLK	I/O	RX high-frequency clock

5.19 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard.

Due to multiplexing limitations of the i.MX 8X SoC, the S/PDIF signals are not available on the Apalis standard module pins. The S/PDIF interface is only available on alternate functions of the parallel RGB interface and therefore not compatible with other Apalis modules.

Features:

- Input sampling rate measurement
- CD-Text
- S/PDIF receiver to S/PDIF transmitter bypass mode
- IEC 60958 consumer format
- Sampling rates from 32kHz to 192kHz

Table 5-84 S/PDIF Data Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
283	LCD1_G7	SPDIF0_TX	ADMA.SPDIF0.TX	O	Serial data output
281	LCD1_G6	SPDIF0_RX	ADMA.SPDIF0.RX	I	Serial data input
255	LCD1_R2	SPDIF0_EXT_CLK	ADMA.SPDIF0.EXT_CLK	I	External clock input

5.20 Medium Quality Sound (MQS)

The medium quality sound interface can be used to generate medium quality audio via a standard GPIO. The PWM output signal does not require an external DAC or codec chip. The advantage over using the high-quality analog audio output of the on-module SGTL5000 is the option to use a simple switching power amplifier circuit (Class-D amplifier).

The MQS is sourced by SAI1 with two-channel 16-bit 44.1 kHz or 48 kHz audio signals, which is basically an I²S signal. Since this is the same SAI channel used by the on-module audio codec, it is impossible to use MQS simultaneous with the analog audio output. The signal-to-noise ratio (SNR) is expected to be no more than 20 dB for signals below 10 kHz. For signals with higher frequencies, the SNR is getting worse.

Table 5-85 MQS Interface Signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
132	UART2_RXD	UART0_RX			
150	MMC1_CMD	USDHC1_CMD	ADMA.MQS.R	O	Right MQS Channel
150	MMC1_CMD	USDHC1_CMD			
126	UART2_TXD	UART0_TX			
160	MMC1_D0	USDHC1_DATA0	ADMA.MQS.L	O	Left MQS Channel
160	MMC1_D0	USDHC1_DATA0			

5.21 Touch Panel Interface

The Apalis iMX8X provides a 4-wire resistive touch interface using the Analog Device AD7879-1 Touchscreen Controller. It is connected with the i.MX 8X SoC via the first I²C interface (ADMA.I2C0). This I²C interface is also connected to the on-module audio codec, the GPIO expander, HDMI bridge, and the USB hub. The AD7879-1 does not support a 5-wire operation mode. Please consult the Analog Device AD7879-1 documentation for more information. The touch interface signals are rated for 1.8V only.

Table 5-86 Touch Interface Pins

X1 Pin#	Apalis Std Function	AD7879-1 Pin#	AD7879-1 Pin Name	I/O	Remarks
315	AN1_TSPX	A3	X+	I/O	X+ (4-wire)
317	AN1_TSMX	C3	X-	I/O	X- (4-wire)
319	AN1_TSPY	B3	Y+	I/O	Y+ (4-wire)
321	AN1_TSMY	D3	Y-	I/O	Y- (4-wire)

5.22 Analogue Inputs

The analog inputs are provided by the NXP i.MX 8X SoC itself. The SoC features one ADCs with six-channel inputs. Only four of these six channels are available on the module edge connector. Pay attention. The input voltage range is only 1.8V and not 3.3V as on other Apalis modules. There are 1k series resistors placed in the ADC lines on the module to protect the SoC input.

Features

- 12-bit ADC
- Linear successive approximation algorithm
- 0 to 1.8V (full scale)
- DMA support
- Trigger detection
- Automatic compare for less-than, greater-than, within range, or out-of-range with “store on true” and “repeat until true” option
- Interrupt support

Table 5-87 Analogue Inputs Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Remarks
305	AN1_ADC0	ADC_IN0	ADMA.ADC.IN0	I	Standard analog input 1 **maximum voltage 1.8V**
307	AN1_ADC1	ADC_IN1	ADMA.ADC.IN1	I	Standard analog input 2 **maximum voltage 1.8V**
309	AN1_ADC2	ADC_IN4	ADMA.ADC.IN4	I	Standard analog input 3 **maximum voltage 1.8V**
311	AN1_TSWIP_ADC3	ADC_IN5	ADMA.ADC.IN5	I	Standard analog input 4 **maximum voltage 1.8V**

5.23 Clock Output

The Apalis iMX8X provides up to two external clock outputs on the module edge connector as a standard interface. One output is dedicated to the camera interface, while the other is for the digital audio interface. The SoC pin of the audio master clock output is shared with the internal codec and is level-shifted. Therefore, the clock frequency must be the same as long as the internal codec is also in use. There is a second audio codec master clock available, but only as an alternate function that is not pin-compatible with other Apalis modules

Table 5-88 Standard Clock Output Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
194	DAP1_MCLK	ADC_IN3	ADMA.ACM.MCLK_OUT0	O	Audio Master clock output. Shared with internal codec. Level shifted.
193	CAM1_MCLK	CSI_MCLK	CI_PI.CSI_MCLK	O	Clock output for the parallel and serial camera interface

Table 5-89 Additional Clock Output Signal Pins (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
247	LCD1_HSYNC	SPI3_CS0	ADMA.ACM.MCLK_OUT1	O	Second master clock output.
243	LCD1_PCLK	MCLK_OUT0	ADMA.ACM.MCLK_OUT0	O	Alternate output for main master clock output. Same clock source as on-module codec master clock.

The PCIe interface requires a 100MHz reference clock for the peripherals and switches. The Apalis standard defines one differential pair for the reference clock. Zero delay clock buffers can be used if more than one reference clock sink is present on the carrier board.

Table 5-90 PCIe Reference clock Signals

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
55	PCIE1_CLK+	PCIE_REFCLK100M_P	HSIO.PCIE_IOB.EXT_REFCLK100M_P	O	100MHz Reference clock differential pair. Sourced by a reference clock oscillator
53	PCIE1_CLK-	PCIE_REFCLK100M_N	HSIO.PCIE_IOB.EXT_REFCLK100M_N		

5.24 Keypad

You can use any free GPIOs to realize a matrix keypad interface. Such a software solution does not come with any additional hardware support. This is the preferred solution if a carrier board needs to be compatible with different Apalis modules.

Additionally, the i.MX 8X SoC features a keyboard controller with hardware support. As the keyboard controller is only available as an alternate function, this interface is incompatible with other Apalis modules. It can only be used if the required pins are being used for their primary function.

The keyboard controller eliminates the requirement for de-bounce capacitors and pull-up resistors. It can handle up to two buttons being pressed without the need for de-ghosting diodes. If the diodes are available, any combination of pressed keys can be detected. The row and column pins can be configured for a keyboard matrix of up to 4 by 4.

Features:

- Open drain design
- Glitch suppression circuit
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- 2-point and 3-point key matrix supported

Table 5-91 Keyboard Matrix Interface Signals (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
11	GPIO5	QSPI0B_SCLK	LSIO.KPP0.COL0	O	Keyboard column 0
13	GPIO6	QSPI0B_DATA0	LSIO.KPP0.COL1	O	Keyboard column 1
15	GPIO7	QSPI0B_DATA1	LSIO.KPP0.COL2	O	Keyboard column 2
17	GPIO8	QSPI0B_DATA2	LSIO.KPP0.COL3	O	Keyboard column 3
1	GPIO1	QSPI0B_DATA3	LSIO.KPP0.ROW0	I	Keyboard row 0
3	GPIO2	QSPI0B_DQS	LSIO.KPP0.ROW1	I	Keyboard row 1
5	GPIO3	QSPI0B_SS0_B	LSIO.KPP0.ROW2	I	Keyboard row 2
7	GPIO4	QSPI0B_SS1_B	LSIO.KPP0.ROW3	I	Keyboard row 3

5.25 Controller Area Network (CAN)

The i.MX 8X SoC features a total of three Flexible Controller Area Network (FlexCAN) interfaces. Two of these three FlexCAN interfaces are available on the Apalis standard pins. The third one is available as alternate functions of GPIO pins. The interfaces fully support CAN-FD (CAN with Flexible Data rate). The CAN protocol complies with the CAN 2.0B specification and ISO11898-1 standard. It features a buffer for up to 64 messages and supports standard and extended message frames.

Features:

- Full implementation of CAN-FD protocol specification
- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of eight-byte data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Timestamp based on 16-bit free-running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 5-92 CAN Signal Pins

X1 Pin#	Apalis Signal Name	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
14	CAN1_TX	FLEXCAN1_TX	ADMA.FLEXCAN1.TX	O	CAN port 1 transmit pin
12	CAN1_RX	FLEXCAN1_RX	ADMA.FLEXCAN1.RX	I	CAN port 1 receive pin
18	CAN2_TX	FLEXCAN2_TX	ADMA.FLEXCAN2.TX	O	CAN port 2 transmit pin
16	CAN2_RX	FLEXCAN2_RX	ADMA.FLEXCAN2.RX	I	CAN port 2 receive pin

Table 5-93 Additional CAN Signal Pins (not compatible with other modules)

X1 Pin#	Apalis Signal Name	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
126	UART2_TXD	UART0_TX	ADMA.FLEXCAN0.TX	O	CAN port 3 transmit pin
130	UART2_CTS	FLEXCAN0_TX			
128	UART2_RTS	FLEXCAN0_RX	ADMA.FLEXCAN0.RX	I	CAN port 3 receive pin
132	UART2_RXD	UART0_RX			
134	UART3_TXD	UART2_TX	ADMA.FLEXCAN1.TX	O	Alternate CAN port 1 transmit pin
136	UART3_RXD	UART2_RX	ADMA.FLEXCAN1.RX	I	Alternate CAN port 1 receive pin

5.26 Media Local Bus (MLB150)

The Media Local Bus is predominantly used in automotive for high-bandwidth audio-video and control information transport. MLB is a standardized on-PCB, inter-chip communication bus for MOST (Media Oriented Systems Transport) based devices. As MLB is not part of the Apalis module specifications, the interface is not compatible with other Apalis modules. The i.MX 8X SoC features a 3-pin (single-ended) interface for the MLB. The standard Toradex BSP might not support the MLB interface.

Table 5-94 MLB Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
293	LCD1_B3	ESAI0_FST	CONN.MLB.CLK	I	Single-ended clock
299	LCD1_B6	ESAI0_TX0	CONN.MLB.DATA	I/O	Single-ended data
297	LCD1_B5	ESAI0_SCKT	CONN.MLB.SIG	I/O	Single-ended signal

5.27 Flexible SPI Controller (FlexSPI)/ Quad Serial Peripheral Interface (QuadSPI, QSPI)

Additional to the regular SPI controller (which is called LPSPI in the NXP documentation), the i.MX 8X features a Flexible SPI Controller (FlexSPI). The controller supports single, dual, quad, and octal mode data transfer. It can be used for interfacing NAND, and NOR flashes with QuadSPI interfaces. Besides that, it can also be used for interfacing HyperBus and FPGA devices.

Features

- Various flash vendor devices supported
- Double Data Rate (DDR) and Single Data Rate (SDR) supported
- Single, dual, quad, and octal mode
- DMA support
- Execute in place (XiP) possible

Table 5-95 QSPI Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
158	MMC1_D7	QSPI0A_SS0_B	LSIO.QSPI0A.SS0_B	O	Chip Select 0
198	DAP1_RESET	QSPI0A_SS1_B	LSIO.QSPI0A.SS1_B	O	Chip Select 1, used to select the second instance of QuadSPI device (dual die flash require CS0 and CS1)
274	USBO1_EN	QSPI0A_SCLK	LSIO.QSPI0A.SCLK	O	Serial Clock
96	USBH_OC#	QSPI0A_DATA0	LSIO.QSPI0A.DATA0	I/O	Serial I/O for command, address, and data
148	MMC1_D4	QSPI0A_DATA1	LSIO.QSPI0A.DATA1	I/O	Serial I/O for command, address, and data
114	UART1_RTS	QSPI0A_DATA2	LSIO.QSPI0A.DATA2	I/O	Serial I/O for command, address, and data
116	UART1_CTS	QSPI0A_DATA3	LSIO.QSPI0A.DATA3	I/O	Serial I/O for command, address, and data
286	BKL1_ON	QSPI0A_DQS	LSIO.QSPI0A.DQS	I	Data Strobe signal, required on some high-speed DDR devices
5	GPIO3	QSPI0B_SS0_B	LSIO.QSPI0B.SS0_B	O	Chip Select 0
7	GPIO4	QSPI0B_SS1_B	LSIO.QSPI0B.SS1_B	O	Chip Select 1, used to select the second instance of QuadSPI device (dual die flash require CS0 and CS1)
11	GPIO5	QSPI0B_SCLK	LSIO.QSPI0B.SCLK	O	Serial Clock
13	GPIO6	QSPI0B_DATA0	LSIO.QSPI0B.DATA0	I/O	Serial I/O for command, address, and data
15	GPIO7	QSPI0B_DATA1	LSIO.QSPI0B.DATA1	I/O	Serial I/O for command, address, and data
17	GPIO8	QSPI0B_DATA2	LSIO.QSPI0B.DATA2	I/O	Serial I/O for command, address, and data
1	GPIO1	QSPI0B_DATA3	LSIO.QSPI0B.DATA3	I/O	Serial I/O for command, address, and data
3	GPIO2	QSPI0B_DQS	LSIO.QSPI0B.DQS	I	Data Strobe signal, required on some high-speed DDR devices

X1 Pin#	Apalis Std Function	i.MX 8X Ball Name	i. MX 8X Function	I/O	Description
5	GPIO3	QSPI0B_SS0_B	LSIO.QSPI1A.SS0_B	O	Chip Select 0
7	GPIO4	QSPI0B_SS1_B	LSIO.QSPI1A.SS1_B	O	Chip Select 1, used to select the second instance of QuadSPI device (dual die flash require CS0 and CS1)
11	GPIO5	QSPI0B_SCLK	LSIO.QSPI1A.SCLK	O	Serial Clock
13	GPIO6	QSPI0B_DATA0	LSIO.QSPI1A.DATA0	I/O	Serial I/O for command, address, and data
15	GPIO7	QSPI0B_DATA1	LSIO.QSPI1A.DATA1	I/O	Serial I/O for command, address, and data
17	GPIO8	QSPI0B_DATA2	LSIO.QSPI1A.DATA2	I/O	Serial I/O for command, address, and data
1	GPIO1	QSPI0B_DATA3	LSIO.QSPI1A.DATA3	I/O	Serial I/O for command, address, and data
3	GPIO2	QSPI0B_DQS	LSIO.QSPI1A.DQS	I	Data Strobe signal, required on some high-speed DDR devices

5.28 JTAG

The JTAG interface is not generally required for software development with the Apalis iMX8X. There is always the possibility of reprogramming the module using the Recovery Mode over USB. To flash the module in recovery mode and debug reasons, it is strongly recommended that the USBO1 interface is accessible even if not needed in the production system. Additionally, UART1 should also be accessible.

The JTAG interface is located as test points on the bottom side of the module. The location is standardized by the Apalis specification. Please be aware, the reference voltage for the interface is **1.8V**. The SoC does not provide the RTCK signal. The pad is left unconnected on the module. Do not connect the other test pad. They are used during production testing.

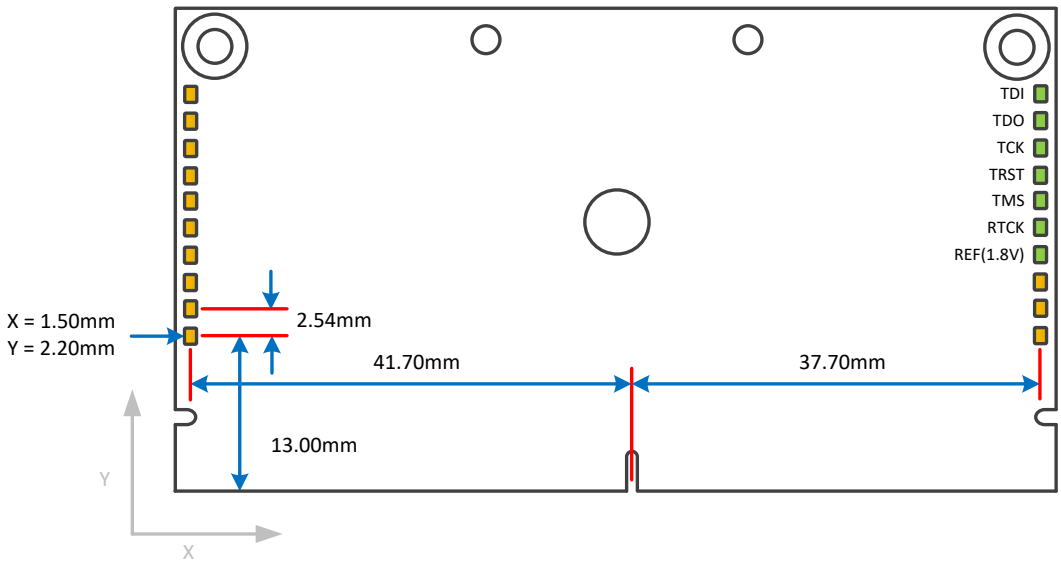


Figure 19 JTAG test point location on the bottom side of the module

6. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Apalis iMX8X even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in recovery mode, the USBO1 interface is used to connect it to a host computer. You will find additional information at our Developer Center (http://developer.toradex.com).

The recovery mode pads need to be shorted during the initial power on (cold boot) of the module to enter recovery mode. Figure 20 shows the location of the pads that need to be shorted for entering the recovery mode.

It is also possible to enter the recovery mode by pulling **up** pin 63 of the module edge connector (TS_1) with a 1kΩ resistor while booting. This pin is located in the type-specific area. It is not guaranteed that other Apalis modules can be set into recovery mode in the same way.

Important: make sure that there is no bootable SD card plugged into the slot. Otherwise, the module tries to boot from the external SD card instead of going into the USB serial loader.

Figure 20 Location of recovery mode pads

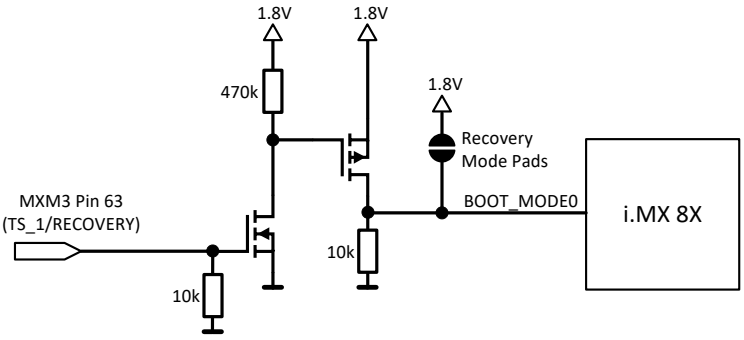


Figure 21: Recovery Mode Circuit

7. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document, which can be downloaded on our website at:

https://developer.toradex.com/products/apalis-som-family/modules/apalis-imx8x#errata

8. Technical Specifications

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_VCC	Main power supply	-0.3	3.6	V
Vmax_AVCC	Analog power supply	-0.3	3.6	V
Vmax_VCC_BACKUP	RTC power supply	-0.3	4.3	V
Vmax_IO_3.3V	SoC IO pins with 3.3V logic level	-0.3	3.6	V
Vmax_AN1	ADC and touch analog input	-0.5	2.1	V
Vmax USBO1_VBUS	Input voltage at USBO1_VBUS	-0.3	5.5	V

8.2 Recommended Operation Conditions

Table 8-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
VCC	Main power supply*	3.135	3.3	3.6	V
AVCC	Analogue power supply	3.0	3.3	3.6	V
VCC_BACKUP	RTC power supply	2.5	3.3	3.6	V

* The limiting device is the KSZ9131 Ethernet PHY. All other devices on the module work from 3.0V to 3.6V.

8.3 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Apalis product family. Following those recommendations ensures that the carrier board being designed is compatible with all existing and future Apalis modules. For details, please refer to the Apalis Family Specification or the Apalis Carrier Board Design Guide.

For designing carrier boards for a particular Apalis module only, please consult our Developer Website for module-specific power consumption information. However, please note that scaling the carrier board power supplies for a particular module only may cause compatibility issues with other existing and future modules within the Apalis family.

8.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Apalis module. This specification can be found in the Apalis Carrier Board Design Guide.

8.5 Mechanical Characteristics

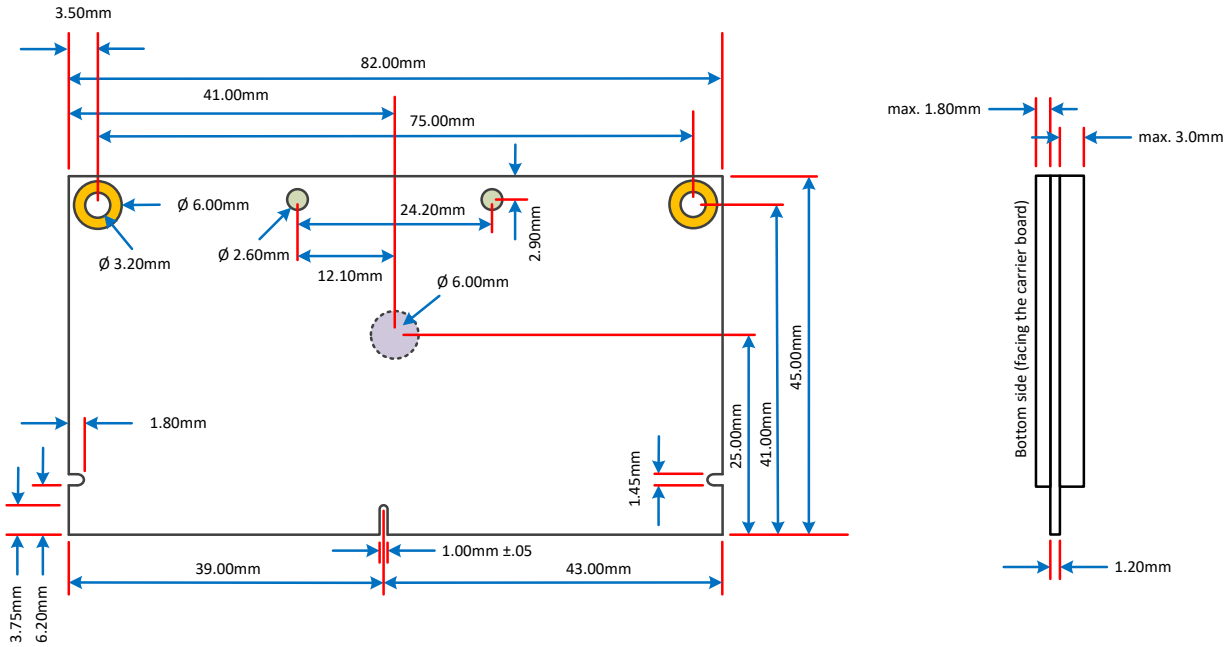


Figure 22 Mechanical dimensions of the Apalis module (top view)
Tolerance for all measures: +/- 0.1mm

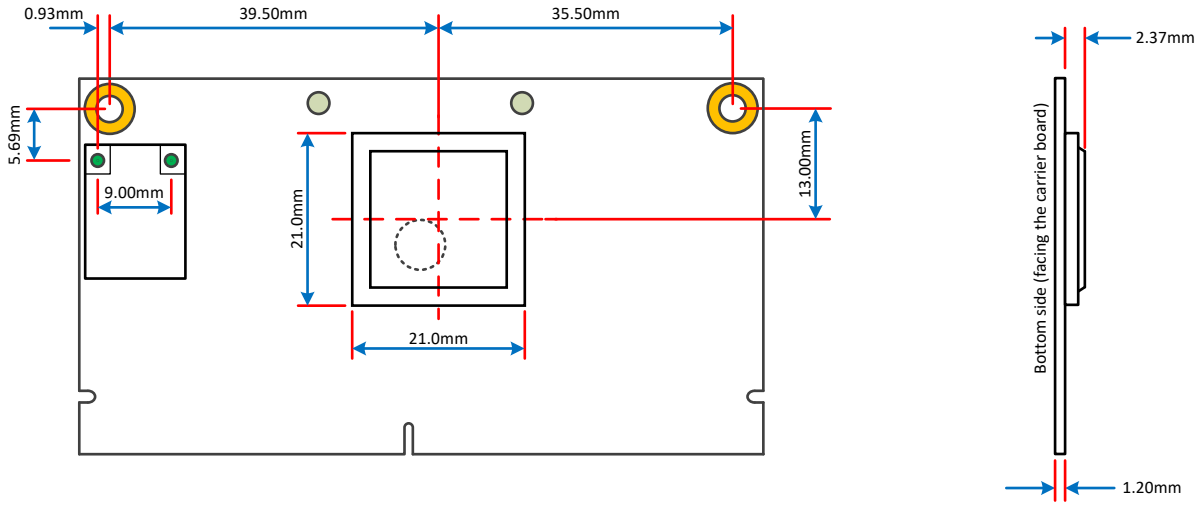


Figure 23 Mechanical position of i.MX 8X SoC (top view)
Tolerance for all measures: +/- 0.1mm

8.5.1 Sockets for the Apalis Modules

The Apalis module uses the MXM3 (Mobile PCI-Express Module) edge connector. This connector is available from different manufacturers in different board-to-board stacking heights from 2.3mm to 11.1mm. Toradex recommends using the JAE MM70-314B1-2-R300, which has a board-to-board height of 3.0mm. This stacking height allows using the MXM SnapLock system for easy fixing of the module to the carrier board.

You can refer to a list of other MXM3 connectors on the developer website.

8.6 Thermal Specification

The Apalis iMX8X incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling, enabling the system to continuously adjust the operating frequency and voltage in response to the changes in workload and temperature. The i.MX 8X SoC features DVFS on the CPU cluster, as well as on the GPU. This allows the Apalis iMX8X to deliver higher performance at lower average power consumption compared to other solutions.

The Apalis iMX8X modules come with embedded temperature sensors. The sensors measure the die (junction) temperature and are used to determine whether the cores need to be throttled to prevent overheating. If the temperature of the i.MX 8X reaches the maximum permitted temperature limit, the system will automatically shut down.

Here are some general considerations for you to follow:

- It is generally advised to use a heat sink on the Apalis iMX8X
- If you need the full CPU/Graphics performance over a long period of time, we recommend well designing the whole heat dissipation solution of the system.
- Toradex provides a heatsink for the Apalis iMX8X. This solution can be used passively as well as in combination with a fan. More information can be found here: http://developer.toradex.com/products/apalis-heatsink
- Suppose you only use the peak performance for a short time. In that case, heat dissipation is less of a problem because advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents in idle. A die temperature increase from 25°C to 125°C will increase the leakage by a factor of 10
- The Cortex-A35 is currently Arm's most efficient Armv8 core

In general, the more effective the thermal solution is, the more performance you can get out of the Apalis iMX8X Module.

In the tables below, the operating temperature range is specified for the ambient temperature. Please pay attention to the maximum temperature value. The specified temperature is only applicable if the cooling solution can keep the junction temperature below the maximum limit.

Table 8-3 1.1 Thermal Specification Apalis iMX8QXP 2GB WB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8X only. ($R_{\theta JA}$)[2]		15.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 8X chip case. ($R_{\theta JCtop}$)[2]		0.7		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The Wi-Fi module is currently only validated from -30°C to 85°C. Validation down to -40°C is pending. The rest of the components are rated for the complete -40°C to 85°C temperature range.

Table 8-4 1.1 Thermal Specification Apalis iMX8QXP 2GB ECC IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C

Description	Min	Typ	Max	Unit
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8X only. ($R_{\theta JA}$)[2]		15.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 8X chip case. ($R_{\theta JCtop}$)[2]		0.7		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] All components are rated to run until -40°C.

Table 8-5 1.1 Thermal Specification Apalis iMX8DXP 1GB

Description	Min	Typ	Max	Unit
Operating temperature range	-30[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	0		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8X only. ($R_{\theta JA}$)[2]		15.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 8X chip case. ($R_{\theta JCtop}$)[2]		0.7		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] All components are rated to run until -30°C.

8.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at http://www.toradex.com/support/product-compliance

DISCLAIMER: