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Colibri iMX6ULL

Errata Document

Document Revision History

Date	Doc. Rev.	Notes
2018-07-04	Rev. 1.0	Initial Release
2019-10-29	Rev. 1.1	Added a note about series resistor
2022-05-16	Rev. 1.2	Errata #3: Added Updating document template Minor changes

Overview

Errata #1: Ethernet can become unusable after power save mode

Affected Version: **Colibri iMX6ULL V1.0**

Fixed in: **Colibri iMX6ULL V1.1**

1.1 Customer impact

The Ethernet PHY might not exit the power save mode correctly.

1.2 Description

Due to the Microchip KSZ8041NL Ethernet PHY errata, the Ethernet can become unusable after exiting the power save mode. The Ethernet PHY is powering down the PLL during the software power down, which can create problems. The issues only appear under certain circumstances and in certain temperature ranges. The issue cannot be reproduced with all modules.

1.3 Workaround

Microchip is recommending not using the software power-down of the Ethernet PHY. This means the Ethernet PHY should be left running even in the module's power save (suspend) mode. However, this increases the module's power consumption in the power save state.

1.4 Fix

Version 1.1 of the Colibri iMX6ULL includes an additional circuit that power gates the Ethernet PHY's rails if the 50MHz reference clock is removed. The software does not need to put the Ethernet PHY into software power down. Instead, make sure the 50MHz reference clock output of the i.MX 6ULL is disabled. This will turn off the power rails of the KSZ8041NL.

Errata #2: The high voltage level is lower on some SODIMM pins

Affected Version: **Colibri iMX6ULL V1.0**

Fixed in: **Colibri iMX6ULL V1.1**

2.1 Customer impact

Some IO pins are powered from the VCC_BATT. Therefore, the high state voltage level might be lower than expected. Any load on these pins can increase the current drain on the RTC battery rail.

2.2 Description

The SNVS pins are not powered by the regular main 3.3V rail. They are powered from the VCC_BATT (SODIMM pin 40) rail:

X1 Pin#	Colibri STD Function	iMX6ULL Ball Name	iMX6ULL Port Name	Remarks
43	WAKEUP Source<0>,SDCard CardDetect	SNVS_TAMPER0	gpio5.IO[0]	
45	WAKEUP Source<1>	SNVS_TAMPER1	gpio5.IO[1]	
93	RDnWR	SNVS_TAMPER6	gpio5.IO[6]	Not available on modules with Wi-Fi
95	RDY	SNVS_TAMPER3	gpio5.IO[3]	
105	nCS0	BOOT_MODE0	gpio5.IO[10]	
107	nCS1	SNVS_TAMPER4	gpio5.IO[4]	
127		BOOT_MODE1	gpio5.IO[11]	Not available on modules with Wi-Fi
131	USB Host Over-Current Detect	SNVS_TAMPER5	gpio5.IO[5]	
137	USB Client Cable Detect, SPDIF_OUT	SNVS_TAMPER2	gpio5.IO[2]	
138	ADDRESS23	SNVS_TAMPER8	gpio5.IO[8]	Not available on modules with Wi-Fi

Depending on the actual implementation on the carrier board, the VCC_BATT is provided by an RTC battery or over a diode from the regular 3.3V rail. Therefore, the VCC_BATT voltage usually is only around 3.0V (the minimum allowed voltage is 2.4V). This means the maximum output high level of the SNVS pins is also at this level.

Any load on the SNVS pin is sourced by the VCC_BATT rail. The current draw on pin 40 could exceed the regular drain on an RTC battery rail.

2.3 Workaround

If the RTC feature on the module is not required, connect pin 40 directly to the main 3.3V rail. Maybe an external RTC can be used on the carrier board to keep the time.

If the RTC feature is required, make sure the diode between the main 3.3V rail and the pin 40 has a low forward voltage drop and can sustain the current draw. Make sure the peripherals on the SNVS pins are tolerant to the lower voltage level. Try to reduce the load on the pins.

Try to avoid using the affected pins. Use other SODIMM GPIO pins instead.

2.4 Fix

Version 1.1 of the Colibri iMX6ULL adds a switch that bridges the main 3.3V rail with the VCC_BATT rail while the module is powered up. This increases the high voltage level of the SNVS pins and makes sure the output current is coming from the main 3.3V rail instead of the VCC_BATT rail.

Errata #3: HAR-8982 – KSZ8041 Errata 2 can cause Ethernet not working at certain temperatures

Affected Version: **Colibri iMX6ULL V1.1**

Fixed in: **TBD**

3.1 Customer impact

On rare occasions, a small amount of Colibri iMX6ULL SoMs may fail to communicate with the Ethernet PHY after power-up, rendering the Ethernet interface unusable until the SoM gets power cycled.

3.2 Description

The Microchip KSZ8041 Ethernet PHY has an errata: https://ww1.microchip.com/downloads/en/DeviceDoc/80000700A.pdf. According to the second item in the document, a small percentage (less than 1%) of the devices can potentially fail to properly read the strapping pins and set the intended configuration if the 3.3V supply rail rises too fast.

On the Colibri iMX6ULL SoM, the 3.3V power rail for the Ethernet rises faster than the required 250us. Therefore, on rare occasions, a small amount of Colibri iMX6ULL SoMs may fail to communicate with the Ethernet PHY after power-up. If the strapping of the PHY configuration fails, the system cannot communicate with the PHY over the MDIO interface. The Ethernet port is not working in this case. According to our tests, the issue mainly appears on the affected modules if the power is enabled at extremely low temperatures (below -30°C).

The pull-up resistors of the Ethernet LEDs on the carrier board can backfeed to the 3.3V Ethernet power rail on the module. This backfeeding actually reduces the risk of strapping failures.

3.3 Workaround

There is currently no permanent workaround. If the Ethernet PHY is not accessible, try to power cycle the Ethernet PHY or the complete Colibri SoM. Disabling the RMII clock turns off the Ethernet power rails. Try waiting at least 1 second before reenabling the RMII clock and initializing the Ethernet PHY.