Hardware Architecture
Hardware_Architecture.SchDoc

REVISION HISTORY

1. Design Revision V1.0 : Preliminary design.
   Date: 23th July 2013

2. Design Revision V1.0 :
   - Added revision history schematic page. Updated schematic page template.
   Date: 15th March 2016

3. Design Revision V2.0 :
   - T30TS_Mezzanine.SchDoc: Updated connection from mezzanine connector X1
   - T30TS_Mezzanine_CSI.SchDoc: Added new MIPI CSI connectors X3 and X4
   - T30TS_Mezzanine_DSI.SchDoc: Added new MIPI DSI connector X5
   Date: 08th November 2017

IF IN DOUBT ASK

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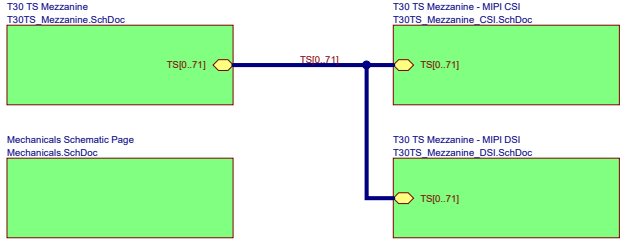
Title *Apalis T30 TS Mezzanine*			*Toradex AG* *Altsagenstrasse 5* *Horw* *6048* *Switzerland*
Size: A3	Number:1.	Revision:V2.0	
Date: 23-03-2018 Time: 16:30:26		Sheet 1 of 6	
File: Revision_History.SchDoc			



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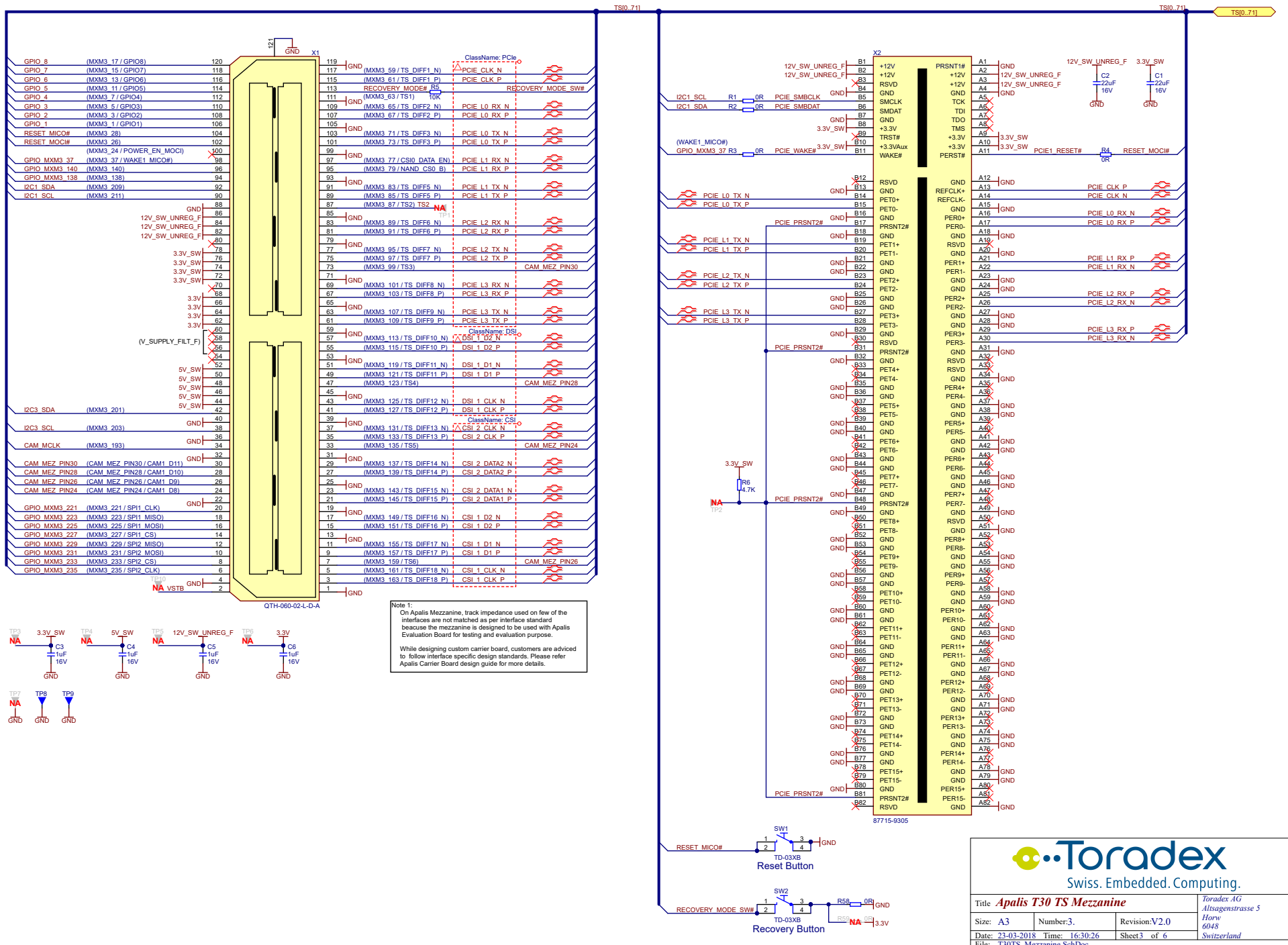
Title *Apalis T30 TS Mezzanine*			*Toradex AG Altsagenstrasse 5 Horw 6048 Switzerland*
Size: A3	Number:2.	Revision:V2.0	
Date: 23-03-2018 Time: 16:30:26		Sheet2 of 6	
File: Hardware Architecture.SchDoc			


TS[0..71]
X1
QTH-060-02-L-D-A
ClassName: PCIe
ClassName: DSI
ClassName: CSI
X2
87715-9305
Note 1:
On Apalis Mezzanine, track impedance used on few of the interfaces are not matched as per interface standard beacuse the mezzanine is designed to be used with Apalis Evaluation Board for testing and evaluation purpose.
While designing custom carrier board, customers are adviced to follow interface specific design standards. Please refer Apalis Carrier Board design guide for more details.
Reset Button
Recovery Button
TD-03XB
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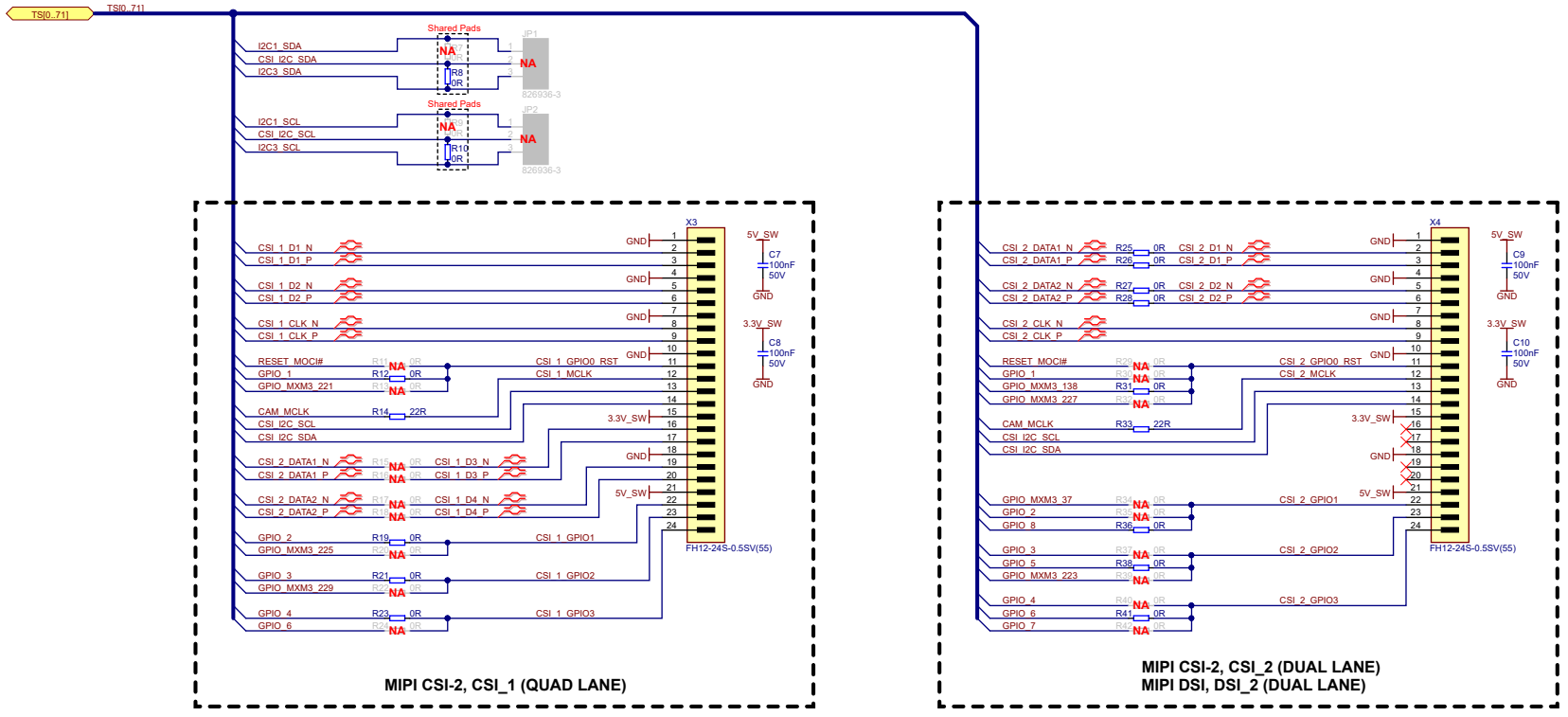
Title Apalis T30 TS Mezzanine
Size: A3
Number:3.
Revision:V2.0
Date: 23-03-2018 Time: 16:30:26
Sheet3 of 6
File: T30TS_Mezzanine.SchDoc
Toradex AG
Altsagenstrasse 5
Horw
6048
Switzerland



Note 2:
Apalis T30 computer-on-module features 2 x Dual-lane OR 1x Quad-lane MIPI CSI interface. MIPI CSI signals CSI_2_DATA1_N/P and CSI_2_DATA2_N/P are shared between connectors X3 and X4.
Please refer to the assembly options below:

Use 1x Quad-lane MIPI-CSI Interface : assemble resistors R15, R16, R17, R18 and disassemble resistors R25, R26, R27, R28.
Use 2x Dual-lane MIPI-CSI Interface (default assembly) : assemble resistors R25, R26, R27, R28 and disassemble resistors R15, R16, R17, R18.

Please refer Apalis T30 datasheet for more details.

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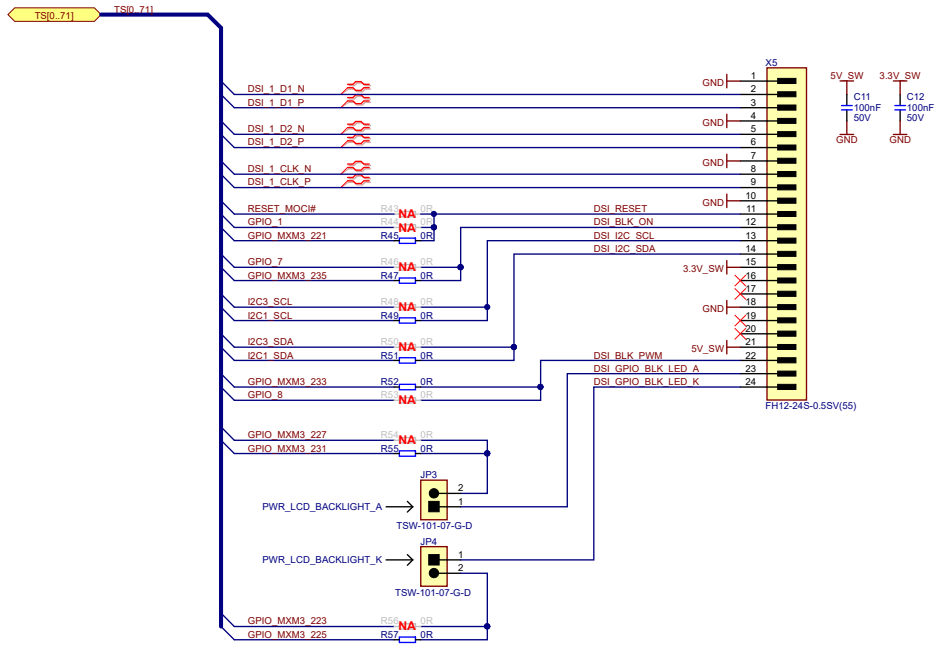
Title: *Apalis T30 TS Mezzanine*		*Toradex AG Altsagenstrasse 5 Horw 6048 Switzerland*
Size: A3	Number:4.	Revision:V2.0
Date: 23-03-2018 Time: 16:30:26	Sheet4 of 6	
File: T30TS_Mezzanine_CSI.SchDoc		

MIPI DSI, DSI_1 (DUAL LANE)



Title	*Apalis T30 TS Mezzanine*		Toradex AG Altsagenstrasse 5 Horw 6048 Switzerland
Size: A3	Number:5.	Revision:V2.0	
Date: 23-03-2018 Time: 16:30:26		Sheet 5 of 6	
File: T30TS_Mezzanine_DSI.SchDoc			

PCB Apalis T30 Mezzanine V2.0

PCB1

Label: "Apalis T30 Mezzanine V2.0A"

LBL1

Toradex Logo

MECH1

Fiducial MECH2 Fiducial MECH3 Fiducial MECH4 Fiducial MECH5

Fiducial MECH6 Fiducial MECH7 Fiducial MECH8 Fiducial MECH9

S1002-OPS60-01G NA SJP1 S1002-OPS60-01G NA SJP2 S1002-OPS60-01G SJP3 S1002-OPS60-01G SJP4

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Title *Apalis T30 TS Mezzanine*			*Toradex AG Altsagenstrasse 5 Horw 6048 Switzerland*
Size: A3	Number:6.	Revision:V2.0	
Date: 23-03-2018 Time: 16:30:26		Sheet6 of 6	
File: Mechanicals.SchDoc			