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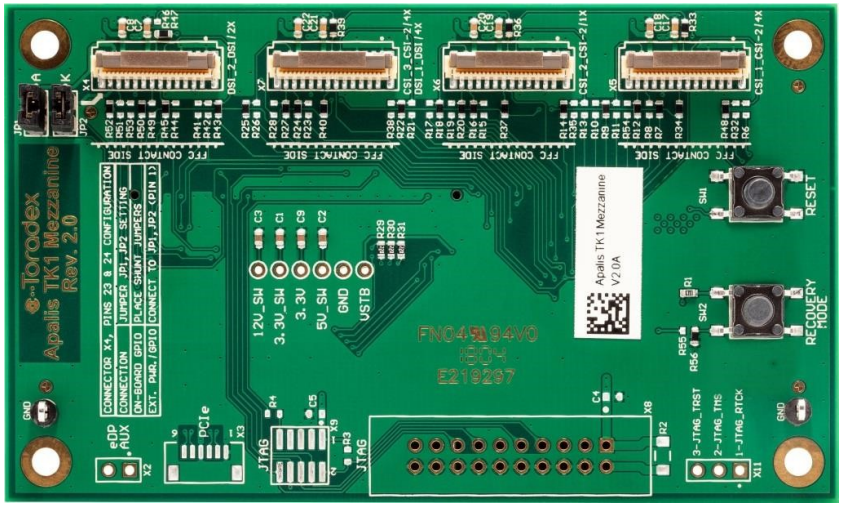
Apalis TK1 Mezzanine

Datasheet



Revision History

Date	Doc. Rev.	Board Version	Changes
02-May-18	Rev. 1.0	V2.0	- Initial Release: Preliminary Version

Contents

1. Introduction

Apalis TK1 Mezzanine is an add-on board for the Apalis Evaluation Board which provides access to the type specific interfaces available on the Apalis TK1 module. It allows the user to test and evaluate the type specific features available on the Apalis TK1 module.

Since type specific features are dependent on the Apalis module. Specific types of mezzanine boards will be available for each Apalis module. Customers are free to develop their own type specific mezzanine board for prototyping and development purposes. Please refer to the datasheets for the individual Apalis module for more information.

1.1. Reference Documents

For detailed technical information about suitable computer modules, please refer to the documents listed below.

1.1.1 Apalis Computer Modules

An overview of the Apalis product family:

https://www.toradex.com/computer-on-modules/apalis-arm-family

An overview of the Apalis TK1 module:

https://www.toradex.com/computer-on-modules/apalis-arm-family/nvidia-tegra-k1

http://developer.toradex.com/products/apalis-tk1

1.1.2 Toradex Developer Website - Apalis Evaluation Board

http://developer.toradex.com/products/apalis-evaluation-board

1.1.3 Toradex Developer Website - Carrier Board Design

http://developer.toradex.com/carrier-board-design

2. Features

2.1. Overview

The Apalis TK1 Board provides the following features and interfaces:

- 3x MIPI CSI (2x Quad-lane or 1x Single-lane) connector
- 1x MIPI DSI (1x Dual-lane) connector
- 1x Recovery mode switch
- 1x Reset switch
- 2x JTAG header
- 1x eDP AUX header (only signal available in Apalis TK1 type specific pins)
- 1x PCIe header (only signal available in Apalis TK1 type specific pins)

2.2. Block Diagram

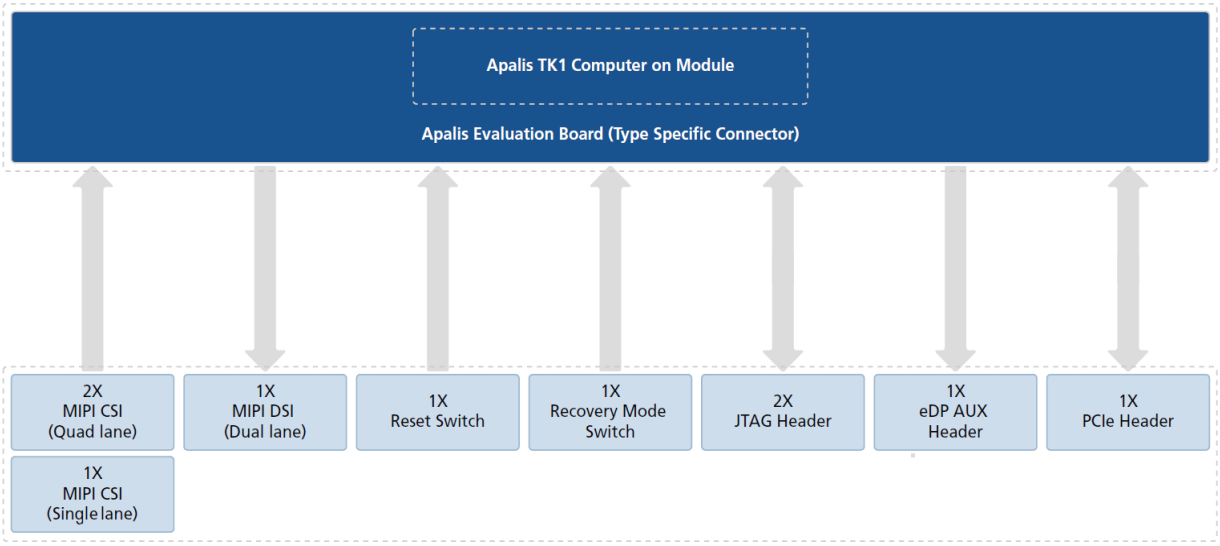


Fig.1 Apalis TK1 Mezzanine Board Hardware Architecture

2.3. Physical Drawings

2.3.1 Top Side Connectors

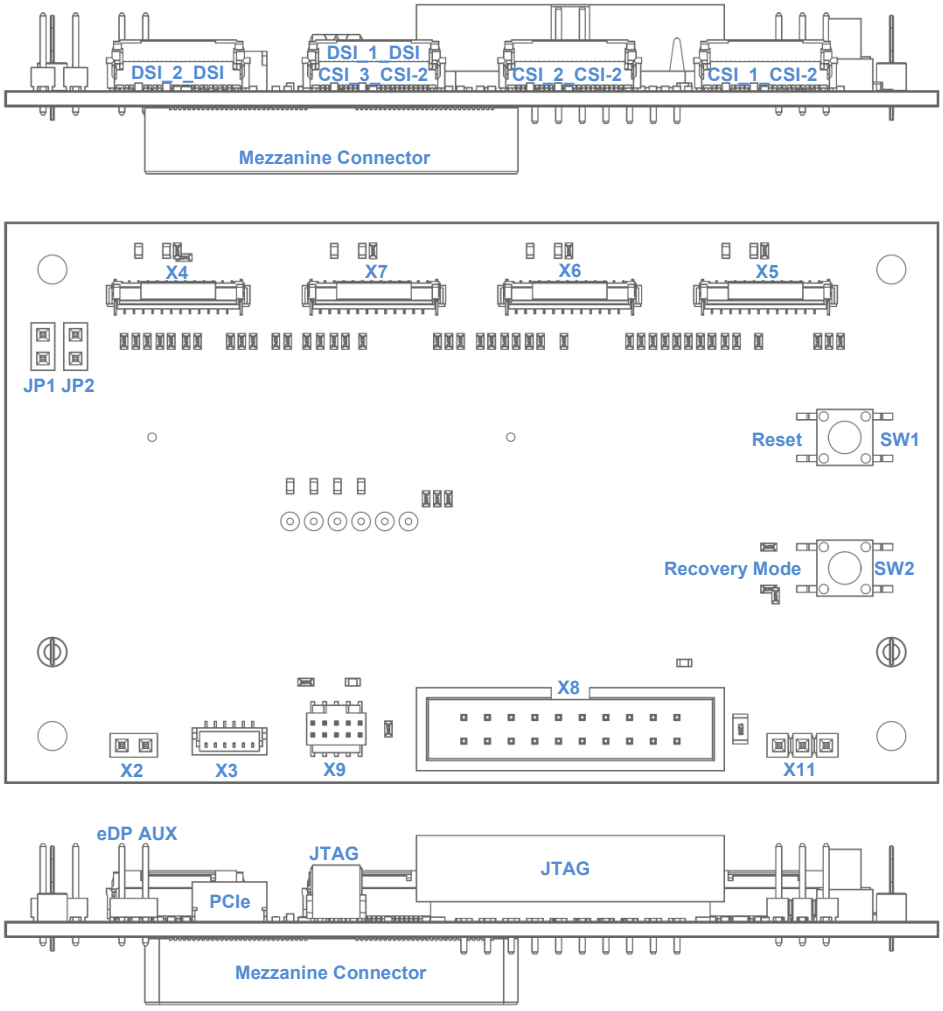


Fig.2 Apalis TK1 Mezzanine Board Connectors – Top Side

Ref	Description	Remarks
X4	DSI_2 Connector	Dual-lane MIPI DSI, DSI_2 Interface
X5	CSI_1 Connector	Quad-lane MIPI CSI-2, CSI_1 Interface
X6	CSI_2 Connector	Single-lane MIPI CSI-2, CSI_2 Interface
X7	CSI_3 Connector	Quad-lane MIPI CSI-2, CSI_3 Interface / Quad-lane MIPI DSI, DSI_1 Interface
JP1	DSI_GPIO_BLK_LED_A Jumper (for X4, Pin 23)	2.54mm pitch header
JP2	DSI_GPIO_BLK_LED_K Jumper (for X4, Pin 24)	2.54mm pitch header
SW1	Reset Switch	
SW2	Recovery Mode Switch	
X2	eDP AUX Connector	Not assembled by default
X3	PCIe signals header	Not assembled by default
X8	JTAG Connector (legacy)	Not assembled by default
X9	JTAG Connector	Not assembled by default
X11	JTAG Header	Not assembled by default

2.3.2 Bottom Side Connectors

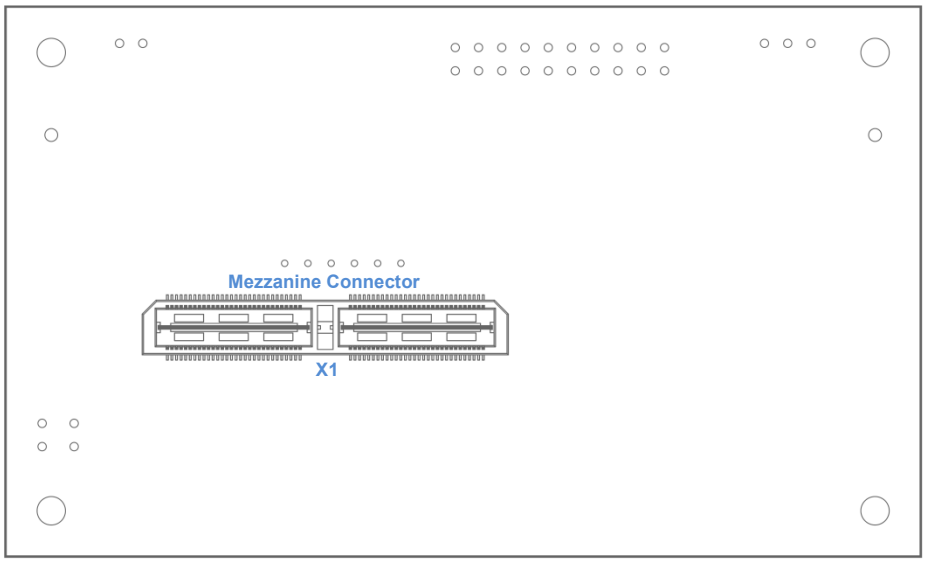


Fig.3 Apalis TK1 Mezzanine Board Connectors – Bottom Side

Ref	Description	Remarks
X1	Mezzanine Connector	

3. Interface Description

3.1. Mezzanine Connector (X1)

Manufacturer: Samtec, QTH-060-02-L-D-A

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	VSTB		PWR	+5V	
3	CSI_1_CLK_P	163	I		
4	GND		PWR		
5	CSI_1_CLK_N	161	I		
6	GPO_MXM3_235	235	O	+3.3V	
7	EZP_CS_b (Refer Note 2)	159			
8	GPO_MXM3_233	233	O	+3.3V	
9	CSI_1_D1_P	157	I		
10	GPO_MXM3_231	231	O	+3.3V	
11	CSI_1_D1_N	155	I		
12	GPI_MXM3_229	229	I	+3.3V	
13	GND		PWR		
14	GPO_MXM3_227	227	O	+3.3V	
15	CSI_1_D2_P	151	I		
16	GPO_MXM3_225	225	O	+3.3V	
17	CSI_1_D2_N	149	I		
18	GPI_MXM3_223	223	I	+3.3V	
19	GND		PWR		
20	GPO_MXM3_221	221	O	+3.3V	
21	CSI_1_D3_P	145	I		
22	GND		PWR		
23	CSI_1_D3_N	143	I		
24	NC				
25	GND		PWR		
26	NC				
27	CSI_1_D4_P	139	I		
28	NC				
29	CSI_1_D4_N	137	I		
30	NC				
31	GND		PWR		
32	GND		PWR		
33	JTAG_TDO (Refer Note 2)	135			
34	CSI_CAM_CLK	193	O	+3.3V	
35	CSI_2_CLK_P	133	I		
36	GND		PWR		
37	CSI_2_CLK_N	131	I		
38	I2C_CAM1_SCL	203	O	+1.8V signal +3.3V tolerant	

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
39	GND		PWR		
40	GND		PWR		
41	CSI_3_CLK_P	127	I		
42	I2C_CAM1_SDA	201	I/O	+1.8V signal +3.3V tolerant	
43	CSI_3_CLK_N	125	I		
44	5V_SW		PWR	+5V	
45	GND		PWR		
46	5V_SW		PWR	+5V	
47	JTAG_TDI (Refer Note 2)	123			
48	5V_SW		PWR	+5V	
49	CSI_3_D1_P	121	I		
50	5V_SW		PWR	+5V	
51	CSI_3_D1_N	119	I		
52	5V_SW		PWR	+5V	
53	GND		PWR		
54	NC				
55	CSI_3_D2_P	115	I		
56	NC				
57	CSI_3_D2_N	113	I		
58	NC				
59	GND		PWR		
60	NC				
61	CSI_3_D3_P	109	I		
62	3.3V		PWR	+3.3V	
63	CSI_3_D3_N	107	I		
64	3.3V		PWR	+3.3V	
65	GND		PWR		
66	3.3V		PWR	+3.3V	
67	CSI_3_D4_P	103	I		
68	3.3V		PWR	+3.3V	
69	CSI_3_D4_N	101	I		
70	NC				
71	GND		PWR		
72	3.3V_SW		PWR	+3.3V	
73	JTAG_TCLK (Refer Note 2)	99			
74	3.3V_SW		PWR	+3.3V	
75	CSI_2_D1_P	97	I		
76	3.3V_SW		PWR	+3.3V	
77	CSI_2_D1_N	95	I		
78	3.3V_SW		PWR	+3.3V	
79	GND		PWR		
80	NC				
81	DSI_1_CLK_P	91	O		

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
82	12V_SW_UNREG_F		PWR	+12V	
83	DSI_1_CLK_N	89	O		
84	12V_SW_UNREG_F		PWR	+12V	
85	GND		PWR		
86	12V_SW_UNREG_F		PWR	+12V	
87	JTAG_RST (Refer Note 2)	87			
88	GND		PWR		
89	DSI_1_D0_P	85	O		
90	I2C1_SCL	211	O	+1.8V signal +3.3V tolerant	
91	DSI_1_D0_N	83	O		
92	I2C1_SDA	209	I/O	+1.8V signal +3.3V tolerant	
93	GND		PWR		
94	GPO_MXM3_138	138	O	+3.3V	
95	DSI_1_D1_P	79	O		
96	GPI_MXM3_140	140	I	+3.3V	
97	DSI_1_D1_N	77	O		
98	GPIO_MXM3_37	37	I/O	+3.3V	
99	GND		PWR		
100	NC				
101	eDP_1_AUX_CH0_P	73	O		
102	RESET_MOCI# (Refer Note 4)	26	O	+3.3V	10K to +3.3V
103	eDP_1_AUX_CH0_N	71	O		
104	RESET_MICO# (Refer Note 4)	28	I	+3.3V	100K to +3.3V
105	GND		PWR		
106	GPIO_1	1	I/O	+3.3V	
107	PCIE1_L1_TX_P	67	O		
108	GPIO_2	3	I/O	+3.3V	
109	PCIE1_L1_TX_N	65	O		
110	GPIO_3 (Refer Note 1)	5	I/O	+3.3V	
111	GND		PWR		
112	GPIO_4 (Refer Note 1)	7	I/O	+3.3V	
113	BOOT_MODE0 / RECOVERY_MODE_SW#	63		I	10K to +3.3V
114	GPIO_5	11	I/O	+3.3V	
115	PCIE1_L1_RX_P	61	I		
116	GPIO_6 (Refer Note 3)	13	I/O	+3.3V	
117	PCIE1_L1_RX_N	59	I		
118	GPIO_7	15	I/O	+3.3V	
119	GND		PWR		
120	GPIO_8	17	I/O	+3.3V	
121	GND		PWR		

Note:

1) On Apalis TK1 (V1.0 and V1.1) module, this pin has limited output capabilities. Please refer to Apalis TK1 errata (Errata #5) for more details.
2) On Apalis TK1 (V1.0 and V1.1) module, this signal is not connected.
3) This signal is hardware multiplexed on the Apalis TK1 module.
4) This signal is connected to Power Management IC.

3.2. MIPI DSI Interface

3.2.1 DSI_2 Connector (X4)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	DSI_2_D1_N	83	O		
3	DSI_2_D1_P	85	O		
4	GND		PWR		
5	DSI_2_D2_N	77	O		
6	DSI_2_D2_P	79	O		
7	GND		PWR		
8	DSI_2_CLK_N	89	O		
9	DSI_2_CLK_P	91	O		
10	GND				
11	DSI_RESET	26 / 1 / 221	O		
12	DSI_BLK_ON	7 / 235	O		
13	DSI_I2C_SCL	203 / 211	I	+1.8V signal +3.3V tolerant	
14	DSI_I2C_SDA	201 / 209	I/O	+1.8V signal +3.3V tolerant	
15	3.3V_SW		PWR	+3.3V	
16	NC				
17	NC				
18	GND		PWR		
19	NC				
20	NC				
21	5V_SW		PWR	+5V	
22	DSI_BLK_PWM	17 / 233	I/O		
23	DSI_GPIO_BLK_LED_A	231	I/O		
24	DSI_GPIO_BLK_LED_K	225	I/O		

As default assembly, I2C1 bus has been connected to the MIPI DSI Connector. Following table describes the assembly options available on the Apalis TK1 Mezzanine V2.0 with respect of the MIPI DSI interface I2C bus selection:

Solution Selected	Assembly Options	Assembled Components on Apalis TK1 Mezzanine V2.0	PCB Side
I2C1	Assemble components R47 and R50 Disassemble components R46 and R49	R47, R50	Top
I2C3	Assemble components R46 and R49 Disassemble components R47 and R50	R47, R50	Top

Please refer to Apalis TK1 Mezzanine V2.0 assembly drawing for the position of the components.

Jumpers JP1 and JP2 are connected to pins 23 and 24 of connector X4. If the jumpers are short circuited using shunt jumpers, default GPIO signals connected to jumpers JP1 and JP2 will be available at pins 23 and 24 of connector X4. In-case customer wants to connect external power or I/O, they can remove the shunt jumpers from jumper JP1 and JP2 and then connect external power or I/O to pin 1 of jumpers JP1 and JP2 using jumper wires.

3.3. MIPI CSI-2 Interface

Apalis TK1 mezzanine provides 3x MIPI CSI-2 interface connectors. The pinout of the connectors are compatible with Toradex CSI connector standard. For configuration and control, I2C1 bus is connected to all the CSI connectors. While connecting multiple camera sensors, please ensure that the I2C bus address of each camera sensor are different.

3.3.1 CSI_1 Connector (X5)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	CSI_1_D1_N	155	I		
3	CSI_1_D1_P	157	I		
4	GND		PWR		
5	CSI_1_D2_N	149	I		
6	CSI_1_D2_P	151	I		
7	GND		PWR		
8	CSI_1_CLK_N	161	I		
9	CSI_1_CLK_P	163	I		
10	GND				
11	CSI_1_GPIO0_RST	26 / 1 / 221	I/O	+3.3V	
12	CSI_1_CAM_CLK	193	O	+3.3V	
13	CSI_1_I2C_SCL	203	I	+1.8V signal +3.3V tolerant	
14	CSI_1_I2C_SDA	201	I/O	+1.8V signal +3.3V tolerant	
15	3.3V_SW		PWR	+3.3V	
16	CSI_1_D3_N	143	I		
17	CSI_1_D3_P	145	I		
18	GND		PWR		
19	CSI_1_D4_N	137	I		
20	CSI_1_D4_P	139	I		
21	5V_SW		PWR	+5V	
22	CSI_1_GPIO1	3 / 229	I/O	+3.3V	
23	CSI_1_GPIO2	11 / 225	I/O	+3.3V	
24	CSI_1_GPIO3	5 / 13	I/O	+3.3V	

3.3.2 CSI_2 Connector (X6)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	CSI_2_D1_N	95	I		
3	CSI_2_D1_P	97	I		
4	GND		PWR		
5	NC		I		
6	NC		I		
7	GND		PWR		

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
8	CSI_2_CLK_N	131	I		
9	CSI_2_CLK_P	133	I		
10	GND				
11	CSI_2_GPIO0_RST	26 / 1 / 138	I/O	+3.3V	
12	CSI_2_CAM_CLK	193	O	+3.3V	
13	CSI_2_I2C_SCL	203	I	+1.8V signal +3.3V tolerant	
14	CSI_2_I2C_SDA	201	I/O	+1.8V signal +3.3V tolerant	
15	3.3V_SW		PWR	+3.3V	
16	NC		I		
17	NC		I		
18	GND		PWR		
19	NC		I		
20	NC		I		
21	5V_SW		PWR	+5V	
22	CSI_2_GPIO1	3 / 37	I/O	+3.3V	
23	CSI_2_GPIO2	5 / 11	I/O	+3.3V	
24	CSI_2_GPIO3	7 / 13	I/O	+3.3V	

3.3.3 CSI_3 Connector (X7)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	CSI_3_D1_N	119	I		
3	CSI_3_D1_P	121	I		
4	GND		PWR		
5	CSI_3_D2_N	113	I		
6	CSI_3_D2_P	115	I		
7	GND		PWR		
8	CSI_3_CLK_N	125	I		
9	CSI_3_CLK_P	127	I		
10	GND				
11	CSI_3_GPIO0_RST	26 / 1 / 127	I/O	+3.3V	
12	CSI_3_CAM_CLK	193	O	+3.3V	
13	CSI_3_I2C_SCL	203	I	+1.8V signal +3.3V tolerant	
14	CSI_3_I2C_SDA	201	I/O	+1.8V signal +3.3V tolerant	
15	3.3V_SW		PWR	+3.3V	
16	CSI_3_D3_N	107	I		
17	CSI_3_D3_P	109	I		
18	GND		PWR		
19	CSI_3_D4_N	101	I		
20	CSI_3_D4_P	103	I		

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
21	5V_SW		PWR	+5V	
22	CSI_3_GPIO1	3 / 17	I/O	+3.3V	
23	CSI_3_GPIO2	7 / 223	I/O	+3.3V	
24	CSI_3_GPIO3	13 / 15	I/O	+3.3V	

3.4. JTAG

3.4.1 JTAG Header (X8)

Connector Type: Molex, 70246-2002

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	3.3V_SW		PWR	+3.3V	
2	3.3V_SW		PWR	+3.3V	
3	JTAG_TRST				
4	GND		PWR		
5	JTAG_TDI	123			
6	GND		PWR		
7	JTAG_TMS				
8	GND		PWR		
9	JTAG_TCLK	99			
10	GND		PWR		
11	JTAG_RTCK				
12	GND		PWR		
13	JTAG_TDO	135			
14	GND		PWR		
15	JTAG_RST	87			
16	GND		PWR		
17	NC				
18	GND		PWR		
19	NC				
20	GND		PWR		

Few of the signals (JTAG_RTCK, JTAG_TMS, JTAG_TRST) connected to JTAG headers X8 and X9 are not available on the mezzanine connector X1. These signals are connected to header X11. Jumper wires can be used to connect these signals from Apalis Evaluation Board to Apalis TK1 mezzanine using header X11 on the Apalis TK1 mezzanine V2.0.

3.4.2 JTAG Header (X9)

Connector Type: Samtec, FTSH-105-01-L-DV-K

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	3.3V_SW		PWR	+3.3V	
2	JTAG_TMS				
3	GND		PWR		
4	JTAG_TCLK	99			
5	GND		PWR		
6	JTAG_TDO	135			
7	NC				
8	JTAG_TDI	123			
9	NC / EZP_CS_b				
10	JTAG_RST	87			

3.5. eDP AUX (X2)

Connector Type: 1x2 Pin Header Male, Pitch 2.54mm

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	eDP_1_AUX_CH0_N	71			
2	eDP_1_AUX_CH0_P	73			

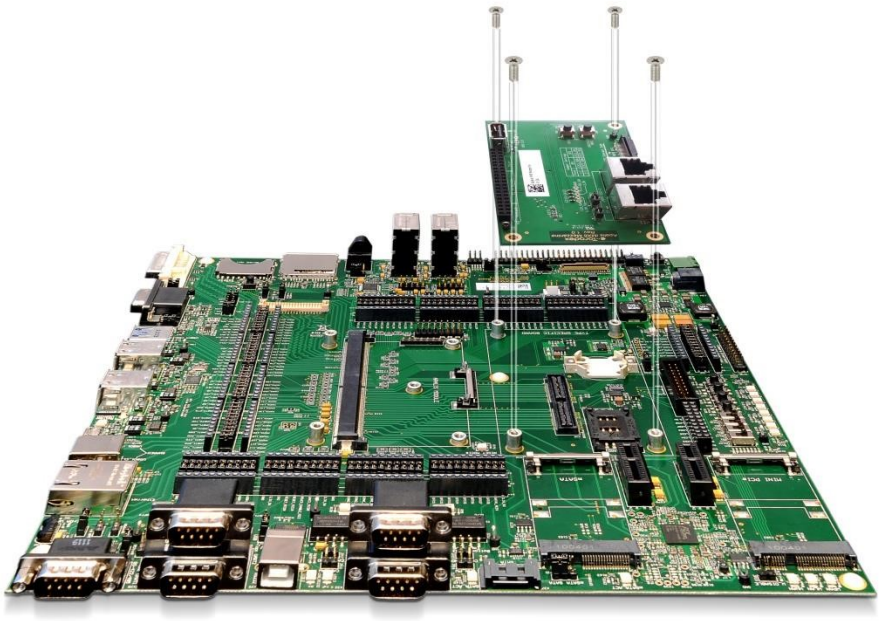
3.6. PCIe (X3)

Connector Type: JST, BM06B-SRSS-TB(LF)(SN)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	PCIE1_L1_RX_N	59			
3	PCIE1_L1_RX_P	61			
4	GND		PWR		
5	PCIE1_L1_TX_N	65			
6	PCIE1_L1_TX_P	67			

4. Assembly

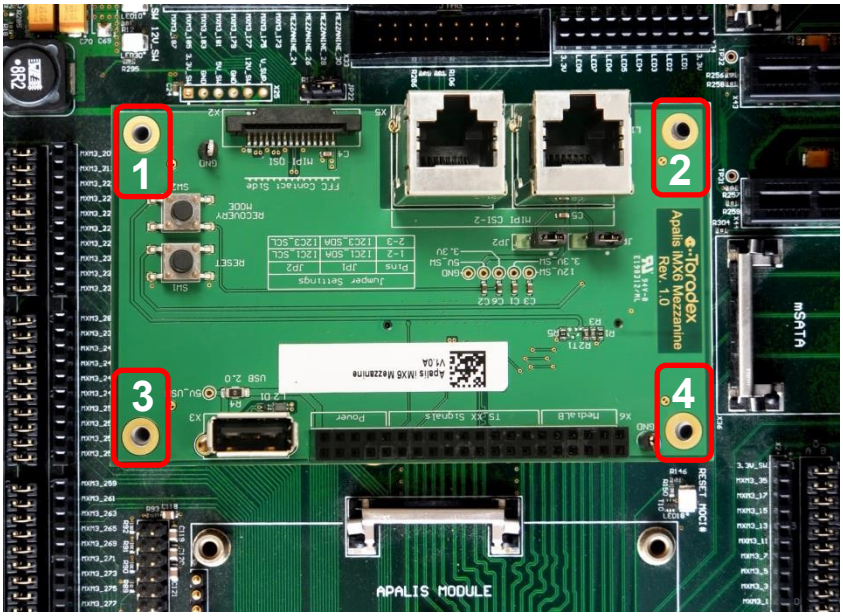
The illustration shown below represents how to attach the Apalis TK1 Mezzanine to the Apalis Carrier Board. *Please note that Apalis iMX6 Mezzanine V1.0A board is used for illustration, actual product may look different from the images shown below:*



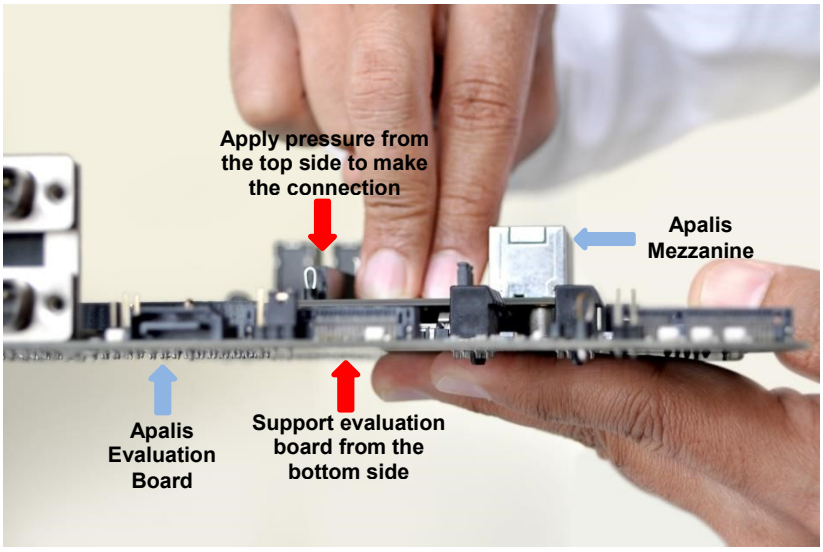
4.1. Assembly Procedure

The following procedure demonstrates how to attach the Apalis TK1 Mezzanine to the Apalis Evaluation Board. Please read the instructions carefully to ensure that the connectors or circuit board does not get damaged. Necessary precautions should be taken to avoid the electrostatic charge.

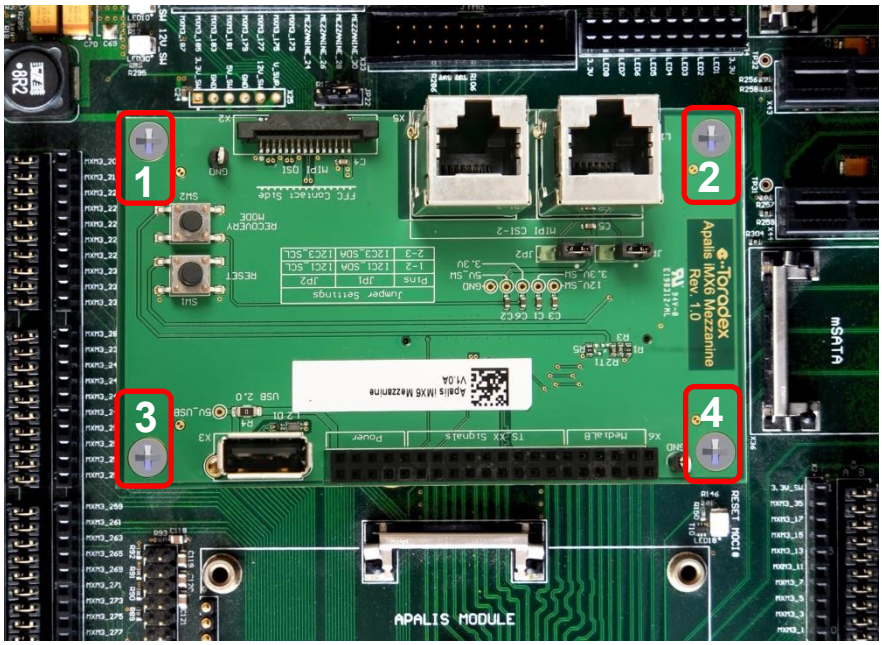
1. Carefully align the mounting holes {1}, {2}, {3}, and {4} on the mezzanine to be in-line with the fasteners available on the Apalis Evaluation board. Place the mezzanine on the Apalis Evaluation Board.



2. As shown in the image below, support the Apalis Evaluation Board from the bottom side, place the fingers just beneath the mezzanine mating connector. Apply pressure on the mezzanine board from the top to make the proper connection. This procedure ensures that the Apalis Evaluation Board PCB does not flex or bent while connecting the Apalis TK1 Mezzanine.



3. Optional: Use 4 units of M3 screws to affix the mezzanine together with the Apalis Evaluation Board.



4. Done. The Apalis TK1 Mezzanine is now firmly connected to the Apalis Evaluation Board.

5. Temperature Range

5.1. Operating Temperature Range

- -40 °C to +85 °C

6. Mechanical Data

6.1. Dimensions - Top Side

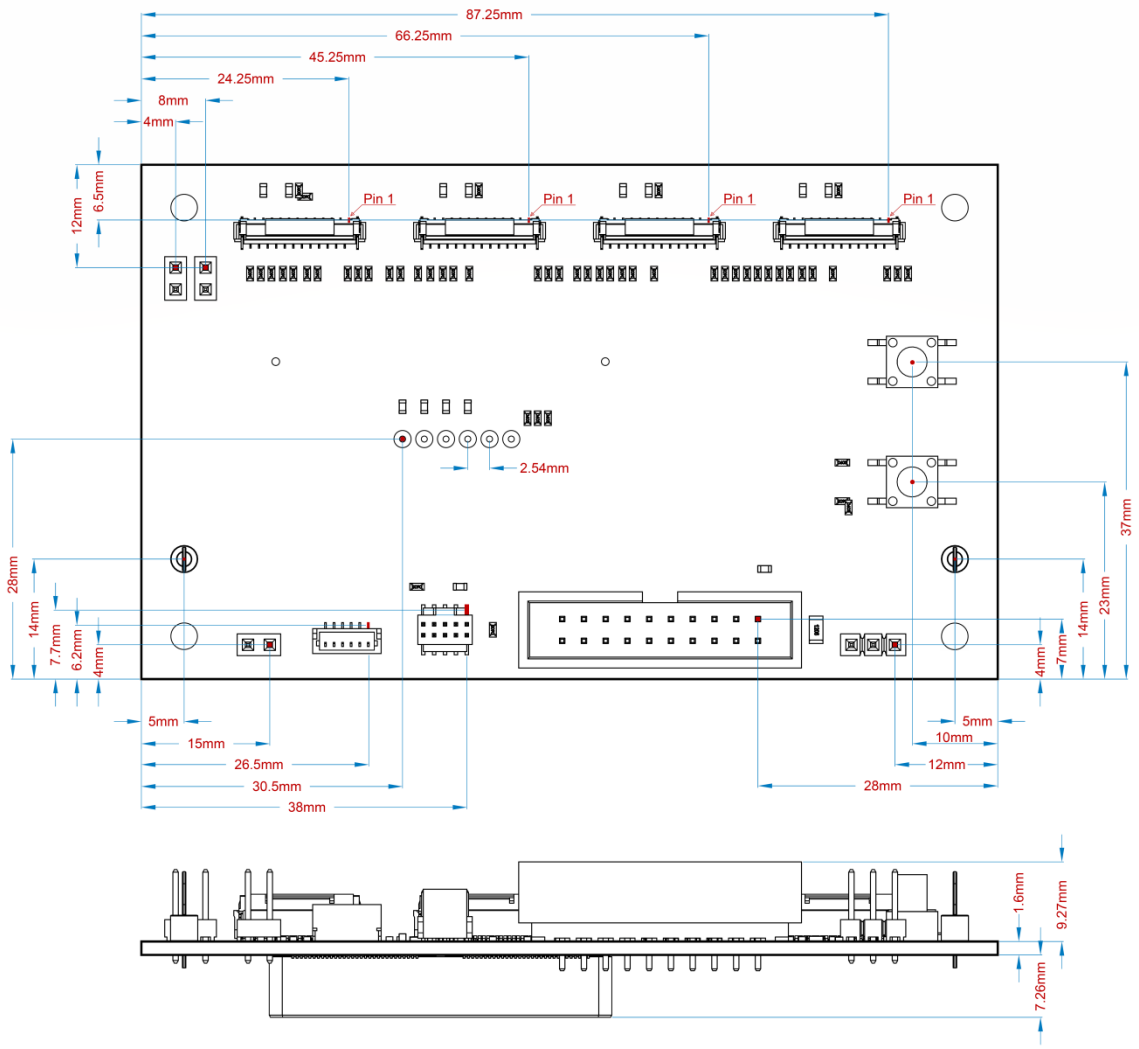


Fig.4 Apalis TK1 Mezzanine Board Mechanical Drawing – Top Side
All dimensions in millimetres (mm)

6.2. Dimensions - Bottom Side

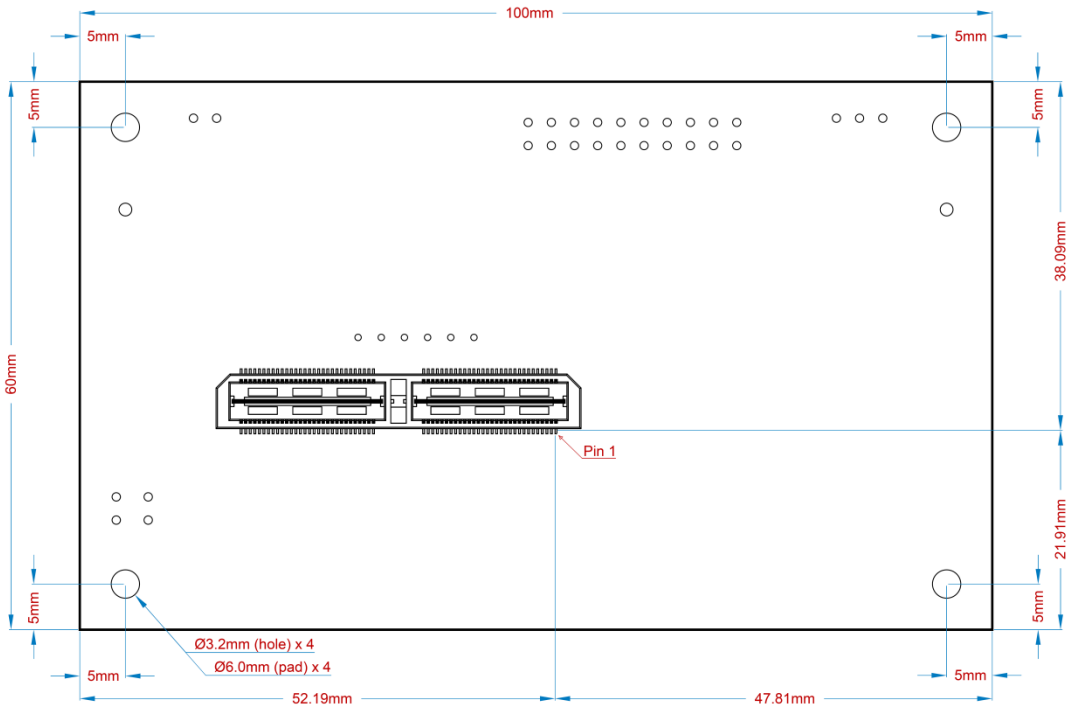


Fig.5 Apalis TK1 Mezzanine Board Mechanical Drawing – Bottom Side
All dimensions in millimetres (mm)

7. Design Data

The design data for the Toradex carrier board and adapter board are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the adapter board design data, please use the web-link below:

http://developer.toradex.com/carrier-board-design/reference-designs

8. Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Materials, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance