Product Change Notification (PCN)

Transition from Apalis TK1 2GB V1.1A to Apalis TK1 2GB V1.2A

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1. Toradex Product Numbers Affected

EOL Product		Replacement Product	
Part Number	Product Name	Part Number	Product Name
00341100	Apalis TK1 2GB V1.1A	00341200	Apalis TK1 2GB V1.2A

2. Product Phase in / Phase out Schedule

EOL Product		Replacement Product	
Part Number	Estimated Schedule	Part Number	Estimated Schedule
00341100	Product will be sold until inventory is depleted.	00341200	Sample Production: Limited numbers available now. Volume Production: July 2018

3. Description of Changes

From 00341100 Apalis TK1 2GB V1.1A to 00341200 Apalis TK1 2GB V1.2A:

3.1. Pin Assignment Changes

MXM Pin	Apalis Function	V1.0 and V1.1	V1.2	Remarks
5	GPIO3	SoC pin: DDC_SCL	SoC pin: USB_VBUS_EN0	Add other 3.3V GPIOs since the original ones have limited output capability (see Errata #5)
7	GPIO4	SoC pin: DDC_SDA	SoC pin: USB_VBUS_EN1	
205	I2C2_SDA (DDC)	SoC pin: GEN2_I2C_SDA	SoC pin: DDC_SDA	The old I2C interface had max. 0.45V threshold for Low Input. This was not compatible with some HDMI monitors.
207	I2C2_SCL (DDC)	SoC pin: GEN2_I2C_SCL	SoC pin: DDC_SCL	
84	USBH_EN	SoC pin: USB_VBUS_EN1	SoC pin: GEN2_I2C_SDA	The new pins emulate GPIO functions. They feature unidirectional level shifter and can only be used as output.
274	USBO1_EN	SoC pin: USB_VBUS_EN0	SoC pin: GEN2_I2C_SCL	
99	TS_3		I210 pin: SPD0	The IEEE1588 synchronization pins of the I210 Ethernet controller have been added to available type specific pins.
123	TS_4		I210 pin: SPD1	
135	TS_5		I210 pin: SPD2	

The TK1 SoC pin assignment has been changed with V1.2 for the following MXM pins. However, the default function (indicated in brackets) remains as defined by the Apalis standard.

- **MXM pin 5 (GPIO3):** Change from TK1 SoC signal DDC_SCL to USB_VBUS_EN0. This allows using the MXM pin as fully-featured GPIO vs. open drain only before (see also Errata #5: http://docs.toradex.com/103358-apalis-tk1-errata.pdf).
  Important: The reset state of this MXM pin is driving low. It was pulled up with 100k previously.
- **MXM pin 7 (GPIO4):** Change from TK1 SoC signal DDC_SDA to USB_VBUS_EN1: This allows using the MXM pin as fully-featured GPIO vs. open drain only before (see also Errata #5: http://docs.toradex.com/103358-apalis-tk1-errata.pdf).
  Important: The reset state of this MXM pin is driving low. It was pulled up with 100k previously.
- **MXM pin 205 (I2C2_SCL (DDC)):** Change from TK1 SoC signal GEN2_I2C_SCL to DDC_SCL: The newly used pin has a wider voltage range and improves the situation described in Errata #7: http://docs.toradex.com/103358-apalis-tk1-errata.pdf
- **MXM pin 207 (I2C2_SDA (DDC)):** Change from TK1 SoC signal GEN2_I2C_SDA to DDC_SDA: The newly used pin has a wider voltage range and improves the situation described in Errata #7: http://docs.toradex.com/103358-apalis-tk1-errata.pdf
- **MXM pin 84 (USBH_EN):** Change from TK1 SoC signal USB_VBUS_EN1 to GEN2_I2C_SDA: The signal swap was a result of the changes indicated above. This MXM pin now features an output level shifter and can no longer be used as input.
- **MXM pin 274 (USBO1_EN):** Change from TK1 SoC signal USB_VBUS_EN0 to GEN2_I2C_SCL: The signal swap was a result of the changes indicated above. This MXM pin now features an output level shifter and can no longer be used as input.

- The Ethernet PHY used on the Apalis TK1 2GB module is real-time Ethernet capable (IEEE 1588). Three of the configurable input/output pins (SPD) of the Ethernet PHY were routed to previously unused MXM pins in order to allow using these hardware features. For further information about the SPD pins, please look at the Intel I210 Ethernet PHY datasheet.
  - MXM pin 99 (TS_3) → I210 SPD0 pin
  - MXM pin 123 (TS_4) → I210 SPD1 pin
  - MXM pin 135 (TS_5) → I210 SPD2 pin

3.2. Additional Changes

- Increased the total capacitance on the Apalis TK1 SoM to further improve voltage stability.
- Add workaround for Intel i210 Ethernet controller Errata #32: https://www.intel.com/content/dam/www/public/us/en/documents/specification-updates/i210-ethernet-controller-spec-update.pdf
- RESET_MOCI# circuit changed. Signal will be held low until the software (bootloader or Linux kernel boot) drives the RESET_MOCI_CTRL signal high. In the previous version, the RESET_MOCI# signal was released together with the CPU reset on the SoM and the Linux kernel had to do a second RESET_MOCI# cycle during boot as a workaround for the PCIe switch which is located on the Evaluation Board.
- The Apalis TK1 2GB modules will ship with pre-installed Toradex Easy Installer software instead of Embedded Linux image. Please have a look at the following website for details about the Toradex Easy Installer: https://developer.toradex.com/software/toradex-easy-installer

4. Customer Impact

4.1. Hardware Design

- The reset status of the MXM pin 5 (GPIO3) and MXM pin 7 (GPIO4) are changed from 100k pulled up to driving low. The status can be changed in the bootloader or in Linux kernel boot up. However, during the power up sequence before the bootloader can reconfigure the pin states, these pins will always be driven low. Customers need to make sure that the different reset level is not causing issues during power up and boot sequence. If these pins are used as input, try to avoid driving them high during the power up sequence.
- Customers who used MXM pins which changed the internal routing and do not use the Apalis default functions need to check in detail if the new signals on these MXM pins support the features they need. For example, MXM pin 84 and 274 (USB power enable output) do no longer feature input functionality.
- Customers who'd like to use the newly available real-time Ethernet pins (SPD0-2) need to redesign their carrier board.

4.2. Software

Once the new 00341200 Apalis TK1 2GB V1.2A hardware revision is available, we will provide an updated BSP that supports all changes. The new BSP will be backwards compatible with older hardware revision. If a custom BSP or an older Toradex BSP version is used, the following modifications will be required:

- Different Pins for Apalis GPIO3 and Apalis GPIO4:
  If those GPIO pins are used in the system, adjustments are needed.
- Different I2C Bus for DDC EDID:
  If DVI-D or HDMI is used, adjustments are needed.

- New Pins for USB Power Enable Signals:
  If USB host functionality is in use, adjustments are needed.
- Support for IEEE1588:
  Our Embedded Linux BSPs come with basic IEEE1588 aka PTP support pre-installed. External IEEE1588 pins are a new optional feature which may require further driver/software adjustments to be done.
- RESET_MOCI_CTRL Reset Value Low:
  On prior hardware versions the reset value of the RESET_MOCI_CTRL signal was already high meaning the RESET_MOCI# output signal was already de-asserted in hardware without any possible software intervention. This has now been changed to a reset value of low which means software needs to actively drive the RESET_MOCI_CTRL signal high to release the RESET_MOCI# signal.
  Current BSPs already release RESET_MOCI# in the boot loader and later during Linux kernel boot assert it again to work around a PCIe switch errata.
  Future BSPs will no longer do this in the boot loader but rather defer releasing RESET_MOCI# to the Linux kernel. This has the added benefit that the RESET_MOCI# signal will only transition once. The disadvantage is that the USB hub on the Apalis Evaluation board is kept in reset in U-Boot and therefore none of its ports are operational in U-Boot. If the old behaviour in newer BSPs is desired, or the new behaviour in older BSPs is required, adjustments are needed.

The pre-installed software changes from embedded Linux to Toradex Easy Installer. This new tool is basically U-Boot and Linux based. Customers relying on a pre-installed standard embedded Linux image might have to adjust their production programming depending on their use case.

Details on above mentioned adjustments may be found in the following article on our developer website: http://developer.toradex.com/knowledge-base/apalis-tk1-v1-2a-specific-software-modifications

5. Definitions

LTB: Last Time Buy

LTS: Last Time Ship

EOL: End Of Life

SoC: System on Chip (Nvidia TK1)

SoM: System on Module (Apalis TK1)

SPD: Software Defined Pin (from Intel I210 Ethernet PHY datasheet)

6. Contact

Please contact Toradex if you have any questions.

For commercial and sales questions please contact shop@toradex.com

For technical questions please contact support@toradex.com