Apalis iMX6

Errata Document

Document Revision History

Date	Doc. Rev.	Notes
2017-11-08	Rev. 1.0	Added Errata #1: Secure Boot Vulnerabilities
2018-10-08	Rev. 1.1	Added Errata #2: Possible Noise on Audio Output during Reset Cycle
2021-07-23	Rev. 1.2	Added Errata #3: POWER_ENABLE_MOCI indeterminate due to backfeeding
2022-12-30	Rev. 1.3	Added Errata #4: SkyHigh eMMC's not properly initialized when booted from other media in pSLC mode Added Errata #5: Endurance degradation of modules with the SkyHigh eMMC in pSLC mode

Overview

Errata #1: Secure Boot Vulnerabilities (NXP ERR010872 and ERR010873)

Affected Version: **Apalis iMX6D 512MB V1.1B and earlier**
Apalis iMX6D 1GB IT V1.1B and earlier
Apalis iMX6Q 1GB V1.1B and earlier
Apalis iMX6Q 2GB IT V1.1C and earlier
Fixed in: not defined yet

1.1 Description

These errata are actually NXP errata affecting all i.MX and Vybrid processors. There are two issues in the boot ROM when using the processors in a security-enabled configuration (SEC_CONFIG[1] eFUSE is programmed). **By default, this fuse is not programmed on Toradex modules. Customers not fusing this setting are therefore not affected by these issues.**

Customers using the security-enabled configuration are affected by these issues. More information can be found in the respective NXP errata documents:
https://docs1.toradex.com/104705-err010872-secure-boot-vulnerability-erratum-preliminary-rev0.pdf
https://docs1.toradex.com/104706-err010873-secure-boot-vulnerability-erratum-preliminary-rev0.pdf

1.2 Workaround

Please refer to the documents mentioned above for workarounds.

Errata #2: Possible Noise on Audio Output during Reset Cycle

Affected Version: **Apalis iMX6D V1.0**
Apalis iMX6D V1.1
Apalis iMX6Q V1.0
Apalis iMX6Q V1.1

Fixed in: No fix planned

2.1 Description

The audio codec on the SGTL5000 on the module does not feature a dedicated reset input. If a sound is playing back during a reset cycle, the SGTL5000 remains in playback mode. The audio codec is then repeating the last short sample, which remains in its buffer. This creates an audible noise at the output. The actual noise depends on the sample which is in the buffer. This noise is retained until the audio codec is reinitialized during the booting process.

The issue only appears if the reset is initiated by the RESET_MICO# reset (e.g., pressing the reset button on the evaluation board). The effect has not been seen during software-initiated reset cycles or regular power cycles.

2.2 Workaround

There is currently no workaround available. Try to avoid pressing the reset button while any sound is played back from the on-module audio codec.

Errata #3: HAR-8210 – POWER_ENABLE_MOCI indeterminate due to backfeeding

Affected Version: **Apalis iMX6D V1.0**
Apalis iMX6D V1.1
Apalis iMX6Q V1.0
Apalis iMX6Q V1.1

Fixed in: No fix planned

3.1 Customer Impact

Depending on the carrier board and the amount of backfeeding, the POWER_ENABLE_MOCI might not go low enough to turn off the peripheral voltage rails in the shutdown state.

3.2 Description

The POWER_ENABLE_MOCI signal is intended to be used for switching the peripheral voltage rails on the carrier board, like the 5V_SW and 3.3V_SW on the Ixora. Depending on the amount of backfeeding over the interface signals from the carrier board to the Apalis iMX6 module, the POWER_ENABLE_MOCI signal can remain between 1.0V and 1.4V in module shutdown. Depending on the carrier board circuit, this can be too high for turning off the peripheral voltage rails.

For example, on the Ixora V1.2, a different buck converter for the 5V_SW is used than on the previous versions. The threshold voltage for the enable signal is lower on the new buck converter. Depending on the backfeeding level, the 5V_SW buck converter does not get disabled in the shutdown state. The Ixora V1.0 and V1.1 are not affected by this issue since they have been using a different buck converter with a higher threshold.

3.3 Workaround

Add a circuit to the carrier board for increasing the POWER_ENABLE_MOCI threshold voltage to between 2.0V and 2.5V. This could be achieved by adding a comparator or similar circuit. Such a solution is implemented in the V1.3 revision of the Ixora.

A simple voltage divider added to the POWER_ENABLE_MOCI signal can shift the voltage levels. Important: make sure that the minimum input voltage for enabling the buck converter is still guaranteed. With the AOZ2260 buck converter (which is used on Ixora V1.2), a 10k/10k voltage divider can be a suitable option. For patching such a divider, replace R15 with a 10k 0603 resistor and add another 10k resistor from the PMIC_EN_5V signal to the ground.

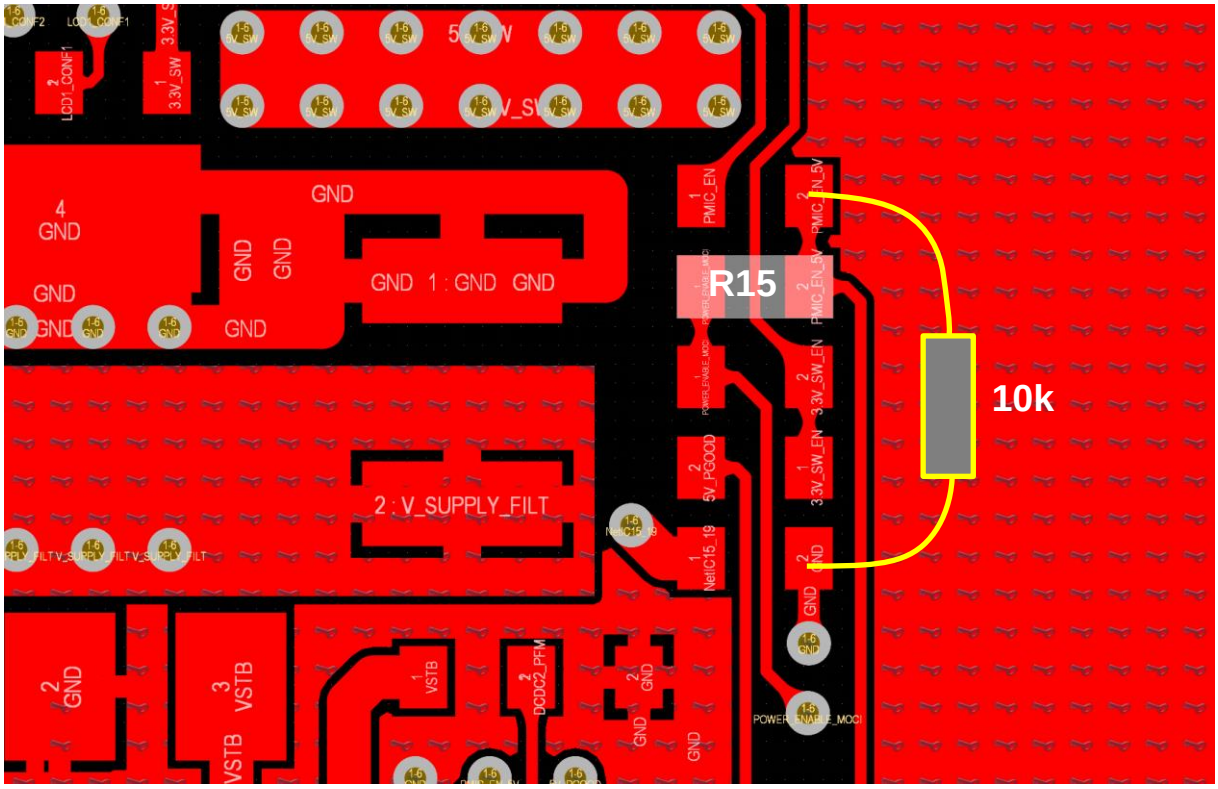

Figure 1 Possible voltage divider workaround on Ixora V1.2

Errata #4: HAR-9468 – SkyHigh eMMC's not properly initialized when booted from other media in pSLC mode

Affected Version:
Apalis iMX6D 512MB V1.1C
Apalis iMX6Q 1GB V1.1C
Apalis iMX6Q 1GB V1.1D
Apalis iMX6Q 1GB V1.1Y

Fixed in:
Apalis iMX6D 512 MB V1.1C
Apalis iMX6Q 1GB V1.1D
Apalis iMX6Q 1GB V1.1Y

4.1 Customer Impact

Customers using pSLC (pseudo-SLC) mode and trying to boot from SD card the module may not work. When configuring and using the SkyHigh eMMC in MLC mode customers are not affected. **Modules produced after December 9, 2022 are not affected.**

4.2 Description

When configuring and using the SkyHigh eMMC in pSLC (pseudo-SLC) mode and trying to boot from SD card the module may not work.

4.3 Workaround

There are two possible workarounds:

1. Access the eMMC from U-Boot before launching the Kernel by using the following command:

   ls mmc 0.4:0 /boot

2. Update the eMMC firmware according to the instructions:

   https://developer.toradex.com/linux-bsp/how-to/hardware-related/firmware-update-skyhigh-emmc

Errata #5: HAR-9439 – Endurance degradation of modules with the SkyHigh eMMC in pSLC mode

Affected Version:
Apalis iMX6D 512MB V1.1C
Apalis iMX6Q 1GB V1.1C
Apalis iMX6Q 1GB V1.1D
Apalis iMX6Q 1GB V1.1Y

Fixed in:
Apalis iMX6D 512MB V1.1C
Apalis iMX6Q 1GB V1.1D
Apalis iMX6Q 1GB V1.1Y

5.1 Customer Impact

Using the SkyHigh eMMC based modules in pSLC (pseudo-SLC) mode and writing more than 32TB to the eMMC will lock up the device, not allowing any further writes to the eMMC. **Modules produced after December 9, 2022 are not affected.**

5.2 Description

When configuring and using the SkyHigh eMMC in pSLC (pseudo-SLC) mode and writing more than 32TB to the eMMC, the eMMC firmware will lock up the device, not allowing any further writes to the eMMC. The theoretical lifetime data write capacity for SkyHigh eMMCs in pSLC mode would be 60TB. By default, Toradex doesn't enable the pSLC mode and therefore doesn't run into this problem.

5.3 Workaround

SkyHigh implemented a FW fix. Customers using pSLC mode and writing more than 32TB during the lifetime of the product can execute a single-step FW update:
https://developer.toradex.com/hardware/hardware-resources/firmware-update-skyhigh-emmc