



# Colibri iMX6

## Errata Document



## Document Revision History

Date	Doc. Rev.	Notes
2016-06-15	Rev. 1.0	Initial Release
2017-04-24	Rev. 1.1	Updating Errata #1 and #2 according to the module V1.1
2017-11-07	Rev. 1.2	Added Errata #3: Secure Boot Vulnerabilities
2018-10-15	Rev. 1.3	Added Errata #4: nRESET_OUT race condition Added Errata #5: Possible Noise on Audio Output during Reset Cycle
2022-12-30	Rev. 1.4	Added Errata #6: SkyHigh eMMC's not properly initialized when booted from other media in pSLC mode Added Errata #7: Endurance degradation of modules with the SkyHigh eMMC in pSLC mode

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## Errata #1: Module cannot wake up from PMIC shutdown mode

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Affected Version: **Colibri iMX6 V1.0**  
Fixed in: **Colibri iMX6 V1.1**

### 1.1 Description

If a module shut down is proceeded by the software which turns off the power management IC (PMIC), the module can only be restarted again if all power rails are removed (including VCC\_BATT) and reapplied. This means, as long as the RTC is running (VCC\_BATT available), the module cannot be started.

All other sleep modes of the modules are not affected by this issue.

### 1.2 Workaround

Do not shut down the PMIC. The current Linux and Windows CE image take this in account. They leave the PMIC running after finishing the software shut down request. The module main input rail can be removed without issue as long as no PMIC shut down request was executed.

In most systems, the PMIC shut down is not needed. The Colibri module concept does anyway not implement a shutdown mode similar to the “Soft-Off-Modus” S5 that is known from the ACPI specifications ([https://en.wikipedia.org/wiki/Advanced\\_Configuration\\_and\\_Power\\_Interface](https://en.wikipedia.org/wiki/Advanced_Configuration_and_Power_Interface)).

## Errata #2: Software initiated reset cycle does not assert nRESET\_OUT

Affected Version: **Colibri iMX6 V1.0**  
Fixed in: **Colibri iMX6 V1.1**

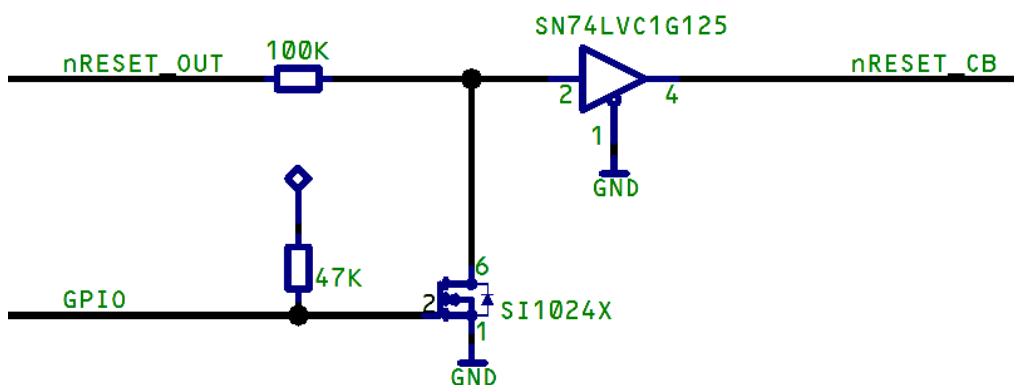
### 2.1 Description

During a software initiated reset cycle, the nRESET\_OUT signal is not asserted on the Colibri iMX6 V1.0 module. Unlike other Colibri modules, the nRESET\_OUT signal remains the whole time high during the software initiated reset.

During power up as well as hardware initiated reset cycles (by pressing the nRESET\_IN/RESET\_EXT button), the nRESET\_OUT signal gets asserted similar to other Colibri modules. This is not an issue as long as external peripheral devices on the carrier board do not need to be reset during a software reset or no software initiated reset cycles are used on a system.

### 2.2 Workaround

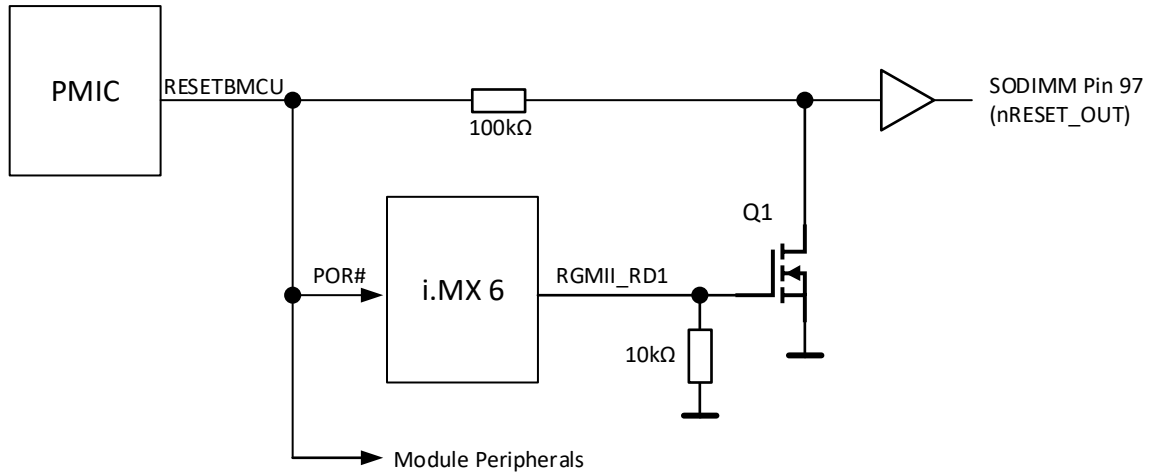
A possible workaround is implementing a small reset circuit on the carrier board that allows driving low the reset signal by using any free GPIO:



Since on the Colibri iMX6 the reset state of regular GPIOs is configured as input with enabled internal pull up resistor, the transistor will pull down the reset line during a software initiated reset cycle. The bootloader or application needs to reconfigure the GPIO as output and drive it low for releasing the external reset signal.

### 2.3 Implemented Fix in V1.1

Beginning with the Colibri iMX6 V1.1, a circuit has been implemented on the module similar to the proposed workaround (see picture below). The module can drive the nRESET\_OUT signal low by setting the RGMII\_RD1 pin of the SoC (GPIO6\_IO27) high. The pull down resistor on this line makes sure that the circuit is compatible with older software versions which do not drive the RGMII\_RD1 pin. The proposed workaround circuit for V1.0 is still compatible with the module V1.1.



## Errata #3: Secure Boot Vulnerabilities (NXP ERR010872 and ERR010873)

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Affected Version: **Colibri iMX6S 256MB (IT) V1.1A and earlier**  
**Colibri iMX6DL 512MB (IT) V1.1A and earlier**  
Fixed in: not defined yet

### 3.1 Description

These errata are actually NXP errata affecting all i.MX and Vybrid processors. There are two issues in the boot rom when using the processors in a security enabled configuration (SEC\_CONFIG[1] eFUSE is programmed). **By default, this fuse is not programmed on Toradex modules. Customers not fusing this setting are therefore not affected by these issues.**

Customers using the security enabled configuration are affected by these issues. More information can be found in the respective NXP errata documents:

<https://docs1.toradex.com/104705-err010872-secure-boot-vulnerability-erratum-preliminary-rev0.pdf>

<https://docs1.toradex.com/104706-err010873-secure-boot-vulnerability-erratum-preliminary-rev0.pdf>

### 3.2 Workaround

Please refer to the above-mentioned documents for workarounds.

**Errata #4: Possible short pulse on nRESET\_OUT if nRESET\_EXT is hold down**

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Affected Version: **Colibri iMX6S 256MB (IT) V1.1A**  
**Colibri iMX6DL 512MB (IT) V1.1A**  
Fixed in: not planned

**4.1 Description**

The nRESET\_EXT (reset input of the module, pin 26) features a debouncing circuit since it is allowed to connect directly a reset button to this pin. The debouncing circuit delays the reset by around 30ms. During a regular power up sequence, the nRESET\_OUT (reset output of the module, pin 87) is released also at around 30ms. If the nRESET\_EXT pin is hold down during the power up, the two delays are racing. If the debouncing circuit wins, everything is OK, the nRESET\_OUT remains until the nRESET\_EXT is released. However, if the debouncing loses the race, there can be as short peak on the nRESET\_OUT.

Whether this peak appears or not as well as the duration depends on different factors. It is depending on the tolerances of the debouncing circuit and therefore can appear on certain modules more often than on others. It also depends on the module temperature and whether an RTC battery is present or not.

**4.2 Workaround**

The Colibri iMX6 module as well as most of the peripheral devices are not affected by the possible nRESET\_OUT pulse. This means in most of the cases, the issue can be ignored. For peripherals that relay on a single reset release during the power up sequence, an additional circuit is required on the carrier board. Such a circuit can be a simple AND gate with the NRESET\_OUT and nRESET\_EXT as inputs can be used.



## Errata #5: Possible Noise on Audio Output during Reset Cycle

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Affected Version: **All Colibri iMX6S and Colibri iMX6DL versions**

Fixed in: No fix planed

### 5.1 Description

The audio codec on the SGTL5000 on the module does not feature a dedicated reset input. If a sound is playing back during a reset cycle, the SGTL5000 remains in playback mode. The audio codec is then repeating the last short sample which is remains in its buffer. This creates an audible noise at the output. The actual noise depends on the sample which is in the buffer. This noise is retained until the audio codec is reinitialized during the booting process.

The issue only appears if the reset is initiated by the RESET\_MICO# reset (e.g. pressing reset button on evaluation board). The effect has not been seed during software initiated reset cycles or regular power cycles.

### 5.2 Workaround

There is currently no workaround available. Try to avoid pressing the reset button while any sound is played back from the on module audio codec.

Errata #6: HAR-9467 – SkyHigh eMMC's not properly initialized when booted from other media in pSLC mode

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Affected Version: **Colibri iMX6S 256MB V1.1B**  
**Colibri iMX6S 256MB V1.1Y**  
**Colibri iMX6DL 512MB V1.1B**  
**Colibri iMX6DL 512MB V1.1Y**

Fixed in: **Colibri iMX6S 256MB V1.1B**  
**Colibri iMX6S 256MB V1.1Y**  
**Colibri iMX6DL 512MB V1.1B**  
**Colibri iMX6DL 512MB V1.1Y**

### 6.1 Customer Impact

Customers using pSLC (pseudo-SLC) mode and trying to boot from SD card the module may not work. When configuring and using the SkyHigh eMMC in MLC mode customers are not affected. **Modules produced after December 9, 2022 are not affected.**

### 6.2 Description

When configuring and using the SkyHigh eMMC in pSLC (pseudo-SLC) mode and trying to boot from SD card the module may not work.

### 6.3 Workaround

There are two possible workarounds:

1. Access the eMMC from U-Boot before launching the Kernel by using the following command:

```
ls mmc 0.4:0 /boot
```

2. Update the eMMC firmware according to the instructions:

<https://developer.toradex.com/linux-bsp/how-to/hardware-related/firmware-update-skyhigh-emmc>

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**Errata #7: HAR-9438 – Endurance degradation of modules with the SkyHigh eMMC in pSLC mode**

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**Affected Version:**

- Colibri iMX6S 256MB V1.1B**
- Colibri iMX6S 256MB V1.1Y**
- Colibri iMX6DL 512MB V1.1B**
- Colibri iMX6DL 512MB V1.1Y**

**Fixed in:**

- Colibri iMX6S 256MB V1.1B**
- Colibri iMX6S 256MB V1.1Y**
- Colibri iMX6DL 512MB V1.1B**
- Colibri iMX6DL 512MB V1.1Y**

### 7.1 Customer Impact

Using the SkyHigh eMMC based modules in pSLC (pseudo-SLC) mode and writing more than 32TB to the eMMC will lock up the device, not allowing any further writes to the eMMC. **Modules produced after December 9, 2022 are not affected.**

### 7.2 Description

When configuring and using the SkyHigh eMMC in pSLC (pseudo-SLC) mode and writing more than 32TB to the eMMC, the eMMC firmware will lock up the device, not allowing any further writes to the eMMC. The theoretical lifetime data write capacity for SkyHigh eMMCs in pSLC mode would be 60TB. By default, Toradex doesn't enable the pSLC mode and therefore doesn't run into this problem.

### 7.3 Workaround

SkyHigh implemented a FW fix. Customers using pSLC mode and writing more than 32TB during the lifetime of the product can execute a single-step FW update:

<https://developer.toradex.com/hardware/hardware-resources/firmware-update-skyhigh-emmc>

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