Apalis TK1
Datasheet
## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Doc. Rev.</th>
<th>Apalis TK1 Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>23-Feb-2016</td>
<td>Rev. 0.9</td>
<td>V1.0A</td>
<td>Initial Release</td>
</tr>
<tr>
<td>09-Jun-2016</td>
<td>Rev. 1.0</td>
<td>V1.0A</td>
<td>Add module picture on front page</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 8: add reference to errata document</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 9.6: add reference for suitable heatsink</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Minor changes</td>
</tr>
<tr>
<td>07-Jul-2016</td>
<td>Rev. 1.1</td>
<td>V1.0C</td>
<td>Section 6.5.5: Add routing information to eDP interface</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 9.6: Correct operation temperature (extend)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Minor changes</td>
</tr>
<tr>
<td>29-Sep-2016</td>
<td>Rev. 1.2</td>
<td>V1.1A</td>
<td>Update assignment of pin 190 (SD1_CD#) according to changes in PCB version 1.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Adding recommendation to non-used input level shifted signals</td>
</tr>
<tr>
<td>07-Nov-2017</td>
<td>Rev. 1.3</td>
<td>V1.2A</td>
<td>Section 1: Correction of maximum CPU frequency</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 1.3.3: Add remark to eMMC flash endurance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 1.3.4: Update number of available interfaces</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 1.4: Update number of available interfaces</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 3.2: Update pin assignment</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 4.5: Update function list</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.2: Update GPIOs and Wake source</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.3: Add IEEE1588 function and SPD pins</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.4: Update pin assignment</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.5: Update DDC interface pins, clarify USB 3.0 OTG</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.6: Update DDC pins, remove I2C on Pin 5/7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.18: Add information about unused touch signals</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.19: Correct I/O direction of CSI clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 9.1: Correction of Vmax USBO1_VBUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 9.3: Typical consumption values added</td>
</tr>
<tr>
<td>08-Oct-2018</td>
<td>Rev. 1.4</td>
<td>V1.2A</td>
<td>Section 3.2: rename DAP1_RESET to DAP1_RESET#</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.14: correct SGTL500 pin number for AAP1_HP_L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 6.15: rename DAP1_RESET to DAP1_RESET#</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 9.5: correct SoC position in Figure 13</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Section 9.6: correct junction temperature specification</td>
</tr>
</tbody>
</table>
Contents

1. Introduction .................................................................................................................... 5
   1.1 Hardware .................................................................................................................. 5
   1.2 Software................................................................................................................... 5
   1.3 Main Features ......................................................................................................... 6
       1.3.1 CPU .................................................................................................................. 6
       1.3.2 MCU.................................................................................................................. 6
       1.3.3 Memory ............................................................................................................ 6
       1.3.4 Interfaces ......................................................................................................... 7
       1.3.5 Graphics Processing Unit ............................................................................... 8
       1.3.6 HD Video Decode ........................................................................................... 8
       1.3.7 HD Video Encode ............................................................................................ 8
       1.3.8 Supported Operating Systems ...................................................................... 8
   1.4 Interface Overview .................................................................................................. 8
   1.5 Reference Documents............................................................................................. 9
       1.5.1 NVIDIA Tegra K1 ......................................................................................... 9
       1.5.2 NXP (Freescale) K20 .................................................................................... 9
       1.5.3 Ethernet Controller ....................................................................................... 10
       1.5.4 Audio Codec ................................................................................................... 10
       1.5.5 Apalis Carrier Board Design Guide .............................................................. 10
       1.5.6 Layout Design Guide ...................................................................................... 10
       1.5.7 Toradex Developer Centre ............................................................................ 10
       1.5.8 Apalis Evaluation Board Schematics .............................................................. 10
       1.5.9 Toradex Pinout Designer ............................................................................... 10

2. Architecture Overview ................................................................................................. 11
   2.1 Block Diagram ........................................................................................................ 11

3. Apalis TK1 Connectors ................................................................................................. 12
   3.1 Pin Numbering ........................................................................................................ 12
   3.2 Assignment ............................................................................................................... 12

4. Tegra K1 I/O Pins ......................................................................................................... 18
   4.1 I/O Pin Types ......................................................................................................... 18
       4.1.1 3.3V Signals .................................................................................................... 18
       4.1.2 1.8V/3.3V Signals ........................................................................................ 18
       4.1.3 3.3V Tolerant Signals .................................................................................. 19
       4.1.4 Output Shifted Signals ............................................................................... 19
       4.1.5 Input Shifted Signals .................................................................................... 19
       4.1.6 Bidirectional Shifted Signals .................................................................... 20
       4.2 TK1 Pin Control .................................................................................................. 20
       4.3 TK1 Function Multiplexing ............................................................................... 21
       4.4 Pin Reset Status ................................................................................................. 21
       4.5 TK1 Functions List ............................................................................................. 21

5. Kinetis K20 Companion MCU I/O Pins .................................................................... 27
   5.1 K20 Pin Control ..................................................................................................... 28
   5.2 K20 Functions List ................................................................................................. 29

6. Interface Description .................................................................................................. 32
   6.1 Power Signals ........................................................................................................ 32
       6.1.1 Digital Supply ............................................................................................... 32
       6.1.2 Analogue Supply ......................................................................................... 32
       6.1.3 Power Management Signals ...................................................................... 32
   6.2 GPIOs ...................................................................................................................... 33
       6.2.1 Wakeup Source .............................................................................................. 33
   6.3 Ethernet .................................................................................................................. 34
6.4 USB .......................................................................................................................... 34
6.4.1 USB Data Signal .................................................................................................. 35
6.4.2 USB Control Signals .......................................................................................... 36
6.5 Display ...................................................................................................................... 36
6.5.1 Parallel RGB LCD Interface .............................................................................. 36
6.5.2 LVDS .................................................................................................................... 37
6.5.3 HDMI ................................................................................................................. 39
6.5.4 Analogue VGA .................................................................................................... 40
6.5.5 Embedded Display Port (eDP) .......................................................................... 40
6.5.6 Display Serial Interface (DSI) .......................................................................... 41
6.6 SATA ....................................................................................................................... 43
6.8 SPI .......................................................................................................................... 44
6.8.1 Real-Time Clock (RTC) recommendation ......................................................... 45
6.9 UART ....................................................................................................................... 46
6.10 OWR (One Wire) ................................................................................................... 52
6.11 SD/MMC ............................................................................................................... 52
6.12 PWM (Pulse Width Modulation) ........................................................................ 50
6.14 Analogue Audio .................................................................................................... 55
6.15 Digital Audio ........................................................................................................ 55
6.16 SPI (Sony-Philips Digital Interface I/O) ............................................................... 56
6.17 Touch Panel Interface ........................................................................................... 56
6.18 Analog Inputs ........................................................................................................ 57
6.19 Camera Interface .................................................................................................. 58
6.20 SPI ........................................................................................................................ 60
6.21 Keypad .................................................................................................................. 61
6.22 Controller Area Network (CAN) ......................................................................... 61
6.23 JTAG ...................................................................................................................... 62
7. Recovery Mode .......................................................................................................... 63
8. Known Issues ............................................................................................................ 64
9. Technical Specifications .......................................................................................... 65
9.1 Absolute Maximum Ratings ............................................................................... 65
9.2 Recommended Operation Conditions .................................................................. 65
9.3 Electrical Characteristics ..................................................................................... 65
9.4 Power Ramp-Up Time Requirements .................................................................. 65
9.5 Mechanical Characteristics ................................................................................. 66
9.5.1 Sockets for the Apalis Modules ...................................................................... 66
9.6 Thermal Specification ............................................................................................ 67
9.7 Product Compliance .............................................................................................. 67
1. Introduction

1.1 Hardware

The Apalis TK1 is a computer module based on the NVIDIA® Tegra® K1 embedded System on Chip (SoC). The Cortex A15 quad-core CPU peaks up to 2.1 GHz (2.07 GHz). Additionally, the Tegra K1 features a fifth low power Cortex A15 processor which can be used instead of the four high performance cores during low compute workload operations.

The Tegra K1 features a powerful NVIDIA® GeForce® Kepler™ Mobile Graphics Processing Unit (GPU) which extends the CUDA® compute architecture to low power consumption devices. Due to its 192 CUDA cores, the GPU shader is able to peak with up to 325 GFLOPS and supports OpenGL® 4.4 and OpenGL® ES 3.1.

The Apalis TK1 incorporates DVFS (Dynamic Voltage and Frequency Switching) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption.

Beside the powerful NVIDIA Tegra K1 SoC, the Apalis TK1 features a NXP (Freescale) Kinetis K20 Micro Controller Unit (MCU) as companion. The K20 features a low power ARM Cortex M4 processor which runs up to 100MHz. The MCU extends the module with two Controller Area Network (CAN) interfaces, several ADC, additional GPIOs and several other low-speed interfaces. Since the controller is independent of the Tegra K1, it can be used for hard real time and security critical tasks.

The module targets a wide range of applications, including: Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment System, POS, Data Acquisition, Thin Clients, Robotics, Gaming, and much more.

It offers a wide range of interfaces from simple GPIOs, industry standard I2C, and SPI buses through to high-speed USB 3.0 interfaces, high-speed PCI Express, and SATA. The HDMI and LVDS interfaces make it very easy to connect large, full HD and beyond resolution displays.

The Apalis TK1 module encapsulates the complexity associated with modern day electronic design, such as high-speed impedance controlled layouts with high component density utilising blind and buried via technology. This allows the customer to create a carrier board which implements the application-specific electronics which is generally much less complicated. The Apalis TK1 module takes this one step further and implements an interface pinout which allows direct connection of real world I/O ports without needing to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high-speed, serial technologies that use impedance controlled differential pairs, as it allows them to easily route such interfaces to common connectors in a simple, robust fashion.

1.2 Software

The Apalis TK1 comes with a preinstalled Embedded Linux Images. Android is available from Toradex partners.
1.3 Main Features

1.3.1 CPU

<table>
<thead>
<tr>
<th>Feature</th>
<th>Apalis TK1 2GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>NVIDIA SoC</td>
<td>CD575M-A1</td>
</tr>
<tr>
<td>CPU Cores</td>
<td>4+1</td>
</tr>
<tr>
<td>ARM Cortex Version</td>
<td>A15</td>
</tr>
<tr>
<td>L1 Instruction Cache (each core)</td>
<td>32KByte</td>
</tr>
<tr>
<td>L1 Data Cache (each core)</td>
<td>32KByte</td>
</tr>
<tr>
<td>L2 Cache (shared by cores)</td>
<td>2MByte</td>
</tr>
<tr>
<td>NEON MPE</td>
<td>✓</td>
</tr>
<tr>
<td>Maximum CPU frequency</td>
<td>2.07GHz</td>
</tr>
</tbody>
</table>

1.3.2 MCU

<table>
<thead>
<tr>
<th>Feature</th>
<th>Apalis TK1 2GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>NXP MCU</td>
<td>MK20DN512VMC10</td>
</tr>
<tr>
<td>CPU Cores</td>
<td>1</td>
</tr>
<tr>
<td>ARM Cortex Version</td>
<td>M4</td>
</tr>
<tr>
<td>Maximum CPU frequency</td>
<td>100MHz</td>
</tr>
<tr>
<td>SRAM</td>
<td>128KByte</td>
</tr>
<tr>
<td>Flash Memory</td>
<td>512KByte</td>
</tr>
</tbody>
</table>

1.3.3 Memory

<table>
<thead>
<tr>
<th>Feature</th>
<th>Apalis TK1 2GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR3L RAM Size</td>
<td>2GByte</td>
</tr>
<tr>
<td>DDR3L RAM Speed</td>
<td>1848MT/s</td>
</tr>
<tr>
<td>DDR3L RAM Memory Width</td>
<td>64bit</td>
</tr>
<tr>
<td>eMMC NAND Flash (8bit)*</td>
<td>16GByte</td>
</tr>
</tbody>
</table>

* eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear levelling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here [http://developer.toradex.com/knowledge-base/flash-memory](http://developer.toradex.com/knowledge-base/flash-memory) and here [https://en.wikipedia.org/wiki/Flash_memory#Write_endurance](https://en.wikipedia.org/wiki/Flash_memory#Write_endurance).
## 1.3.4 Interfaces

<table>
<thead>
<tr>
<th>Interface</th>
<th>Apalis TK1 2GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD RGB (24bit, 225 Mpixel/s)</td>
<td>-</td>
</tr>
<tr>
<td>LVDS (1x single channel 165 MHz)</td>
<td>1</td>
</tr>
<tr>
<td>HDMI 1.4b (max 4096x2160)</td>
<td>1</td>
</tr>
<tr>
<td>VGA Analogue Video</td>
<td>-</td>
</tr>
<tr>
<td>eDP</td>
<td>1*</td>
</tr>
<tr>
<td>MIPI DSI</td>
<td>1x 4 Data Lanes* + 1x 2 Data Lanes*</td>
</tr>
<tr>
<td>Resistive Touch Screen</td>
<td>4 Wire</td>
</tr>
<tr>
<td>Analogue Audio Headphone out</td>
<td>1 (Stereo)</td>
</tr>
<tr>
<td>Analogue Audio Line in</td>
<td>1 (Stereo)</td>
</tr>
<tr>
<td>Analogue Audio Mic in</td>
<td>1 (Mono)</td>
</tr>
<tr>
<td>I²S</td>
<td>1</td>
</tr>
<tr>
<td>S/PDIF</td>
<td>1 in / 1 out</td>
</tr>
<tr>
<td>Parallel Camera Interface</td>
<td>-</td>
</tr>
<tr>
<td>MIPI CSI-2</td>
<td>2x 4 Data Lanes* + 1x 1 Data Lane*</td>
</tr>
<tr>
<td>I²C</td>
<td>3+3*</td>
</tr>
<tr>
<td>SPI</td>
<td>2+3*</td>
</tr>
<tr>
<td>UART</td>
<td>4+6*</td>
</tr>
<tr>
<td>SD/SDIO/MMC</td>
<td>2+1*</td>
</tr>
<tr>
<td>GPIO</td>
<td>87*</td>
</tr>
<tr>
<td>USB 3.0 OTG (host/device)</td>
<td>1</td>
</tr>
<tr>
<td>USB 3.0 host</td>
<td>1</td>
</tr>
<tr>
<td>USB 2.0 host</td>
<td>1</td>
</tr>
<tr>
<td>PCIe (Gen 2.0)</td>
<td>1+1* (max. 1x2 + 1x1)</td>
</tr>
<tr>
<td>Serial ATA II (3Gbit/s)</td>
<td>1</td>
</tr>
<tr>
<td>10/100/1000 MBit/s Ethernet</td>
<td>1</td>
</tr>
<tr>
<td>Ethernet Controller</td>
<td>Intel i210</td>
</tr>
<tr>
<td>PWM</td>
<td>4+12*</td>
</tr>
<tr>
<td>Analogue Inputs</td>
<td>4<em>17</em></td>
</tr>
<tr>
<td>CAN</td>
<td>2</td>
</tr>
</tbody>
</table>

*These interfaces are available on pins that are not defined as standard interfaces in the Apalis architecture. The pins are either located in the type-specific area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. Some interfaces are provided by the companion MCU. The software support for the MCU interfaces might be limited. For more information, please check the list of type-specific interfaces in section 1.4 and the description of the associated interface in section 5.*
1.3.5 Graphics Processing Unit

<table>
<thead>
<tr>
<th></th>
<th>Apalis TK1 2GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kepler Mobile GPU Units</td>
<td>1</td>
</tr>
<tr>
<td>CUDA cores</td>
<td>192</td>
</tr>
<tr>
<td>OpenGL® ES 3.1</td>
<td>✓</td>
</tr>
<tr>
<td>OpenGL 4.4</td>
<td>✓</td>
</tr>
<tr>
<td>DirectX 12</td>
<td>✓</td>
</tr>
<tr>
<td>PhysX</td>
<td>✓</td>
</tr>
</tbody>
</table>

1.3.6 HD Video Decode

- ✓ MPEG-2 – 1080p60
- ✓ MPEG4/XviD (Simple Profile) – 1080p30
- ✓ H.264 (Baseline, Main, High, Stereo SEI Profile) – 2160p30, 1440p60, 1080p120
- ✓ H.264 Multiple Stream – 4x 1080p30
- ✓ VC1 (Simple, Main, Advanced Profile) – 2160p30, 1080p120
- ✓ WEBM VP8 – 2160p30, 1080p120
- ✓ MJPEG – 120MPixel/s

1.3.7 HD Video Encode

- ✓ MPEG4 (Simple Profile)
- ✓ H.263 (Profile 0)
- ✓ H.264 (Baseline, Main, High, Stereo SEI Profile) – 2160p24, 1440p30, 1080p60)
- ✓ WEBM VP8 – 2160p24, 1440p30, 1080p60)
- ✓ MJPEG – 120MPixel/s
- ✓ VC1 (Advanced Profile) –720p30

1.3.8 Supported Operating Systems

- ✓ Embedded Linux
- ✓ Android available through Toradex partners

1.4 Interface Overview

The table in Figure 1 shows the interfaces that are supported on the Apalis® TK1 module, and whether an interface is provided on standard or type-specific pins. Additionally, the table shows also whether the interface is provided by the NVIDIA Tegra K1 SoC or by the NXP K20 MCU. The I²C interface is an example of an interface that makes use of standard and type-specific pins – three USB ports are provided as part of the standard interface pinout while additionally four ports are type-specific. Two out of these additional four ports are not provided by the SoC, they are provided by the companion MCU.

The CAN, analogue inputs as well as the resistive touch interface that are provided by the MCU will be supported in the Toradex Linux image. Other interfaces provided by the MCU might be not supported by the standard OS image.

Some interfaces are available as an alternate function of a pin. This function can only be used if the primary function of the pin is not used. Check section 4.5 for a list of all alternate functions of the MXM3 pins. The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Colibri iMX7 Module. The tool allows comparing the interfaces of different Colibri modules. More information to this tool can be found here: [http://developer.toradex.com/knowledge-base/pinout-designer](http://developer.toradex.com/knowledge-base/pinout-designer)
<table>
<thead>
<tr>
<th>Feature</th>
<th>Total</th>
<th>TK1 SoC</th>
<th>K20 MCU</th>
<th>Standard</th>
<th>Type Specific</th>
<th>Alternate Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 Wire Resistive Touch</td>
<td>4</td>
<td>4</td>
<td></td>
<td>4</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Analogue Inputs</td>
<td>21</td>
<td>21</td>
<td></td>
<td>4</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>Analogue Audio (Line in/out, Mic in)</td>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAN</td>
<td>2</td>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSI Ports</td>
<td>3</td>
<td>3</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSI Ports</td>
<td>2</td>
<td>2</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single Channel LVDS Display</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gigabit Ethernet</td>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO</td>
<td>87</td>
<td>36</td>
<td>51</td>
<td>8</td>
<td>4</td>
<td>74</td>
</tr>
<tr>
<td>GPI (Only Input possible)</td>
<td>15</td>
<td>15</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>GPO (Only Output possible)</td>
<td>24</td>
<td>24</td>
<td></td>
<td></td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>I²S</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HDMI (TDMS)</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>eDP</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I²C</td>
<td>6</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Parallel Camera</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel LCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCI-Express (lane count)</td>
<td>3</td>
<td>3</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PWM</td>
<td>16</td>
<td>4</td>
<td>12</td>
<td>4</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>SATA</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD/SDIO/MMC</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>S/PDIF In</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/PDIF Out</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPI</td>
<td>5</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td>10</td>
<td>4</td>
<td>6</td>
<td>4</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>USB 3.0 host/device</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>USB 3.0 host</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>USB 2.0 host</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>USB 1.1 host</td>
<td>1</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VGA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Figure 1: Apalis® TK1 Module Interfaces*

### 1.5 Reference Documents

#### 1.5.1 NVIDIA Tegra K1


#### 1.5.2 NXP (Freescale) K20

You will find the details about Kinetis K20 MCU in the Datasheet and Reference Manual provided by NXP.
1.5.3 Ethernet Controller

Apalis TK1 uses the Intel I210-AT Gigabit Ethernet Controller Chip.  

1.5.4 Audio Codec

Apalis TK1 uses the NXP SGTL5000 Audio Codec.  

1.5.5 Apalis Carrier Board Design Guide

This document provides additional information about the Apalis form factor. A custom carrier board should follow the Apalis Carrier Board Design Guide in order to make the board compatible within the Apalis module family. Please study this document in detail prior to starting your carrier board design.  

1.5.6 Layout Design Guide

This document contains information about high-speed layout design and additional information that helps to get the carrier board layout the first time right.  

1.5.7 Toradex Developer Centre

You can find a lot of additional information in the Toradex Developer Centre, which is updated with the latest product support information on a regular basis.  
Please note that the Developer Centre is common for all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Apalis TK1.  
http://www.developer.toradex.com

1.5.8 Apalis Evaluation Board Schematics

We provide the completed schematics plus the Altium project file which includes library symbols and IPC-7351 compliant footprints for the Apalis Evaluation Board free of charge. This is of a great help when designing your own Carrier Board.  
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.5.9 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparing the interfaces of different modules.  
2. Architecture Overview

2.1 Block Diagram

![Apalis TK1 Block Diagram]

Figure 2 Apalis TK1 Block Diagram
3. Apalis TK1 Connectors

3.1 Pin Numbering

The diagrams in Figure 3 and Figure 4 show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema. Pins on the top side of the module have even numbers and pins on the bottom side have odd numbers.

The pin number increases linearly as a multiple of the pitch – that is, pins which are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins which do not exist due to the connector notch are also accounted for (pins 166 through 172).

![Top Side](image)

Figure 3: Pin numbering schema on the top side of the module

![Bottom Side](image)

Figure 4: Pin numbering schema on the bottom side of the module

3.2 Assignment

The following table describes the MXM3 connector pin out. Some pins are shaded dark grey as type-specific interfaces. These pins might not be compatible with other modules in the Apalis family. Please be aware that you might lose compatibility with other Apalis modules on your carrier board if you make use of these interfaces. It should be noted that type-specific interfaces will be kept common across modules that share such interfaces wherever possible. For example, if both module A and module B have three additional PCI-Express lanes which are available in the same configurations as a type-specific interface, then they shall be assigned to the same pins in the type-
specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type-specific interface.

- **X1:** Pin number on the MXM3 module edge connector (X1).
- **Apalis Signal Name:** The name of the signal according to the Apalis form factor definition. This name corresponds to the default usage of the pin. Some of the pins also have alternate function, but in order to be compatible with other Apalis modules, only the default function should be used and the carrier board should be implemented according to the Apalis Carrier Board Design Guide.
- **TK1 Ball Name:** The name of the pin of the Tegra K1 SoC.

### Table 3-1 X1 Connector

<table>
<thead>
<tr>
<th>X1</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GPIO1</td>
<td>GPIO_PFF2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>GPIO2</td>
<td>DP_HP0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>GPIO3</td>
<td>USB_VBUS_EN0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>GPIO4</td>
<td>USB_VBUS_EN1</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>GPIO5</td>
<td>PEX_L1_RST_N</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>GPIO6</td>
<td>PEX_L1_CLKREQ_N / OWR</td>
<td>Two Soc Pins connected</td>
</tr>
<tr>
<td>15</td>
<td>GPIO7</td>
<td>PEX_L0_RST_N</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>GPIO8</td>
<td>PEX_L0_CLKREQ_N</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>SATA1_RX+</td>
<td>SATA_L0_RXP</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>SATA1_RX-</td>
<td>SATA_L0_RXN</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>SATA1_TX-</td>
<td>SATA_L0_TXN</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>SATA1_TX+</td>
<td>SATA_L0_TXP</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>SAT1ACT#</td>
<td>DAP1_DOUT</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>37</td>
<td>WAKE1_MICO</td>
<td>PEX_WAKE_N</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>PCIE1_RX-</td>
<td>PEX_RX4N</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>PCIE1_RX+</td>
<td>PEX_RX4P</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>PCIE1_TX-</td>
<td>PEX_TX4N</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>PCIE1_TX+</td>
<td>PEX_TX4P</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>PCIE1_CLK-</td>
<td>PEX_CLK1N</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>POWER_ENABLE_MOCI</td>
<td>PWR Management</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>RESET_MOCI#</td>
<td>PWR Management</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>RESET_MICO#</td>
<td>PWR Management</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>ETH1_MDI2+</td>
<td>I210 Pin 32</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>ETH1_MDI2-</td>
<td>I210 Pin 34</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>ETH1_MDI3+</td>
<td>I210 Pin 38</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>ETH1_MDI3-</td>
<td>I210 Pin 40</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>ETH1_ACT</td>
<td>I210 Pin 42</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>ETH1_LINK</td>
<td>I210 Pin 44</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>ETH1_CTRREF</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>ETH1_MDI0-</td>
<td>I210 Pin 57</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>ETH1_MDI0+</td>
<td>I210 Pin 58</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>ETH1_MDI1-</td>
<td>I210 Pin 54</td>
<td></td>
</tr>
<tr>
<td>X1</td>
<td>Apalis Signal Name</td>
<td>TK1 Ball Name</td>
<td>Notes</td>
</tr>
<tr>
<td>---</td>
<td>------------------</td>
<td>---------------</td>
<td>-------</td>
</tr>
<tr>
<td>55</td>
<td>PCIE1_CLK+</td>
<td>PEX_CLK1P</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>TS_DIFF1-</td>
<td>PEX_RX3N</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>TS_DIFF1+</td>
<td>PEX_RX3P</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>TS_1</td>
<td>Recovery Circuit</td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>TS_DIFF2-</td>
<td>PEX_TX3N</td>
<td></td>
</tr>
<tr>
<td>67</td>
<td>TS_DIFF2+</td>
<td>PEX_TX3P</td>
<td></td>
</tr>
<tr>
<td>69</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>71</td>
<td>TS_DIFF3-</td>
<td>DP_AUX_CH0_N</td>
<td></td>
</tr>
<tr>
<td>73</td>
<td>TS_DIFF3+</td>
<td>DP_AUX_CH0_P</td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>TS_DIFF4-</td>
<td>DSI_A_D1_N</td>
<td></td>
</tr>
<tr>
<td>79</td>
<td>TS_DIFF4+</td>
<td>DSI_A_D1_P</td>
<td></td>
</tr>
<tr>
<td>81</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>83</td>
<td>TS_DIFF5-</td>
<td>DSI_A_D0_N</td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>TS_DIFF5+</td>
<td>DSI_A_D0_P</td>
<td></td>
</tr>
<tr>
<td>87</td>
<td>TS_2</td>
<td>PMIC Power Button</td>
<td></td>
</tr>
<tr>
<td>89</td>
<td>TS_DIFF6-</td>
<td>DSI_A_CLK_N</td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>TS_DIFF6+</td>
<td>DSI_A_CLK_P</td>
<td></td>
</tr>
<tr>
<td>93</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>95</td>
<td>TS_DIFF7-</td>
<td>CSI_E_D0_N</td>
<td></td>
</tr>
<tr>
<td>97</td>
<td>TS_DIFF7+</td>
<td>CSI_E_D0_P</td>
<td></td>
</tr>
<tr>
<td>99</td>
<td>TS_3</td>
<td>I210 Pin 63 SDP0</td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>TS_DIFF8-</td>
<td>DSI_B_D3_N</td>
<td></td>
</tr>
<tr>
<td>103</td>
<td>TS_DIFF8+</td>
<td>DSI_B_D3_P</td>
<td></td>
</tr>
<tr>
<td>105</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>107</td>
<td>TS_DIFF9-</td>
<td>DSI_B_D2_N</td>
<td></td>
</tr>
<tr>
<td>109</td>
<td>TS_DIFF9+</td>
<td>DSI_B_D2_P</td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>113</td>
<td>TS_DIFF10-</td>
<td>DSI_B_D1_N</td>
<td></td>
</tr>
<tr>
<td>115</td>
<td>TS_DIFF10+</td>
<td>DSI_B_D1_P</td>
<td></td>
</tr>
<tr>
<td>117</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>119</td>
<td>TS_DIFF11-</td>
<td>DSI_B_D0_N</td>
<td></td>
</tr>
<tr>
<td>121</td>
<td>TS_DIFF11+</td>
<td>DSI_B_D0_P</td>
<td></td>
</tr>
<tr>
<td>123</td>
<td>TS_4</td>
<td>I210 Pin 61 SDP1</td>
<td></td>
</tr>
<tr>
<td>125</td>
<td>TS_DIFF12-</td>
<td>DSI_B_CLK_N</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>X1</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>56</td>
<td>ETH1_MD1+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>USB01_VBUS</td>
<td>USB0_VBUS</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>USB01_SSRX+</td>
<td>PEX_USB3_RX1P</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>USB01_SSRX-</td>
<td>PEX_USB3_RX1N</td>
<td></td>
</tr>
<tr>
<td>66</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>USB01_SSTX+</td>
<td>PEX_USB3_TX1P</td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>USB01_SSTX-</td>
<td>PEX_USB3_TX1N</td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>USB01_ID</td>
<td>USB0_ID</td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>USB01_D+</td>
<td>USB0_DP</td>
<td></td>
</tr>
<tr>
<td>76</td>
<td>USB01_D-</td>
<td>USB0_DN</td>
<td></td>
</tr>
<tr>
<td>78</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>USBH2_D+</td>
<td>USB1_DP</td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>USBH2_D-</td>
<td>USB1_DN</td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>USBH_EN</td>
<td>GEN2_I2C_SDA</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>86</td>
<td>USBH3_D+</td>
<td>K20 USB0_DP</td>
<td></td>
</tr>
<tr>
<td>88</td>
<td>USBH3_D-</td>
<td>K20 USB0_DM</td>
<td></td>
</tr>
<tr>
<td>90</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>92</td>
<td>USBH4_SSRX-</td>
<td>USB3_RX0N</td>
<td></td>
</tr>
<tr>
<td>94</td>
<td>USBH4_SSRX+</td>
<td>USB3_RX0P</td>
<td></td>
</tr>
<tr>
<td>96</td>
<td>USBH_OC#</td>
<td>GPIO_PBB0</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>98</td>
<td>USBH4_D+</td>
<td>USB2_DP</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>USBH4_D-</td>
<td>USB2_DN</td>
<td></td>
</tr>
<tr>
<td>102</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>104</td>
<td>USBH4_SSTX+</td>
<td>USB3_TX0N</td>
<td></td>
</tr>
<tr>
<td>106</td>
<td>USBH4_SSTX-</td>
<td>USB3_TX0P</td>
<td></td>
</tr>
<tr>
<td>108</td>
<td>VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>UART1_DTR</td>
<td>UART3_RTS_N</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>112</td>
<td>UART1_TXD</td>
<td>GPIO_PU0</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>114</td>
<td>UART1_RTS</td>
<td>GPIO_PU3</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>116</td>
<td>UART1_CTS</td>
<td>GPIO_PU2</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>118</td>
<td>UART1_RXD</td>
<td>GPIO_PU1</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>120</td>
<td>UART1_DSR</td>
<td>UART3_CTS_N</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>122</td>
<td>UART1_RI</td>
<td>GPIO_PK7</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>124</td>
<td>UART1_DCD</td>
<td>GPIO_PB1</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>126</td>
<td>UART2_TXD</td>
<td>UART2_TXD</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>X1</td>
<td>Apalis Signal Name</td>
<td>TK1 Ball Name</td>
<td>Notes</td>
</tr>
<tr>
<td>----</td>
<td>------------------</td>
<td>--------------</td>
<td>-------</td>
</tr>
<tr>
<td>127</td>
<td>TS_DIFF12+</td>
<td>DSI_B_CLK_P</td>
<td></td>
</tr>
<tr>
<td>129</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>131</td>
<td>TS_DIFF13-</td>
<td>CSI_E_CLK_N</td>
<td></td>
</tr>
<tr>
<td>133</td>
<td>TS_DIFF13+</td>
<td>CSI_E_CLK_P</td>
<td></td>
</tr>
<tr>
<td>135</td>
<td>TS_5</td>
<td>I2C10 Pin 62 SDP2</td>
<td></td>
</tr>
<tr>
<td>137</td>
<td>TS_DIFF14-</td>
<td>CSI_B_D1_N</td>
<td></td>
</tr>
<tr>
<td>139</td>
<td>TS_DIFF14+</td>
<td>CSI_B_D1_P</td>
<td></td>
</tr>
<tr>
<td>141</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>143</td>
<td>TS_DIFF15-</td>
<td>CSI_B_D0_N</td>
<td></td>
</tr>
<tr>
<td>145</td>
<td>TS_DIFF15+</td>
<td>CSI_B_D0_P</td>
<td></td>
</tr>
<tr>
<td>147</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>149</td>
<td>TS_DIFF16-</td>
<td>CSI_A_D1_N</td>
<td></td>
</tr>
<tr>
<td>151</td>
<td>TS_DIFF16+</td>
<td>CSI_A_D1_P</td>
<td></td>
</tr>
<tr>
<td>153</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>155</td>
<td>TS_DIFF17-</td>
<td>CSI_A_D0_N</td>
<td></td>
</tr>
<tr>
<td>157</td>
<td>TS_DIFF17+</td>
<td>CSI_A_D0_P</td>
<td></td>
</tr>
<tr>
<td>159</td>
<td>TS_6</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>161</td>
<td>TS_DIFF18-</td>
<td>CSI_A_CLK_N</td>
<td></td>
</tr>
<tr>
<td>163</td>
<td>TS_DIFF18+</td>
<td>CSI_A_CLK_P</td>
<td></td>
</tr>
<tr>
<td>165</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>X1</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>128</td>
<td>UART2_RTS</td>
<td>UART2_RTS_N</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>130</td>
<td>UART2_CTS</td>
<td>UART2_CTS_N</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>132</td>
<td>UART2_RXD</td>
<td>UART2_RXD</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>134</td>
<td>UART3_TXD</td>
<td>UART3_TXD</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>136</td>
<td>UART3_RXD</td>
<td>UART3_RXD</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>138</td>
<td>UART4_TXD</td>
<td>GPIO_PJ7</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>140</td>
<td>UART4_RXD</td>
<td>GPIO_PB0</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>142</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>144</td>
<td>MMC1_D2</td>
<td>SDMMC1_DAT2</td>
<td></td>
</tr>
<tr>
<td>146</td>
<td>MMC1_D3</td>
<td>SDMMC1_DAT3</td>
<td></td>
</tr>
<tr>
<td>148</td>
<td>MMC1_D4</td>
<td>CLK2_REQ</td>
<td></td>
</tr>
<tr>
<td>150</td>
<td>MMC1_CMD</td>
<td>SDMMC1_CMD</td>
<td></td>
</tr>
<tr>
<td>152</td>
<td>MMC1_D5</td>
<td>CLK2_OUT</td>
<td></td>
</tr>
<tr>
<td>154</td>
<td>MMC1_CLK</td>
<td>SDMMC1_CLK</td>
<td></td>
</tr>
<tr>
<td>156</td>
<td>MMC1_D6</td>
<td>SDMMC3_CLK_LB_I N</td>
<td></td>
</tr>
<tr>
<td>158</td>
<td>MMC1_D7</td>
<td>USB_VBUS_EN2</td>
<td></td>
</tr>
<tr>
<td>160</td>
<td>MMC1_D0</td>
<td>SDMMC1_DAT0</td>
<td></td>
</tr>
<tr>
<td>162</td>
<td>MMC1_D1</td>
<td>SDMMC1_DAT1</td>
<td></td>
</tr>
<tr>
<td>164</td>
<td>MMC1_CD#</td>
<td>SDMMC1_WP_N</td>
<td></td>
</tr>
<tr>
<td>173</td>
<td>CAM1_D7</td>
<td>K20 PTE1</td>
<td></td>
</tr>
<tr>
<td>175</td>
<td>CAM1_D6</td>
<td>K20 PTE0</td>
<td></td>
</tr>
<tr>
<td>177</td>
<td>CAM1_D5</td>
<td>K20 PTB17</td>
<td></td>
</tr>
<tr>
<td>179</td>
<td>CAM1_D4</td>
<td>K20 PTE3</td>
<td></td>
</tr>
<tr>
<td>181</td>
<td>CAM1_D3</td>
<td>K20 PTE5</td>
<td></td>
</tr>
<tr>
<td>183</td>
<td>CAM1_D2</td>
<td>K20 PTE24</td>
<td></td>
</tr>
<tr>
<td>185</td>
<td>CAM1_D1</td>
<td>K20 PTE4</td>
<td></td>
</tr>
<tr>
<td>187</td>
<td>CAM1_D0</td>
<td>K20 PTA17</td>
<td></td>
</tr>
<tr>
<td>189</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>191</td>
<td>CAM1_PCLK</td>
<td>K20 PTE25</td>
<td></td>
</tr>
<tr>
<td>193</td>
<td>CAM1_MCLK</td>
<td>CAM_MCLK</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>195</td>
<td>CAM1_VSYNC</td>
<td>K20 PTA5</td>
<td></td>
</tr>
<tr>
<td>197</td>
<td>CAM1_HSYNC</td>
<td>K20 PTA3</td>
<td></td>
</tr>
<tr>
<td>174</td>
<td>VCC_BACKUP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>176</td>
<td>SD1_D2</td>
<td>SDMMC3_DAT2</td>
<td></td>
</tr>
<tr>
<td>178</td>
<td>SD1_D3</td>
<td>SDMMC3_DAT3</td>
<td></td>
</tr>
<tr>
<td>180</td>
<td>SD1_CMD</td>
<td>SDMMC3_CMD</td>
<td></td>
</tr>
<tr>
<td>182</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>184</td>
<td>SD1_CLK</td>
<td>SDMMC3_CLK</td>
<td></td>
</tr>
<tr>
<td>186</td>
<td>SD1_D0</td>
<td>SDMMC3_DAT0</td>
<td></td>
</tr>
<tr>
<td>188</td>
<td>SD1_D1</td>
<td>SDMMC3_DAT1</td>
<td></td>
</tr>
<tr>
<td>190</td>
<td>SD1_CD#</td>
<td>SDMMC3_CD_N</td>
<td>Input Shifter (diode circuit)</td>
</tr>
<tr>
<td>192</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>194</td>
<td>DAP1_MCLK</td>
<td>CLK3_OUT</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>196</td>
<td>DAP1_D_OUT</td>
<td>DAP2_DOUT</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>198</td>
<td>DAP1_RESET#</td>
<td></td>
<td>Output Shifter</td>
</tr>
<tr>
<td>X1</td>
<td>Apalis Signal Name</td>
<td>TK1 Ball Name</td>
<td>Notes</td>
</tr>
<tr>
<td>----</td>
<td>-------------------</td>
<td>---------------</td>
<td>-------</td>
</tr>
<tr>
<td>199</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>201</td>
<td>I2C3_SDA (CAM)</td>
<td>CAM_I2C_SDA</td>
<td>1.8V signal, 3.3V tolerant</td>
</tr>
<tr>
<td>203</td>
<td>I2C3_SCL (CAM)</td>
<td>CAM_I2C_SCL</td>
<td>1.8V signal, 3.3V tolerant</td>
</tr>
<tr>
<td>205</td>
<td>I2C2_SDA (DDC)</td>
<td>DDC_SDA</td>
<td>OD and input only</td>
</tr>
<tr>
<td>207</td>
<td>I2C2_SCL (DDC)</td>
<td>DDC_SCL</td>
<td>OD and input only</td>
</tr>
<tr>
<td>209</td>
<td>I2C1_SDA</td>
<td>GEN1_I2C_SDA</td>
<td>1.8V signal, 3.3V tolerant</td>
</tr>
<tr>
<td>211</td>
<td>I2C1_SCL</td>
<td>GEN1_I2C_SCL</td>
<td>1.8V signal, 3.3V tolerant</td>
</tr>
<tr>
<td>213</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>215</td>
<td>SPDIF1_OUT</td>
<td>SPDIF_OUT</td>
<td></td>
</tr>
<tr>
<td>217</td>
<td>SPDIF1_IN</td>
<td>SPDIF_IN</td>
<td></td>
</tr>
<tr>
<td>219</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>221</td>
<td>SPI1_CLK</td>
<td>ULPI_NXT</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>223</td>
<td>SPI1_MISO</td>
<td>ULPI_DIR</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>225</td>
<td>SPI1_MOSI</td>
<td>ULPI_CLK</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>227</td>
<td>SPI1_CS</td>
<td>ULPI_STP</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>229</td>
<td>SPI2_MISO</td>
<td>GPIO_PG7</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>231</td>
<td>SPI2_MOSI</td>
<td>GPIO_PG6</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>233</td>
<td>SPI2_CS</td>
<td>GPIO_PI3</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>235</td>
<td>SPI2_CLK</td>
<td>GPIO_PG5</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>237</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>239</td>
<td>BKL1_PWM</td>
<td>GPIO_PU6</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>241</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>243</td>
<td>LCD1_PCLK</td>
<td>K20 PTD7</td>
<td></td>
</tr>
<tr>
<td>245</td>
<td>LCD1_VSYNC</td>
<td>K20 PTD5</td>
<td></td>
</tr>
<tr>
<td>247</td>
<td>LCD1_HSYNC</td>
<td>K20 PTD4</td>
<td></td>
</tr>
<tr>
<td>249</td>
<td>LCD1_DE</td>
<td>K20 PTC4</td>
<td></td>
</tr>
<tr>
<td>251</td>
<td>LCD1_R0</td>
<td>K20 PTD9</td>
<td></td>
</tr>
<tr>
<td>253</td>
<td>LCD1_R1</td>
<td>K20 PTD8</td>
<td></td>
</tr>
<tr>
<td>255</td>
<td>LCD1_R2</td>
<td>K20 PTD6</td>
<td></td>
</tr>
<tr>
<td>257</td>
<td>LCD1_R3</td>
<td>K20 PTD3</td>
<td></td>
</tr>
<tr>
<td>259</td>
<td>LCD1_R4</td>
<td>K20 PTC7</td>
<td></td>
</tr>
<tr>
<td>261</td>
<td>LCD1_R5</td>
<td>K20 PTC3</td>
<td></td>
</tr>
<tr>
<td>263</td>
<td>LCD1_R6</td>
<td>K20 PTC0</td>
<td></td>
</tr>
<tr>
<td>265</td>
<td>LCD1_R7</td>
<td>K20 PTB16</td>
<td></td>
</tr>
<tr>
<td>267</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>269</td>
<td>LCD1_G0</td>
<td>K20 PTD12</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>X1</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>DAP1_BIT_CLBK</td>
<td>DAP2_SCLK</td>
<td>Bidirectional Shifter</td>
</tr>
<tr>
<td>202</td>
<td>DAP1_D_IN</td>
<td>DAP2_DIN</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>204</td>
<td>DAP1_SYNC</td>
<td>DAP2_FS</td>
<td>Bidirectional Shifter</td>
</tr>
<tr>
<td>206</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>208</td>
<td>VGA1_R</td>
<td></td>
<td>NC</td>
</tr>
<tr>
<td>210</td>
<td>VGA1_G</td>
<td></td>
<td>NC</td>
</tr>
<tr>
<td>212</td>
<td>VGA1_B</td>
<td></td>
<td>NC</td>
</tr>
<tr>
<td>214</td>
<td>VGA1_HSYNC</td>
<td></td>
<td>NC</td>
</tr>
<tr>
<td>216</td>
<td>VGA1_VSYNC</td>
<td></td>
<td>NC</td>
</tr>
<tr>
<td>218</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>220</td>
<td>HDMI1_CEC</td>
<td>HDMI_CEC</td>
<td></td>
</tr>
<tr>
<td>222</td>
<td>HDMI1_TXD2+</td>
<td>HDMI_TXD2P</td>
<td></td>
</tr>
<tr>
<td>224</td>
<td>HDMI1_TXD2-</td>
<td>HDMI_TXD2N</td>
<td></td>
</tr>
<tr>
<td>226</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>228</td>
<td>HDMI1_TXD1+</td>
<td>HDMI_TXD1P</td>
<td></td>
</tr>
<tr>
<td>230</td>
<td>HDMI1_TXD1-</td>
<td>HDMI_TXD1N</td>
<td></td>
</tr>
<tr>
<td>232</td>
<td>HDMI1_HP</td>
<td>HDMI_INT</td>
<td>Level shifted</td>
</tr>
<tr>
<td>234</td>
<td>HDMI1_TXD0+</td>
<td>HDMI_TXD0P</td>
<td></td>
</tr>
<tr>
<td>236</td>
<td>HDMI1_TXD0-</td>
<td>HDMI_TXD0N</td>
<td></td>
</tr>
<tr>
<td>238</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>HDMI1_TXC+</td>
<td>HDMI_TXCP</td>
<td></td>
</tr>
<tr>
<td>242</td>
<td>HDMI1_TXC-</td>
<td>HDMI_TXCN</td>
<td></td>
</tr>
<tr>
<td>244</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>246</td>
<td>LVDS1_A_CLK-</td>
<td>LVDS0_TXD4N</td>
<td></td>
</tr>
<tr>
<td>248</td>
<td>LVDS1_A_CLK+</td>
<td>LVDS0_TXD4P</td>
<td></td>
</tr>
<tr>
<td>250</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>252</td>
<td>LVDS1_A_TX0-</td>
<td>LVDS0_TXD0N</td>
<td></td>
</tr>
<tr>
<td>254</td>
<td>LVDS1_A_TX0+</td>
<td>LVDS0_TXD0P</td>
<td></td>
</tr>
<tr>
<td>256</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>258</td>
<td>LVDS1_A_TX1-</td>
<td>LVDS0_TXD1N</td>
<td></td>
</tr>
<tr>
<td>260</td>
<td>LVDS1_A_TX1+</td>
<td>LVDS0_TXD1P</td>
<td></td>
</tr>
<tr>
<td>262</td>
<td>USBO1_OC#</td>
<td>GPIO_PBB4</td>
<td>Input Shifter</td>
</tr>
<tr>
<td>264</td>
<td>LVDS1_A_TX2-</td>
<td>LVDS0_TXD2N</td>
<td></td>
</tr>
<tr>
<td>266</td>
<td>LVDS1_A_TX2+</td>
<td>LVDS0_TXD2P</td>
<td></td>
</tr>
<tr>
<td>268</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>270</td>
<td>LVDS1_A_TX3-</td>
<td>LVDS0_TXD3N</td>
<td></td>
</tr>
<tr>
<td>X1</td>
<td>Apalis Signal Name</td>
<td>TK1 Ball Name</td>
<td>Notes</td>
</tr>
<tr>
<td>----</td>
<td>--------------------</td>
<td>---------------</td>
<td>-------</td>
</tr>
<tr>
<td>271</td>
<td>LCD1_G1</td>
<td>K20 PTD11</td>
<td></td>
</tr>
<tr>
<td>273</td>
<td>LCD1_G2</td>
<td>K20 PTD2</td>
<td></td>
</tr>
<tr>
<td>275</td>
<td>LCD1_G3</td>
<td>K20 PTC6</td>
<td></td>
</tr>
<tr>
<td>277</td>
<td>LCD1_G4</td>
<td>K20 PTC2</td>
<td></td>
</tr>
<tr>
<td>279</td>
<td>LCD1_G5</td>
<td>K20 PTB19</td>
<td></td>
</tr>
<tr>
<td>281</td>
<td>LCD1_G6</td>
<td>K20 PTB11</td>
<td></td>
</tr>
<tr>
<td>283</td>
<td>LCD1_G7</td>
<td>K20 PTD14</td>
<td></td>
</tr>
<tr>
<td>285</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>287</td>
<td>LCD1_B0</td>
<td>K20 PTD13</td>
<td></td>
</tr>
<tr>
<td>289</td>
<td>LCD1_B1</td>
<td>K20 PTD1</td>
<td></td>
</tr>
<tr>
<td>291</td>
<td>LCD1_B2</td>
<td>K20 PT00</td>
<td></td>
</tr>
<tr>
<td>293</td>
<td>LCD1_B3</td>
<td>K20 PTC1</td>
<td></td>
</tr>
<tr>
<td>295</td>
<td>LCD1_B4</td>
<td>K20 PTB18</td>
<td></td>
</tr>
<tr>
<td>297</td>
<td>LCD1_B5</td>
<td>K20 PTB10</td>
<td></td>
</tr>
<tr>
<td>299</td>
<td>LCD1_B6</td>
<td>K20 PTD15</td>
<td></td>
</tr>
<tr>
<td>301</td>
<td>LCD1_B7</td>
<td>K20 PTE2</td>
<td></td>
</tr>
<tr>
<td>303</td>
<td>AGND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>305</td>
<td>AN1_ADC0</td>
<td>K20 PTB0</td>
<td></td>
</tr>
<tr>
<td>307</td>
<td>AN1_ADC1</td>
<td>K20 PTB1</td>
<td></td>
</tr>
<tr>
<td>309</td>
<td>AN1_ADC2</td>
<td>K20 PTB2</td>
<td></td>
</tr>
<tr>
<td>311</td>
<td>AN1_TSWP_A</td>
<td>K20 PTB3</td>
<td></td>
</tr>
<tr>
<td>313</td>
<td>AGND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>315</td>
<td>AN1_TSPX</td>
<td>Touch Circuit</td>
<td></td>
</tr>
<tr>
<td>317</td>
<td>AN1_TSMX</td>
<td>Touch Circuit</td>
<td></td>
</tr>
<tr>
<td>319</td>
<td>AN1_TSPY</td>
<td>Touch Circuit</td>
<td></td>
</tr>
<tr>
<td>321</td>
<td>AN1_TSMY</td>
<td>Touch Circuit</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>X1</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>272</td>
<td>LVDS1_A_TX3+</td>
<td>LVDS0_TXD3P</td>
<td></td>
</tr>
<tr>
<td>274</td>
<td>USBO1_EN</td>
<td>GEN2_I2C_SCL</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>276</td>
<td>LVDS1_B_CLK-</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>278</td>
<td>LVDS1_B_CLK+</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>280</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>282</td>
<td>LVDS1_B_TX0-</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>284</td>
<td>LVDS1_B_TX0+</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>286</td>
<td>BKL1_ON</td>
<td>GPIO_PBB5</td>
<td>Output Shifter</td>
</tr>
<tr>
<td>288</td>
<td>LVDS1_B_TX1-</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>290</td>
<td>LVDS1_B_TX1+</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>292</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>294</td>
<td>LVDS1_B_TX2-</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>296</td>
<td>LVDS1_B_TX2+</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>298</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>LVDS1_B_TX3-</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>302</td>
<td>LVDS1_B_TX3+</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>304</td>
<td>AGND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>306</td>
<td>AAP1_MICIN</td>
<td>SGTL5000</td>
<td>Pin 10</td>
</tr>
<tr>
<td>308</td>
<td>AGND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>310</td>
<td>AAP1_LIN_L</td>
<td>SGTL5000</td>
<td>Pin 9</td>
</tr>
<tr>
<td>312</td>
<td>AAP1_LIN_R</td>
<td>SGTL5000</td>
<td>Pin 8</td>
</tr>
<tr>
<td>314</td>
<td>AVCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>316</td>
<td>AAP1_HP_L</td>
<td>SGTL5000</td>
<td>Pin 4</td>
</tr>
<tr>
<td>318</td>
<td>AAP1_HP_R</td>
<td>SGTL5000</td>
<td>Pin 1</td>
</tr>
<tr>
<td>320</td>
<td>AVCC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4. Tegra K1 I/O Pins

4.1 I/O Pin Types

In order to understand the capabilities of the Tegra K1 I/O Pins, we need to distinguish between different types of Pins. The I/O pins are grouped into power rail blocks. Pins in the same block have the same I/O voltage. Since the I/O voltage of some of the blocks is limited to 1.8V, there are level shifters located on the module in order to get the 3.3V I/O voltage level of the Apalis standard. Since the level shifter changes the behaviour and usage of the pins, this document needs to distinguish the I/O pin types according of the type of level shifter.

The Tegra K1 SoC itself distinguishes different MPIO Pad Types. The different types are:

- **ST**: Standard. Most common pads on the SoC.
- **DD**: Dual Drive. These pins are similar to the standard pin, but allow a 3.3V tolerant true open-drain mode.
- **CZ**: Controlled Output Impedance. These are mainly the SDMMC interface pins.
- **LV**: Low Voltage. These pins are optimized for low power supply. The maximum I/O voltage is 1.8V. Therefore, all these pins need to be level shifted on the Apalis module.
- **OD**: Open Drain: These pins do not have a push-pull output driver.

This differentiation of MPIO Pad Type is only applicable if there is no level shifter present on the module (3.3V, 1.8/3.3V, and 3.3V Tolerant signal types).

4.1.1 3.3V Signals

These are regular I/O pins that are connected directly from the Tegra K1 SoC to the module edge connector. The different function of the pin can be used without any restriction. The corresponding I/O block supply voltage is 3.3V. The pin can usually be used as input as well as output. Since there are no level shifters in between these signals, the Tegra K1 pin control options (for example enabling internal pull up/down resistors, drive strength, slew rate etc.) are applicable. More information on the available options can be found in section 4.2 as well as in the NVIDIA reference manual.

![3.3V I/O Block Diagram](image1)

4.1.2 1.8V/3.3V Signals

There are two I/O blocks which are sourced by an I/O voltage that can be changed between 1.8V and 3.3V. The I/O voltage of one block can be changed independently from the other block, but all signals of the corresponding block change their voltage together. One block contains the signals for the Apalis SD1 interface (TK1 function block SDMMC3) while the other block contains mainly the signals of the Apalis MMC1 interface (TK1 function block SDMMC1).

Beside the fact that the I/O voltage of these signals can be changed from 3.3V to 1.8V, the signals are similar to the type of the regular 3.3V signals. This means, the signals are also connected directly from the SoC to the module edge pin and all pin control options are applicable.

![1.8V/3.3V I/O Block Diagram](image2)
4.1.3 3.3V Tolerant Signals

There are a couple of signals (Apalis I2C1 and I2C3 interface signals) with 1.8V I/O voltage level but they are 3.3V tolerant. This means, if they are used as output signals, the high level is only 1.8V. The signals can be configured as open drain. It is possible to add a pull-up resistor to 3.3V on the carrier board in order to get a 3.3V logic level. If the pins are configured to be used as input, the input voltage level is allowed to be up to 3.3V.

The signals itself are connected directly from the Tegra K1 SoC to the module edge connector. This means, all pin control options are applicable.

4.1.4 Output Shifted Signals

The I/O voltage of the corresponding block on the Tegra K1 is 1.8V. Since the pins on the module edge connector need to be 3.3V (tolerant) according to the Apalis specifications, there are output level shifters on the module. The direction of the level shifter cannot be changed and the output cannot be disabled. This means, these pins can only be used as output. The carrier board is not allowed to drive these pins. It is not possible to use these pins as real GPIO. The pins can only be used as GPO (general purpose output) signals. Due to the restriction of the signal direction, some alternate function of these pins might be not usable.

Due to the level shifter, the Tegra K1 pin control option registers are available but not applicable; for example, changing the drive strength does not have any effect on the actual drive strength of the signal at the module edge connector.

4.1.5 Input Shifted Signals

The I/O voltage of the corresponding block on the Tegra K1 is 1.8V. Since the pins on the module edge connector need to be 3.3V (tolerant) according to the Apalis specifications, there are input level shifters on the module. The direction of the level shifter cannot be changed and the level shifter cannot be disabled. This means, these pins can only be used as input. It is not possible to use these pins as real GPIO. The pins can only be used as GPI (general purpose input) signals. Due to the restriction of the signal direction, some alternate functions of these pins might be unusable.

Due to the level shifter, the Tegra K1 pin control option registers are available but not applicable; for example, changing the enabling of the internal pull up/down resistors does not have any effect on the actual input at the module edge connector. Since there are no pull up/down options available at the module edge connector, it is recommended tying the signal to ground or VCC on the carrier board if unused.
4.1.6 Bidirectional Shifted Signals

There are two signals which feature a bidirectional level shifter. The signals are Pin 200 DAP1_BIT_CLK (TK1 signal DAP2_SCLK) and Pin 204 DAP1_SYNC (TK1 signal DAP2_FS). The direction of the level shifter can be changed from input to output. Important, the direction cannot be changed individually. It can only be changed for both signals together.

Due to the level shifter, the Tegra K1 pin control option registers are available but not applicable; for example, changing the enabling of the internal pull up/down resistors does not have any effect on the actual input at the module edge connector.

4.2 TK1 Pin Control

As previously described, the Tegra K1 pin control settings are only applicable on pins that do not feature a level shifter on the module (3.3V, 1.8/3.3V, and 3.3V Tolerant signal types). The actual available pin control settings depend on the MPIO Pad Type. The following table describes the differences between the types:

<table>
<thead>
<tr>
<th>Abbr.</th>
<th>MPIO Pad type</th>
<th>Input buffer</th>
<th>Output buffer</th>
<th>Nominal pull strength</th>
<th>Slew rate control</th>
<th>Drive strength control</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST</td>
<td>Standard</td>
<td>Schmitt / CMOS</td>
<td>Push- Pull</td>
<td>100kΩ</td>
<td>2-bits, up &amp; down</td>
<td>5-bits, up &amp; down</td>
</tr>
<tr>
<td>DD</td>
<td>Dual driver</td>
<td>Schmitt / CMOS</td>
<td>Push-Pull / Open-Drain</td>
<td>50kΩ</td>
<td>2-bits, up &amp; down</td>
<td>5-bits, up &amp; down</td>
</tr>
<tr>
<td>CZ</td>
<td>Controlled output impedance</td>
<td>Schmitt / CMOS</td>
<td>Push- Pull</td>
<td>15kΩ</td>
<td>2-bits, up &amp; down</td>
<td>7-bits, up &amp; down</td>
</tr>
<tr>
<td>OD</td>
<td>Open drain</td>
<td>Schmitt / CMOS</td>
<td>Open-Drain</td>
<td>100kΩ down only</td>
<td>2-bits, down only</td>
<td>5-bits, up only</td>
</tr>
<tr>
<td>LV</td>
<td>Low voltage</td>
<td>CMOS (level Shifter)</td>
<td>Push- Pull</td>
<td>5kΩ</td>
<td>4-bits, up &amp; down</td>
<td>5-bits, up &amp; down</td>
</tr>
</tbody>
</table>

For each GPIO pin, the following controls can be changed individually if the function is available for this pad type:

- Output Enable Control: Normal I/O or tristate
- Input Receiver: Enable/Disable input receiver
- Pull-up/down Control: Normal, pull-up or pull-down
- Open Drain option: Option only available on DD and OD pins
- Alternative Function Selection: Up to 4 special functions are available per pin.

If the following functions are available for this pad type, they can only be set for a whole pad group (power rail block):

- High Speed Mode (Enable/Disable)
- Schmitt Trigger (Enable/Disable)
- Low Power Mode (LPMD)
- Drive strength control down / up
- Slew rate control falling / rising
4.3 TK1 Function Multiplexing

The NVIDIA Tegra K1 SoC (low-speed) I/O pins can be configured for any of the (and up to) four alternate functions. Theoretically, most of the pins can also be used as GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). Due to the presence of level shifter at some of the I/O pins, the direction of the interface is fixed. Therefore, it is not possible to use those pins are real GPIO. They can only be used as General Purpose Output (GPO) or General Purpose Input (GPI). See the different types of I/O pins in the previous sections.

As an example: the Tegra K1 signal pin on the MXM3 finger pin 118 has the primary function UA3_RXD (Apalis standard function UART1_RXD). The TK1 would allow using the pin also as GPIO3_PU.01. Since the pin features an input level shifter, the GPIO functionality is limited to be used as input, this means it is actually possible to only use it as UART1_RX and GPI.

The default setting for this pin is the primary function UA3_RXD. It is strongly recommended to, whenever possible, use a pin for a function which is compatible with all Apalis modules. This guarantees the best compatibility with the standard software and with the other modules in the Apalis family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behaviour.

In the table listed in chapter 4.5, you will find a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

4.4 Pin Reset Status

After a reset the Tegra K1 pins can be in different modes. Most of them are tri-stated, pulled up or pulled low. A few are driven low or high. Please check the table in chapter 4.5 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

For pins with level shifter, the reset status of the Tegra K1 is only relevant for the output level of the level shifter. The output of the level shifter itself is always driving.

4.5 TK1 Functions List

Below is a list of all the Tegra K1 pins which are available on the MXM3 connector. It shows the alternate functions that are available for each pin. The table contains the information of the I/O Pin Types as well as the MPIO Pad Types. The alternate functions used to provide the primary interfaces to ensure best compatibility with other Apalis modules are highlighted. Some of the alternate functions might be unusable due to the unidirectional level shifter.

Additional caution is required when using pin 13 (GPIO6). This module edge connector pin is connected to two different Tegra K1 signals, the ball named PEX_L1_CLKREQ_N as well as OWR. Set the unused ball to input (High-Z) when using the other. Make sure that both balls are not driving simultaneously.

Reset Status Description

\[
\begin{array}{ll}
z & \text{Tristate} \\
pd & \text{Pull-Down} \\
pu & \text{Pull-Up} \\
0 & \text{Drive Low} \\
1 & \text{Drive High} \\
\end{array}
\]
**Function Short Forms**

- **CSI:** Camera Serial Interface
- **DSI:** Display Serial Interface
- **DTV:** Digital TV input
- **eDP:** embedded Display Port
- **HDMI:** High Definition Multimedia Interface
- **I2C:** Inter Integrated Circuit
- **I2S:** Inter IC Sound
- **LVDS:** Low Voltage Differential Signalling (also known as FPD-Link or FlatLink)
- **OWR:** One Wire Interface
- **PEX:** PCI Express
- **PWM:** Pulse Width Modulation
- **SATA:** Serial Advanced Technology Attachment
- **SDMMC:** Secure Card I/O (SD, MMC, CE-ATA, eMMC)
- **SPDIF:** S/PDIF (Sony-Philips Digital Interface I/O)
- **SPI:** Serial Peripheral Interface Bus
- **UART:** Serial Ports (Universal Asynchronous Receiver/Transmitter)
- **USB:** Universal Serial Bus
- **VGP:** Video General Purpose I/O
<table>
<thead>
<tr>
<th>X1 Pin</th>
<th>Tk1 Ball Name</th>
<th>GPIO</th>
<th>SFI0</th>
<th>SFI1</th>
<th>SFI2</th>
<th>SFI3</th>
<th>Wake/Strap</th>
<th>I/O Type</th>
<th>MPIO Type</th>
<th>Reset State</th>
<th>Pull</th>
<th>Power Block</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GPIO_PFF2</td>
<td>GPIO3_PFF.02</td>
<td>SATA_DA</td>
<td></td>
<td></td>
<td></td>
<td>wake59</td>
<td>3.3V</td>
<td>DD</td>
<td>z</td>
<td>50k</td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>3</td>
<td>DP_HPD</td>
<td>GPIO3_PFF.00</td>
<td>DP_HPD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3V</td>
<td>DD</td>
<td>z</td>
<td>100k</td>
<td>vddio_hv</td>
</tr>
<tr>
<td>5</td>
<td>USB_VBUS_EN0</td>
<td>GPIO3_PN.04</td>
<td>usb_vbus_en0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3V</td>
<td>DD</td>
<td>0</td>
<td>100k</td>
<td>vddio_hv</td>
</tr>
<tr>
<td>7</td>
<td>USB_VBUS_EN1</td>
<td>GPIO3_PN.05</td>
<td>usb_vbus_en1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3V</td>
<td>DD</td>
<td>0</td>
<td>100k</td>
<td>vddio_hv</td>
</tr>
<tr>
<td>11</td>
<td>PEX_L1_RST_N</td>
<td>GPIO3_PDD.05</td>
<td>pe1_rst_l</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3V</td>
<td>ST</td>
<td>z</td>
<td>100k</td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>13</td>
<td>OWR</td>
<td>OWR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3V</td>
<td>OD</td>
<td>z</td>
<td>100k</td>
<td>vddio_hv</td>
</tr>
<tr>
<td>15</td>
<td>PEX_L0_RST_N</td>
<td>GPIO3_PDD.01</td>
<td>pe0_rst_l</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3V</td>
<td>ST</td>
<td>z</td>
<td>100k</td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>17</td>
<td>PEX_L0_CLKREQ_N</td>
<td>GPIO3_PDD.02</td>
<td>pe0_clkreq_l</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3V</td>
<td>ST</td>
<td>z</td>
<td>100k</td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>25</td>
<td>SATA_L0_RXP</td>
<td>SATA_L0_RXP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SATA_LED_ACTIVE</td>
<td>3.3V</td>
<td>ST</td>
<td>pd</td>
<td>100k</td>
<td>vddio_audio</td>
</tr>
<tr>
<td>27</td>
<td>SATA_L0_RXN</td>
<td>SATA_L0_RXN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_sata</td>
</tr>
<tr>
<td>31</td>
<td>SATA_L0_TXN</td>
<td>SATA_L0_TXN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_sata</td>
</tr>
<tr>
<td>33</td>
<td>SATA_L0_TXP</td>
<td>SATA_L0_TXP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_sata</td>
</tr>
<tr>
<td>35</td>
<td>DAP1_DOUT</td>
<td>GPIO3_PN.02</td>
<td>I2S0_SDATA_OUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>37</td>
<td>PEX_WAKE_N</td>
<td>GPIO3_PDD.03</td>
<td>pe_wake_l</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>41</td>
<td>PEX_RX4N</td>
<td>PEX_RX4N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>43</td>
<td>PEX_RX4P</td>
<td>PEX_RX4P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>47</td>
<td>PEX_TX4N</td>
<td>PEX_TX4N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>49</td>
<td>PEX_TX4P</td>
<td>PEX_TX4P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>53</td>
<td>PEX_CLK1N</td>
<td>PEX_CLK1N</td>
<td>PEX_CLK_OUT_1_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>55</td>
<td>PEX_CLK1P</td>
<td>PEX_CLK1P</td>
<td>PEX_CLK_OUT_1_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex_ctl</td>
</tr>
<tr>
<td>59</td>
<td>PEX_RX3N</td>
<td>PEX_RX3N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>61</td>
<td>PEX_RX3P</td>
<td>PEX_RX3P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>65</td>
<td>PEX_TX3N</td>
<td>PEX_TX3N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>67</td>
<td>PEX_TX3P</td>
<td>PEX_TX3P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_pex</td>
</tr>
<tr>
<td>71</td>
<td>DP_AUX_CH0_N</td>
<td>I2C6_DAT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_hv</td>
</tr>
<tr>
<td>73</td>
<td>DP_AUX_CH0_P</td>
<td>I2C6_CLK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddio_hv</td>
</tr>
<tr>
<td>77</td>
<td>DSI_A_D1_N</td>
<td>DSI_A_D1_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>79</td>
<td>DSI_A_D1_P</td>
<td>DSI_A_D1_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>83</td>
<td>DSI_A_D0_N</td>
<td>DSI_A_D0_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>85</td>
<td>DSI_A_D0_P</td>
<td>DSI_A_D0_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>89</td>
<td>DSI_A_CLK_N</td>
<td>DSI_A_CLK_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>91</td>
<td>DSI_A_CLK_P</td>
<td>DSI_A_CLK_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>95</td>
<td>CSI_E_D0_N</td>
<td>CSI_E_D0_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>97</td>
<td>CSI_E_D0_P</td>
<td>CSI_E_D0_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>101</td>
<td>DSI_B_D2_N</td>
<td>DSI_B_D2_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>103</td>
<td>DSI_B_D3_P</td>
<td>DSI_B_D3_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>107</td>
<td>DSI_B_D2_N</td>
<td>DSI_B_D2_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>109</td>
<td>DSI_B_D2_P</td>
<td>DSI_B_D2_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>113</td>
<td>DSI_B_D1_N</td>
<td>DSI_B_D1_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>115</td>
<td>DSI_B_D1_P</td>
<td>DSI_B_D1_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>119</td>
<td>DSI_B_D0_N</td>
<td>DSI_B_D0_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>121</td>
<td>DSI_B_D0_P</td>
<td>DSI_B_D0_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>125</td>
<td>DSI_B_CLK_N</td>
<td>DSI_B_CLK_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>127</td>
<td>DSI_B_CLK_P</td>
<td>DSI_B_CLK_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>131</td>
<td>CSI_E_CLK_N</td>
<td>CSI_E_CLK_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>133</td>
<td>CSI_E_CLK_P</td>
<td>CSI_E_CLK_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>137</td>
<td>CSI_B_D1_N</td>
<td>CSI_B_D1_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
</tr>
<tr>
<td>X1 Pin</td>
<td>TK1 Ball Name</td>
<td>GPIO</td>
<td>SFI00</td>
<td>SFI01</td>
<td>SFI02</td>
<td>SFI03</td>
<td>Wake/Strap</td>
<td>I/O Type</td>
<td>MPIO Type</td>
<td>Reset State</td>
<td>Pull</td>
<td>Power Block</td>
</tr>
<tr>
<td>-------</td>
<td>---------------</td>
<td>------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>------------</td>
<td>----------</td>
<td>-----------</td>
<td>-------------</td>
<td>------</td>
<td>-------------</td>
</tr>
<tr>
<td>139</td>
<td>CSI_B_D1_P</td>
<td>CSI_B_D1_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>143</td>
<td>CSI_B_D0_N</td>
<td>CSI_B_D0_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>145</td>
<td>CSI_B_D0_P</td>
<td>CSI_B_D0_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>149</td>
<td>CSI_A_D1_N</td>
<td>CSI_A_D1_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>151</td>
<td>CSI_A_D1_P</td>
<td>CSI_A_D1_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>155</td>
<td>CSI_A_D0_N</td>
<td>CSI_A_D0_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>157</td>
<td>CSI_A_D0_P</td>
<td>CSI_A_D0_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>161</td>
<td>CSI_A_CLK_N</td>
<td>CSI_A_CLK_N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>163</td>
<td>CSI_A_CLK_P</td>
<td>CSI_A_CLK_P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_csi_dsi</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>193</td>
<td>CAM_MCLK</td>
<td>GPIO3_PCC.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>201</td>
<td>CAM_IOC_SDA</td>
<td>GPIO3_PBB.02</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>203</td>
<td>CAM_IOC_SCL</td>
<td>GPIO3_PBB.01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>206</td>
<td>DDC_SCL</td>
<td>GPIO3_PV.05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>211</td>
<td>GEN1_IOC_SCL</td>
<td>GPIO3_PC.04</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>215</td>
<td>SPDIF_OUT</td>
<td>GPIO3_PK.05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>217</td>
<td>SPDIF_IN</td>
<td>GPIO3_PK.06</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>221</td>
<td>ULPI_NXT</td>
<td>GPIO3_PY.02</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>223</td>
<td>ULPI_DIR</td>
<td>GPIO3_PY.01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>225</td>
<td>ULPI_CLK</td>
<td>GPIO3_PY.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>227</td>
<td>ULPI_STP</td>
<td>GPIO3_PY.03</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>229</td>
<td>GPIO3_PG7</td>
<td>GPIO3_PG.07</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>231</td>
<td>GPIO3_PG6</td>
<td>GPIO3_PG.06</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>233</td>
<td>GPIO3_PG1</td>
<td>GPIO3_PG.03</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>235</td>
<td>GPIO3_PG5</td>
<td>GPIO3_PG.05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>239</td>
<td>GPIO3_PU6</td>
<td>GPIO3_PU.06</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GPIO3_P0</td>
<td>GPIO3_P0.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>GPIO3_P1</td>
<td>GPIO3_P1.01</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>GPIO3_P2</td>
<td>GPIO3_P2.02</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>GPIO3_P3</td>
<td>GPIO3_P3.03</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>USBO_VBUS</td>
<td>USBO_VBUS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>PEX_USB3_RX1P</td>
<td>PEX_USB3_RX1P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_pex</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>PEX_USB3_RX1N</td>
<td>PEX_USB3_RX1N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_pex</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>PEX_USB3_TX1P</td>
<td>PEX_USB3_TX1P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_pex</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>PEX_USB3_TX1N</td>
<td>PEX_USB3_TX1N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_pex</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>USB0_ID</td>
<td>USB0_ID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>USB0_DP</td>
<td>USB0_DP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>76</td>
<td>USB0_DN</td>
<td>USB0_DN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>USB1_DP</td>
<td>USB1_DP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>USB1_DN</td>
<td>USB1_DN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>GEN2_IOC_SDA</td>
<td>GPIO3_PV.06</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>92</td>
<td>USB3_RX0N</td>
<td>USB3_RX0N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>94</td>
<td>USB3_RX0P</td>
<td>USB3_RX0P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>96</td>
<td>GPIO3_PBB0</td>
<td>GPIO3_PBB.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Shift ST</td>
<td>pu</td>
<td>100k</td>
<td>vddio_cam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>98</td>
<td>USB2_DP</td>
<td>USB2_DP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>USB2_DN</td>
<td>USB2_DN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>104</td>
<td>USB3_TX0N</td>
<td>USB3_TX0N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_usb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X1 Pin</td>
<td>TK1 Ball Name</td>
<td>GPIO</td>
<td>SFI00</td>
<td>SFI01</td>
<td>SFI02</td>
<td>SFI03</td>
<td>Wake/ Strap</td>
<td>I/O Type</td>
<td>MPIO Type</td>
<td>Reset State</td>
<td>Pull</td>
<td>Power Block</td>
</tr>
<tr>
<td>-----</td>
<td>---------------</td>
<td>------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------------</td>
<td>----------</td>
<td>-----------</td>
<td>-------------</td>
<td>------</td>
<td>-------------</td>
</tr>
<tr>
<td>106</td>
<td>USB3_TX0P</td>
<td>USB3_TX0P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>UART3_RTS_N</td>
<td>GPIO3_PC.00</td>
<td>UC3_RTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>112</td>
<td>GPIO0_PU0</td>
<td>GPIO0_PU.00</td>
<td>UA3_TXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>114</td>
<td>GPIO0_PU3</td>
<td>GPIO0_PU.03</td>
<td>UA3_RTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>116</td>
<td>GPIO0_PU0</td>
<td>GPIO0_PU.02</td>
<td>UC3_RTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>118</td>
<td>GPIO0_PU1</td>
<td>GPIO0_PU.01</td>
<td>UA3_RXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>120</td>
<td>UART3_CTS_N</td>
<td>GPIO3_PA.01</td>
<td>UC3_CTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>122</td>
<td>GPIO0_PK7</td>
<td>GPIO0_PK.07</td>
<td>UD3_RTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>124</td>
<td>GPIO0_PB1</td>
<td>GPIO0_PB.01</td>
<td>UD3_CTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>126</td>
<td>UART2_TXD</td>
<td>GPIO3_PC.02</td>
<td>IR3_TXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>128</td>
<td>UART2_RTS_N</td>
<td>GPIO3_PJ.06</td>
<td>UB3_RTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>130</td>
<td>UART2_CTS_N</td>
<td>GPIO3_PJ.05</td>
<td>UB3_CTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>132</td>
<td>UART2_RXD</td>
<td>GPIO3_PC.03</td>
<td>IR3_RXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>134</td>
<td>UART3_TXD</td>
<td>GPIO3_PW.06</td>
<td>UC3_TXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>136</td>
<td>UART3_RXD</td>
<td>GPIO3_PW.07</td>
<td>UC3_RXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>138</td>
<td>GPIO0_PB0</td>
<td>GPIO3_PB.00</td>
<td>UD3_RXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>140</td>
<td>GPIO0_PB0</td>
<td>GPIO3_PB.00</td>
<td>UD3_RXD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>144</td>
<td>SDMMC1_DAT2</td>
<td>GPIO3_PY.05</td>
<td>SDMMC1_DAT2</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>146</td>
<td>SDMMC1_DAT3</td>
<td>GPIO3_PY.04</td>
<td>SDMMC1_DAT3</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>148</td>
<td>CLK2_REQ</td>
<td>GPIO3_PCC.05</td>
<td>arm_jtag0</td>
<td>Output Shift</td>
<td>CZ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>150</td>
<td>SDMMC1_CMD</td>
<td>GPIO3_PZ.01</td>
<td>SDMMC1_CMD</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152</td>
<td>CLK2_OUT</td>
<td>GPIO3_PW.05</td>
<td>extherpi2_clk</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>154</td>
<td>SDMMC1_CLK</td>
<td>GPIO3_PZ.00</td>
<td>SDMMC1_CLK</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>156</td>
<td>SDMMC3_CLK_LB_IN</td>
<td>GPIO3_PEE.05</td>
<td>SDMMC3_CLK_LB_IN</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>158</td>
<td>USB2_VBUS_ENS</td>
<td>GPIO3_PFF.01</td>
<td>stub vbus en2</td>
<td>3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>160</td>
<td>SDMMC1_DAT0</td>
<td>GPIO3_PY.07</td>
<td>SDMMC1_DAT0</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>162</td>
<td>SDMMC1_DAT1</td>
<td>GPIO3_PY.06</td>
<td>SDMMC1_DAT1</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>164</td>
<td>SDMMC1_WN</td>
<td>GPIO3_PY.03</td>
<td>SDMMC1_WN</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>166</td>
<td>SDMMC2_DAT2</td>
<td>GPIO3_PB.05</td>
<td>SDMMC2_DAT2</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>168</td>
<td>SDMMC3_DAT3</td>
<td>GPIO3_PB.04</td>
<td>SDMMC3_DAT3</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>170</td>
<td>SDMMC3_DAT2</td>
<td>GPIO3_PA.07</td>
<td>SDMMC3_DAT2</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>172</td>
<td>SDMMC2_DAT2</td>
<td>GPIO3_PA.07</td>
<td>SDMMC2_DAT2</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>174</td>
<td>SDMMC3_DAT2</td>
<td>GPIO3_PB.07</td>
<td>SDMMC3_DAT2</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>176</td>
<td>SDMMC3_DAT0</td>
<td>GPIO3_PB.06</td>
<td>SDMMC3_DAT0</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>178</td>
<td>SDMMC3_DAT1</td>
<td>GPIO3_PB.06</td>
<td>SDMMC3_DAT1</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>180</td>
<td>SDMMC3_DAT1</td>
<td>GPIO3_PB.06</td>
<td>SDMMC3_DAT1</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>182</td>
<td>SDMMC3_DAT1</td>
<td>GPIO3_PB.06</td>
<td>SDMMC3_DAT1</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>184</td>
<td>SDMMC3_DAT1</td>
<td>GPIO3_PB.06</td>
<td>SDMMC3_DAT1</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>186</td>
<td>SDMMC3_DAT1</td>
<td>GPIO3_PB.06</td>
<td>SDMMC3_DAT1</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>188</td>
<td>SDMMC3_DAT1</td>
<td>GPIO3_PB.06</td>
<td>SDMMC3_DAT1</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>190</td>
<td>SDMMC3_CD_N</td>
<td>GPIO3_PW.02</td>
<td>SDMMC3_CD_N</td>
<td>1.8V/3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>192</td>
<td>CLK3_OUT</td>
<td>GPIO3_PEE.00</td>
<td>extherpi3_clk</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>194</td>
<td>CLK3_OUT</td>
<td>GPIO3_PEE.00</td>
<td>extherpi3_clk</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>196</td>
<td>DAP2_DOUT</td>
<td>GPIO3_PA.05</td>
<td>i2s1_SDATA_OUT</td>
<td>Output Shift</td>
<td>ST</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>198</td>
<td>GPIO0_PBB3</td>
<td>GPIO0_PBB.03</td>
<td>VGP3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>DAP2_SCLK</td>
<td>GPIO0_PA.03</td>
<td>i2s1_SCLK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>202</td>
<td>DAP2_DIN</td>
<td>GPIO0_PA.04</td>
<td>i2s1_SDATA_IN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>204</td>
<td>DAP2_FS</td>
<td>GPIO0_PA.02</td>
<td>i2s1_LRCK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>220</td>
<td>HDMI CEC</td>
<td>GPIO3_PEE.03</td>
<td>CEC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>222</td>
<td>HDMI_TXD2P</td>
<td>HDMI_TXD2P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>224</td>
<td>HDMI_TXD2N</td>
<td>HDMI_TXD2N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>226</td>
<td>HDMI_TXD1P</td>
<td>HDMI_TXD1P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>230</td>
<td>HDMI_TXD1N</td>
<td>HDMI_TXD1N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>232</td>
<td>HDMI_INT</td>
<td>GPIO3_PN.07</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>234</td>
<td>HDMI_TXD0P</td>
<td>HDMI_TXD0P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X1 Pin</td>
<td>TK1 Ball Name</td>
<td>GPIO</td>
<td>SFI00</td>
<td>SFI01</td>
<td>SFI02</td>
<td>SFI03</td>
<td>Wake/ Strap</td>
<td>I/O Type</td>
<td>MPIO Type</td>
<td>Reset State</td>
<td>Pull</td>
<td>Power Block</td>
</tr>
<tr>
<td>--------</td>
<td>---------------</td>
<td>------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------------</td>
<td>----------</td>
<td>-----------</td>
<td>-------------</td>
<td>------</td>
<td>-------------</td>
</tr>
<tr>
<td>236</td>
<td>HDMI_TXD0N</td>
<td></td>
<td>HDMI_TXD0N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_hdmi</td>
</tr>
<tr>
<td>240</td>
<td>HDMI_TXCP</td>
<td></td>
<td>HDMI_TXCP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_hdmi</td>
</tr>
<tr>
<td>242</td>
<td>HDMI_TXCN</td>
<td></td>
<td>HDMI_TXCN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_hdmi</td>
</tr>
<tr>
<td>246</td>
<td>LVDS0_TXD4N</td>
<td></td>
<td>LVDS0_TXD4N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>248</td>
<td>LVDS0_TXD4P</td>
<td></td>
<td>LVDS0_TXD4P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>252</td>
<td>LVDS0_TXD0N</td>
<td></td>
<td>LVDS0_TXD0N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>254</td>
<td>LVDS0_TXD0P</td>
<td></td>
<td>LVDS0_TXD0P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>258</td>
<td>LVDS0_TXD1N</td>
<td></td>
<td>LVDS0_TXD1N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>260</td>
<td>LVDS0_TXD1P</td>
<td></td>
<td>LVDS0_TXD1P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>262</td>
<td>GPIO_PBB4</td>
<td></td>
<td>GPIO3_PBB.04</td>
<td>VGP4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddo_cam</td>
</tr>
<tr>
<td>264</td>
<td>LVDS0_TXD2N</td>
<td></td>
<td>LVDS0_TXD2N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>266</td>
<td>LVDS0_TXD2P</td>
<td></td>
<td>LVDS0_TXD2P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>270</td>
<td>LVDS0_TXD3N</td>
<td></td>
<td>LVDS0_TXD3N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>272</td>
<td>LVDS0_TXD3P</td>
<td></td>
<td>LVDS0_TXD3P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>avdd_lvds0_io</td>
</tr>
<tr>
<td>274</td>
<td>GEN2_I2C_SCL</td>
<td></td>
<td>GPIO3_PT.05</td>
<td>I2C2_CLK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddo_gmi</td>
</tr>
<tr>
<td>286</td>
<td>GPIO_PBB5</td>
<td></td>
<td>GPIO3_PBB.05</td>
<td>VGP5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>vddo_cam</td>
</tr>
</tbody>
</table>
5. Kinetis K20 Companion MCU I/O Pins

The Apalis TK1 features an additional NXP (Freescale) Kinetis K20 microcontroller. The main purpose of this companion MCU is to extend the following interfaces:

- 2x CAN (FlexCAN)
- 4x ADC inputs
- Resistive touch interface
- Additional GPIOs

These main interfaces are supported by the standard Linux BSP that comes with the module. The Kinetis Microcontroller features additional interfaces that are available as alternate functions. The software support for these interfaces is very limited. Drivers and/or firmware might need to be written by the customer. A few examples of such additional interfaces are:

- Additional I2C
- Additional PWM
- Additional ADC inputs
- Additional SD interface
- Additional UART ports
- Additional SPI
- Additional USB 1.1 interface
- Timer interface
- Capacitive touch buttons

The communication between the Tegra K1 SoC and the K20 companion MCU takes place over an SPI interface. The Tegra K1 is the SPI master. In addition to the K20 SPI slave input, the SPI interface between the two controllers is also connected to the EzPort of the K20 for flashing the firmware of the MCU. In order to be able to set the K20 into programming mode, the Tegra K1 will need to drive the reset of K20.

![Figure 5: Connections between SoC and MCU](image-url)
Table 5-1 Interface Signals between SoC and MCU

<table>
<thead>
<tr>
<th>TK1 Ball Name</th>
<th>TK1 Function</th>
<th>K20 Function</th>
<th>K20 Ball Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_X4_AUD</td>
<td>SPI2C_DOUT</td>
<td>SPI2_SIN</td>
<td>PTB23</td>
<td>SPI MOSI for communication</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EZP_DI</td>
<td>PTA1</td>
<td>Programming data input of MCU</td>
</tr>
<tr>
<td>GPIO_X5_AUD</td>
<td>SPI2C_SCK</td>
<td>SPI2_SCK</td>
<td>PTB21</td>
<td>SPI CLK for communication</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EZP_CLK</td>
<td>PTA0</td>
<td>Programming clock input of MCU</td>
</tr>
<tr>
<td>GPIO_X7_AUD</td>
<td>SPI2C_DIN</td>
<td>SPI2_SOUT</td>
<td>PTB22</td>
<td>SPI MISO for communication</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EZP_DO</td>
<td>PTA2</td>
<td>Programming data output of MCU</td>
</tr>
<tr>
<td>GPIO_X6_AUD</td>
<td>SPI2C_DS1</td>
<td>SPI2_PCS0</td>
<td>PTB20</td>
<td>SPI CS for communication</td>
</tr>
<tr>
<td>GPIO_W2_AUD</td>
<td>SPI2C_DS2</td>
<td>EZP_CS_b</td>
<td>PTA4</td>
<td>Chip select for programming the MCU</td>
</tr>
<tr>
<td>GPIO_PBB6</td>
<td>GPIO3_PBB.06</td>
<td>RESET_b</td>
<td>RESET_b</td>
<td>Reset input of K20. K20 features also a power on Reset.</td>
</tr>
<tr>
<td>GPIO_PK2</td>
<td>GPIO3_PK.02</td>
<td>PTA16</td>
<td>PTA16</td>
<td>MCU interrupt output 1 (no level shifter!)</td>
</tr>
<tr>
<td>GPIO_PJ2</td>
<td>GPIO3_PJ.02</td>
<td>PTA29</td>
<td>PTA29</td>
<td>MCU interrupt output 2 (no level shifter!)</td>
</tr>
<tr>
<td>GPIO_PI5</td>
<td>GPIO3_PI.05</td>
<td>PTB8</td>
<td>PTB8</td>
<td>MCU interrupt output 3 (no level shifter!)</td>
</tr>
<tr>
<td>GPIO_PJ0</td>
<td>GPIO3_PJ.00</td>
<td>PTE26</td>
<td>PTE26</td>
<td>MCU interrupt output 4 (no level shifter!)</td>
</tr>
</tbody>
</table>

There are four interrupt lines from the K20 MCU to the TK1 SoC. There is no level shifter between the two controllers. The SoC pins are only 1.8V capable while all K20 pins do have 3.3V logic level. Therefore, it is very important to configure the interrupt pins correctly on both sides. The interrupt output pins of the MCU need to be configured as open drain output without enabling the internal pull up resistors. The pull-up resistors need to be enabled at the SoC input since they are pulling up the signal to just 1.8V.

5.1 K20 Pin Control

Most of the K20 pins can be configured to any of up to eight alternate functions. Most pins can also be used as regular GPIOs. All K20 pins are 3.3V logic level. Therefore, no level shifters are needed. This means that there are no limitations for using the pins as GPIO as with the level shifted TK1 signals.

For each regular K20 pin, following controls can be changed individually:

- Pin mux control (selecting the alternate function)
- Interrupt configuration
- DMA configuration
- Drive strength
- Open drain mode
- Passive filter (low pass filter for signals below 2MHz)
- Slew rate
- Pull-up or -down resistor enabling
5.2 K20 Functions List

The following list contains all K20 MCU pins which are available on the MXM3 connector. It shows the alternate functions that are available for each pin. The alternate functions used to provide the primary interfaces to ensure best compatibility with other Apalis modules are highlighted. Please be aware that not all listed functions are supported by the standard Linux BSP. In order to use them, additional firmware and/or drivers need to be developed.

Most of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behaviour.

Function Short Forms

- **ADC**: Analogue to Digital Converter
- **CAN**: Controller Area Network
- **CMP**: Comparator
- **EWM**: External Watchdog Monitor
- **FB**: FlexBus, external bus
- **FTM**: FlexTimer, general purpose timer, can be used as PWM output
- **I2C**: Inter Integrated Circuit
- **I2S**: Inter IC Sound
- **PDB**: Programmable Delay Block
- **PTx**: General Purpose IO (GPIO)
- **SDHC**: Secure Digital Memory Card High Capacity (SD, MMC, CE-ATA, eMMC)
- **SPI**: Serial Peripheral Interface Bus
- **TSI**: Touch Sense Input
- **UART**: Serial Ports (Universal Asynchronous Receiver/Transmitter)
- **USB**: Universal Serial Bus
<table>
<thead>
<tr>
<th>X1 Pin</th>
<th>K20 Pin</th>
<th>Ball Name</th>
<th>ALT0</th>
<th>ALT1</th>
<th>ALT2</th>
<th>ALT3</th>
<th>ALT4</th>
<th>ALT5</th>
<th>ALT6</th>
<th>ALT7</th>
<th>Reset Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 K20_PTA13/LLWU_P4</td>
<td>CMP2_IN1</td>
<td>PTA13/LLWU_P4</td>
<td>CAN0_RX</td>
<td>FTM1_CH1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14 K20_PTA12</td>
<td>CMP2_IN0</td>
<td>PTA12</td>
<td>CAN0_TX</td>
<td>FTM1_CH0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 K20_PTC16</td>
<td>PTC16</td>
<td>CAN1_RX</td>
<td>UART3_RX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18 K20_PTC17</td>
<td>PTC17</td>
<td>CAN1_TX</td>
<td>UART3_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>86 K20_USB0_DP</td>
<td>USB0_DP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>88 K20_USB0_DM</td>
<td>USB0_DM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>173 K20_PTE1/LLWU_P0</td>
<td>ADC1_SE5a</td>
<td>PTE1/LLWU_P0</td>
<td>SPI1_SOUT</td>
<td>UART1_RX</td>
<td>SDHC0_D0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>175 K20_PTE0</td>
<td>ADC1_SE4a</td>
<td>PTE0</td>
<td>SPI1_PCS1</td>
<td>UART1_TX</td>
<td>SDHC0_D1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>177 K20_PTB17</td>
<td>TS0_CH10</td>
<td>PIB17</td>
<td>SPI1_SIN</td>
<td>UART0_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>181 K20_PTE5</td>
<td>ADC1_SE7a</td>
<td>PTE5</td>
<td>SPI1_PCS2</td>
<td>UART3_RX</td>
<td>SDHC0_D2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>183 K20_PTE24</td>
<td>ADC0_SE17</td>
<td>PTE24</td>
<td>CAN1_TX</td>
<td>UART4_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>185 K20_PTE4/LLWU_P5</td>
<td>PTE4/LLWU_P2</td>
<td>SPI1_PCS0</td>
<td>UART3_TX</td>
<td>SDHC0_D3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>187 K20_PTA17</td>
<td>ADC1_SE17</td>
<td>PTA17</td>
<td>SPI0_SIN</td>
<td>UART0_RTS_b</td>
<td>i2S0_MCLK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>191 K20_PTE25</td>
<td>ADC0_SE18</td>
<td>PTE25</td>
<td>CAN1_RX</td>
<td>UART4_RX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>195 K20_PTA5</td>
<td>PTA5</td>
<td>USB_CLKIN</td>
<td>FTM0_CH2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>197 K20_PTA3</td>
<td>TS0_CH4</td>
<td>PTA3</td>
<td>UART0_RTS_b</td>
<td>FTM0_CH0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>243 K20_PTD7</td>
<td>PTD7</td>
<td>CMT_IRO</td>
<td>UART0_TX</td>
<td>FTM0_CH7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>245 K20_PTD5</td>
<td>ADC0_SE6b</td>
<td>PTD5</td>
<td>SPI0_PCS2</td>
<td>UART0_RTS_b</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>247 K20_PTD4/LLWU_P14</td>
<td>PTD4/LLWU_P14</td>
<td>SPI0_PCS1</td>
<td>UART0_RTS_b</td>
<td>FTM0_CH4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>249 K20_PTC4/LLWU_P8</td>
<td>PTC4/LLWU_P8</td>
<td>SPI0_PCS0</td>
<td>UART1_TX</td>
<td>FTM0_CH3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>251 K20_PTD9</td>
<td>PTD9</td>
<td>i2C0_SDA</td>
<td>UART5_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>253 K20_PTD8</td>
<td>PTD8</td>
<td>i2C0_SCL</td>
<td>UART5_RX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>255 K20_PTD6/LLWU_P15</td>
<td>ADC0_SE7b</td>
<td>PTD6/LLWU_P15</td>
<td>SPI0_PCS3</td>
<td>UART0_RX</td>
<td>FTM0_CH6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>257 K20_PTD3</td>
<td>PTD3</td>
<td>SPI0_SIN</td>
<td>UART2_TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>259 K20_PTC7</td>
<td>CMP0_In1</td>
<td>PTC7</td>
<td>SPI0_SIN</td>
<td>USB_SOFTWARE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>261 K20_PTC3/LLWU_P7</td>
<td>CMP1_In1</td>
<td>PTC3/LLWU_P7</td>
<td>SPI0_PCS1</td>
<td>UART1_RX</td>
<td>FTM0_CH2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>263 K20_PTC0</td>
<td>ADC0_SE14/TS0_CH13</td>
<td>PTC0</td>
<td>SPI0_PCS4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>265 K20_PTB16</td>
<td>TS0_CH9</td>
<td>PBT16</td>
<td>SPI1_SOUT</td>
<td>UART0_RX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>269 K20_PTD12</td>
<td>PTD12</td>
<td>SPI2_SCK</td>
<td>SDHC0_D4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>271 K20_PTD11</td>
<td>PTD11</td>
<td>SPI2_PCS0</td>
<td>UART5_CTS_b</td>
<td>SDHC0_CLKIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>273 K20_PTD2/LLWU_P13</td>
<td>PTD2/LLWU_P13</td>
<td>SPI0_SOUT</td>
<td>UART2_RX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>275 K20_PTC6/LLWU_P10</td>
<td>CMP0_IN0</td>
<td>PTC6/LLWU_P10</td>
<td>SPI0_SOUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X1 Pin</td>
<td>K20 Ball Name</td>
<td>ALT0</td>
<td>ALT1</td>
<td>ALT2</td>
<td>ALT3</td>
<td>ALT4</td>
<td>ALT5</td>
<td>ALT6</td>
<td>ALT7</td>
<td>Reset Default</td>
<td></td>
</tr>
<tr>
<td>-------</td>
<td>--------------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>----------------</td>
<td></td>
</tr>
<tr>
<td>277</td>
<td>K20_PTC2</td>
<td>ADC0_SE4b/CMP1_IN0/</td>
<td>PTC2</td>
<td>SPI0_PCS2</td>
<td>UART1_CTS_b</td>
<td>FTM0_CH1</td>
<td>FB_AD12</td>
<td>I2S0_TX_FS</td>
<td>ADC0_SE4b/CMP1_IN0/</td>
<td></td>
<td></td>
</tr>
<tr>
<td>279</td>
<td>K20_PTB19</td>
<td>TS10_CH12</td>
<td>PTB19</td>
<td>CAN0_RX</td>
<td>FTM2_CH1</td>
<td>I2S0_TX_FS</td>
<td>FB_OE_b</td>
<td>FTM2_QD_PHB</td>
<td>TS10_CH12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>281</td>
<td>K20_PTB11</td>
<td>ADC1_SE15</td>
<td>PTB11</td>
<td>SPI1_SCK</td>
<td>UART3_TX</td>
<td>FTM0_FLT2</td>
<td>FB_AD18</td>
<td>ADC1_SE15</td>
<td>TS10_CH12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>283</td>
<td>K20_PTD14</td>
<td>SPI2_IN</td>
<td>SPI2_SOUT</td>
<td>SDHC0_D6</td>
<td>SDHC0_D5</td>
<td>FB_A22</td>
<td>DISABLED</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>287</td>
<td>K20_PTD13</td>
<td>PTD13</td>
<td>SPI2_SOUT</td>
<td>SDHC0_D5</td>
<td>SDHC0_D5</td>
<td>FB_A21</td>
<td>DISABLED</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>289</td>
<td>K20_PTD1</td>
<td>ADC0_SE5b</td>
<td>PTD1</td>
<td>SPI0_SCK</td>
<td>UART2_CTS_b</td>
<td>FB_CS0_b</td>
<td>ADC0_SE5b</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>291</td>
<td>K20_PTD0/LLWU_P12</td>
<td>SPI0_PCS0</td>
<td>PTD0/LLWU_P12</td>
<td>SPI0_PCS0</td>
<td>UART2_RTS_b</td>
<td>FB_ALE</td>
<td>FB_CS1_b</td>
<td>FB_TS_b</td>
<td>DISABLED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>293</td>
<td>K20_PTC1/LLWU_P6</td>
<td>ADC0_SE15/TS10_CH14</td>
<td>PTC1/LLWU_P6</td>
<td>SPI0_PCS3</td>
<td>UART1_RTS_b</td>
<td>FTM0_CH0</td>
<td>FB_AD13</td>
<td>I2S0_TXD0</td>
<td>ADC0_SE15/TS10_CH14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>295</td>
<td>K20_PTB18</td>
<td>TS10_CH11</td>
<td>PTB18</td>
<td>CAN0_TX</td>
<td>FTM2_CH0</td>
<td>I2S0_TX_BCLK</td>
<td>FB_AD15</td>
<td>FTM2_QD_PHA</td>
<td>TS10_CH11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>297</td>
<td>K20_PTB10</td>
<td>ADC1_SE14</td>
<td>PTB10</td>
<td>SPI1_PCS0</td>
<td>UART3_RX</td>
<td>FTM0_FLT1</td>
<td>FB_AD19</td>
<td>ADC1_SE14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>299</td>
<td>K20_PTD15</td>
<td>SPI2_PCS1</td>
<td>PTD15</td>
<td>SPI2_PCS1</td>
<td>SDHC0_D7</td>
<td>SDHC0_DCLK</td>
<td>FB_A23</td>
<td>DISABLED</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>301</td>
<td>K20_PTE2/LLWU_P1</td>
<td>ADC1_SE6a</td>
<td>PTE2/LLWU_P1</td>
<td>SPI1_SCK</td>
<td>UART1_CTS_b</td>
<td>SDHC0_DCLK</td>
<td>ADC1_SE6a</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>305</td>
<td>K20_PTB0/LLWU_P5</td>
<td>ADC0_SE8/ADC1_SE8/TS10_CH0</td>
<td>PTB0/LLWU_P5</td>
<td>I2C0_SCL</td>
<td>FTM1_CH0</td>
<td>FTM1_QD_PHA</td>
<td>ADC0_SE8/ADC1_SE8/TS10_CH0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>307</td>
<td>K20_PTB1</td>
<td>ADC0_SE9/ADC1_SE9/TS10_CH6</td>
<td>PTB1</td>
<td>I2C0_SDA</td>
<td>FTM1_CH1</td>
<td>FTM1_QD_PHB</td>
<td>ADC0_SE9/ADC1_SE9/TS10_CH6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>309</td>
<td>K20_PTB2</td>
<td>ADC0_SE12/TS10_CH7</td>
<td>PTB2</td>
<td>I2C0_SDA</td>
<td>UART0_RTS_b</td>
<td>FTM0_FLT3</td>
<td>ADC0_SE12/TS10_CH7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>311</td>
<td>K20_PTB3</td>
<td>ADC0_SE13/TS10_CH8</td>
<td>PTB3</td>
<td>I2C0_SDA</td>
<td>UART0_CTS_b/UART0_COL_b</td>
<td>FTM0_FLT0</td>
<td>ADC0_SE13/TS10_CH8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>315</td>
<td>K20_PTB6</td>
<td>ADC1_SE12</td>
<td>PTB6</td>
<td>FB_AD23</td>
<td>ADC1_SE12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>317</td>
<td>K20_PTB7</td>
<td>ADC1_SE13</td>
<td>PTB7</td>
<td>FB_AD22</td>
<td>ADC1_SE13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>319</td>
<td>K20_PTC8</td>
<td>ADC1_SE4b/CMP0_IN2</td>
<td>PTB8</td>
<td>I2S0_MCLK</td>
<td>FB_AD7</td>
<td>ADC1_SE4b/CMP0_IN2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>321</td>
<td>K20_PTC9</td>
<td>ADC1_SE5b/CMP0_IN3</td>
<td>TPC9</td>
<td>I2S0_RX_BCLK</td>
<td>FB_AD6</td>
<td>FTM2_FLT0</td>
<td>ADC1_SE5b/CMP0_IN3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6. Interface Description

6.1 Power Signals

6.1.1 Digital Supply

Table 6-1 Digital Supply Pins

<table>
<thead>
<tr>
<th>X1 Pin #</th>
<th>Apalis Signal Name</th>
<th>I/O</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10, 30, 36, 52, 58, 66, 78, 90, 102, 108</td>
<td>VCC</td>
<td>I</td>
<td>3.3V main power supply</td>
<td>Use decoupling capacitors on all pins.</td>
</tr>
<tr>
<td>9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298</td>
<td>GND</td>
<td>I</td>
<td>Digital Ground</td>
<td></td>
</tr>
<tr>
<td>174</td>
<td>VCC_BACKUP</td>
<td>I/O</td>
<td>RTC Power supply can be connected to a backup battery.</td>
<td>Can be left unconnected if the internal RTC is not used.</td>
</tr>
</tbody>
</table>

6.1.2 Analogue Supply

Table 6-2 Analogue Supply Pins

<table>
<thead>
<tr>
<th>X1 Pin #</th>
<th>Apalis Signal Name</th>
<th>I/O</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>314, 320</td>
<td>AVCC</td>
<td>I</td>
<td>3.3V Analogue supply</td>
<td>Connect this pin to a 3.3V supply. For better audio accuracy we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the VCC 3.3V input supply.</td>
</tr>
<tr>
<td>303, 304, 308</td>
<td>AGND</td>
<td>I</td>
<td>Analogue Ground</td>
<td>Connect this pin to GND. For better audio accuracy we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Apalis TK1.</td>
</tr>
</tbody>
</table>

6.1.3 Power Management Signals

Table 6-3 Power Management Pins

<table>
<thead>
<tr>
<th>X1 Pin #</th>
<th>Apalis Signal Name</th>
<th>I/O</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>RESET_MICO#</td>
<td>I</td>
<td>Reset Input</td>
<td>This pin is low active and resets the Apalis module. This pin is connected to the power manager IC. There is a 100k pull-up resistor on the module.</td>
</tr>
<tr>
<td>26</td>
<td>RESET_MOCI#</td>
<td>O</td>
<td>Reset Output</td>
<td>This pin is active low. This pin is driven low at boot up. This is an open drain signal with a 10k pull-up resistor on the module.</td>
</tr>
<tr>
<td>24</td>
<td>POWER_ENABLE_MOCI</td>
<td>O</td>
<td>Signal for the carrier board to enable the peripheral voltage rails</td>
<td>More information about the required power management on the carrier board can be found in the Apalis Carrier Board Design Guide</td>
</tr>
</tbody>
</table>
6.2 GPIOs

The Apalis form factor features 8 dedicated general purpose input output (GPIO) pins. Beside these 8 GPIOs, several pins can be used as GPIO if their primary function is not in use. For compatibility reason, it is recommended to use the 8 dedicated GPIOs first.

Since some of the Tegra K1 signal pins feature a unidirectional level shifter, these pins can only be used as general purpose input or output but not as regular GPIO. Other pins are provided by the companion MCU instead of the main SoC. Therefore, it is very important to check the type of pin before selecting it as GPIO. More information can be found in the section 4 and 5.

Table 6-4 Dedicated GPIO signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GPIO1</td>
<td>GPIO_PFF2</td>
<td>GPIO3_PFF.02</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>GPIO2</td>
<td>DP_HPD</td>
<td>GPIO3_PFF.00</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>GPIO3</td>
<td>USB_VBUS_EN0</td>
<td>GPIO3_PN.04</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>GPIO4</td>
<td>USB_VBUS_EN1</td>
<td>GPIO3_PN.05</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>GPIO5</td>
<td>PEX_L1_RST_N</td>
<td>GPIO3_PDD.05</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>GPIO6</td>
<td>PEX_L1_CLKREQ_N</td>
<td>GPIO3_PDD.06</td>
<td>I/O</td>
<td>Second SoC ball connected to this MXM3 pin</td>
</tr>
<tr>
<td>15</td>
<td>GPIO7</td>
<td>PEX_L0_RST_N</td>
<td>GPIO3_PDD.01</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>GPIO8</td>
<td>PEX_L0_CLKREQ_N</td>
<td>GPIO3_PDD.02</td>
<td>I/O</td>
<td></td>
</tr>
</tbody>
</table>

6.2.1 Wakeup Source

There are several Tegra K1 pins which can be used to wake up the Apalis module from a suspended state. In the Apalis module standard, pin 37 is the default wakeup source. Only this pin is guaranteed to be wake up compatible with other Apalis modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Apalis modules.

Table 6-5 TK1 Wakeup Sources

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 GPIO Name</th>
<th>Wake Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>37</td>
<td>WAKE1_MICO</td>
<td>PEX_WAKE_N</td>
<td>GPIO3_PDD.03</td>
<td>wake14</td>
</tr>
<tr>
<td>1</td>
<td>GPIO1</td>
<td>GPIO_PFF2</td>
<td>GPIO3_PFF.02</td>
<td>wake59</td>
</tr>
<tr>
<td>35</td>
<td>SATA1_ACT#</td>
<td>DAP1_DOUT</td>
<td>GPIO3_PN.02</td>
<td>wake30</td>
</tr>
<tr>
<td>120</td>
<td>UART1_DSR</td>
<td>UART3_CTS_N</td>
<td>GPIO3_PA.01</td>
<td>wake55</td>
</tr>
<tr>
<td>162</td>
<td>MMC1_D1</td>
<td>SDMMC1_DAT1</td>
<td>GPIO3_PY.06</td>
<td>wake13</td>
</tr>
<tr>
<td>188</td>
<td>SD1_D1</td>
<td>SDMMC3_DAT1</td>
<td>GPIO3_PB.06</td>
<td>wake3</td>
</tr>
<tr>
<td>201</td>
<td>I2C3_SDA (CAM)</td>
<td>CAM_I2C_SDA</td>
<td>GPIO3_PBB.02</td>
<td>wake48</td>
</tr>
<tr>
<td>203</td>
<td>I2C3_SCL (CAM)</td>
<td>CAM_I2C_SCL</td>
<td>GPIO3_PBB.01</td>
<td>wake53</td>
</tr>
<tr>
<td>209</td>
<td>I2C1_SDA</td>
<td>GEN1_I2C_SDA</td>
<td>GPIO3_PC.05</td>
<td>wake44</td>
</tr>
<tr>
<td>217</td>
<td>SPDIF1_IN</td>
<td>SPDIF_IN</td>
<td>GPIO3_PK.06</td>
<td>wake57</td>
</tr>
<tr>
<td>220</td>
<td>HDMI1_CEC</td>
<td>HDMI_CEC</td>
<td>GPIO3_PEE.03</td>
<td>wake52</td>
</tr>
<tr>
<td>232</td>
<td>HDMI1_HPD</td>
<td>HDMI_INT</td>
<td>GPIO3_PN.07</td>
<td>wake4</td>
</tr>
<tr>
<td>239</td>
<td>BKL1_PWM</td>
<td>GPIO_PU6</td>
<td>GPIO3_PU.06</td>
<td>wake7</td>
</tr>
</tbody>
</table>
The wake signal of the Ethernet controller (pin 16, PE_WAKE_N) is connected to the ULPI_DATA4 ball of the TK1 (GPIO3_PO.05). This pin features wake source “wake0” and allows the Ethernet controller to wake up the Tegra K1.

### 6.3 Ethernet

The Apalis Module features a 10/100/1000 Mbit Ethernet interface. The MAC/PHY is integrated on the module, therefore only the magnetics are required on the carrier board. The Intel I210-AT Gigabit Ethernet Controller chip is connected over the PCIe port 1 (lane 2) of the Tegra K1. The Ethernet controller supports IEEE1588 and IEEE802.1AS time synchronization. There are up to three externally available pins available which can be used for the time synchronization.

#### Table 6-6 Ethernet Pins

<table>
<thead>
<tr>
<th>X1 Pin #</th>
<th>Apalis Signal Name</th>
<th>I210-AT Signal Name</th>
<th>I/O</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>ETH1_MDI0+</td>
<td>MDI_0_P</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Transmit +</td>
</tr>
<tr>
<td>48</td>
<td>ETH1_MDI0-</td>
<td>MDI_0_N</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Transmit -</td>
</tr>
<tr>
<td>56</td>
<td>ETH1_MDI1+</td>
<td>MDI_1_P</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Receive +</td>
</tr>
<tr>
<td>54</td>
<td>ETH1_MDI1-</td>
<td>MDI_1_N</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Receive -</td>
</tr>
<tr>
<td>32</td>
<td>ETH1_MDI2+</td>
<td>MDI_2_P</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Unused</td>
</tr>
<tr>
<td>34</td>
<td>ETH1_MDI2-</td>
<td>MDI_2_N</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Unused</td>
</tr>
<tr>
<td>38</td>
<td>ETH1_MDI3+</td>
<td>MDI_3_P</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Unused</td>
</tr>
<tr>
<td>40</td>
<td>ETH1_MDI3-</td>
<td>MDI_3_N</td>
<td>I/O</td>
<td>Media Dependent Interface</td>
<td>100BASE-TX: Unused</td>
</tr>
<tr>
<td>46</td>
<td>ETH+_CTREF</td>
<td>NC</td>
<td>O</td>
<td>Centre tap supply</td>
<td>I210 does not need centre tap supply</td>
</tr>
<tr>
<td>42</td>
<td>ETH1_ACT</td>
<td>LED1</td>
<td>O</td>
<td>LED indication output</td>
<td>Mode can be configured individually</td>
</tr>
<tr>
<td>44</td>
<td>ETH1_LINK</td>
<td>LED2</td>
<td>O</td>
<td>LED indication output</td>
<td>Mode can be configured individually</td>
</tr>
<tr>
<td>99</td>
<td>TS_3</td>
<td>SDP0</td>
<td>I/O</td>
<td>Software-defined pin 0</td>
<td>The SDP can be individually configured to act as either standard input, General-Purpose Interrupt input, or output pin. Can be used for IEEE1588 time synchronization to auxiliary devices.</td>
</tr>
<tr>
<td>123</td>
<td>TS_4</td>
<td>SDP1</td>
<td>I/O</td>
<td>Software-defined pin 1</td>
<td></td>
</tr>
<tr>
<td>135</td>
<td>TS_5</td>
<td>SDP2</td>
<td>I/O</td>
<td>Software-defined pin 2</td>
<td></td>
</tr>
</tbody>
</table>

The Intel I210-AT does not require a central tap supply on the magnetics. Nevertheless, follow the Apalis Carrier Board Design Guide and connect the centre tap of the magnetics to pin 46 of the Apalis module. This guarantees the full compatibility to Apalis modules which require a centre tap supply.

If only fast Ethernet is required, 10/100Mbit magnetics with only 2 lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

### 6.4 USB

The Apalis module form factor features up to four USB interfaces, two USB 3.0 SuperSpeed (backward compatible) and two USB 2.0 High-Speed interfaces. The NVIDIA Tegra K1 features only two USB 3.0 SuperSpeed (5Gbit/s) and one USB 2.0 High-Speed (480 Mbit/s) interfaces with integrated physical layer. Therefore, USB_H3 cannot be provided by the TK1 SoC. The USBO1 is used for the USB recovery mode. See the section 7 “Recovery Mode” for more information.

The USB 3.0 SuperSpeed feature of the USBO port can only be used in the host mode. In client mode, the OTG port supports only USB 2.0 High-Speed. Both USB 3.0 ports (USBO and USBH4) share one Super Speed Bus Instance. The 5Gb/s bandwidth is distributed across these ports.
The USB_H3 port of the Apalis module edge connector is not provided by the TK1 SoC, it is provided by the Kinetis companion MCU which communicates over SPI with the SoC. The K20 MCU follows the USB 2.0 specifications but is only Full Speed (12Mbit/s) and Low-Speed (1.5Mbit/s) capable. This limitation is colloquially called as “limited to USB 1.1”. The standard Toradex Linux BSP does not include K20 firmware and drivers for using this port.

### 6.4.1 USB Data Signal

#### Table 6-7 USB0 Data Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>74</td>
<td>USB01_D+</td>
<td>USB0_DP</td>
<td>I/O</td>
<td>Positive Differential USB Signal, OTG capable</td>
</tr>
<tr>
<td>76</td>
<td>USB01_D-</td>
<td>USB0_DN</td>
<td>I/O</td>
<td>Negative Differential USB Signal, OTG capable</td>
</tr>
<tr>
<td>62</td>
<td>USB01_SSRX+</td>
<td>PEX_USB3_RX1P</td>
<td>I</td>
<td>Positive differential receiving signal for USB3.0</td>
</tr>
<tr>
<td>64</td>
<td>USB01_SSRX-</td>
<td>PEX_USB3_RX1N</td>
<td>I</td>
<td>Negative differential receiving signal for USB3.0</td>
</tr>
<tr>
<td>68</td>
<td>USB01_SSTX+</td>
<td>PEX_USB3_TX1P</td>
<td>O</td>
<td>Positive differential transmission signal for USB3.0</td>
</tr>
<tr>
<td>70</td>
<td>USB01_SSTX-</td>
<td>PEX_USB3_TX1N</td>
<td>O</td>
<td>Negative differential transmission signal for USB3.0</td>
</tr>
</tbody>
</table>

#### Table 6-8 USBH2 Data Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>80</td>
<td>USBH2_D+</td>
<td>USB1_DP</td>
<td>I/O</td>
<td>Positive Differential USB Signal</td>
</tr>
<tr>
<td>82</td>
<td>USBH2_D-</td>
<td>USB1_DN</td>
<td>I/O</td>
<td>Negative Differential USB Signal</td>
</tr>
</tbody>
</table>

#### Table 6-9 USBH3 Data Pins (K20 companion MCU)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>86</td>
<td>USBH3_D+</td>
<td>USB0_DP</td>
<td>I/O</td>
<td>Positive Differential USB Signal, Interface of K20 companion MCU</td>
</tr>
<tr>
<td>88</td>
<td>USBH3_D-</td>
<td>USB0_DM</td>
<td>I/O</td>
<td>Negative Differential USB Signal, Interface of K20 companion MCU</td>
</tr>
</tbody>
</table>

#### Table 6-10 USBH4 Data Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>98</td>
<td>USBH4_D+</td>
<td>USB2_DP</td>
<td>I/O</td>
<td>Positive Differential USB Signal</td>
</tr>
<tr>
<td>100</td>
<td>USBH4_D-</td>
<td>USB2_DN</td>
<td>I/O</td>
<td>Negative Differential USB Signal</td>
</tr>
<tr>
<td>94</td>
<td>USBH4_SSRX+</td>
<td>USB3_RX0P</td>
<td>I</td>
<td>Positive differential receiving host signal for USB3.0</td>
</tr>
<tr>
<td>92</td>
<td>USBH4_SSRX-</td>
<td>USB3_RX0N</td>
<td>I</td>
<td>Negative differential receiving host signal for USB3.0</td>
</tr>
<tr>
<td>106</td>
<td>USBH4_SSTX+</td>
<td>USB3_TX0P</td>
<td>O</td>
<td>Positive differential transmission host signal for USB3.0</td>
</tr>
<tr>
<td>104</td>
<td>USBH4_SSTX-</td>
<td>USB3_TX0N</td>
<td>O</td>
<td>Negative differential transmission host signal for USB3.0</td>
</tr>
</tbody>
</table>
6.4.2 USB Control Signals

Table 6-11 USB OTG Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72</td>
<td>USBO1_ID</td>
<td>USB0_ID</td>
<td>USB0_ID</td>
<td>I</td>
<td>Use this pin to detect the ID pin if you use USB OTG.</td>
</tr>
<tr>
<td>60</td>
<td>USBO1_VBUS</td>
<td>USB0_VBUS</td>
<td>USB0_VBUS</td>
<td>I</td>
<td>Use this pin to detect if VBUS is present.</td>
</tr>
</tbody>
</table>

If you use the USB Host function you need to provide the 5V USB supply voltage on your carrier board for the interfaces. The Apalis TK1 provides additional signals for controlling the USB supply. We recommend using the following pins to guarantee the best possible compatibility. However, if required you can use other GPIOs or not use them at all. The USBH2, USBH3, and USBH4 interfaces share the bus power control signals whereas USBO1 has its own dedicated control signals.

Table 6-12 USB Power Control Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>274</td>
<td>USBO1_EN</td>
<td>GEN2_I2C_SCL</td>
<td>GPIO3_PT.05</td>
<td>O</td>
<td>This pin enables the external USB voltage supply for the USBO1 interface. The function is provided by a regular GPIO. There is an output level shifter on the module.</td>
</tr>
<tr>
<td>262</td>
<td>USBO1_OC#</td>
<td>GPIO_PBB4</td>
<td>GPIO3_PBB.04</td>
<td>I</td>
<td>USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBO1 interface. The pin features an input level shifter on the module</td>
</tr>
<tr>
<td>84</td>
<td>USBH_EN</td>
<td>GEN2_I2C_SDA</td>
<td>GPIO3_PT.06</td>
<td>O</td>
<td>This pin enables the external USB voltage supply for the USBH2, USBH3, and USBH4 interfaces. The function is provided by a regular GPIO. There is an output level shifter on the module.</td>
</tr>
<tr>
<td>96</td>
<td>USBH_OC#</td>
<td>GPIO_PBB0</td>
<td>GPIO3_PBB.00</td>
<td>I</td>
<td>USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBH2, USBH3, and USBH4 interfaces. The pin features an input level shifter on the module</td>
</tr>
</tbody>
</table>

The USBO1_OC# and USBH_OC# pins are level shifted on the module. Therefore, it is recommended adding pull up or pull down resistors to the non-used input pins in order to make sure they are not floating. See also section 4.1.5. The USBO1_EN and USBH_EN pins are featuring output level shifter and can be left floating if not used.

6.5 Display

The display controller subsystem of the Tegra K1 features two independent display controllers that support HDMI, LVDS, DSI, as well as eDP. The controller can support two independent display devices. Each display controller can run at different clock rates and drive different resolution panels.

6.5.1 Parallel RGB LCD interface

The Apalis TK1 does not feature a parallel RGB LCD interface. The K20 MCU pins that are located on the dedicated module edge pins do not feature any LCD interface. Nevertheless, it is possible to implement an LVDS or DSI to RGB converter on the carrier board in order to attach such a display.
6.5.2 LVDS

The LVDS interface (official name: FPD-Link/FlatLink) serialises the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to 7 parallel signals. For an 18-bit RGB interface including the control signals (Display Enable, Vertical, and Horizontal Synch), each FPD Link/FlatLink channel requires three LVDS data pairs. The additional colours bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two colour mapping standards for the 24-bit interface. The less common “24-bit / 18-bit compatible” (JEIDA format, Intel 24.0 LVDS data format) standard packs the two low significant bits of each colour into the fourth LVDS pair. This standard is backward compatible with the 18-bit mode. It is possible to connect an 18-bit display to a 24-bit interface or vice versa. The more common 24-bit colour mapping standard (VESA format, Intel 24.1 LVDS data format) serializes the two most significant bits of each colour into the fourth LVDS pair. This mode is not backward compatible. Therefore, only 24-bit displays can be connected to a 24-bit host with this colour mapping. The LVDS interface of Apalis TK1 is configurable to support different colour mappings and depths. This ensures compatibility with 18-bit and 24-bit displays with both kinds of colour mappings.

Figure 6 shows the LVDS output signals for the “24-bit /18-bit Compatible Colour Mapping” (JEIDA format, Intel 24.0 LVDS data format). In order to enable this mode, the DOTDAT[2:0] needs to be set to 0 in the SOR_NV_PDISP_SOR_CSTM_0 register.

Figure 7 shows the LVDS output signals for the common 24-bit colour mapping (VESA format, Intel 24.1 LVDS data format). In order to enable this mode the DOTDAT[2:0] needs to be set to 6 in the SOR_NV_PDISP_SOR_CSTM_0 register.
Figure 8 shows the LVDS output signals for the 18-bit interface.

The NVIDIA Tegra K1 features only single-channel LVDS; dual-channel is not supported. The interface features a maximum pixel clock frequency of 165MHz and can be used for display panels up to 1920x1200 pixels @60Hz. Most of the displays above 1366x768 pixels @60 normally interface with dual-channel LVDS. Some displays allow changing to single-channel mode. If it is not supported by the display, a single-to-dual-channel circuit on the carrier board is needed.

Table 6-13 LVDS interface signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>248</td>
<td>LVDS1_A_CLK+</td>
<td>LVDS0_TXD4P</td>
<td>O</td>
<td>LVDS Clock out for channel A</td>
</tr>
<tr>
<td>246</td>
<td>LVDS1_A_CLK-</td>
<td>LVDS0_TXD4N</td>
<td>O</td>
<td>LVDS out for channel A</td>
</tr>
<tr>
<td>254</td>
<td>LVDS1_A_TX0+</td>
<td>LVDS0_TXD0P</td>
<td>O</td>
<td>LVDS data lane 0 for channel A</td>
</tr>
<tr>
<td>252</td>
<td>LVDS1_A_TX0-</td>
<td>LVDS0_TXD0N</td>
<td>O</td>
<td>LVDS data lane 0 for channel A</td>
</tr>
<tr>
<td>260</td>
<td>LVDS1_A_TX1+</td>
<td>LVDS0_TXD1P</td>
<td>O</td>
<td>LVDS data lane 1 for channel A</td>
</tr>
<tr>
<td>258</td>
<td>LVDS1_A_TX1-</td>
<td>LVDS0_TXD1N</td>
<td>O</td>
<td>LVDS data lane 1 for channel A</td>
</tr>
<tr>
<td>266</td>
<td>LVDS1_A_TX2+</td>
<td>LVDS0_TXD2P</td>
<td>O</td>
<td>LVDS data lane 2 for channel A</td>
</tr>
<tr>
<td>264</td>
<td>LVDS1_A_TX2-</td>
<td>LVDS0_TXD2N</td>
<td>O</td>
<td>LVDS data lane 2 for channel A</td>
</tr>
<tr>
<td>272</td>
<td>LVDS1_A_TX3+</td>
<td>LVDS0_TXD3P</td>
<td>O</td>
<td>LVDS data lane 3 for channel A</td>
</tr>
<tr>
<td>270</td>
<td>LVDS1_A_TX3-</td>
<td>LVDS0_TXD3N</td>
<td>O</td>
<td>LVDS data lane 3 for channel A</td>
</tr>
<tr>
<td>278</td>
<td>LVDS1_B_CLK+</td>
<td></td>
<td>O</td>
<td>LVDS Clock out for channel B</td>
</tr>
<tr>
<td>276</td>
<td>LVDS1_B_CLK-</td>
<td></td>
<td>O</td>
<td>LVDS Clock out for channel B</td>
</tr>
<tr>
<td>284</td>
<td>LVDS1_B_TX0+</td>
<td></td>
<td>O</td>
<td>LVDS data lane 0 for channel B</td>
</tr>
<tr>
<td>282</td>
<td>LVDS1_B_TX0-</td>
<td></td>
<td>O</td>
<td>LVDS data lane 0 for channel B</td>
</tr>
<tr>
<td>290</td>
<td>LVDS1_B_TX1+</td>
<td></td>
<td>O</td>
<td>LVDS data lane 1 for channel B</td>
</tr>
<tr>
<td>288</td>
<td>LVDS1_B_TX1-</td>
<td></td>
<td>O</td>
<td>LVDS data lane 1 for channel B</td>
</tr>
<tr>
<td>296</td>
<td>LVDS1_B_TX2+</td>
<td></td>
<td>O</td>
<td>LVDS data lane 2 for channel B</td>
</tr>
<tr>
<td>294</td>
<td>LVDS1_B_TX2-</td>
<td></td>
<td>O</td>
<td>LVDS data lane 2 for channel B</td>
</tr>
<tr>
<td>302</td>
<td>LVDS1_B_TX3+</td>
<td></td>
<td>O</td>
<td>LVDS data lane 3 for channel B</td>
</tr>
<tr>
<td>300</td>
<td>LVDS1_B_TX3-</td>
<td></td>
<td>O</td>
<td>LVDS data lane 3 for channel B</td>
</tr>
</tbody>
</table>
Table 6-14 Additional Display Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>239</td>
<td>BKL1_PWM</td>
<td>GPIO_PU6</td>
<td>PM3_PWM3</td>
<td>O</td>
<td>Backlight PWM for contrast or brightness control</td>
</tr>
<tr>
<td>286</td>
<td>BKL1_ON</td>
<td>GPIO_PBB5</td>
<td>GPIO3_PBB.05</td>
<td>O</td>
<td>Enable signal for the backlight</td>
</tr>
<tr>
<td>205</td>
<td>I2C2_SDA (DDC)</td>
<td>DDC_SDA</td>
<td>I2C4_DAT</td>
<td>I/O</td>
<td>I2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces</td>
</tr>
<tr>
<td>207</td>
<td>I2C2_SCL (DDC)</td>
<td>DDC_SCL</td>
<td>I2C4_CLK</td>
<td>O</td>
<td>I2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces</td>
</tr>
</tbody>
</table>

6.5.3 HDMI

HDMI provides a unified method of transferring both video and audio data over a TMDS compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI standard.

Features
- HDMI 1.4b up to 4096x2160@24Hz, 3840x2160@30Hz, or 1920x1080@120Hz (3D)
- Pixel Clock from 25.2MHz up to 300MHz
- Supports digital sound
- High-bandwidth Content Protection (HDCP, separate license needed)
- CEC interface

Table 6-15 HDMI Interface Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>240</td>
<td>HDMI1_TXC+</td>
<td>HDMI_TXCP</td>
<td>O</td>
<td>HDMI Differential Clock</td>
</tr>
<tr>
<td>242</td>
<td>HDMI1_TXC-</td>
<td>HDMI_TXCN</td>
<td>O</td>
<td>HDMI Differential Data</td>
</tr>
<tr>
<td>234</td>
<td>HDMI1_TXD0+</td>
<td>HDMI_TXD0P</td>
<td>O</td>
<td>HDMI Differential Data</td>
</tr>
<tr>
<td>236</td>
<td>HDMI1_TXD0-</td>
<td>HDMI_TXD0N</td>
<td>O</td>
<td>HDMI Differential Data</td>
</tr>
<tr>
<td>228</td>
<td>HDMI1_TXD1+</td>
<td>HDMI_TXD1P</td>
<td>O</td>
<td>HDMI Differential Data</td>
</tr>
<tr>
<td>230</td>
<td>HDMI1_TXD1-</td>
<td>HDMI_TXD1N</td>
<td>O</td>
<td>HDMI Differential Data</td>
</tr>
<tr>
<td>222</td>
<td>HDMI1_TXD2+</td>
<td>HDMI_TXD2P</td>
<td>O</td>
<td>HDMI Differential Data</td>
</tr>
<tr>
<td>224</td>
<td>HDMI1_TXD2-</td>
<td>HDMI_TXD2N</td>
<td>O</td>
<td>HDMI Differential Data</td>
</tr>
</tbody>
</table>

Table 6-16 Additional Display Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>220</td>
<td>HDMI1_CEC</td>
<td>HDMI_CEC</td>
<td>CEC</td>
<td>I/O</td>
<td>HDMI Consumer Electronic Control.</td>
</tr>
<tr>
<td>232</td>
<td>HDMI1_HPDP</td>
<td>HDMI_INT</td>
<td>GPIO3_PN.07</td>
<td>I</td>
<td>Hot Plug Detect</td>
</tr>
<tr>
<td>205</td>
<td>I2C2_SDA (DDC)</td>
<td>DDC_SDA</td>
<td>I2C4_DAT</td>
<td>I/O</td>
<td>Display Data Channel, shared with the other display interfaces</td>
</tr>
<tr>
<td>207</td>
<td>I2C2_SCL (DDC)</td>
<td>DDC_SCL</td>
<td>I2C4_CLK</td>
<td>O</td>
<td>Display Data Channel, shared with the other display interfaces</td>
</tr>
</tbody>
</table>
6.5.4  Analogue VGA

The Apalis TK1 does not feature an analogue VGA interface.

6.5.5  Embedded Display Port (eDP)

The LVDS interface pins of the Tegra K1 can be configured to be used as embedded Display Port interface. The eDP interface can be used for driving local displays, but not external Display Port (DP) monitors. The interface is not compatible with the Display Port standard for external displays.

Since the eDP interface is not part of the Apalis module specifications, it is not guaranteed that other Apalis modules also have the possibility to use the LVDS interface pins as eDP. Use this interface only if compatibility with other modules is not mandatory.

The eDP requires additional 10nF series capacitors to be placed in the data lines as well as the AUX channel. If the port is used as LVDS interface, the capacitors are not allowed. Filters (for example common mode chokes) are not recommended. Be aware of the different numbering of the data lanes if the LVDS interface is used as eDP port.

Features:

- 1, 2, and 4 lanes supported
- RBR, HBR, and HBR2 supported
- 18 or 24 bit color depth
- Pixel clock up to 450MHz
- Up to 3200x2000@60Hz (software limited for embedded devices)

The eDP signals are located as secondary function of the LVDS interface. Therefore, other Apalis modules will be compatible with this interface. The routing requirements of the eDP signals are different from the LVDS interface.

Table 6-17 eDP Signal Routing Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Frequency</td>
<td>1.62 Gb/s per lane (RBR)</td>
</tr>
<tr>
<td></td>
<td>2.7 Gb/s per lane (HBR)</td>
</tr>
<tr>
<td></td>
<td>5.4 Gb/s per lane (HBR2)</td>
</tr>
<tr>
<td>Configuration/Device Organisation</td>
<td>1 load</td>
</tr>
<tr>
<td>Reference Plane</td>
<td>GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)</td>
</tr>
<tr>
<td>Trace Impedance</td>
<td>90Ω ±15% differential; 50Ω ±15% single ended</td>
</tr>
<tr>
<td>Max Intra-pair Skew</td>
<td>&lt;1ps =150µm</td>
</tr>
<tr>
<td>Max Trace Length Skew between different data pairs</td>
<td>&lt;150ps =22.5mm</td>
</tr>
<tr>
<td>Max Trace Length from Module Connector</td>
<td>215mm (RBR and HBR)</td>
</tr>
<tr>
<td></td>
<td>127mm (HBR2)</td>
</tr>
</tbody>
</table>

The Apalis TK1 supports up to 4 lanes of embedded Display Port signals. The interface is backward compatible with one or two lane displays. Simply use only the lane 0 for a single lane display respectively lane 0 and 1 for a two lane display. The eDP requires a different voltage level of the AVD_LVDS0_PLL rail. The PMIC on the module allows to switch between 1.8V for LVDS (default) and 3.3V for eDP. Make sure the voltage is set correctly.
Table 6-18 eDP interface signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>eDP Signal Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>266</td>
<td>LVDS1_A_TX2+</td>
<td>LVDS0_TXD2P</td>
<td>eDP_1_D0+</td>
<td>O</td>
<td>Link Lane 0</td>
</tr>
<tr>
<td>264</td>
<td>LVDS1_A_TX2-</td>
<td>LVDS0_TXD2N</td>
<td>eDP_1_D0-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>260</td>
<td>LVDS1_A_TX1+</td>
<td>LVDS0_TXD1P</td>
<td>eDP_1_D1+</td>
<td>O</td>
<td>Link Lane 1</td>
</tr>
<tr>
<td>258</td>
<td>LVDS1_A_TX1-</td>
<td>LVDS0_TXD1N</td>
<td>eDP_1_D1-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>254</td>
<td>LVDS1_A_TX0+</td>
<td>LVDS0_TXD0P</td>
<td>eDP_1_D2+</td>
<td>O</td>
<td>Link Lane 2</td>
</tr>
<tr>
<td>252</td>
<td>LVDS1_A_TX0-</td>
<td>LVDS0_TXD0N</td>
<td>eDP_1_D2-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>248</td>
<td>LVDS1_A_CLK+</td>
<td>LVDS0_TXD4P</td>
<td>eDP_1_D3+</td>
<td>O</td>
<td>Link Lane 3</td>
</tr>
<tr>
<td>246</td>
<td>LVDS1_A_CLK-</td>
<td>LVDS0_TXD4N</td>
<td>eDP_1_D3-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>73</td>
<td>TS_DIFF3+</td>
<td>DP_AUX CH0_P</td>
<td>eDP_1_AUX CH0_P</td>
<td>I/O</td>
<td>Aux channel, contains control data such as EDID information</td>
</tr>
<tr>
<td>71</td>
<td>TS_DIFF3-</td>
<td>DP_AUX CH0_N</td>
<td>eDP_1_AUX CH0_N</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>GPIO2</td>
<td>DP_HPD</td>
<td>eDP_1_HPD</td>
<td>I</td>
<td>Hot plug detect</td>
</tr>
</tbody>
</table>

6.5.6 Display Serial Interface (DSI)

The Tegra K1 SoC supports two MIPI DSI interfaces to connect compatible displays. One port can be used with up to four data lanes, while the other is limited to maximum two lanes since not all signals are located on the module edge connector that are needed for quad lane mode. Each data lane is capable of up to 1.5Gbps data rate. Lane 1 of the interface is bidirectional (high-speed out, low power/speed in from display). The interface uses the MIPI D-PHY for the physical layer. The maximum supported resolution is 2560x1440@60Hz.

The DSI signals are located in the type-specific area of the Apalis module. Therefore, it is not guaranteed that other Apalis modules will be compatible with this interface. If you are planning on using the DSI interface, please be aware that other Apalis modules might not be compatible with your carrier board.

As the DSI is a high-speed interface, some additional layout requirements need to be met on the carrier board. These requirements are not detailed in the Apalis Carrier Board Design Guide as the interface is type specific.

Table 6-19 DSI Signal Routing Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Frequency</td>
<td>750MHz (1.5GT/S per data lane)</td>
</tr>
<tr>
<td>Configuration/Device Organisation</td>
<td>1 load</td>
</tr>
<tr>
<td>Reference Plane</td>
<td>GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)</td>
</tr>
<tr>
<td>Trace Impedance</td>
<td>90Ω ±15% differential; 50Ω ±15% single ended</td>
</tr>
<tr>
<td>Max Intra-pair Skew</td>
<td>&lt;1ps =150µm</td>
</tr>
<tr>
<td>Max Trace Length Skew between clock and data lanes</td>
<td>&lt;10ps =1.5mm</td>
</tr>
<tr>
<td>Max Trace Length from Module Connector</td>
<td>200mm</td>
</tr>
</tbody>
</table>
### Table 6-20 DSI interface signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>DSI Signal Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>127</td>
<td>TS_DIFF12+</td>
<td>DSI_B_CLK_P</td>
<td>DSI1_CLK+</td>
<td>O</td>
<td>DSI Interface 1 clock</td>
</tr>
<tr>
<td>125</td>
<td>TS_DIFF12-</td>
<td>DSI_B_CLK_N</td>
<td>DSI1_CLK-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>121</td>
<td>TS_DIFF11+</td>
<td>DSI_B_D0_P</td>
<td>DSI1_D1+</td>
<td>I/O</td>
<td>DSI Interface 1 data lane 1</td>
</tr>
<tr>
<td>119</td>
<td>TS_DIFF11-</td>
<td>DSI_B_D0_N</td>
<td>DSI1_D1-</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>115</td>
<td>TS_DIFF10+</td>
<td>DSI_B_D1_P</td>
<td>DSI1_D2+</td>
<td>O</td>
<td>DSI Interface 1 data lane 2</td>
</tr>
<tr>
<td>113</td>
<td>TS_DIFF10-</td>
<td>DSI_B_D1_N</td>
<td>DSI1_D2-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>109</td>
<td>TS_DIFF9+</td>
<td>DSI_B_D2_P</td>
<td>DSI1_D3+</td>
<td>O</td>
<td>DSI Interface 1 data lane 3</td>
</tr>
<tr>
<td>107</td>
<td>TS_DIFF9-</td>
<td>DSI_B_D2_N</td>
<td>DSI1_D3-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>103</td>
<td>TS_DIFF8+</td>
<td>DSI_B_D3_P</td>
<td>DSI1_D4+</td>
<td>O</td>
<td>DSI Interface 1 data lane 4</td>
</tr>
<tr>
<td>101</td>
<td>TS_DIFF8-</td>
<td>DSI_B_D3_N</td>
<td>DSI1_D4-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>TS_DIFF6+</td>
<td>DSI_A_CLK_P</td>
<td>DSI2_CLK+</td>
<td>O</td>
<td>DSI Interface 2 clock</td>
</tr>
<tr>
<td>89</td>
<td>TS_DIFF6-</td>
<td>DSI_A_CLK_N</td>
<td>DSI2_CLK-</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>TS_DIFF5+</td>
<td>DSI_A_D0_P</td>
<td>DSI2_D1+</td>
<td>I/O</td>
<td>DSI Interface 2 data lane 1</td>
</tr>
<tr>
<td>83</td>
<td>TS_DIFF5-</td>
<td>DSI_A_D0_N</td>
<td>DSI2_D1-</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>79</td>
<td>TS_DIFF4+</td>
<td>DSI_A_D1_P</td>
<td>DSI2_D2+</td>
<td>O</td>
<td>DSI Interface 2 data lane 2</td>
</tr>
<tr>
<td>77</td>
<td>TS_DIFF4-</td>
<td>DSI_A_D1_N</td>
<td>DSI2_D2-</td>
<td>O</td>
<td></td>
</tr>
</tbody>
</table>

### Table 6-21 Additional Display Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>239</td>
<td>BKL1_PWM</td>
<td>GPIO_PU6</td>
<td>PM3_PWM3</td>
<td>O</td>
<td>Backlight PWM for contrast or brightness control</td>
</tr>
<tr>
<td>286</td>
<td>BKL1_ON</td>
<td>GPIO_PBB5</td>
<td>GPIO3_PBB.05</td>
<td>O</td>
<td>Enable signal for the backlight</td>
</tr>
<tr>
<td>205</td>
<td>I2C2_SDA (DDC)</td>
<td>DDC_SDA</td>
<td>I2C4_DAT</td>
<td>I/O</td>
<td>I2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces</td>
</tr>
<tr>
<td>207</td>
<td>I2C2_SCL (DDC)</td>
<td>DDC_SCL</td>
<td>I2C4_CLK</td>
<td>O</td>
<td>I2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces</td>
</tr>
</tbody>
</table>
6.6  PCI Express

The Tegra K1 SoC features two PCI Express (PCIe) interfaces. One interface is available externally on the module edge connector. It is possible to use the interface with maximum two lanes. The other interface is used on the module for the Ethernet controller. Since it is possible to map the PCIe signals in different ways, it is also alternatively possible to use the second PCIe port externally as alternate functions of the USB 3.0 SuperSpeed signals of the USB_H4 port. The following table shows all possible PCIe signal mappings.

**Table 6-22 PCIe mapping options**

<table>
<thead>
<tr>
<th>Use Case</th>
<th>Lane 0</th>
<th>Lane 1</th>
<th>Lane 2</th>
<th>Lane 3</th>
<th>Lane 4</th>
<th>SATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>USB_H4</td>
<td>USB_O1</td>
<td>Ethernet</td>
<td>NA</td>
<td>PCIE_1</td>
<td>SATA_1</td>
</tr>
<tr>
<td>1</td>
<td>USB_H4</td>
<td>USB_O1</td>
<td>Ethernet</td>
<td>PCIE_1 L1</td>
<td>PCIE_1 L0</td>
<td>SATA_1</td>
</tr>
<tr>
<td>3</td>
<td>PCIE_2</td>
<td>USB_O1</td>
<td>NA</td>
<td>PCIE_1 L1</td>
<td>PCIE_1 L0</td>
<td>SATA_1</td>
</tr>
<tr>
<td>4</td>
<td>PCIE_2</td>
<td>NA</td>
<td>NA</td>
<td>PCIE_1 L1</td>
<td>PCIE_1 L0</td>
<td>USB_O1</td>
</tr>
</tbody>
</table>

The PCIe interface is compliant with the PCIe 2.0 specification and supports 5 Gb/s data rate. It is backward compatible with the PCIe 1.1 standard which supports 2.5 Gb/s. PCIe is a high speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

**Table 6-23 PCIe Interface Signals**

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>PCIe Signal Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>55</td>
<td>PCIE1_CLK+</td>
<td>PEX_CLK1P</td>
<td>PCIE1_CLK+</td>
<td></td>
<td>Reference clock differential pair</td>
</tr>
<tr>
<td>53</td>
<td>PCIE1_CLK-</td>
<td>PEX_CLK1N</td>
<td>PCIE1_CLK-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>PCIE1_TX+</td>
<td>PEX_TX4P</td>
<td>PCIE1_L0_TX+</td>
<td></td>
<td>Transmit data lane 0</td>
</tr>
<tr>
<td>47</td>
<td>PCIE1_TX-</td>
<td>PEX_TX4N</td>
<td>PCIE1_L0_TX-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>PCIE1_RX+</td>
<td>PEX_RX4P</td>
<td>PCIE1_L0_RX+</td>
<td></td>
<td>Receive data lane 0</td>
</tr>
<tr>
<td>41</td>
<td>PCIE1_RX-</td>
<td>PEX_RX4N</td>
<td>PCIE1_L0_RX-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>67</td>
<td>TS_DIFF2+</td>
<td>PEX_TX3P</td>
<td>PCIE1_L1_TX+</td>
<td></td>
<td>Transmit data lane 1, incompatible with other modules</td>
</tr>
<tr>
<td>65</td>
<td>TS_DIFF2-</td>
<td>PEX_TX3N</td>
<td>PCIE1_L1_TX-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>TS_DIFF1+</td>
<td>PEX_RX3P</td>
<td>PCIE1_L1_RX+</td>
<td></td>
<td>Receive data lane 1, incompatible with other modules</td>
</tr>
<tr>
<td>59</td>
<td>TS_DIFF1-</td>
<td>PEX_RX3N</td>
<td>PCIE1_L1_RX-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>106</td>
<td>USBH4_SSTX+</td>
<td>USB3_TX0P</td>
<td>PCIE2_L0_TX+</td>
<td></td>
<td>Transmit data, only available if Ethernet is unused, incompatible with other modules</td>
</tr>
<tr>
<td>104</td>
<td>USBH4_SSTX-</td>
<td>USB3_TX0N</td>
<td>PCIE2_L0_TX-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>94</td>
<td>USBH4_SSRX+</td>
<td>USB3_RX0P</td>
<td>PCIE2_L0_RX+</td>
<td></td>
<td>Receive data, only available if Ethernet is unused, incompatible with other modules</td>
</tr>
<tr>
<td>92</td>
<td>USBH4_SSRX-</td>
<td>USB3_RX0N</td>
<td>PCIE2_L0_RX-</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The second interface which is only usable if the Ethernet controller on the module is not in use does not feature a dedicated reference clock output. Use a zero delay clock distributor in order to generate a copy of the reference clock of the first Ethernet port (Pin 55/53).
Table 6-24 Additional PCIe Control Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>37</td>
<td>WAKE1_MICO</td>
<td>PEX_WAKE_N</td>
<td>pe_wake_I</td>
<td>I</td>
<td>General purpose wake signal</td>
</tr>
<tr>
<td>26</td>
<td>RESET_MOCI#</td>
<td></td>
<td></td>
<td>O</td>
<td>General reset output</td>
</tr>
<tr>
<td>209</td>
<td>I2C1_SDA</td>
<td>GEN1_I2C_SDA</td>
<td>I2C1_DAT</td>
<td>I/O</td>
<td>Some PCIe devices need the SMB interface for special configurations. I2C1 should be used if interface is necessary</td>
</tr>
<tr>
<td>211</td>
<td>I2C1_SCL</td>
<td>GEN1_I2C_SCL</td>
<td>I2C1_CLK</td>
<td>O</td>
<td></td>
</tr>
</tbody>
</table>

6.7 SATA

The Serial ATA (SATA) interface can be used to attach, for example, an external hard drive, SSD or an mSATA SSD. The interface is a single Gen 2 SATA link with a maximum transfer rate of 3 Gb/s. The interface is backward compatible with Gen 1 (1.5Gb/s). SATA is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 6-25 Apalis standard SATA Interface Signals (x1)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>33</td>
<td>SATA1_TX+</td>
<td>SATA_L0_TXP</td>
<td>O</td>
<td>SATA transmit data</td>
</tr>
<tr>
<td>31</td>
<td>SATA1_TX-</td>
<td>SATA_L0_TXN</td>
<td>O</td>
<td>Series decoupling capacitor are provided on the module</td>
</tr>
<tr>
<td>25</td>
<td>SATA1_RX+</td>
<td>SATA_L0_RXP</td>
<td>I</td>
<td>SATA receive data</td>
</tr>
<tr>
<td>27</td>
<td>SATA1_RX-</td>
<td>SATA_L0_RXN</td>
<td>I</td>
<td>Series decoupling capacitor are provided on the module</td>
</tr>
<tr>
<td>35</td>
<td>SATA1_ACT#</td>
<td>DAP1_DOUT</td>
<td>O</td>
<td>SATA activity indicator</td>
</tr>
</tbody>
</table>

6.8 I²C

The NVIDIA Tegra K1 offers up to six I²C controllers. They implement the I²C V3.0 specification. All of them can be used in either master or slave mode. The port I2C5 is used for power management and is not available externally. Port I2C1 is available as general purpose I²C on the module connector. Port I2C4 is intend to be used as DDC interface for the displays while port I2C3 is intended to be used in combination with the camera interface. Both I2C interfaces can also be used for other general purpose.

One of the additional two I²C interfaces of the K1 SoC is available as alternate function. The main purpose of this port (I2C6) is using it as embedded display port aux channel. Due to the output level shifter, the I2C2 interface cannot be used externally.

The TK1 I²C ports Features:
- Supports standard and fast mode of operation (0-400KHz), Fm+ (1Mbit/s) as well as high-speed mode (3.4 MHz).
- Independent Master Controller and Slave Controller
- Master supports clock stretching by the slave
- Supports one to eight-bytes burst data transfers
- 7-bit or 10-bit addressing
- Fully programmable 7-bit or 10-bit address for the slave
- Supports general call addressing
- Supports Recognition and Transfer of data to peripherals that do not send an acknowledgement
- Master supports packet based DMA
- Supports 4kByte of transfer in packet mode (can be extended by using multiple packets)
Table 6-26 I²C Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I²C Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>209</td>
<td>I²C1_SDA</td>
<td>GEN1_I²C_SDA</td>
<td>I²C1_DAT</td>
<td>I²C1</td>
<td>Generic I²C</td>
</tr>
<tr>
<td>211</td>
<td>I²C1_SCL</td>
<td>GEN1_I²C_SCL</td>
<td>I²C1_CLK</td>
<td>I²C1</td>
<td></td>
</tr>
<tr>
<td>205</td>
<td>I²C2_SDA (DDC)</td>
<td>DDC_SDA</td>
<td>I²C4_DAT</td>
<td>I²C4</td>
<td>I²C port for the camera interface, can also be used for other purpose</td>
</tr>
<tr>
<td>207</td>
<td>I²C2_SCL (DDC)</td>
<td>DDC_SCL</td>
<td>I²C4_CLK</td>
<td>I²C4</td>
<td></td>
</tr>
<tr>
<td>201</td>
<td>I²C3_SDA (CAM)</td>
<td>CAM_I²C_SDA</td>
<td>I²C3_DAT</td>
<td>I²C3</td>
<td>I²C port for the DDC interface, can also be used for other purpose</td>
</tr>
<tr>
<td>203</td>
<td>I²C3_SCL (CAM)</td>
<td>CAM_I²C_SCL</td>
<td>I²C3_CLK</td>
<td>I²C3</td>
<td></td>
</tr>
</tbody>
</table>

Table 6-27 Alternate TK1 I²C Signals (additional, not compatible with other Apalis family modules)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I²C Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71</td>
<td>TS_DIFF3-</td>
<td>DP_AUX_CH0_N</td>
<td>I²C6_DAT</td>
<td>I²C6</td>
<td>Aux channel for eDP</td>
</tr>
<tr>
<td>73</td>
<td>TS_DIFF3+</td>
<td>DP_AUX_CH0_P</td>
<td>I²C6_CLK</td>
<td>I²C6</td>
<td></td>
</tr>
</tbody>
</table>

Additional to the I²C interfaces that are provided by the main SoC, the companion MCU also features I²C interfaces. Please note that these I²C interfaces are not supported by the standard Linux BSP.

Table 6-28 Alternate K20 I²C Signals (additional, not compatible with other Apalis family modules)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I²C Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>251</td>
<td>LCD1_R0</td>
<td>PTD9</td>
<td></td>
<td>I²C0_SDA</td>
<td>Companion MCU I²C interface</td>
</tr>
<tr>
<td>307</td>
<td>AN1_ADC1</td>
<td>PTB1</td>
<td></td>
<td>I²C0_SDA</td>
<td></td>
</tr>
<tr>
<td>311</td>
<td>AN1_TSWIP_ADC3</td>
<td>PTB3</td>
<td></td>
<td>I²C0_SDA</td>
<td></td>
</tr>
<tr>
<td>253</td>
<td>LCD1_R1</td>
<td>PTD8</td>
<td></td>
<td>I²C0_SDA</td>
<td></td>
</tr>
<tr>
<td>305</td>
<td>AN1_ADC0</td>
<td>PTB0/ LLWU_P5</td>
<td></td>
<td>I²C0_SCL</td>
<td>Companion MCU I²C interface</td>
</tr>
<tr>
<td>309</td>
<td>AN1_ADC2</td>
<td>PTB2</td>
<td></td>
<td>I²C0_SDA</td>
<td></td>
</tr>
<tr>
<td>175</td>
<td>CAM1_D6</td>
<td>PTE0</td>
<td></td>
<td>I²C1_SDA</td>
<td>Companion MCU I²C interface</td>
</tr>
<tr>
<td>173</td>
<td>CAM1_D7</td>
<td>PTE1/ LLWU_P0</td>
<td></td>
<td>I²C1_SCL</td>
<td></td>
</tr>
</tbody>
</table>

6.8.1 Real-Team Clock (RTC) recommendation

The Apalis module features a RTC circuit which is located inside the Power Management IC (PMIC). The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for time keeping. As long as the main power supply is provided to the module, the RTC is sourced from this rail. If the RTC needs to be retained even without the module’s main voltage, a coin cell needs to be applied to the VCC_BACKUP (pin 174) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section 9.3). Therefore, a standard lithium coin cell battery can drain faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the I²C1 interface of the module and leave the VCC_BACKUP pin unconnected. A suitable reference schematic can be found in the schematic diagram of the Apalis evaluation board.
6.9 UART

The Apalis TK1 provides up to ten serial UART interfaces. Four of them are provided by the Nvidia Tegra K1 SoC and are available on dedicated UART pins as defined in the Apalis standard. The additional six UARTs are provided by the companion MCU. Please note that these six UART interfaces are not supported by the standard Linux BSP.

The Apalis UART1 (provided by the Tegra K1 UA3 interface) is according to the Apalis specification a full featured UART. Since the Tegra K1 does not feature the DTR, DSR, DCD, and RI signals, only RX/TX, as well as RTS/CTS is available. The UART1 is used as standard debug interface for the Toradex Linux operating systems. Therefore, it is desirable to keep this port accessible for system debugging.

 UART Features (TK1 signals only)
- Support 16450 and 16550 compatible modes
- 16 byte FIFO
- Up to 4.5 Mbaud
- Word length 5 to 8 bit, optional parity, one or two stop bits
- Auto sense baud detection

VFIR Features (TK1 signals only)
- Supports up to IrDA version 1.4 with 16Mbit/s
- 32bit x 16 deep FIFO

Table 6-29 UART1 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>118</td>
<td>UART1_RXD</td>
<td>GPIO_PU1</td>
<td>UA3_RXD</td>
<td>I</td>
<td>Received Data</td>
</tr>
<tr>
<td>112</td>
<td>UART1_TXD</td>
<td>GPIO_PU0</td>
<td>UA3_TXD</td>
<td>O</td>
<td>Transmitted Data</td>
</tr>
<tr>
<td>114</td>
<td>UART1_RTS</td>
<td>GPIO_PU3</td>
<td>UA3_RTS</td>
<td>O</td>
<td>Request to Send</td>
</tr>
<tr>
<td>116</td>
<td>UART1_CTS</td>
<td>GPIO_PU2</td>
<td>UA3_CTS</td>
<td>I</td>
<td>Clear to Send</td>
</tr>
<tr>
<td>110</td>
<td>UART1_DTR</td>
<td>UART3_RTS_N</td>
<td>GPIO3_PC.00</td>
<td>O</td>
<td>DTR function not available, only GPO</td>
</tr>
<tr>
<td>120</td>
<td>UART1_DSR</td>
<td>UART3_CTS_N</td>
<td>GPIO3_PA.01</td>
<td>I</td>
<td>CTS function not available, only GPI</td>
</tr>
<tr>
<td>122</td>
<td>UART1_RI</td>
<td>GPIO_PK7</td>
<td>GPIO3_PK.07</td>
<td>I</td>
<td>RI function not available, only GPI</td>
</tr>
<tr>
<td>124</td>
<td>UART1_DCD</td>
<td>GPIO_PB1</td>
<td>GPIO3_PB.01</td>
<td>I</td>
<td>DCD function not available, only GPI</td>
</tr>
</tbody>
</table>

Table 6-30 UART2 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>132</td>
<td>UART2_RXD</td>
<td>UART2_RXD</td>
<td>IR3_RXD</td>
<td>I</td>
<td>Received Data</td>
</tr>
<tr>
<td>126</td>
<td>UART2_TXD</td>
<td>UART2_TXD</td>
<td>IR3_TXD</td>
<td>O</td>
<td>Transmitted Data</td>
</tr>
<tr>
<td>128</td>
<td>UART2_RTS</td>
<td>UART2_RTS_N</td>
<td>UB3_RTS</td>
<td>O</td>
<td>Request to Send</td>
</tr>
<tr>
<td>130</td>
<td>UART2_CTS</td>
<td>UART2_CTS_N</td>
<td>UB3_CTS</td>
<td>I</td>
<td>Clear to Send</td>
</tr>
</tbody>
</table>

Table 6-31 UART3 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>136</td>
<td>UART3_RXD</td>
<td>UART3_RXD</td>
<td>UC3_RXD</td>
<td>I</td>
<td>Received Data</td>
</tr>
<tr>
<td>134</td>
<td>UART3_TXD</td>
<td>UART3_TXD</td>
<td>UC3_TXD</td>
<td>O</td>
<td>Transmitted Data</td>
</tr>
</tbody>
</table>
Table 6-32 UART4 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>140</td>
<td>UART4_RXD</td>
<td>GPIO_PB0</td>
<td>UD3_RXD</td>
<td>I</td>
<td>Received Data</td>
</tr>
<tr>
<td>138</td>
<td>UART4_TXD</td>
<td>GPIO_PJ7</td>
<td>UD3_TXD</td>
<td>O</td>
<td>Transmitted Data</td>
</tr>
</tbody>
</table>

For the UART3 and UART4 port, there are additional hardware flow signals available. These signals are located on the DTR, DSR, and DCD signals of the UART1 port. The signals are not compatible with other Apalis modules.

Table 6-33 Additional UART3 and UART4 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>110</td>
<td>UART1_DTR</td>
<td>UART3_RTS_N</td>
<td>UC3_RTS</td>
<td>O</td>
<td>Additional Request to Send for UART 3</td>
</tr>
<tr>
<td>120</td>
<td>UART1_DSR</td>
<td>UART3_CTS_N</td>
<td>UC3_CTS</td>
<td>I</td>
<td>Additional Clear to Send UART 3</td>
</tr>
<tr>
<td>124</td>
<td>UART1_DCD</td>
<td>GPIO_PB1</td>
<td>UD3_CTS</td>
<td>I</td>
<td>Additional Clear to Send UART 4</td>
</tr>
</tbody>
</table>

The Apalis TK1 UART pins are level shifted on the module. Therefore, it is recommended adding pull up or pull down resistors to the non-used input pins (UART1_RXD, UART1_CTS, UART1_DSR, UART1_RI, UART1_DCD, UART2_RXD, UART2_CTS, UART3_RXD, UART4_RXD) in order to make sure they are not floating. See also section 4.1.5. The output pins can be left floating.

In addition to the four UARTs of the Tegra K1 SoC, the Kinetis K20 companion MCU provides up to six UART interfaces. These UARTs are not compatible with other Apalis modules. Please note that these UARTs are not supported by the standard Linux BSP.

Table 6-34 Additional K20 UART Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>255</td>
<td>LCD1_R2</td>
<td>PTD6/ LLWU_P15</td>
<td>UART0_RX</td>
<td>I</td>
<td>Received Data</td>
</tr>
<tr>
<td>265</td>
<td>LCD1_R7</td>
<td>PTB16</td>
<td>UART0_TX</td>
<td>O</td>
<td>Transmitted Data</td>
</tr>
<tr>
<td>177</td>
<td>CAM1_D5</td>
<td>PTB17</td>
<td>UART0_RTS_b</td>
<td>O</td>
<td>Request to Send</td>
</tr>
<tr>
<td>243</td>
<td>LCD1_PCLK</td>
<td>PTD7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>187</td>
<td>CAM1_D0</td>
<td>PTA17</td>
<td>UART0_CTS_b/ UART0_COL_b</td>
<td>I</td>
<td>Clear to Send</td>
</tr>
<tr>
<td>197</td>
<td>CAM1_HSYNC</td>
<td>PTA3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>247</td>
<td>LCD1_HSYNC</td>
<td>PTD4/ LLWU_P14</td>
<td>UART0_RTS_b</td>
<td>O</td>
<td>Request to Send</td>
</tr>
<tr>
<td>309</td>
<td>AN1_ADC2</td>
<td>PTB2</td>
<td>UART0_CTS_b/ UART0_COL_b</td>
<td>I</td>
<td>Clear to Send</td>
</tr>
<tr>
<td>245</td>
<td>LCD1_VSYNC</td>
<td>PTD5</td>
<td>UART0_CTS_b/ UART0_COL_b</td>
<td>I</td>
<td>Clear to Send</td>
</tr>
<tr>
<td>311</td>
<td>AN1_TSWIP_ADC3</td>
<td>PTB3</td>
<td>UART0_CTS_b/ UART0_COL_b</td>
<td>I</td>
<td>Clear to Send</td>
</tr>
</tbody>
</table>
6.10 SPI

The Apalis module standard features two SPI ports. The signals of the two ports are provided by the NVIDIA Tegra K1 SoC. Since the corresponding Tegra pins are only 1.8V capable, level shifters are required on these pins. Therefore, the two main SPI interfaces can only be used as master since the signal direction is fixed.

The Tegra K1 features an additional SPI port (SPI3) that is available as an alternate function of the SD1 interface. Since these pins do not need a level shifter, this interface can be used as master as well as slave. Please note that this interface is not compatible with other Apalis modules.

A fourth SPI port (TK1: SPI2C) of the Tegra K1 SoC is used for the communication with the companion MCU (K20: SPI2). The SoC is the master in this communication interface while the MCU is the slave. More information on the interface between SoC and MCU can be found in section 5.

The SPI ports operate at up to 50 Mbps and provide full duplex, synchronous, serial communication between the Apalis module and internal or external peripheral devices. Each SPI port consists of four signals; clock, chip select (frame), data in, and data out. The third SPI port features some additional chip-select signals available as alternate function to support multiple peripherals.

Features:
- Up to 50 Mbps
- 32-bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable (SPI1 and SPI2 only Master)
- Simultaneous receive and transmit

Each SPI channel supports four different modes of the SPI protocol:
Table 6-35 SPI Modes

<table>
<thead>
<tr>
<th>SPI Mode</th>
<th>Clock Polarity</th>
<th>Clock Phase</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Clock is positive polarity and the data is latched on the positive edge of SCK</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Clock is positive polarity and the data is latched on the negative edge of SCK</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>Clock is negative polarity and the data is latched on the positive edge of SCK</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>Clock is negative polarity and the data is latched on the negative edge of SCK</td>
</tr>
</tbody>
</table>

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCD displays require configuration over SPI prior to being driven via the RGB or LVDS interface.

Table 6-36 Apalis SPI Port 1 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>225</td>
<td>SPI1_MOSI</td>
<td>ULPI_CLK</td>
<td>SPI1A_DOUT</td>
<td>O</td>
<td>Master Output, Slave Input</td>
</tr>
<tr>
<td>223</td>
<td>SPI1_MISO</td>
<td>ULPI_DIR</td>
<td>SPI1A_DIN</td>
<td>I</td>
<td>Master Input, Slave Output</td>
</tr>
<tr>
<td>227</td>
<td>SPI1_CS</td>
<td>ULPI_STP</td>
<td>SPI1A_CS0</td>
<td>O</td>
<td>Slave Select</td>
</tr>
<tr>
<td>221</td>
<td>SPI1_CLK</td>
<td>ULPI_NXT</td>
<td>SPI1A_SCK</td>
<td>O</td>
<td>Serial Clock</td>
</tr>
</tbody>
</table>

Table 6-37 Apalis SPI Port 2 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>231</td>
<td>SPI2_MOSI</td>
<td>GPIO_PG6</td>
<td>SPI4C_DOUT</td>
<td>O</td>
<td>Master Output, Slave Input</td>
</tr>
<tr>
<td>229</td>
<td>SPI2_MISO</td>
<td>GPIO_PG7</td>
<td>SPI4C_DIN</td>
<td>I</td>
<td>Master Input, Slave Output</td>
</tr>
<tr>
<td>233</td>
<td>SPI2_CS</td>
<td>GPIO_PI3</td>
<td>SPI4C_CS0</td>
<td>O</td>
<td>Slave Select</td>
</tr>
<tr>
<td>235</td>
<td>SPI2_CLK</td>
<td>GPIO_PG5</td>
<td>SPI4C_SCK</td>
<td>O</td>
<td>Serial Clock</td>
</tr>
</tbody>
</table>

The SPI1_MISO and SPI2_MISO input pins are level shifted on the module. Therefore, it is recommended adding pull up or pull down resistors if they are not used in order to make sure they are not floating. See also section 4.1.5. The rest of the SPI pins can be left floating.

Table 6-38 Additional TK1 SPI port, incompatible with other modules

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>188</td>
<td>SD1_D1</td>
<td>SDMMC3_DAT1</td>
<td>SPI3D_DOUT</td>
<td>O</td>
<td>Master Output, Slave Input</td>
</tr>
<tr>
<td>186</td>
<td>SD1_D0</td>
<td>SDMMC3_DAT0</td>
<td>SPI3D_DIN</td>
<td>I</td>
<td>Master Input, Slave Output</td>
</tr>
<tr>
<td>176</td>
<td>SD1_D2</td>
<td>SDMMC3_DAT2</td>
<td>SPI3D_CS0</td>
<td>I/O</td>
<td>Slave Select 0</td>
</tr>
<tr>
<td>178</td>
<td>SD1_D3</td>
<td>SDMMC3_DAT3</td>
<td>SPI3D_CS1</td>
<td>O</td>
<td>Slave Select 1</td>
</tr>
<tr>
<td>180</td>
<td>SD1_CMD</td>
<td>SDMMC3_CMD</td>
<td>SPI3D_CS2</td>
<td>O</td>
<td>Slave Select 2</td>
</tr>
<tr>
<td>184</td>
<td>SD1_CLK</td>
<td>SDMMC3_CLK</td>
<td>SPI3D_SCK</td>
<td>I/O</td>
<td>Serial Clock</td>
</tr>
</tbody>
</table>

Additional to the three SPI port that are provided by the main SoC, the companion MCU features also two SPI ports that can be used. Please note that these SPI ports are not supported by the standard Linux BSP.
### 6.11 PWM (Pulse Width Modulation)

The NVIDIA Tegra K1 features a four channel Pulse Width Modulator (PWM). The duty cycle has an 8-bit resolution (it can be set to a value between 0 and 255 in steps of 1/256). The maximum output frequency is 187.5 kHz.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights or servo motors.

The Apalis standard defines a fifth, dedicated PWM output for the display backlight. As the Tegra K1 features only four PWM controllers, the backlight PWM shares the Tegra K1 PM3_PWM3 output with the module edge connector pin 8 PWM4.

---

**Table 6-39 Additional K20 SPI port, not compatible with other modules**

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>273</td>
<td>LCD1_G2</td>
<td>PTD2/LLWU_P13</td>
<td>SPI0_SOUT</td>
<td>O</td>
<td>Master Output, Slave Input</td>
</tr>
<tr>
<td>275</td>
<td>LCD1_G3</td>
<td>PTC6/LLWU_P10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>187</td>
<td>CAM1_D0</td>
<td>PTA17</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>257</td>
<td>LCD1_R3</td>
<td>PTD3</td>
<td>SPI0_SIN</td>
<td>I</td>
<td>Master Input, Slave Output</td>
</tr>
<tr>
<td>259</td>
<td>LCD1_R4</td>
<td>PTC7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>249</td>
<td>LCD1_DE</td>
<td>PTC4/LLWU_P8</td>
<td>SPI0_PCS0</td>
<td>I/O</td>
<td>Slave Select 0</td>
</tr>
<tr>
<td>291</td>
<td>LCD1_B2</td>
<td>PTD0/LLWU_P12</td>
<td>SPI0_PCS1</td>
<td>O</td>
<td>Slave Select 1</td>
</tr>
<tr>
<td>247</td>
<td>LCD1_HSYNC</td>
<td>PTD4/LLWU_P14</td>
<td>SPI0_PCS2</td>
<td>O</td>
<td>Slave Select 2</td>
</tr>
<tr>
<td>261</td>
<td>LCD1_R5</td>
<td>PTC3/LLWU_P7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>245</td>
<td>LCD1_VSYNC</td>
<td>PTD5</td>
<td>SPI0_PCS3</td>
<td>O</td>
<td>Slave Select 3</td>
</tr>
<tr>
<td>277</td>
<td>LCD1_G4</td>
<td>PTC2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>255</td>
<td>LCD1_R2</td>
<td>PTD6/LLWU_P15</td>
<td>SPI0_SCK</td>
<td>I/O</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>293</td>
<td>LCD1_B3</td>
<td>PTC1/LLWU_P6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>263</td>
<td>LCD1_R6</td>
<td>PTC0</td>
<td>SPI1_PCS4</td>
<td>O</td>
<td>Slave Select 4</td>
</tr>
<tr>
<td>289</td>
<td>LCD1_B1</td>
<td>PTD1</td>
<td>SPI1_SCK</td>
<td>I/O</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>173</td>
<td>CAM1_D7</td>
<td>PTE1/LLWU_P0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>179</td>
<td>CAM1_D4</td>
<td>PTE3</td>
<td>SPI1_SOUT</td>
<td>O</td>
<td>Master Output, Slave Input</td>
</tr>
<tr>
<td>265</td>
<td>LCD1_R7</td>
<td>PTB16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>173</td>
<td>CAM1_D7</td>
<td>PTE1/LLWU_P0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>177</td>
<td>CAM1_D5</td>
<td>PTE17</td>
<td>SPI1_SIN</td>
<td>I</td>
<td>Master Input, Slave Output</td>
</tr>
<tr>
<td>179</td>
<td>CAM1_D4</td>
<td>PTE3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>185</td>
<td>CAM1_D1</td>
<td>PTE4/LLWU_P2</td>
<td>SPI1_PCS0</td>
<td>I/O</td>
<td>Slave Select 0</td>
</tr>
<tr>
<td>297</td>
<td>LCD1_B5</td>
<td>PTB10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>175</td>
<td>CAM1_D6</td>
<td>PTE0</td>
<td>SPI1_PCS1</td>
<td>O</td>
<td>Slave Select 1</td>
</tr>
<tr>
<td>181</td>
<td>CAM1_D3</td>
<td>PTE5</td>
<td>SPI1_PCS2</td>
<td>O</td>
<td>Slave Select 2</td>
</tr>
<tr>
<td>281</td>
<td>LCD1_G6</td>
<td>PTB11</td>
<td>SPI1_SCK</td>
<td>I/O</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>301</td>
<td>LCD1_B7</td>
<td>PTE2/LLWU_P1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 6-40 PWM Interface Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>PWM1</td>
<td>GPIO_PH0</td>
<td>PM3_PWM0</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PWM2</td>
<td>GPIO_PH1</td>
<td>PM3_PWM1</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PWM3</td>
<td>GPIO_PH2</td>
<td>PM3_PWM2</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>PWM4</td>
<td>GPIO_PH3</td>
<td>PM3_PWM3</td>
<td>O</td>
<td>Shared PWM output with BKL1_PWM</td>
</tr>
<tr>
<td>239</td>
<td>BKL1_PWM</td>
<td>GPIO_PU6</td>
<td>PM3_PWM3</td>
<td>O</td>
<td>Shared PWM output with PWM4</td>
</tr>
</tbody>
</table>

In addition to the four PWM channels provided by the main SoC, the companion MCU features three FlexTimers with totally 12 output channels. Each channel can be configured for input capture, output compare, or PWM mode. Please note that these FlexTimers are not supported by the standard Linux BSP.

Table 6-41 TK20 FlexTimer Signals (not compatible with other Apalis modules)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>197</td>
<td>CAM1_HSYNC</td>
<td>PTA3</td>
<td>FTM0_CH0</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 0</td>
</tr>
<tr>
<td>293</td>
<td>LCD1_B3</td>
<td>PTC1/LLWU_P6</td>
<td>FTM0_CH1</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 1</td>
</tr>
<tr>
<td>195</td>
<td>CAM1_VSYNC</td>
<td>PTA5</td>
<td>FTM0_CH2</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 2</td>
</tr>
<tr>
<td>261</td>
<td>LCD1_R5</td>
<td>PTC3/LLWU_P7</td>
<td>FTM0_CH3</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 3</td>
</tr>
<tr>
<td>249</td>
<td>LCD1_DE</td>
<td>PTC4/LLWU_P8</td>
<td>FTM0_CH4</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 4</td>
</tr>
<tr>
<td>247</td>
<td>LCD1_HSYNC</td>
<td>PTD4/LLWU_P14</td>
<td>FTM0_CH5</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 5</td>
</tr>
<tr>
<td>255</td>
<td>LCD1_R2</td>
<td>PTD6/LLWU_P15</td>
<td>FTM0_CH6</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 6</td>
</tr>
<tr>
<td>243</td>
<td>LCD1_PCLK</td>
<td>PTD7</td>
<td>FTM0_CH7</td>
<td>I/O</td>
<td>FlexTimer 0 Channel 7</td>
</tr>
<tr>
<td>14</td>
<td>CAN1_TX</td>
<td>PTA12</td>
<td>FTM1_CH0</td>
<td>I/O</td>
<td>FlexTimer 1 Channel 0</td>
</tr>
<tr>
<td>305</td>
<td>AN1_ADC0</td>
<td>PTB0/LLWU_P5</td>
<td>FTM1_CH1</td>
<td>I/O</td>
<td>FlexTimer 1 Channel 1</td>
</tr>
<tr>
<td>12</td>
<td>CAN1_RX</td>
<td>PTA13/LLWU_P4</td>
<td>FTM1_CH1</td>
<td>I/O</td>
<td>FlexTimer 1 Channel 1</td>
</tr>
<tr>
<td>307</td>
<td>AN1_ADC1</td>
<td>PTB1</td>
<td>FTM2_CH0</td>
<td>I/O</td>
<td>FlexTimer 2 Channel 0</td>
</tr>
<tr>
<td>295</td>
<td>LCD1_B4</td>
<td>PTB18</td>
<td>FTM2_CH1</td>
<td>I/O</td>
<td>FlexTimer 2 Channel 1</td>
</tr>
<tr>
<td>279</td>
<td>LCD1_G5</td>
<td>PTB19</td>
<td>FTM2_CH1</td>
<td>I/O</td>
<td>FlexTimer 2 Channel 1</td>
</tr>
</tbody>
</table>
6.12 OWR (One Wire)

The One Wire Controller (OWR) implements a device communications bus system that provides low-speed data, signalling, and power over a single wire. The OWR uses two signals for this - one for ground, and the other for power and data.

On the Apalis TK1, the one wire protocol is primarily intended for communication with battery controller chips. The OWR is multiplexed with the GPIO6 interface on the module and is not part of the Apalis module specification. Therefore the compatibility with other Apalis modules is not guaranteed.

Table 6-42 OWR Interface Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>GPIO6</td>
<td>OWR</td>
<td>OWR</td>
<td>I/O</td>
<td>Pay attention, second SoC pin (PEX_L1_RST_N) connected with MXM pin.</td>
</tr>
</tbody>
</table>

6.13 SD/MMC

The NVIDIA Tegra K1 provides 4 SDIO interfaces; one is used internally for the eMMC Flash and two are available on the module edge connector Pins. The fourth SD/MMC interface is neither available externally nor used internally. Even though in the Apalis standard, the eMMC interface is specified with 8 data pins, on the Apalis TK1, only a 4-bit interface can be used.

The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards, and eMMC devices. The controllers can act as both master and slave simultaneously.

Features
- Supports SD Memory Card Specification 4.0 (up to UHS-I, no UHS-II)
- Supports SDIO Card Specification Version 4.0 (up to UHS-I, no UHS-II)
- Supports MMC System Specification Version 4.51 (limited to 4-bit, no 8-bit)
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Support SPI mode
- Both interface supports 3.3V and 1.8V IO voltage mode (Apalis standard is only 3.3V)

<table>
<thead>
<tr>
<th>TK1 SDIO interface</th>
<th>Max Bus Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDMMC1</td>
<td>4-bit</td>
<td>Apalis Standard MMC1 interface, only 4 bit</td>
</tr>
<tr>
<td>SDMMC2</td>
<td>8-bit</td>
<td>Unused, not available externally</td>
</tr>
<tr>
<td>SDMMC3</td>
<td>4-bit</td>
<td>Apalis Standard SD1 interface</td>
</tr>
<tr>
<td>SDMMC4</td>
<td>8-bit</td>
<td>Connected to internal eMMC boot device. Not available at the module edge connector</td>
</tr>
</tbody>
</table>

According to the Apalis module specification, the IO voltage level of the SD/MMC interface supports only 3.3V logic level. Therefore, the SD interfaces are limited to default or high-speed mode; UHS-I modes are not supported. Nevertheless, the MMC1 interface (Tegra SDMMC1) as well as the SD1 interface (Tegra SDMMC3) are capable to switch independently to the 1.8V IO level. This allows using the interface in UHS-I mode with higher speed. Please note that this IO voltage level is not mandatory in the Apalis module specification and therefore other modules might not support this mode as well. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interfaces are used in the 1.8V mode, it is recommended to remove the pull up resistors on the carrier board. The Tegra features internal pull-up resistors which can be used instead.
### Bus Speed Mode Table

<table>
<thead>
<tr>
<th>Bus Speed Mode</th>
<th>Max. Clock Frequency</th>
<th>Max. Bus Speed</th>
<th>Signal Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default Speed</td>
<td>25 MHz</td>
<td>12.5 MByte/s</td>
<td>3.3V</td>
</tr>
<tr>
<td>High Speed</td>
<td>50 MHz</td>
<td>25 MByte/s</td>
<td>3.3V</td>
</tr>
<tr>
<td>SDR12</td>
<td>25 MHz</td>
<td>12.5 MByte/s</td>
<td>1.8V</td>
</tr>
<tr>
<td>SDR25</td>
<td>50 MHz</td>
<td>25 MByte/s</td>
<td>1.8V</td>
</tr>
<tr>
<td>DDR50</td>
<td>50 MHz</td>
<td>50 MByte/s</td>
<td>1.8V</td>
</tr>
<tr>
<td>SDR50</td>
<td>100 MHz</td>
<td>50 MByte/s</td>
<td>1.8V</td>
</tr>
<tr>
<td>SDR104</td>
<td>208 MHz</td>
<td>104 MByte/s</td>
<td>1.8V</td>
</tr>
</tbody>
</table>

The I/O voltage of one power block can be changed independently from the other block, but all signals of the corresponding block change their voltages together. The signals of the Apalis SD1 interface (TK1 function block SDMMC3) are located on one block while the signals of the Apalis MMC1 interface (TK1 function block SDMMC1) are on a different block. This means the SD1 and the MMC1 can change the I/O Voltage level independently. Since there are additional signals on each block that are not used for the interface, there will be other pins changing the voltage. Make sure that these pins are not used if the I/O voltages of the SD/MMC interfaces are changed. More information can be found in section 4. The following tables show all pins that are in the SDMMC1 and SDMMC3 power blocks:

#### Table 6-43 TK1 SDMMC1 Power Block Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>MMC1_CMD</td>
<td>SDMMC1_CMD</td>
<td></td>
</tr>
<tr>
<td>160</td>
<td>MMC1_D0</td>
<td>SDMMC1_DAT0</td>
<td></td>
</tr>
<tr>
<td>162</td>
<td>MMC1_D1</td>
<td>SDMMC1_DAT1</td>
<td></td>
</tr>
<tr>
<td>144</td>
<td>MMC1_D2</td>
<td>SDMMC1_DAT2</td>
<td></td>
</tr>
<tr>
<td>146</td>
<td>MMC1_D3</td>
<td>SDMMC1_DAT3</td>
<td></td>
</tr>
<tr>
<td>154</td>
<td>MMC1_CLK</td>
<td>SDMMC1_CLK</td>
<td></td>
</tr>
<tr>
<td>164</td>
<td>MMC1_CD#</td>
<td>SDMMC1_WP_N</td>
<td>Used as standard MMC1 interface</td>
</tr>
<tr>
<td>148</td>
<td>MMC1_D4</td>
<td>CLK2_REQ</td>
<td>Pay attention with this additional signals since they may not be used for MMC1 interface</td>
</tr>
<tr>
<td>152</td>
<td>MMC1_D5</td>
<td>CLK2_OUT</td>
<td></td>
</tr>
</tbody>
</table>

#### Table 6-44 TK1 SDMMC3 Power Block Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>SD1_CMD</td>
<td>SDMMC3_CMD</td>
<td></td>
</tr>
<tr>
<td>186</td>
<td>SD1_D0</td>
<td>SDMMC3_DAT0</td>
<td>Used as standard SD1 interface</td>
</tr>
<tr>
<td>188</td>
<td>SD1_D1</td>
<td>SDMMC3_DAT1</td>
<td></td>
</tr>
<tr>
<td>176</td>
<td>SD1_D2</td>
<td>SDMMC3_DAT2</td>
<td></td>
</tr>
<tr>
<td>178</td>
<td>SD1_D3</td>
<td>SDMMC3_DAT3</td>
<td></td>
</tr>
<tr>
<td>184</td>
<td>SD1_CLK</td>
<td>SDMMC3_CLK</td>
<td></td>
</tr>
<tr>
<td>156</td>
<td>MMC1_D6</td>
<td>SDMMC3_CLK_LB_IN</td>
<td>Pay attention with this additional signal since it may not be used for the SD1 interface</td>
</tr>
</tbody>
</table>

The I/O voltage of the Apalis SD1 interface (TK1 function block SDMMC3) is provided by the LDO6 output of the power management IC. The I/O voltage of the Apalis MMC1 interface (TK1 function block SDMMC1) is provided by the LDO1 output. The voltages are changed by setting the according LDO output voltage register of the PMIC.
### Table 6-45 Apalis MMC1 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>MMC1_CMD</td>
<td>SDMMC1_CMD</td>
<td>SDMMC1_CMD</td>
<td>I/O</td>
<td>Command</td>
</tr>
<tr>
<td>160</td>
<td>MMC1_D0</td>
<td>SDMMC1_DAT0</td>
<td>SDMMC1_DAT0</td>
<td>I/O</td>
<td>Serial Data 0</td>
</tr>
<tr>
<td>162</td>
<td>MMC1_D1</td>
<td>SDMMC1_DAT1</td>
<td>SDMMC1_DAT1</td>
<td>I/O</td>
<td>Serial Data 1</td>
</tr>
<tr>
<td>144</td>
<td>MMC1_D2</td>
<td>SDMMC1_DAT2</td>
<td>SDMMC1_DAT2</td>
<td>I/O</td>
<td>Serial Data 2</td>
</tr>
<tr>
<td>146</td>
<td>MMC1_D3</td>
<td>SDMMC1_DAT3</td>
<td>SDMMC1_DAT3</td>
<td>I/O</td>
<td>Serial Data 3</td>
</tr>
<tr>
<td>154</td>
<td>MMC1_CLK</td>
<td>SDMMC1_CLK</td>
<td>SDMMC1_CLK</td>
<td>O</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>164</td>
<td>MMC1_CD#</td>
<td>SDMMC1_WP_N</td>
<td>GPIO3_PV.03</td>
<td>I</td>
<td>Card Detect (standard GPIO)</td>
</tr>
</tbody>
</table>

### Table 6-46 Apalis SD1 Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>SD1_CMD</td>
<td>SDMMC3_CMD</td>
<td>SDMMC3_CMD</td>
<td>I/O</td>
<td>Command</td>
</tr>
<tr>
<td>186</td>
<td>SD1_D0</td>
<td>SDMMC3_DAT0</td>
<td>SDMMC3_DAT0</td>
<td>I/O</td>
<td>Serial Data 0</td>
</tr>
<tr>
<td>188</td>
<td>SD1_D1</td>
<td>SDMMC3_DAT1</td>
<td>SDMMC3_DAT1</td>
<td>I/O</td>
<td>Serial Data 1</td>
</tr>
<tr>
<td>176</td>
<td>SD1_D2</td>
<td>SDMMC3_DAT2</td>
<td>SDMMC3_DAT2</td>
<td>I/O</td>
<td>Serial Data 2</td>
</tr>
<tr>
<td>178</td>
<td>SD1_D3</td>
<td>SDMMC3_DAT3</td>
<td>SDMMC3_DAT3</td>
<td>I/O</td>
<td>Serial Data 3</td>
</tr>
<tr>
<td>184</td>
<td>SD1_CLK</td>
<td>SDMMC3_CLK</td>
<td>SDMMC3_CLK</td>
<td>O</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>190</td>
<td>SD1_CD#</td>
<td>SDMMC3_CD_N</td>
<td>GPIO3_PV.02</td>
<td>I</td>
<td>Card Detect (standard GPIO with input level shifter)</td>
</tr>
</tbody>
</table>

Additional to the two SD/MMC interfaces that are provided by the main SoC, the companion MCU features an additional SD/MMC interface. Please note that this interface is not supported by the standard Linux BSP.

### Table 6-47 Additional K20 SD/MMC Interface Signal Pins (not compatible with other modules)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>179</td>
<td>CAM1_D4</td>
<td>PTE3</td>
<td>SDHC0_CMD</td>
<td>I/O</td>
<td>Command</td>
</tr>
<tr>
<td>173</td>
<td>CAM1_D7</td>
<td>PTE1/ LLWU_P0</td>
<td>SDHC0_D0</td>
<td>I/O</td>
<td>Serial Data 0</td>
</tr>
<tr>
<td>175</td>
<td>CAM1_D6</td>
<td>PTE0</td>
<td>SDHC0_D1</td>
<td>I/O</td>
<td>Serial Data 1</td>
</tr>
<tr>
<td>181</td>
<td>CAM1_D3</td>
<td>PTE5</td>
<td>SDHC0_D2</td>
<td>I/O</td>
<td>Serial Data 2</td>
</tr>
<tr>
<td>185</td>
<td>CAM1_D1</td>
<td>PTE4/ LLWU_P2</td>
<td>SDHC0_D3</td>
<td>I/O</td>
<td>Serial Data 3</td>
</tr>
<tr>
<td>301</td>
<td>LCD1_B7</td>
<td>PTE2/ LLWU_P1</td>
<td>SDHC0_DCLK</td>
<td>O</td>
<td>Serial Clock</td>
</tr>
</tbody>
</table>
6.14 Analogue Audio

The Apalis TK1 offers analogue audio input and output channels. On the module, a NXP SGTL5000 chip handles the analogue audio interface. The SGTL5000 is connected over I2S (I2S2) with the NVIDIA Tegra K1. Please consult the NXP SGTL5000 datasheet for more information.

Table 6-48 Analogue Audio Interface Pins

<table>
<thead>
<tr>
<th>X1 Pin #</th>
<th>Apalis Signal Name</th>
<th>I/O</th>
<th>Description</th>
<th>Pin on the SGTL5000 (20pin QFN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>306</td>
<td>AAP1_MICIN</td>
<td>I/O</td>
<td>Analogue Input</td>
<td>Microphone input</td>
</tr>
<tr>
<td>310</td>
<td>AAP1_LIN_L</td>
<td>I/O</td>
<td>Analogue Input</td>
<td>Left Line Input</td>
</tr>
<tr>
<td>312</td>
<td>AAP1_LIN_R</td>
<td>I/O</td>
<td>Analogue Input</td>
<td>Right Line Input</td>
</tr>
<tr>
<td>316</td>
<td>AAP1_HP_L</td>
<td>I/O</td>
<td>Analogue Output</td>
<td>Headphone Left Output</td>
</tr>
<tr>
<td>318</td>
<td>AAP1_HP_R</td>
<td>I/O</td>
<td>Analogue Output</td>
<td>Headphone Right Output</td>
</tr>
</tbody>
</table>

6.15 Digital Audio

The Apalis module standard provides one digital audio interface. Even though other Apalis modules might support Intel® Audio Codec '97 (also known as AC'97 or AC97) or Intel® High Definition Audio (also known as HD Audio, HDA or Azalia), the Apalis TK1 supports only I2S (also known as Inter-IC Sound, Integrated Interchip Sound or IIS).

Depending on the used audio codec, the bit clock as well as the left-right-sync is sourced by the codec or by the processor. In order to be able to interface audio codecs of both variants, the Apalis TK1 module features bidirectional level shifters on these two signals. Please note, the direction of these two pins cannot be changed individually. Both pins are either inputs or outputs. The direction is controlled with the GPIO3_PS.03 of the SoC.

Table 6-49 Digital Audio Port Signals (compatible with other modules)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>202</td>
<td>DAP1_D_IN</td>
<td>DAP2_DIN</td>
<td>I2S1_SDATA_IN</td>
<td>I/O</td>
<td>Data Input to TK1 (input level shifter)</td>
</tr>
<tr>
<td>196</td>
<td>DAP1_D_OUT</td>
<td>DAP2_DOUT</td>
<td>I2S1_SDATA_OUT</td>
<td>I/O</td>
<td>Data Output from TK1 (output level shifter)</td>
</tr>
<tr>
<td>204</td>
<td>DAP1_SYNC</td>
<td>DAP2_FS</td>
<td>I2S1_LRCK</td>
<td>I/O</td>
<td>Field Select (bidirectional level shifter)</td>
</tr>
<tr>
<td>200</td>
<td>DAP1_BIT_CLK</td>
<td>DAP2_SCLK</td>
<td>I2S1_SCLK</td>
<td>I/O</td>
<td>Serial Clock (bidirectional level shifter)</td>
</tr>
<tr>
<td>194</td>
<td>DAP1_MCLK</td>
<td>CLK3_OUT</td>
<td>exterph3_clk</td>
<td>O</td>
<td>External Peripheral Clock (output level shifter)</td>
</tr>
<tr>
<td>198</td>
<td>DAP1_RESET#</td>
<td>GPIO_PBB3</td>
<td>GPIO3_PBB.03</td>
<td>O</td>
<td>Audio codec reset (normal GPO, output level shifter)</td>
</tr>
</tbody>
</table>

The DAP1_D_IN pin is level shifted on the module. Therefore, it is recommended adding a pull up or pull down resistor if the pin is not in use in order to make sure they are not floating. See also section 4.1.5. The rest of the digital audio pins can be left floating.
6.16 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard.

Features:

- Supports 5 data formats
  - 16-bit
  - 20-bit
  - 24-bit
  - Raw
  - 16-bit packed
- Supports “autolock” mode to automatically detect “spdifin” sample rate and lock onto the data stream.
- Supports override mode to provide a manual control to sample “spdifin” data stream.

Table 6-50 S/PDIF Data Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>215</td>
<td>SPDIF1_OUT</td>
<td>SPDIF_OUT</td>
<td>SPDIF_OUT</td>
<td>O</td>
<td>Serial data output</td>
</tr>
<tr>
<td>217</td>
<td>SPDIF1_IN</td>
<td>SPDIF_IN</td>
<td>SPDIF_IN</td>
<td>I</td>
<td>Serial data input</td>
</tr>
</tbody>
</table>

6.17 Touch Panel Interface

The Apalis TK1 offers a 4-wire resistive touch interface. The touch interface is implemented in the K20 companion MCU with a simple external circuit. The external circuit allows drawing more current than the standard GPIO of the K20 would allow. This is necessary since some resistive touch panel require higher current. The standard Linux BSP contains the support of the resistive touch panel interface.

Figure 9: External Circuit for Touch Panel Interface
Table 6-51 Touch Interface Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>315</td>
<td>AN1_TSPX</td>
<td>PTB6</td>
<td>ADC1_SE12</td>
<td>I</td>
<td>ADC input for X+ (ADC1_SE12)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PTE6</td>
<td>PTE6</td>
<td>O</td>
<td>FET gate driver (GPIO PTE6)</td>
</tr>
<tr>
<td>317</td>
<td>AN1_TSMX</td>
<td>PTB7</td>
<td>ADC1_SE13</td>
<td>I</td>
<td>ADC input for X- (ADC1_SE13)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PTB9</td>
<td>PTB9</td>
<td>O</td>
<td>FET gate driver (GPIO PTB9)</td>
</tr>
<tr>
<td>319</td>
<td>AN1_TSPY</td>
<td>PTC8</td>
<td>ADC1_SE4b/</td>
<td>I</td>
<td>ADC input for Y+ (ADC1_SE4b)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CMP0_IN2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>PTC5/ LLWU_P9</td>
<td>PTC5</td>
<td>O</td>
<td>FET gate driver (GPIO PTC5)</td>
</tr>
<tr>
<td>321</td>
<td>AN1_TSMY</td>
<td>PTC9</td>
<td>ADC1_SE5b/</td>
<td>I</td>
<td>ADC input for Y- (ADC1_SE5b)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CMP0_IN3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>PTC13</td>
<td>PTC13</td>
<td>O</td>
<td>FET gate driver (GPIO PTC13)</td>
</tr>
</tbody>
</table>

If the touch panel interface is unused, leave the pins unconnected and disable the driver. Connecting the pins to ground (especially TSPX and TSPY) while having the driver still enabled could cause a short circuit if the driver turns on the high side FET.

6.18 Analogue Inputs

The Apalis module standard features four dedicated pins for analogue inputs. These analogue inputs are read by the ADCs that are located in the Kinetis K20 companion MCU. The K20 features two ADC with totally up to 21 channels that are available at the module edge connector. Only four of these 21 channels are compatible with other Apalis modules, the other 17 channels are located as alternate functions of other pins. The standard Linux BSP supports the ADC inputs of the MCU.

Features
- Two independent converters
- 12-bit ADC
- 0 to 3.3V rail to rail
- Conversion rate up to 818 KS/s
- Input resistance typical 2kΩ

Table 6-52 Analogue Inputs Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>305</td>
<td>AN1_ADC0</td>
<td>PTB0/ LLWU_P5</td>
<td>ADC0_SEB/</td>
<td>I</td>
<td>Dedicated ADC input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ADC1_SEB/</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TSI0_GH0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>307</td>
<td>AN1_ADC1</td>
<td>PTB1</td>
<td>ADC0_SEB/</td>
<td>I</td>
<td>Dedicated ADC input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ADC1_SEB/</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TSI0_GH6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>309</td>
<td>AN1_ADC2</td>
<td>PTB2</td>
<td>ADC0_SE12/</td>
<td>I</td>
<td>Dedicated ADC input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TSI0_GH7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>311</td>
<td>AN1_TSWIP_ADC3</td>
<td>PTB3</td>
<td>ADC0_SE13/</td>
<td>I</td>
<td>Dedicated ADC input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TSI0_GH8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 6-53 Additional Analogue Inputs Pins (not compatible with other modules)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>315</td>
<td>AN1_TSPX</td>
<td>PTB6</td>
<td>ADC1_SE12</td>
<td>I</td>
<td>ADC input (primary used as touch interface)</td>
</tr>
<tr>
<td>317</td>
<td>AN1_TSMX</td>
<td>PTB7</td>
<td>ADC1_SE13</td>
<td>I</td>
<td>ADC input (primary used as touch interface)</td>
</tr>
<tr>
<td>319</td>
<td>AN1_TSPY</td>
<td>PTC8</td>
<td>ADC1_SE4b/CMP0_IN2</td>
<td>I</td>
<td>ADC input (primary used as touch interface)</td>
</tr>
<tr>
<td>321</td>
<td>AN1_TSMY</td>
<td>PTC9</td>
<td>ADC1_SE5b/CMP0_IN3</td>
<td>I</td>
<td>ADC input (primary used as touch interface)</td>
</tr>
<tr>
<td>277</td>
<td>LCD1_G4</td>
<td>PTC2</td>
<td>ADC0_SE4b/CMP1_IN0/TSl0_CH15</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>289</td>
<td>LCD1_B1</td>
<td>PTD1</td>
<td>ADC0_SE5b</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>245</td>
<td>LCD1_VSYNC</td>
<td>PTD5</td>
<td>ADC0_SE6b</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>255</td>
<td>LCD1_R2</td>
<td>PTD6/LLWU_P15</td>
<td>ADC0_SE7b</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>263</td>
<td>LCD1_R6</td>
<td>PTC0</td>
<td>ADC0_SE14/TSl0_CH13</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>293</td>
<td>LCD1_B3</td>
<td>PTC1/LLWU_P6</td>
<td>ADC0_SE15/TSl0_CH14</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>183</td>
<td>CAM1_D2</td>
<td>PTE24</td>
<td>ADC0_SE17</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>191</td>
<td>CAM1_PCLK</td>
<td>PTE25</td>
<td>ADC0_SE18</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>301</td>
<td>LCD1_B7</td>
<td>PTE2/LLWU_P1</td>
<td>ADC1_SE6a</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>179</td>
<td>CAM1_D4</td>
<td>PTE3</td>
<td>ADC1_SE7a</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>297</td>
<td>LCD1_B5</td>
<td>PTB10</td>
<td>ADC1_SE14</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>281</td>
<td>LCD1_G6</td>
<td>PTB11</td>
<td>ADC1_SE15</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
<tr>
<td>187</td>
<td>CAM1_D0</td>
<td>PTA17</td>
<td>ADC1_SE17</td>
<td>I</td>
<td>Additional ADC input</td>
</tr>
</tbody>
</table>

6.19 Camera Interface

Even though the Apalis module standard reserves dedicated pins for parallel camera inputs, the Apalis TK1 module does not feature such an interface. Nevertheless, the Apalis TK1 features up to three MIPI/CSI-2 compatible camera inputs. The interfaces use the MIPI D-PHY as physical layer.

The CSI signals are located in the type-specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules will be compatible with this interface. If you are planning to use the CSI interface, please be aware that other modules may not be compatible with your carrier board.

As the CSI is a high-speed interface, some additional layout requirements need to be followed on the carrier board. These requirements are not defined in the Apalis Carrier Board Design Guide as this interface is type specific. Please find the according information in the table below.
### Table 6-54 CSI Signal Routing Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Frequency</td>
<td>750MHz (1.5GT/S per data lane)</td>
</tr>
<tr>
<td>Configuration/Device Organisation</td>
<td>1 load</td>
</tr>
<tr>
<td>Reference Plane</td>
<td>GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)</td>
</tr>
<tr>
<td>Trace Impedance</td>
<td>90Ω ±15% differential; 50Ω ±15% single ended</td>
</tr>
<tr>
<td>Max Intra-Pair Skew</td>
<td>&lt;1ps ≈150µm</td>
</tr>
<tr>
<td>Max Trace Length Skew between clock and data lanes</td>
<td>&lt;10ps ≈1.5mm</td>
</tr>
<tr>
<td>Max Trace Length from Module Connector</td>
<td>200mm</td>
</tr>
</tbody>
</table>

### Table 6-55 CSI interface signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>CSI Signal Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>163</td>
<td>TS_DIFF18+</td>
<td>CSI_A_CLK_P</td>
<td>CSI1_CLK+</td>
<td>I</td>
<td>CSI interface 1 clock</td>
</tr>
<tr>
<td>161</td>
<td>TS_DIFF18-</td>
<td>CSI_A_CLK_N</td>
<td>CSI1_CLK-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>157</td>
<td>TS_DIFF17+</td>
<td>CSI_A_D0_P</td>
<td>CSI1_D1+</td>
<td>I/O</td>
<td>CSI interface 1 data lane 1</td>
</tr>
<tr>
<td>155</td>
<td>TS_DIFF17-</td>
<td>CSI_A_D0_N</td>
<td>CSI1_D1-</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>151</td>
<td>TS_DIFF16+</td>
<td>CSI_A_D1_P</td>
<td>CSI1_D2+</td>
<td>I</td>
<td>CSI interface 1 data lane 2</td>
</tr>
<tr>
<td>149</td>
<td>TS_DIFF16-</td>
<td>CSI_A_D1_N</td>
<td>CSI1_D2-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>145</td>
<td>TS_DIFF15+</td>
<td>CSI_B_D0_P</td>
<td>CSI1_D3+</td>
<td>I</td>
<td>CSI interface 1 data lane 3</td>
</tr>
<tr>
<td>143</td>
<td>TS_DIFF15-</td>
<td>CSI_B_D0_N</td>
<td>CSI1_D3-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>139</td>
<td>TS_DIFF14+</td>
<td>CSI_B_D1_P</td>
<td>CSI1_D4+</td>
<td>I</td>
<td>CSI interface 1 data lane 4</td>
</tr>
<tr>
<td>137</td>
<td>TS_DIFF14-</td>
<td>CSI_B_D1_N</td>
<td>CSI1_D4-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>133</td>
<td>TS_DIFF13+</td>
<td>CSI_E_CLK_P</td>
<td>CSI2_CLK+</td>
<td>I</td>
<td>CSI interface 2 clock</td>
</tr>
<tr>
<td>131</td>
<td>TS_DIFF13-</td>
<td>CSI_E_CLK_N</td>
<td>CSI2_CLK-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>97</td>
<td>TS_DIFF7+</td>
<td>CSI_E_D0_P</td>
<td>CSI2_D1+</td>
<td>I/O</td>
<td>CSI interface 2 data lane 1</td>
</tr>
<tr>
<td>95</td>
<td>TS_DIFF7-</td>
<td>CSI_E_D0_N</td>
<td>CSI2_D1-</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>127</td>
<td>TS_DIFF12+</td>
<td>DSI_B_CLK_P</td>
<td>CSI3_CLK+</td>
<td>I</td>
<td>CSI interface 3 clock</td>
</tr>
<tr>
<td>125</td>
<td>TS_DIFF12-</td>
<td>DSI_B_CLK_N</td>
<td>CSI3_CLK-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>121</td>
<td>TS_DIFF11+</td>
<td>DSI_B_D0_P</td>
<td>CSI3_D1+</td>
<td>I/O</td>
<td>CSI interface 3 data lane 1</td>
</tr>
<tr>
<td>119</td>
<td>TS_DIFF11-</td>
<td>DSI_B_D0_N</td>
<td>CSI3_D1-</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>115</td>
<td>TS_DIFF10+</td>
<td>DSI_B_D1_P</td>
<td>CSI3_D2+</td>
<td>I</td>
<td>CSI interface 3 data lane 2</td>
</tr>
<tr>
<td>113</td>
<td>TS_DIFF10-</td>
<td>DSI_B_D1_N</td>
<td>CSI3_D2-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>109</td>
<td>TS_DIFF9+</td>
<td>DSI_B_D2_P</td>
<td>CSI3_D3+</td>
<td>I</td>
<td>CSI interface 3 data lane 3</td>
</tr>
<tr>
<td>107</td>
<td>TS_DIFF9-</td>
<td>DSI_B_D2_N</td>
<td>CSI3_D3-</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>103</td>
<td>TS_DIFF8+</td>
<td>DSI_B_D3_P</td>
<td>CSI3_D4+</td>
<td>I</td>
<td>CSI interface 3 data lane 4</td>
</tr>
<tr>
<td>101</td>
<td>TS_DIFF8-</td>
<td>DSI_B_D3_N</td>
<td>CSI3_D4-</td>
<td>I</td>
<td></td>
</tr>
</tbody>
</table>
Table 6-56 Additional Camera Interface Signals (Apalis Standard)

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>193</td>
<td>CAM1_MCLK</td>
<td>CAM_MCLK</td>
<td>vimclk_alt3</td>
<td>O</td>
<td>Master clock output for camera</td>
</tr>
<tr>
<td>201</td>
<td>I2C3_SDA (CAM)</td>
<td>CAM_I2C_SDA</td>
<td>I2C3_DAT</td>
<td>I/O</td>
<td>Camera control I2C</td>
</tr>
<tr>
<td>203</td>
<td>I2C3_SCL (CAM)</td>
<td>CAM_I2C_SCL</td>
<td>I2C3_CLK</td>
<td>O</td>
<td>Camera control I2C</td>
</tr>
</tbody>
</table>

6.20 Clock Output

The Apalis TK1 provides up to four external clock outputs on the module edge connector. One output is dedicated for the camera interface while the other is dedicated for the digital audio interface. If the clock outputs are not required for those interfaces, they can also be used as general purpose clock outputs.

The on-module audio codec has its own master clock source (extperiph1_clk). This source is not shared with the externally available sources.

Table 6-57 Clock Output Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>TK1 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>194</td>
<td>DAP1_MCLK</td>
<td>CLK3_OUT</td>
<td>extperiph3_clk</td>
<td>O</td>
<td>Clock output for the digital audio interface, see section 0</td>
</tr>
<tr>
<td>193</td>
<td>CAM1_MCLK</td>
<td>CAM_MCLK</td>
<td>vimclk_alt3</td>
<td>O</td>
<td>Clock output for the parallel and serial camera interface, see section 6.19</td>
</tr>
</tbody>
</table>

Two additional clock outputs are located as alternate function of pins. One of these two additional clock signals is sourced by the companion MCU. Please be aware that the standard Linux BSP does not support the MCU clock output.

Table 6-58 Additional Clock Output Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1/K20 Ball Name</th>
<th>TK1/K20 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>152</td>
<td>MMC1_D5</td>
<td>CLK2_OUT</td>
<td>extperiph2_clk</td>
<td>O</td>
<td>Clock output, sourced by main SoC</td>
</tr>
<tr>
<td>261</td>
<td>LCD1_R5</td>
<td>PTC3/ LLWU_P7</td>
<td>CLKOUT</td>
<td>O</td>
<td>Clock output, sourced by companion MCU</td>
</tr>
</tbody>
</table>

The PCIe interface requires a 100MHz reference clock for all the peripherals and switches. The Apalis standard defines one differential pair for the reference clock. Zero delay clock buffers can be used if more than one reference clock sink is present on the carrier board.

Table 6-59 PCIe Reference clock Signals

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>TK1 Ball Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>55</td>
<td>PCIe1_CLK+</td>
<td>PEX_CLK1P</td>
<td>O</td>
<td>Apalis standard reference clock differential pair</td>
</tr>
<tr>
<td>53</td>
<td>PCIe1_CLK-</td>
<td>PEX_CLK1N</td>
<td>O</td>
<td></td>
</tr>
</tbody>
</table>
6.21 Keypad

The Apalis TK1 does not feature a dedicated keypad interface. However, you can use any free GPIOs to realize a matrix keypad interface.

6.22 Controller Area Network (CAN)

The two Flexible Controller Area Network (FlexCAN) interfaces are provided by the Kinetis K20 companion MCU. The CAN protocol complies with the CAN 2.0B specification. It supports both standard and extended message frames. The CAN interface is supported by the standard Linux BSP.

Features
- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of zero to eight bytes data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Timestamp based on 16-bit free running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 6-60 CAN Signal Pins

<table>
<thead>
<tr>
<th>X1 Pin#</th>
<th>Apalis Signal Name</th>
<th>K20 Ball Name</th>
<th>K20 Port Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>CAN1_TX</td>
<td>PTA12</td>
<td>CAN0_TX</td>
<td>O</td>
<td>CAN port 1 transmit pin</td>
</tr>
<tr>
<td>12</td>
<td>CAN1_RX</td>
<td>PTA13/LLWU_P4</td>
<td>CAN0_RX</td>
<td>I</td>
<td>CAN port 1 receive pin</td>
</tr>
<tr>
<td>18</td>
<td>CAN2_TX</td>
<td>PTC17</td>
<td>CAN1_TX</td>
<td>O</td>
<td>CAN port 2 transmit pin</td>
</tr>
<tr>
<td>16</td>
<td>CAN2_RX</td>
<td>PTC16</td>
<td>CAN1_RX</td>
<td>I</td>
<td>CAN port 2 receive pin</td>
</tr>
</tbody>
</table>
6.23 JTAG

The JTAG interface is not normally required for software development with the Apalis TK1. There is always the possibility of reprogramming the module using the Recovery Mode over USB. To flash the module in recovery mode and for debug reasons, it is strongly recommended that the USBO1 interface is accessible even if not needed in the production system. Additionally, UART1 should also be accessible.

The JTAG interface is located as test points on the bottom side of the module. The location is standardised by the Apalis specification. Please be aware, the reference voltage for the interface is 1.8V.

![Figure 10 JTAG test point location on bottom side of module](image-url)
7. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Apalis TK1 even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in the recovery mode, the USB01 interface is used to connect it to a host computer. You will find additional information at our Developer Centre (http://developer.toradex.com).

In order to enter recovery mode, the recovery mode pads need to be shorted during the initial power on or reset of the module. Figure 11 show the location of the pads that need to be shorted for entering the recovery mode.

It is also possible to enter the recovery mode by pulling down pin 63 of the module edge connector (TS_1) with a 1kΩ resistor while booting. This pin is located in the type-specific area. It is not guaranteed that other Apalis modules will be able to be placed into recovery mode in the same way.

![Figure 11 Location of recovery mode pads](image)
8. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document which can be downloaded on our website at:

http://docs.toradex.com/103358-apalis-tk1-errata.pdf
9. Technical Specifications

9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vmax_VCC</td>
<td>Main power supply</td>
<td>-0.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_AVCC</td>
<td>Analogue power supply</td>
<td>-0.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_VCC_BACKUP</td>
<td>RTC power supply</td>
<td>-0.5</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_IO_3.3V</td>
<td>TK1 IO pins with 3.3V logic level</td>
<td>-0.5</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_IO_1.8V_3.3V</td>
<td>TK1 IO pins with 1.8V/3.3V switchable logic level</td>
<td>-0.5</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_IO_3.3V_Tol</td>
<td>TK1 1.8V IO pins which are 3.3V tolerant</td>
<td>-0.5</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_IO_In_Shift</td>
<td>TK1 IO pins which feature a input level shifter</td>
<td>-0.5</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_IO_Bi_Shift</td>
<td>TK1 IO pins which feature a bidirectional level shifter</td>
<td>-0.5</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_IO_K20</td>
<td>IO pins of the K20 companion MCU</td>
<td>-0.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_AN1</td>
<td>ADC and touch analogue input</td>
<td>-0.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Vmax_USB01_VBUS</td>
<td>Input voltage at USBO1_VBUS</td>
<td>-0.5</td>
<td>6.0</td>
<td>V</td>
</tr>
</tbody>
</table>

9.2 Recommended Operation Conditions

Table 9-2 Recommended Operation Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Main power supply</td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>AVCC</td>
<td>Analogue power supply</td>
<td>3.0</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>VCC_BACKUP</td>
<td>RTC power supply</td>
<td>2.5</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
</tbody>
</table>

9.3 Electrical Characteristics

Table 9-3 Typical Power Consumption

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description (VCC = 3.3V)</th>
<th>Typical</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD_IDL</td>
<td>CPU idle</td>
<td>0.46</td>
<td>A</td>
</tr>
<tr>
<td>IDD_HIGHCPU</td>
<td>Maximal CPU Load, 3D-graphic test</td>
<td>3.3</td>
<td>A</td>
</tr>
<tr>
<td>IDD_HD</td>
<td>Full HD Video on HDMI (h.264 decoding, CPU full load)</td>
<td>2.02</td>
<td>A</td>
</tr>
<tr>
<td>IDD_SUSPEND</td>
<td>Module in Suspend State</td>
<td>TBD</td>
<td>mA</td>
</tr>
<tr>
<td>IDD_BACKUP</td>
<td>Current consumption of internal RTC</td>
<td>8.9</td>
<td>µA</td>
</tr>
</tbody>
</table>

These typical values are just for indication. The actual consumption varies between different modules and is temperature dependent. The current consumption can be higher than IDD_HIGHCPU, depending on the load of the GPU and the temperature.

9.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Apalis module. This specification can be found in the Apalis Carrier Board Design Guide.
9.5 Mechanical Characteristics

Figure 12 Mechanical dimensions of the Apalis module (top view)
Tolerance for all measures: +/- 0.1mm

Figure 13 Mechanical position of NVIDIA Tegra K1 SoC (top view)
Tolerance for all measures: +/- 0.1mm

9.5.1 Sockets for the Apalis Modules

The Apalis module uses the MXM3 (Mobile PCI-Express Module) edge connector. This connector is available from different manufacturers in different board-to-board stacking heights from 2.3mm to 11.1mm. Toradex recommends using the JAE MM70-314-310B1 which has a board-to-board height of 3.0mm. This stacking height allows using the MXM SnapLock system for easy fixing of the module to the carrier board.
A list of other MXM3 connector manufacturers is given below:

- Aces Connectors: http://www.acesconn.com/
- JAE (MM70 Series) http://jae-connectors.com/

### 9.6 Thermal Specification

The Apalis TK1 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust the operating frequency and voltage in response to the changes in workload and temperature. The Tegra K1 SoC features DVFS on the CPU, GPU, as well as the Core voltage. This allows the Apalis TK1 to deliver higher performance at lower average power consumption compared to other solutions. The Apalis TK1 modules come with 2 temperature sensors - one which measures the temperature of the CPU die and another on the Apalis PCB. In the event that the temperature of the Tegra K1 reaches the maximum permitted temperature limit, the system will automatically shut down.

Here are some general considerations for you to follow:

- It is generally advised to use a heat sink on the Apalis TK1
- If you need the full CPU/Graphics performance over a long period of time, we recommend well designing the whole heat dissipation solution of the system.
- Toradex provides a heatsink for the Apalis TK1. This solution can be used passively as well as in combination with a fan. The Apalis Heatsink Type 3 is compatible with the Apalis TK1. More information can be found here: [http://developer.toradex.com/products/apalis-heatsink](http://developer.toradex.com/products/apalis-heatsink)
- If you only use the peak performance for a short time period, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents.

In general, the more effective the thermal solution is, the more performance you can get out of the Apalis TK1 Module.

**Table 9-4.1.1 Thermal Specification**

<table>
<thead>
<tr>
<th>Module</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apalis TK1</td>
<td>Operating temperature range</td>
<td>-25</td>
<td>85¹</td>
<td>85²</td>
<td>°C</td>
</tr>
<tr>
<td>Apalis TK1</td>
<td>Storage Temperature (eMMC flash memory is the limiting device)</td>
<td>-40</td>
<td>85²</td>
<td>105²</td>
<td>°C</td>
</tr>
<tr>
<td>Apalis TK1</td>
<td>Junction temperature SoC (sensed from thermal diode)</td>
<td>-25</td>
<td>105²</td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>Apalis TK1</td>
<td>Thermal Resistance Junction-to-Ambient, TK1 only. (ΘJA)²</td>
<td></td>
<td>12.3</td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>Apalis TK1</td>
<td>Thermal Resistance Junction-to-Top of TK1 chip case. (ΨJCtop)²</td>
<td></td>
<td>0.02</td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

¹ Depending on cooling solution.
² A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

### 9.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: [http://www.toradex.com/support/product-compliance](http://www.toradex.com/support/product-compliance)
DISCLAIMER:

Copyright © Toradex AG. All rights reserved. All data is for information purposes only and not guaranteed for legal purposes. Information has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

Brand and product names are trademarks or registered trademarks of their respective owners. Specifications are subject to change without notice.