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Colibri Computer Module

Carrier Board Design Guide

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Purpose:	This document is a guideline for developing a carrier board that confirms to the specifications for the Colibri Computer Module

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28 Sept 2015	V1.1	Correct figure 3 and figure 4 in section 2.3.3 (positive and negative USB signals were swapped in schematics)
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1 Introduction

1.1 Overview

This document guides the development of a customized carrier board for the Colibri computer module. It describes the different interfaces and contains reference schematics. This document reflects only the standardized primary function of the Colibri modules. The alternative functions are not guaranteed to be compatible between different Colibri modules. These interfaces are described in the datasheet of each computer module. Some Colibri modules do not feature the complete set of standard interfaces. Therefore, it is strongly recommended to read the datasheets of the modules that are intended to be used with the carrier board.

Some of the Colibri computer module interfaces, such as High-Speed USB and Ethernet, require special layout considerations regarding trace impedance and length matching. Please carefully read the Toradex Layout Design Guide for additional information related to the routing of these interfaces.

1.2 Additional Documents

1.2.1 Layout Design Guide

This document contains layout requirement specifications for the high-speed signals and avoids problems related to the layout.

http://developer.toradex.com/carrier-board-design/carrier-board-design-guides

1.2.2 Colibri Module Datasheets

There is a datasheet available for every Colibri module. Amongst other things, this document describes the type-specific interfaces and the alternative function of the pins. Before starting the development of a customized carrier board, please check this document to determine whether the required interfaces are available on the selected modules.

https://www.toradex.com/computer-on-modules/colibri-arm-family

1.2.3 Toradex Developer Center

You can find a lot of additional information at the Toradex Developer Center, which is updated with the latest product support information regularly.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information is valid or relevant for the specific Colibri modules.

http://www.developer.toradex.com

1.2.4 Colibri Evaluation Board Schematics

We provide the complete schematics plus the Altium project file for the Colibri Evaluation Board for free. This is a great help when designing your own Carrier Board.

http://developer.toradex.com/products/colibri-evaluation-board

1.2.5 Pinout Designer

This is an interactive and helpful tool for configuring the pin muxing of the Colibri and Apalis modules. It can be beneficial in custom carrier board development for Toradex modules and for checking the compatibility of existing carrier boards with our modules.

http://developer.toradex.com/carrier-board-design/pinout-designer-tool

1.3 Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
AGND	Analog Ground - separate ground for analog signals
Auto-MDIX	Automatically Medium Dependent Interface Crossing - a PHY with Auto-MDIX it can detect whether RX and TX need to be crossed (MDI or MDIX)
CAD	Computer-Aided Design – in this document it is referred to PCB Layout tools
CAN	Controller Area Network - a bus that is manly used in the automotive and industrial environment
CDMA	Code Division Multiplex Access - abbreviation often used for a mobile phone standard for data communication
CEC	Consumer Electronic Control - HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel - interface for reading out the capability of a monitor. In this document DDC2B (based on I^2C) is always meant
DRC	Design Rule Check - a tool for checking whether all design rules are satisfied in a CAD tool
DSI	Display Serial Interface
DVI	Digital Visual Interface - digital signals are electrically compatible with HDMI
DVI-A	Digital Visual Interface Analog only - signals are compatible with VGA
DVI-D	Digital Visual Interface Digital only - signals are electrically compatible with HDMI
DVI-I	Digital Visual Interface Integrated - combines digital and analog video signals in one connector
EDA	Electronic Design Automation - software for schematic capture and PCB layout (CAD or ECAD)
EDID	Extended Display Identification Data - timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference - high-frequency disturbances
eMMC	Embedded Multi Media Card - flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge - high voltage spike or spark that can damage electrostatic- sensitive devices
FPD-Link	Flat Panel Display Link - high-speed serial interface for liquid crystal displays. In this document, it is also called the LVDS interface.
GBE	Gigabit Ethernet - Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GPIO	General Purpose Input/Output pin that can be configured to be either an input or output
GSM	Global System for Mobile Communications
HDA	High Definition Audio (HD Audio) - a digital audio interface between CPU and audio codec
HDCP	High-Bandwidth Digital Content Protection - copy protection system that is used by HDMI beside others
HDMI	High-Definition Multimedia Interface - combines audio and video signal for connecting monitors, TV sets or Projectors, electrical compatible with DVI-D
I^2C	Inter-Integrated Circuit - two-wire interface for connecting low-speed peripherals
I^2S	Integrated Interchip Sound - serial bus for connecting PCM audio data between two devices
IrDA	Infrared Data Association - infrared interface for connecting peripherals
JTAG	Joint Test Action Group - widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling - electrical interface standard that can transport very high-speed signals over twisted-pair cables. Many standard interfaces like PCIe or SATA use this interface standard.

Abbreviation	Explanation
	Since the first successful application was the Flat Panel Display Link, LVDS has become synonymous with this interface. In this document, the term LVDS is used for the FPD-Link interface.
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface - a physical interface between Ethernet PHY and cable connector
MDIX	Medium Dependent Interface Crossed - an MDI interface with crossed RX and TX interfaces
mini PCIe	PCI Express Mini Card - card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard - flash memory card
MSB	Most Significant Bit
mSATA	Mini-SATA - a standardized form factor for small solid-state drive, similar dimensions as mini PCIe
N/A	Not Available
N/C	Not Connected
OD	Open-Drain
OTG	USB On-The-Go - a USB host interface that can also act as a USB client when connected to another host interface
OWR	One Wire (1-Wire) - a low-speed interface that needs just one data wire plus ground
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect - parallel computer expansion bus for connecting peripherals
PCIe	PCI Express - high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation - digital representation of analog signals and a standard interface for digital audio
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC - integrated circuit that manages amongst others the power sequence of a system
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue - color channels in standard display interfaces
RJ45	Registered Jack - common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	Single-ended serial port interface
RS422	Differential signaling serial port interface - full-duplex
RS485	Differential signaling serial port interface - half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module - identifications card for CDMA phones and networks, an extension of the GSM SIM card
S/PDIF	Sony/Philips Digital Interconnect Format - optical or coaxial interface for audio signals
SATA	Serial ATA, high-speed differential signaling interface for hard drives and SSD
SD	Secure Digital - flash memory card
SDIO	Secure Digital Input Output - an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module - identification card for GSM phones
SMBus	System Management Bus (SMB) - a two-wire bus based on the I^2C specifications, used mainly in x86 design for system management.
SoC	System on a Chip - IC which integrates the main component of a computer on a single chip
SO-DIMM	Small Outline Dual Inline Memory Module - form factor for mobile RAM modules, the Colibri module uses the SO-DIMM (DDR, 2.5V variant) connector as the primary interface
SPI	Serial Peripheral Interface Bus - synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material - thermal conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling - serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode - diode that is used to protect interfaces against voltage spikes
UART	Universal Asynchronous Receiver/Transmitter - serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA, or similar interface can be achieved
USB	Universal Serial Bus - serial interface for internal and external peripherals
VCC	Positive supply voltage
VGA	Video Graphics Array - analog video interface for monitors

Table 1: Abbreviations

2 Interfaces

2.1 Architecture

2.1.1 Standard Interfaces

The Colibri module family's standard interfaces intend to provide electrical and functional compatibility between module family members. The table below shows an overview of the standard interfaces that are provided by a Colibri module. The "GPIO Capable" column indicates whether the assigned pins intend to be also used as GPIOs. "Yes" and "No" are self-Explanatory. "Optional" indicates that it may be possible for some modules, but not all.

The "Standard" column indicates the number of interfaces that the specification allows for the standard pinout. Customers should consult the datasheet for specific Colibri module variants to check which of the interfaces are available for that module.

Description	Standard	Note	GPIO Capable
4/5 Wire Resistive Touch	1	Touch wiper shared with analog input 4	No
Analog Inputs	4	Minimum 8-bit resolution, 0-3.3V nominal range	No
Analog Audio	1	Line in L&R, Microphone in, Headphone out L&R	No
Fast Ethernet	1		No
HDMI (TDMS)	1	Located on a dedicated FFC connector (availability depending on Module)	No
I2C	1	Additional dedicated DDC available on FFC connector	Yes
Parallel Camera	1	8-bit BT.656 (other modes may be available)	Yes
Parallel LCD	1	18-bit resolution (additional bits may be available)	Yes
Parallel Memory Bus	1	Supported bus width depends on Module	Optional
PWM	4		Yes
SDIO	1	4 bit	Yes
SPI	1		Yes
UART	3	1x Full Featured, 1x CTS/RTS, 1x RXD/TXD only	Yes
USB	2	1x shared host/client, 1x host only	No
VGA	1	Located on a dedicated FFC connector (availability depending on Module)	No

Table 2: Standard Interfaces

2.1.2 Interfaces on Alternative Functions

Many SoC pins can be used for more than one function. This allows the modules to provide many additional interfaces to the standard set. For example, in the Colibri standard, there is only one SPI interface listed. Nevertheless, some modules can provide up to 6 SPI interfaces.

Please note that there are a few restrictions on using the interfaces provided as alternative functions of the pins. There is limited compatibility between their availability at different modules. For a design to be compatible with a wide range of Colibri modules, it is recommended to use the standard interfaces mainly. The various pins can be used for only one function simultaneously.

The configuration of the alternative function interfaces can be pretty complex. Toradex provides a powerful tool that helps the development engineer to resolve pin muxing conflicts. The tool is called Pinout Designer. It reduces the complexity of this critical task. More information, including its download link, can be found here:
http://developer.toradex.com/carrier-board-design/pinout-designer-tool

The interfaces on the alternative functions are not described in this document since they differ between the modules. Information related to these functions can be found in the datasheets of the modules.

2.1.3 Pin Numbering

The diagrams in the figures below show the pin numbering schema on both sides of the module. The schema is equal to the JEDEC MO-224 DDR SO-DIMM standard. The odd pin numbers are located on the top side of the module.

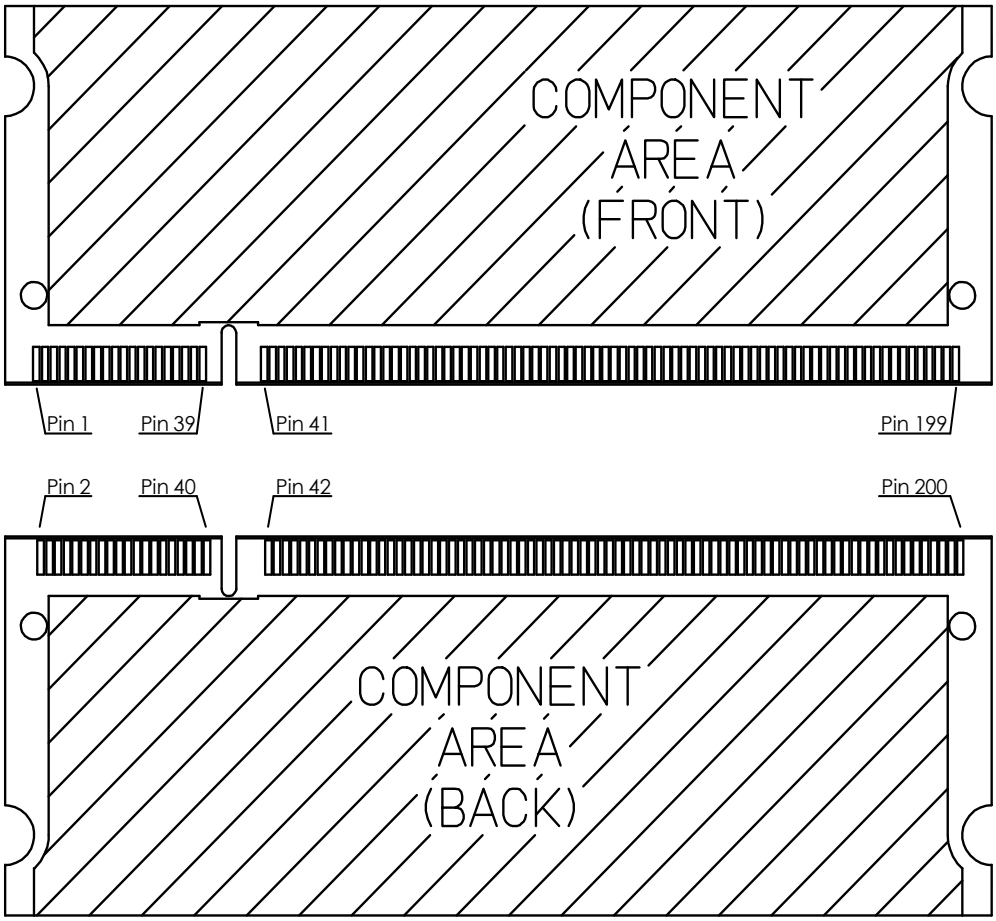

Figure 1: Colibri Module Pin Numbering Schema

2.1.4 Pin Reset State

The datasheets of the Colibri module provide information about the default reset status of the IO pins. Please be aware that the pin reset status is only guaranteed during the release of the reset signal. Some of the modules switch the IO bank voltages to follow the power-up sequence of the SoC. This means the IO pins can have an undefined state between applying the main power to the module until the nRESET_OUT is released. For carrier board designs that do not allow undefined pin states, it is recommended to ensure that the peripheral devices are not powered before the nRESET_OUT is released. Another solution can be gating the related IO signals with the nRESET_OUT signal.

2.2 Ethernet

The Colibri module standard features a fast 10/100Mbit Ethernet (10/100Base-TX) interface port. The required center tap circuit can differ between the modules. Different assembly options might be needed to support the complete Colibri module family. Some modules support Auto MDIX, which means they can swap the transmitting with the receiving lanes. Read the corresponding datasheet of the module for more information about the availability of the Auto MDIX function.

2.2.1 Ethernet Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
189	ETH_1_TXO+	I	Analog		100BASE-TX: Transmit + (Auto MDIX: Receive +)
187	ETH_1_TXO-	I	Analog		100BASE-TX: Transmit - (Auto MDIX: Receive -)
195	ETH_1_RXI+	O	Analog		100BASE-TX: Receive + (Auto MDIX: Transmit +)
193	ETH_1_RXI-	O	Analog		100BASE-TX: Receive - (Auto MDIX: Transmit -)
191	AGND_LAN				Ethernet ground, on some modules connected to common GND
183	ETH_1_LINK_AKT	O	CMOS	3.3V	LED indication output for link activity on the Ethernet port
185	ETH_1_SPEED100	O	CMOS	3.3V	LED indication output for 100Mbit/s

Table 3: Ethernet Signals

2.2.2 Reference Schematics

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care must be taken to route the signals between the magnetics and Ethernet connector.

The LED output signals ETH_1_LINK_AKT and ETH_1_SPEED100 can be connected directly to the LED of the Ethernet jack with suitable serial resistors. There is no need for additional buffering if the current drawn does not exceeds 10mA. However, the LED signals are prone to back feed to the module if the Ethernet PHY rails are powered off while the carrier board rails are still on. Therefore, decoupling the ETH_1_LINK_AKT and ETH_1_SPEED100 signals from the LEDs is recommended. The simplest solution is adding double-FET circuit buffers, as in the reference schematics below.

The Fast Ethernet interface uses the ETH_1_TXO as transmitting lanes and the ETH_1_RXI as receiving lane. If the Ethernet PHY features Auto-MDIX, the signal lanes RX and TX could be swapped. We strongly recommend not swapping the RX and TX lanes to keep the compatibility with all Colibri modules.

The required center tap circuit depends on the supported modules. Currently, the Ethernet controller on the PXA270 module is the only one that requires a different center tap circuit since it does not support Auto-MDIX. All the other currently available modules feature a current control PHY that requires a 3.3V supply at the center tap of the RX and TX lanes. Since all the Ethernet PHY manufacturers tend to change from current mode to voltage mode, which requires leaving the center tab pins of the magnetics unconnected, we recommend adding additional 0R resistors into the center tab lines. This ensures that the carrier board design is ready for any future Colibri module with voltage-mode PHY.

The magnetics provide a certain ESD protection which is sufficient for many designs. However, especially in Power over Ethernet (PoE) systems, additional transient voltage suppressor diodes (TVS) are highly recommended between the module and the magnetics. More information can be found in the following application note from Microchip:
http://ww1.microchip.com/downloads/en/AppNotes/00002157B.pdf

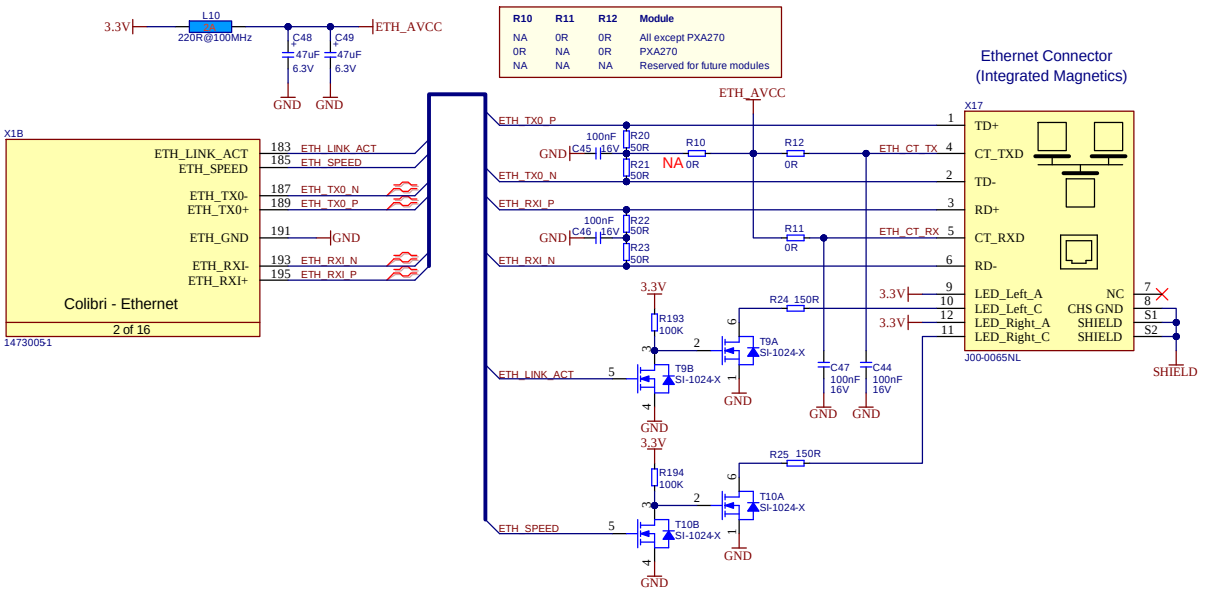

Figure 2: Fast Ethernet with Integrated Magnetics Reference Schematic

2.2.3 Capacitive Coupling of Ethernet Interface

A traditional Ethernet connection between a Colibri module and an Ethernet switch might look like this:

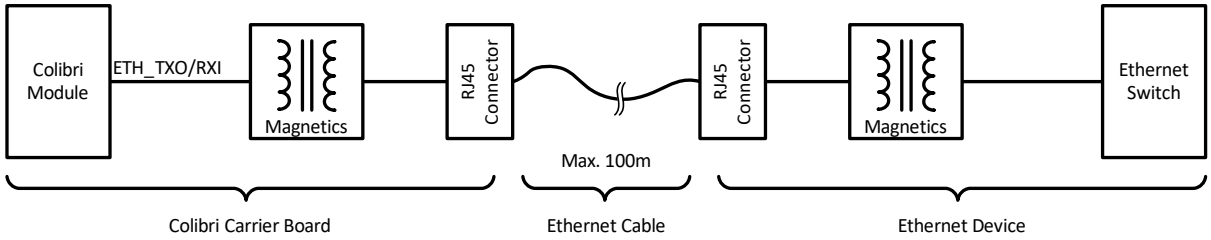

Figure 3: Regular Ethernet connection with magnetics

The media-dependent Ethernet signals from the Colibri module are routed on the carrier board to a transformer (magnetics) and the RJ45 (8P8C) connector. The magnetics might be integrated into the RJ45 connector, but the galvanic isolation with the transformer remains the same. 100BASE-TX Fast Ethernet allows for a cable of up to 100 m in length. The other side of the cable might be connected to an Ethernet switch. The PCB of the Ethernet switch also requires having galvanic insulating magnetics. The whole chain consists of two transformers that ensure the connection does not have any DC offset and is galvanic insulated.

The Ethernet interface is often used for connecting different devices inside a system. For example, the Ethernet connects different boards on a backplane system. In such systems, the connection between the two magnetics probably is shorter than 1 m and might not even be a cable. The two Ethernet ports might be connected using just traces on a backplane PCB.

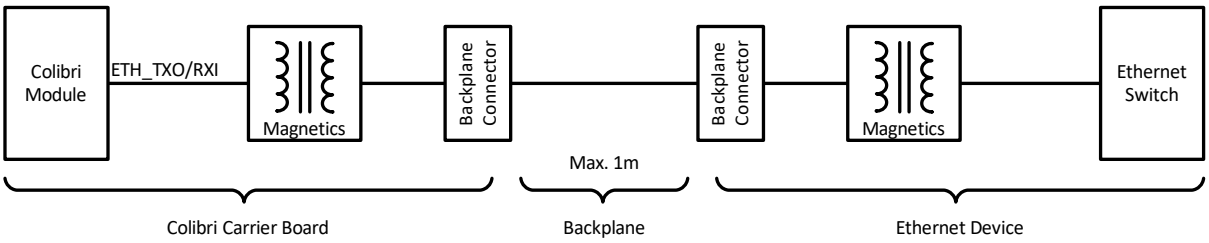

Figure 4: Backplane Ethernet connection with magnetics

It is possible to use the same magnetic transformers on both sides of the Ethernet connection. However, magnetics are relatively expensive components and consume significant space on the PCB. If the connection between the two Ethernet ports is relatively short (below 1 m), replacing the magnetic transformers with capacitors for capacitive coupling is possible.

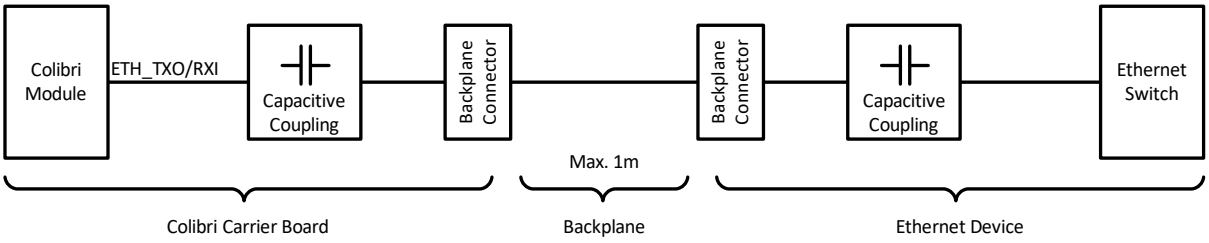

Figure 5: Backplane Ethernet connection with capacitive coupling

Combinations between capacitive coupling and magnetics are possible.

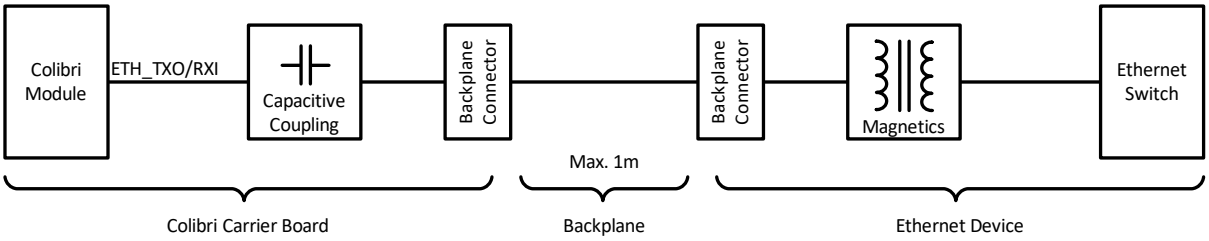

Figure 6: Backplane Ethernet connection with hybrid coupling

It is possible to reduce the coupling in a backplane system to a single capacitive coupling. This coupling could be on the backplane PCB.

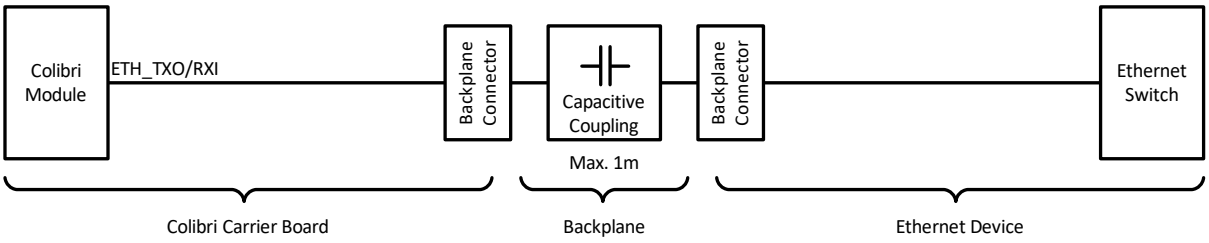

Figure 7: Backplane Ethernet connection with single capacitive coupling

Please note that the capacitive coupling does not provide galvanic isolation, as a continuous ground connection is required. The differential pair Ethernet signals are referenced to the ground plane on both sides of the capacitive coupling. The capacitive coupling only insulates DC offsets of the Ethernet signals. Therefore, capacitive coupling can only be used if both Ethernet ports use the same ground reference in the system and have relatively short connections. This is especially true if

both devices are on the same carrier board. Capacitive coupling is the preferred method for embedding an Ethernet switch directly on the Colibri carrier board.

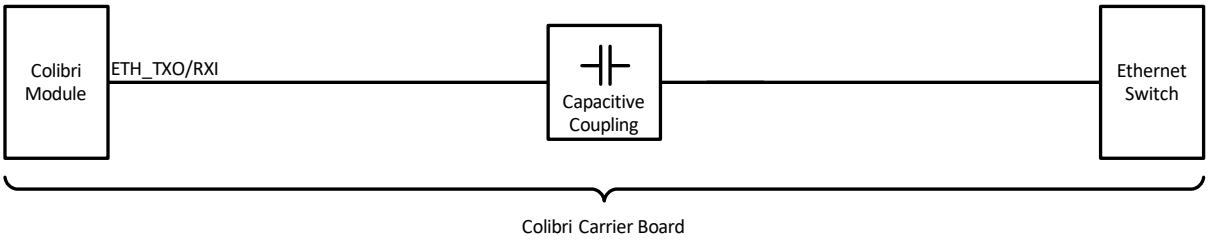

Figure 8: Capacitive coupling on Colibri Carrier Board

When implementing capacitive coupling, it is crucial to understand the type of Ethernet PHY used. Voltage-mode Ethernet PHY do not require any center tap voltage or termination. Voltage-mode PHYs can be connected directly to the series capacitors. 100nF is a good value.

The Colibri module on the other hand uses a current-mode PHY. This PHY requires a center tap voltage on the carrier board. With capacitive coupling, the center tap voltage must be injected using two 50Ω resistors.

Both ports need to be referenced to the same ground. All signals should be routed over the same ground reference. The capacitive coupling does not provide any galvanic isolation. It is essential to use non-polarized capacitors. The voltage across the capacitor will typically be ±3.3 V depending on the bias voltages of the PHYs. Therefore, a 16 V rated capacitor is a good solution.

The differential pair assignment can be optimized for the layout. Since the Colibri modules feature Auto MDI-X (except for the Colibri PXA270) the Ethernet differential pair signals can swap their role from RX to TX and vice versa. Therefore, the center tap voltage is required on both pairs and it does not matter which pair is connected to the lane 0 of the Verdin module.

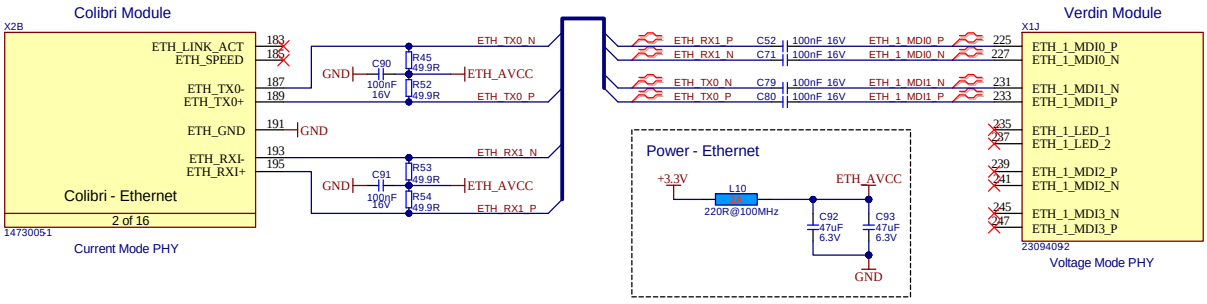

Figure 9: Reference schematic of capacitive coupling to a voltage-mode PHY

2.2.4 Unused Ethernet Signals Termination

All unused Ethernet signals can be left unconnected.

2.3 USB

The Colibri modules feature two USB interfaces. One of the two USB interfaces can be configured to be used as either the host or client. The other interface can only be used as a host. Some Colibri modules use the USB client port for debugging and recovery purposes. Therefore, it is recommended to have the interface accessible even for carrier board designs that do not need any USB ports.

2.3.1 USB Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
139	USB_H_DP	I/O	USB	3.3V	Positive Differential Signal for USB Host port
141	USB_H_DM	I/O	USB	3.3V	Negative Differential Signal for USB Host port
143	USB_C_DP	I/O	USB	3.3V	Positive Differential Signal for the shared USB Host / Client port
145	USB_C_DM	I/O	USB	3.3V	Negative Differential Signal for the shared USB Host / Client port

Table 4: USB Data Signals

If you use the USB Host function, you need to generate the 5V USB supply voltage on your carrier board. The Colibri modules provide two optional signals for USB power supply control (PWR_EN and OC). We recommend using the following pins to ensure the best possible compatibility. However, using these signals is not mandatory, and other GPIOs may be used instead.
In the USB client mode, an additional signal is required that detects whether the client is connected to a host interface (VBUS_DETECT). Please note that this pin is only 3.3V tolerant. Therefore, an additional logic level shifter (the simplest solution is a voltage divider) is required.

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
129	USB_H_PWR_EN	O	CMOS	3.3V	This pin enables the external USB voltage supply. By default, this pin is active low.
131	USB_H_OC	I	CMOS	3.3V	USB overcurrent, this pin can signal an overcurrent condition in the USB supply
137	USB_C_VBUS_DETECT	I	CMOS	3.3V	Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant

Table 5: USB Control Signals

2.3.2 USB-C

USB-C has initially also been known as USB Type-C. The term USB-C basically describes a 24-pin connector system that allows for an orientation-agnostic insertion of the plugs into the sockets (rotational symmetry). USB-C in itself does not denote any transfer speeds or special capabilities. On the other hand, the additional pins provided by USB-C may support additional features, such as USB Power Delivery or any Alternate Modes.

Before USB-C, the connector on the host side was typically a USB Type-A, while the client-side was typically a USB Type-B. If the port could act as both host and client (OTG), the jack was called USB Type-AB. In a fully adopted USB-C system, only one connector type is used, regardless of the role. If the port is used as a host, the term Downstream-Facing Port (DFP) should be used. The client-side port becomes an Upstream-Facing Port (UFP). With USB-C, the term OTG is no longer used to describe a port that can act as a host and a client. Such port is called Dual-Role Data (DRD) port instead.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBus	CC1	D+	D-	SBU1	VBus	RX2-	RX2+	GND
GND	RX1+	RX1-	VBus	SBU2	D-	D+	CC2	VBus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 10: USB-C connector pinout

The following table describes the USB-C pins. The "USB Type-A Cable" column indicates whether the signals are used in USB-C to USB Type-A cables. These cables require a 56kΩ pull-up resistor between the CC1 pin and the VBus to be compatible with the USB-C system.

USB-C Pin(s)	**USB-C** Signal Name	**USB Type-A Cable**	Description
A6, B6	D+	✓	USB 2.0 differential pair signals. There is only a single USB 2.0 differential pair in the cable. The B6/B7 pins are not connected inside the cable's plug. Both signal pairs must be connected to the USB-C receptacle to provide rotational symmetry.
A7, B7	D-	✓	
A2	TX1+	-	USB 3.x SuperSpeed differential pair signals. The Colibri standard does not feature any SuperSpeed signals. Therefore, these pins can be left unconnected. Some receptacles omit these pins. Besides offering a lower price, such receptacles are easier to fan out in the layout.
A3	TX1-	-	
B11	RX1+	-	
B10	RX1-	-	
B2	TX2+	-	
B3	TX2-	-	
A11	RX2+	-	
A10	RX2-	-	
A4, B9, A9, B4	VBus	✓	USB Bus power. In combination with the USB power delivery negotiation, a maximum of 20V/5A is possible.
A1, B12 A12, B1	GND	✓	Ground for power and signal return
A5	CC1	Resistor	Configuration channel. These pins have multiple functions. They are used for detecting the orientation of the connection. Either simple resistor combinations are used to detect the interface type, or the pins are used as a bus for negotiating the roles and power capabilities between the devices and the cable.
B5	CC2	-	
A8	SBU1	-	Sideband use. These signals are for alternate interface modes (for example, analog audio).
B8	SBU2	-	

Table 6: USB-C signals

The USB-C connector can be used in different modes. The connector can be used as a convenient replacement for Type-A (host) or Type-B (client) receptacles for Low, Full, and High Speed (USB 1.1/2.0) modes. In this case, only the following pins of the USB-C connector are used (mandatory pins are in black):

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBus	CC1	D+	D-	SBU1	VBus	RX2-	RX2+	GND
GND	RX1+	RX1-	VBus	SBU2	D-	D+	CC2	VBus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 11: USB-C connector pins used for USB 1.1/2.0

The USB cable only connects the High-Speed USB 2.0 signal cables on the pins A6 and A7. To ensure the cable can be plugged in both orientations, the receptacle needs to connect the USB 2.0 data signals to both pin pairs, the A6-A7 and B6-B7. The stubs are relatively short since these pins are located in the center. Therefore, no signal multiplexer is required. The configuration channel signals (CC1 and CC2) are used for detecting the plug orientation, the desired role, and the power negotiation. For many USB 2.0 applications, simple resistor circuits are sufficient for the configuration channel. For more information, please check the USB-C schematic examples.

2.3.2.1 USB-C Power Delivery

USB-C Power Delivery (PD) makes it possible to deliver up to 100W to a device by providing up to 5A at up to 20V. The power delivery feature of USB-C is also backward compatible with previous USB specifications. On a standard USB Type-A interface (without battery charging capabilities), it is possible to draw up to 2.5W (5V at 0.5A) in case of USB 2.0 and up to 4.5W (5V at 0.9A) in case of USB 3.0. For a USB-C power delivery-only interface, the following pins are required. It is possible to combine the power delivery with data interfaces. The following signals are required on the USB-C connector to provide for all potential power delivery methods.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBus	CC1	D+[1]	D-[1]	SBU1	VBus	RX2-	RX2+	GND
GND	RX1+	RX1-	VBus	SBU2	D-[1]	D+[1]	CC2	VBus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

[1] *the D+ and D- signals can be omitted if USB BC 1.2 and the default USB 3.x and 2.0 modes don't need to be supported*

Figure 12: USB-C connector pins used for power delivery

Depending on the role of the port, USB-C devices can either advertise or request different power modes. In the negotiation process, the system settles for the highest common power mode that also complies with the attached cable. The configuration channel signals (CC1 and CC2) are used for this negotiation. Either different resistor values are attached to the CC signals, or the configuration channel is used as a data bus.

Power Mode	CC Usage	Detection	Voltage	Maximum Current	Maximum Power
USB PD	Bus	Bus communication between DFP, UFP, and the cable	5-20 V	5 A	100 W
USB-C 5V/3A	10kΩ pull-up at DFP	UFP detects the pull-up resistor value at the CC pin	5 V	3 A	15 W
USB-C 5V/1.5A	22kΩ pull-up at DFP	UFP detects the pull-up resistor value at the CC pin	5 V	1.5 A	7.5 W
USB BC 1.2	56kΩ pull-up at DFP or in Type-A adapter cable	The host measures the resistance between the D+ and D- signals to detect the presence of the battery charger	5 V	1.5 A	7.5 W
Default USB 3.x	56kΩ pull-up at DFP or in Type-A adapter cable	USB enumeration is required over the D+ and D- signals (without enumeration, only 150 mA is allowed)	5 V	0.9 A	4.5 W
Default USB 2.0	56kΩ pull-up at DFP or in Type-A adapter cable	USB enumeration is required over the D+ and D- signals (without enumeration, only 100 mA is allowed)	5 V	0.5 A	2.5 W

Table 7: USB-C power modes

In the USB-C Power Delivery mode (USB PD), the device providing the power is referred to as the source (DFP), while the one receiving the power is called the sink (UFP). One CC signal is used for data, while the other one provides 5V (up to 1W) as VCONN. This voltage is used to power the USB PD negotiation devices (including active cables with an embedded marker IC). The VCONN is not to be confused with the VBus, which is the bus power that carries the USB-C connection's

actual power. The USB PD protocol is used for negotiating the voltage and the maximum current the source can provide, the sink requires, and the cable can handle. Using USB PD with a legacy USB Type-A to USB-C cable is impossible. For USB-C PD to function, a fully compliant USB-C cable connection is required.

The USB-C 5V/3A and 5V/1.5A modes also require a fully compliant USB-C connection. Adapters with USB Type-A or Type-B connectors will not work since they do not conduct the CC signals between the DFP and the UFP. These modes use different pull-up values at the CC signals for detecting the capabilities. No data communication is performed on the CC signals. This simplifies the implementation. All USB-C PD devices (UFP, DFP, and DRP) also need to support the resistor detection solution. One of the drawbacks of this solution is that bus voltages other than 5V are not feasible.

If the pull-up resistor at the CC line is 56kΩ, the USB port runs in one of the legacy modes. The pull-up resistor is either located at the USB-C source (DFP) or inside the cable (if a Type-A to USB-C cable is used).

The USB Battery Charger standard (BC 1.2) is a legacy mode introduced for detecting wall chargers with USB Type-A connectors at their output. They are still widely used for mobile phones having either a USB Micro-B or USB-C receptacle. In the BC 1.2 standard, the charger (source/DFP) places a resistance smaller than 200Ω across the D+ and D- signals of the USB 2.0 signals. The device (sink/UFP) detects this resistance, and it is allowed to draw up to 7.5W (1.5A at 5V) without enumerating on the USB bus (while observing the voltage).

The BC 1.2 mode is not mandatory in the USB-C specifications. Some sources (DFP) may not support it, and some sinks (UFP) may not be able to detect it. In this case, they fall back to the standard USB 2.0 or 3.x power delivery modes. In this case, the client needs to get enumerated by the host and ask for the current it requires (up to 0.9A for USB 3.x). The host can either accept or decline this power request (depending on the available power budget). If the request was declined or the sink (UFP) did not get enumerated, then it is allowed to draw 100mA (USB 2.0) or 150mA (USB 3.x) only.

2.3.3 Reference Schematics

The USB ports of the Colibri module can be used in many ways. The following table provides an overview of this design guide's different reference schematics.

Section	Title	Role Capability	Connector Type
2.3.3.1	USB High-Speed OTG (With Type Micro-AB Connector)	OTG / Client and Host	Micro-AB
2.3.3.2.1	USB-C High-Speed Downstream-Facing-Only (With Type-C Connector)	DFP / Host	USB-C
2.3.3.2.2	USB High-Speed Host-Only (With Type-A Connector)	Host	Type-A
2.3.3.3.1	USB-C High-Speed Upstream-Facing-Only (With Type-C Connector)	UFP / Client	USB-C
0	USB High-Speed Client-Only (With Type-B Connector)	Client	Type-B

Table 8: USB Reference Schematics Overview

2.3.3.1 USB High-Speed OTG (With Type Micro-AB Connector)

The Colibri standard does not support the full USB OTG function. However, it is possible to implement a circuit on the carrier board that allows changing the role from host to client depending on the level of the ID pin of a Micro-AB jack. The reference schematic differs from other USB OTG solutions since the module itself does not directly use the ID pin to detect whether the port is supposed to be set in client or host mode. The pin is indirectly used.

If no cable is plugged into the Micro-AB jack, the port is configured to host mode, and the 5V power output (VCC_USB2 in the schematic below) is disabled. If a Micro-B is plugged in (ID pin is floating on such plugs), the VCC_USB2 comes from the cable since the system gets plugged into a host. With the help of the voltage divider, the USB_C_DET signal gets around 3.3V. This signalizes to the module that it has been connected to a host and needs to switch to client mode.

The ID pin gets shorted to the ground if a Micro-A connector is inserted. This ID pin enables the output of the TPS2042 power switch. This voltage on the VCC_USB2 rail is used to power any client device connected to the port. Additionally, the ID pin keeps the USB_C_DET signal low over a diode, even though the VCC_USB2 rail goes to 5V. This ensures the module remains in host mode to communicate with the client device that is plugged in.

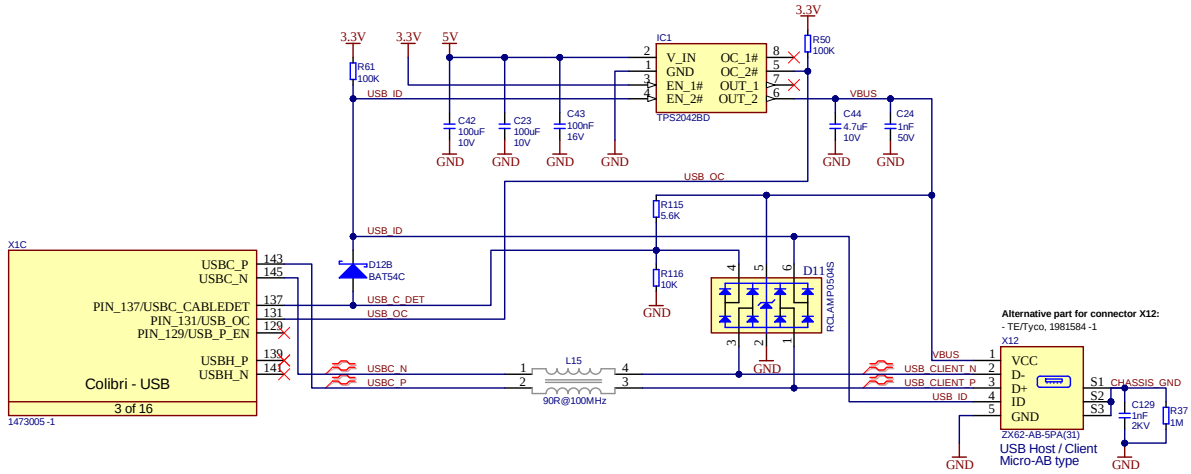

Figure 13: USB 2.0 OTG (with Type Micro-AB connector) reference schematic

2.3.3.2 Downstream-Facing / Host-Only

2.3.3.2.1 USB-C High-Speed Downstream-Facing-Only (With Type-C Connector)

A Downstream Facing Port (DFP) is a USB-C port that can act only as a host. The USB_H port of the Colibri module is intended to be used as a host port. However, it would be possible to implement a DFP interface also with the USB_C port of the Colibri module.

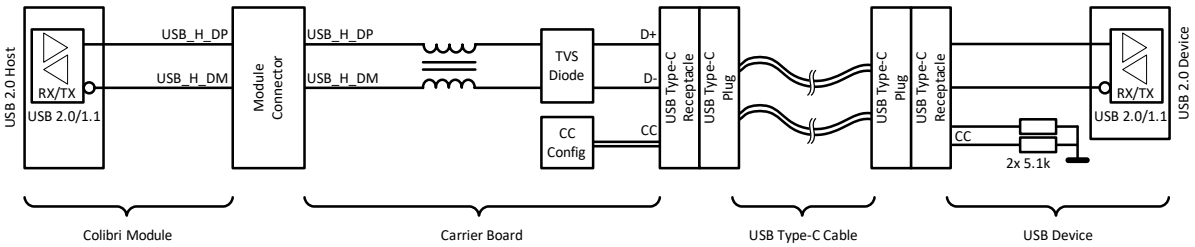

Figure 14: USB-C High-Speed DFP-Only (with Type-C connector) block diagram

The CC pins serve multiple purposes on a Type-C connector. They are used to detect the connector's orientation in the receptacle, negotiate the power delivery parameters (voltage and current), and negotiate the device's role. Even though the connector orientation information is not required in this example, and the role is fixed, a port control IC is still recommended for the power negotiation. The TUSB321 is a suitable option for this purpose. The TUSB321 can be strapped to announce different current levels to the device. The over-current protection IC on the carrier board needs to be set to a level that complies with the announced current.

The USB 2.0 signals are in the center of the USB Type-C connector. Therefore, the signals of the connector's top and bottom sides can be connected without the risk of creating stubs with a significant length.

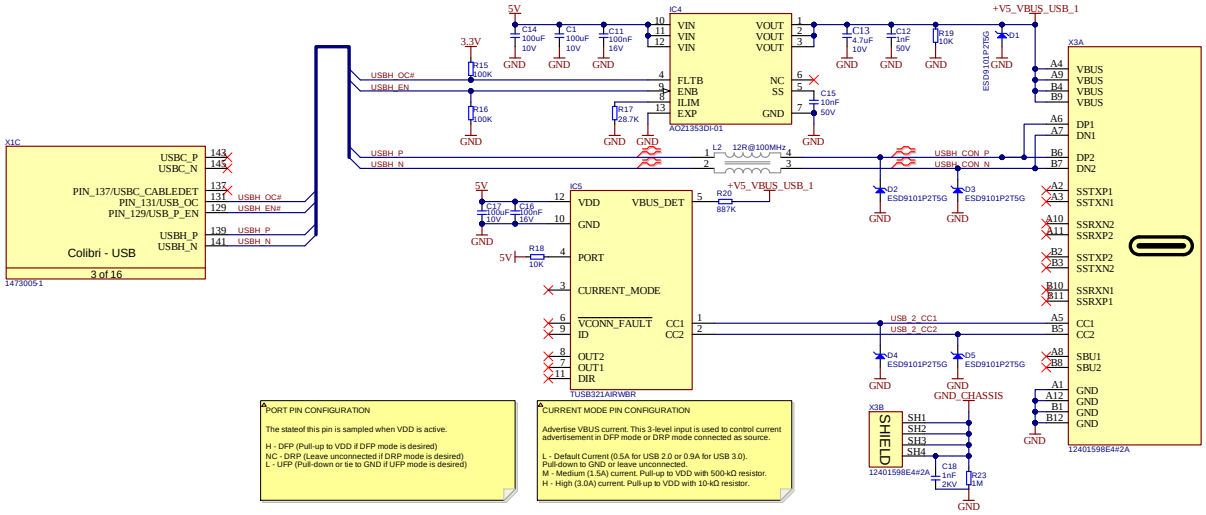

Figure 15: USB-C High-Speed DFP-Only (with Type-C connector) reference schematic

2.3.3.2.2 USB High-Speed Host-Only (With Type-A Connector)

The carrier board must provide 5V USB bus power on the USB host port. According to the USB 2.0 specifications, the maximum current drawn per port is limited by 500mA. The bus power needs to be in the range of 4.75V to 5.25V measured at the USB host receptacle for any load current from 0mA to 500mA. Adding a current limiting IC is recommended to ensure that an out-of-spec device or a defective device is not damaging the 5V power rail on the carrier board. This device detects an overcurrent situation and switches off the corresponding USB bus power. The overcurrent signal (USB_H_OC) is used to notify the host controller about the occurrence of an overcurrent shutdown event.

The inrush current needs to be considered while designing the USB bus power. USB devices are allowed to have a maximum input capacitor at the bus power of 10µF. The maximum inrush charge is limited to 50µC. This means that the power rail at the USB host jack needs to be tolerant of this inrush current. A good approach is to place a large capacitor (e.g., 150µF) at the rail.

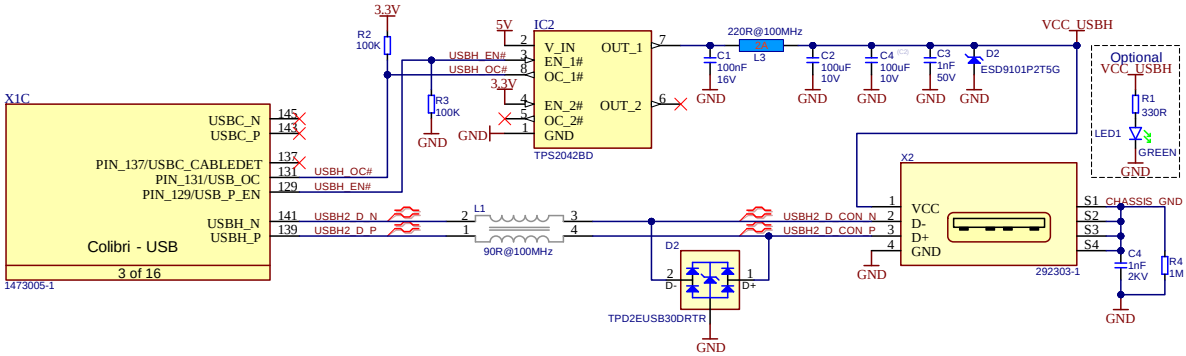

Figure 16: USB 2.0 Host-Only (with Type-A connector) reference schematic

2.3.3.3 Upstream-Facing / Client-Only

2.3.3.3.1 USB-C High-Speed Upstream-Facing-Only (With Type-C Connector)

The Upstream-Facing Port (UFP) is the most straightforward USB-C implementation. In this case, the Colibri module can only be used as a client (for example, for the recovery mode or an RNDIS client). The host function (Downstream-Facing Port, DFP) is impossible with this approach.

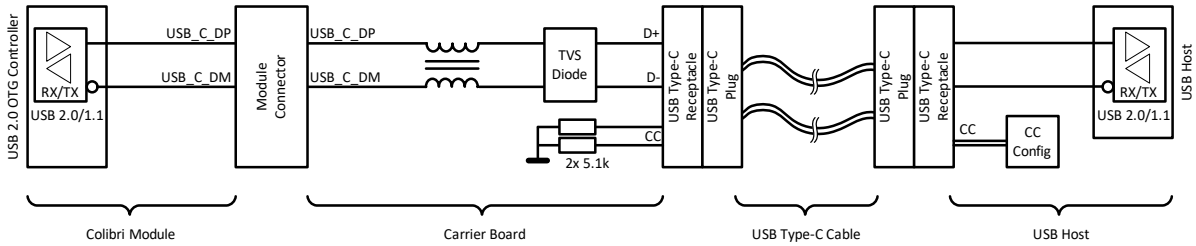

Figure 17: USB-C High-Speed UFP-Only (with Type-C connector) block diagram

In this approach, the configuration channel IC is no longer needed. Two simple 5.1kΩ pull-down resistors are sufficient to tell the other side of the USB-C connection that the port only supports UFP. It is essential to have two individual resistors. Otherwise, the port would be wrongly identified as an accessory port.

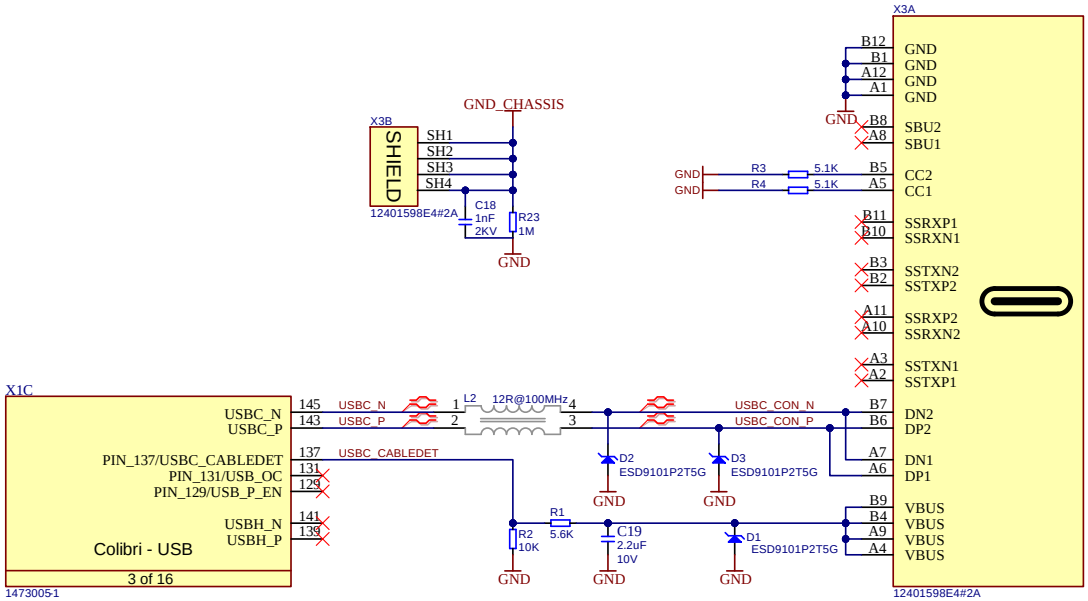

Figure 18: USB-C High-Speed UFP-Only (with Type-C connector) reference schematic

2.3.3.3.2 USB High-Speed Client-Only (With Type-B Connector)

The differential USB data signals require a common mode choke to be placed. Make sure that the selected choke is certified for USB 2.0 High Speed. The same is also required for the TVS diodes. The VBUS_DETECT signal is only 3.3V tolerant on the Colibri module. The simplest solution is to use a voltage divider.

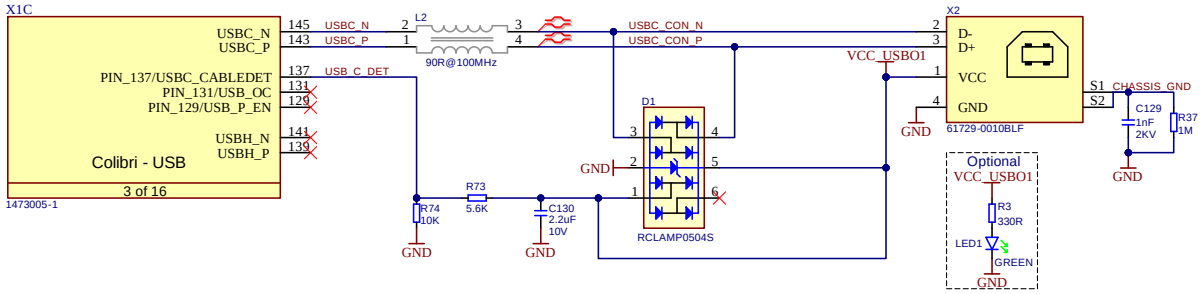

Figure 19: USB 2.0 Client-Only (with Type B connector) reference schematic

2.3.4 Unused USB Signal Termination

Colibri Pin	Colibri Signal Name	Recommended Termination
139	USB_H_DP	Leave NC if not used
141	USB_H_DM	Leave NC if not used
143	USB_C_DP	Leave NC if not used
145	USB_C_DM	Leave NC if not used
129	USB_H_PWR_EN	Leave NC if not used
131	USB_H_OC	Add a pull-up resistor or disable the overcurrent function in the software
137	USB_C_VBUS_DETECT	Leave NC if not used

Table 9: Unused USB Signals Termination

2.4 Parallel RGB LCD Interface

The Colibri modules feature one parallel RGB LCD interface as the primary display interface. As standard, the Colibri modules feature an interface with 18-bit color depth. Some modules support a color depth of 16-bit or 24-bit. Unfortunately, the color mapping of these modes can be different between the modules. Therefore, Toradex recommends using the interface in the 18-bit color mode for the best compatibility between all Colibri modules. Dithering can help to reduce the visible color banding of gradients in lower color depth systems. Consider using 18-bit color mapping with enabled dithering instead of 24-bit mapping. Carefully check which modules support color dithering.

2.4.1 Parallel RGB LCD Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
52	LCD_1_18bit_R0	O	CMOS	3.3V	Red LCD data signals (LSB: 0, MSB: 5)
54	LCD_1_18bit_R1	O	CMOS	3.3V	
66	LCD_1_18bit_R2	O	CMOS	3.3V	
64	LCD_1_18bit_R3	O	CMOS	3.3V	
57	LCD_1_18bit_R4	O	CMOS	3.3V	
61	LCD_1_18bit_R5	O	CMOS	3.3V	
80	LCD_1_18bit_G0	O	CMOS	3.3V	Green LCD data signals (LSB: 0, MSB: 5)
46	LCD_1_18bit_G1	O	CMOS	3.3V	
62	LCD_1_18bit_G2	O	CMOS	3.3V	
48	LCD_1_18bit_G3	O	CMOS	3.3V	
74	LCD_1_18bit_G4	O	CMOS	3.3V	
50	LCD_1_18bit_G5	O	CMOS	3.3V	
76	LCD_1_18bit_B0	O	CMOS	3.3V	Blue LCD data signals (LSB: 0, MSB: 5)
70	LCD_1_18bit_B1	O	CMOS	3.3V	
60	LCD_1_18bit_B2	O	CMOS	3.3V	
58	LCD_1_18bit_B3	O	CMOS	3.3V	
78	LCD_1_18bit_B4	O	CMOS	3.3V	
72	LCD_1_18bit_B5	O	CMOS	3.3V	
44	LCD_1_18bit_DE	O	CMOS	3.3V	Data Enable (other names: Output Enable)
56	LCD_1_18bit_PCLK	O	CMOS	3.3V	Pixel Clock (other names: Dot Clock, L_PCLK_WR)
68	LCD_1_18bit_HSYNC	O	CMOS	3.3V	Horizontal Sync (other names: Line Clock, L_LCKL_A0)
82	LCD_1_18bit_VSYNC	O	CMOS	3.3V	Vertical Sync (other names: Frame Clock, L_FCLK)

Table 10: Parallel RGB LCD Signals

2.4.2 Reference Schematics

2.4.2.1 18-bit Display Schematic Example

The parallel RGB interface can cause problems in passing the electromagnetic radiation tests when used with high pixel clock frequency, especially if a display is connected over long flat flex cables. The reduction of radiation needs to be taken into account. Keep the flat flex cables as short as possible. Series resistors in the data lines reduce the slew rate of the signals, which reduces the radiation problem but can introduce signal quality and timing problems. The serial resistor value is a trade-off between electromagnetic radiation reduction and signal quality. A good starting value is 22Ω.

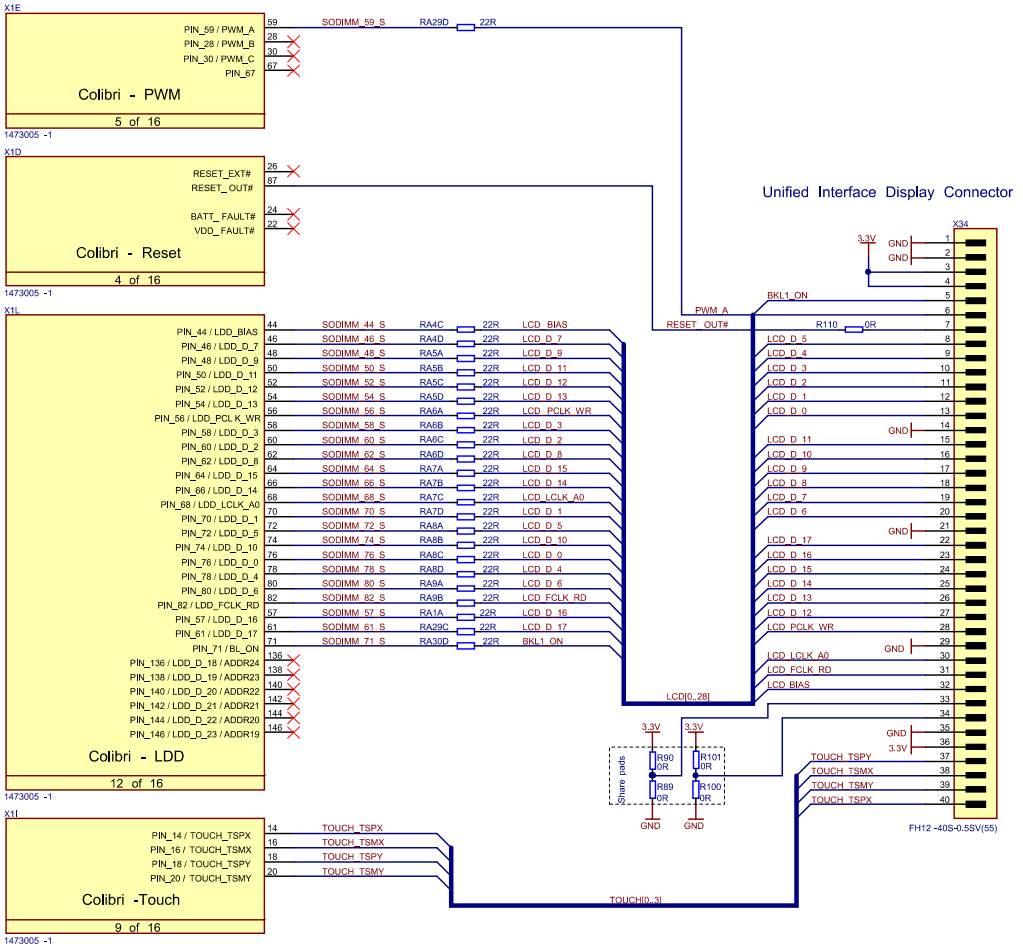

Figure 20: 18bit Parallel RGB Display Reference Schematic

2.4.2.2 VGA DAC Schematic Example

A few Colibri modules feature a dedicated VGA interface on an FFC connector. Nevertheless, adding a parallel RGB to VGA converter is recommended if a VGA interface is needed, which is compatible with all modules. Since only the 18-bit color depth is compatible between the different modules, it is recommended to use this mode even if the DAC is capable of 24-bit.

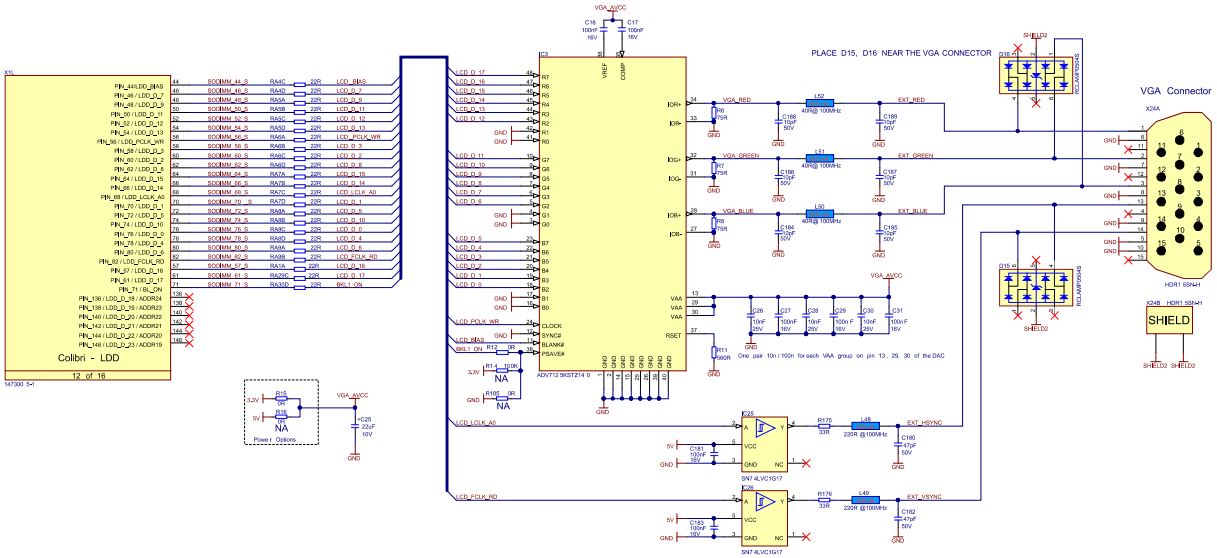

Figure 21: VGA DAC Reference Schematic

2.4.2.3 LVDS Transmitter Schematic Example

Since the electromagnetic radiation of the parallel RGB interface is not easy to handle, it is recommended to attach liquid crystal displays with high resolutions by using an LVDS interface. LVDS also reduces problems associated with long cables. The Colibri standard does not feature a dedicated LVDS LCD interface. Nevertheless, a parallel RGB to LVDS transmitter can be placed on the carrier board to get an LVDS interface.

Since there are different LVDS color mapping available, check with your display vendor how the RGB signals need to be connected to the transmitter in order to be compatible.

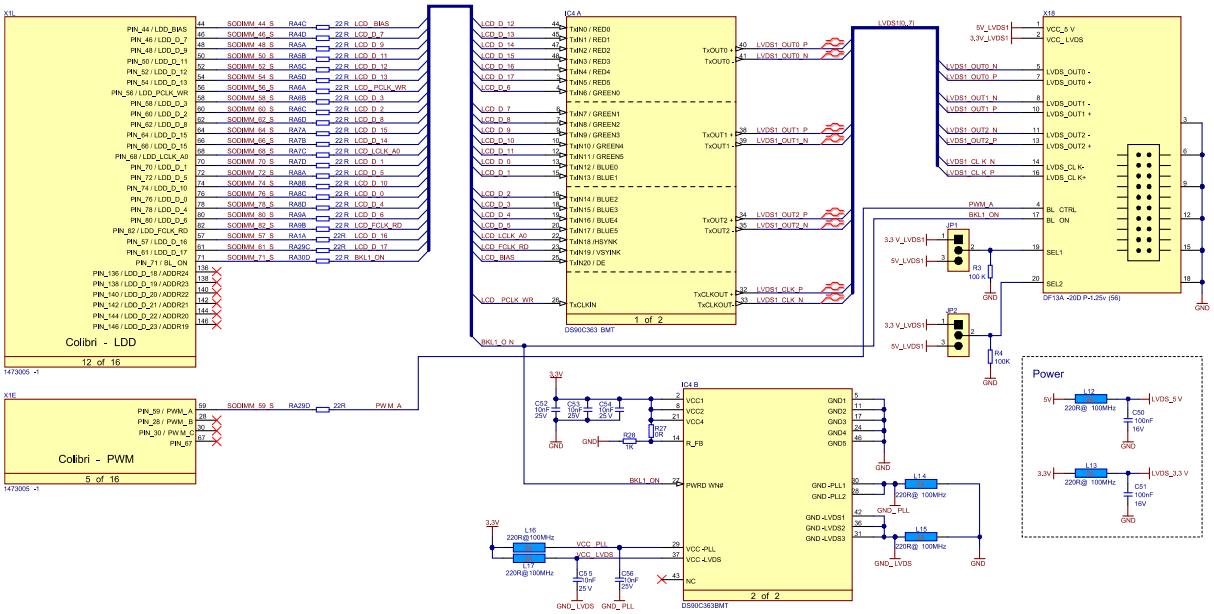

Figure 22: LVDS Transmitter Reference Schematic

18-bit Color Mapping

The color mapping for the 18-bit LVDS interface is standardized and is shown in the following picture:

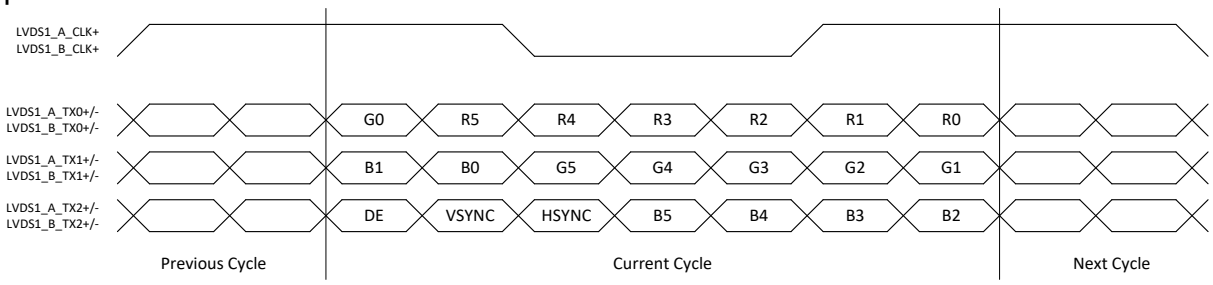

Figure 23: 18-bit LVDS Color Mapping

24-bit JEIDA Color Mapping

The JEIDA color mapping is compatible with the 18bit LVDS interface. Therefore, the mapping is sometimes also called "24bit / 18bit Compatible Color Mapping". The signal names of the color bits are renamed (e.g., the 18bit R5 is renamed to 24bit R7), but the MSB position is kept the same. The additional least significant bits R0, R1, G0, G1, B0, and B1 are located at the additional fourth LVDS data pair.

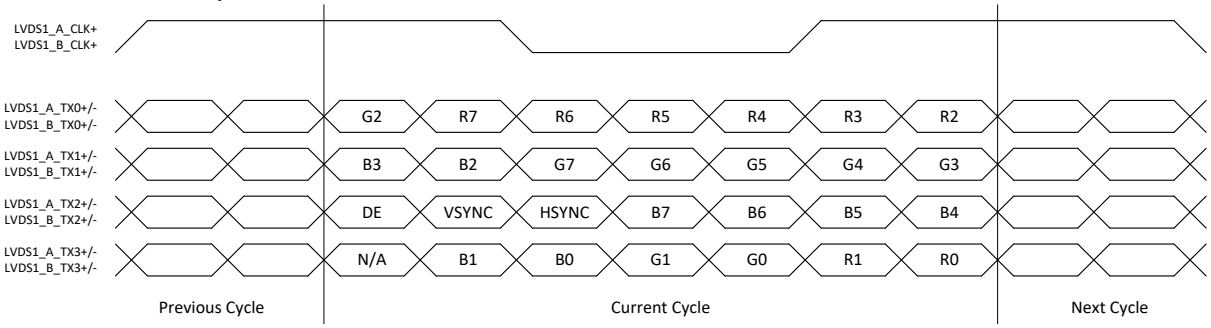

Figure 24: 24-bit JEIDA LVDS Color Mapping

24-bit VESA Color Mapping

Most of the 24bit LVDS displays follow the VESA Color mapping. The VESA color mapping does not rename the signal bits. This means that the MSB position is changed since they are available at the additional data pair. Therefore, the VESA color mapping is not compatible with the 18bit interface.

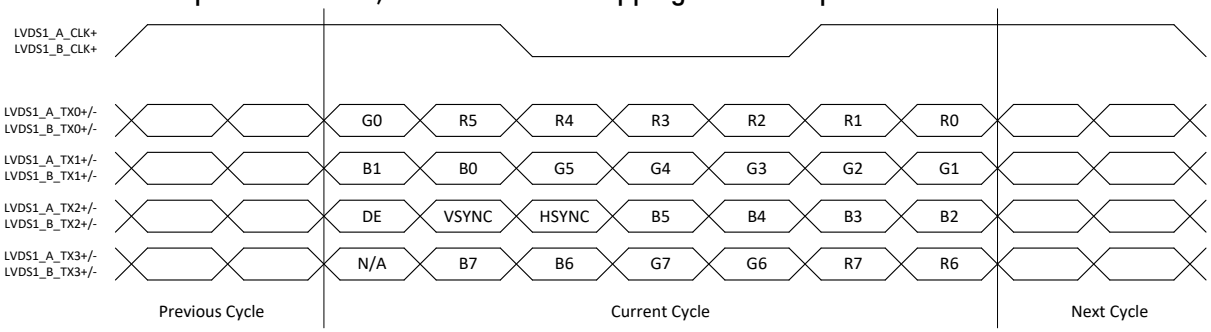

Figure 25: 24-bit VESA LVDS Color Mapping

2.4.3 Unused Parallel RGB Interface Signal Termination

All unused parallel RGB interface signals can be left unconnected.

2.5 HDMI/DVI

The HDMI and DVI interface uses a TMDS compatible physical link to transfer video and optional audio data. While electrically, HDMI and DVI are similar, but there can be a few differences in their protocols. HDMI is the DVI successor and specifies the additional transport for audio data and content protection (HDCP). As HDMI is backward compatible, HDMI devices (monitor, television set, and others) work with DVI signals. Forward compatibility is not guaranteed. Not all DVI displays accept the HDMI protocol or are HDCP compatible. Please read the datasheet of the Colibri modules for more information about the provided HDMI and DVI protocols.

The HDMI and DVI interface define different connectors. There are passive adapters available in both types. Please be advised that HDMI and HDCP are required to be licensed. The HDMI/DVI signals are available on a dedicated FFC connector. Check carefully to confirm which modules provide the interface.

2.5.1 HDMI/DVI Signals

Colibri FFC Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
2	HDMI_1_CLK_P	O	TDMS		HDMI/DVI differential clock positive
3	HDMI_1_CLK_N	O	TDMS		HDMI/DVI differential clock negative
5	HDMI_1_DATA0_P	O	TDMS		HDMI/DVI differential data lane 0 positive
6	HDMI_1_DATA0_N	O	TDMS		HDMI/DVI differential data lane 0 negative
8	HDMI_1_DATA1_P	O	TDMS		HDMI/DVI differential data lane 1 positive
9	HDMI_1_DATA1_N	O	TDMS		HDMI/DVI differential data lane 1 negative
11	HDMI_1_DATA2_P	O	TDMS		HDMI/DVI differential data lane 2 positive
12	HDMI_1_DATA2_N	O	TDMS		HDMI/DVI differential data lane 2 negative
14	HDMI_1_HPD	I	CMOS	3.3V	Hot-plug detect
16	HDMI_DDC_SDA	I/O	OD	3.3V	I^2C interface for reading the extended display identification data (EDID) over DDC.
15	HDMI_DDC_SCL	O	OD	3.3V	

Table 11: HDMI/DVI Signals

2.5.2 Reference Schematics

2.5.2.1 DVI Schematic Example

There are different configurations of DVI connectors available. The DVI-D (digital) contains only the native DVI signals. The DVI-A (analog) provides no DVI signals. Only the analog VGA signals are provided. The DVI-I (integrated) combines the digital DVI signals and the analog VGA signals. For the DVI-A and DVI-I, there are passive adapters available for the D-SUB VGA connector. There is only one DDC channel available on the DVI-I interface. Therefore, the connector is not designed to use both links (DVI and VGA) contemporaneously. Nevertheless, there are Y-cables available that provide a DVI and VGA output contemporaneously. Such cables are not standardized and usually provide the DDC only on the DVI or VGA output. Please be aware of the DDC when using such a Y-cable.
The following schematic example shows a DVI-I implementation. It can also be used as an example for a DVI-D design. Just remove the analog VGA signals. The sync signals for the VGA signals need to be level shifted from 3.3V to 5V. The same is necessary for the DDC signals. The TDMS signals need to be ESD protected by using diodes. The schematic example shows a discrete solution for the level shifting and protection. There are also integrated solutions available.

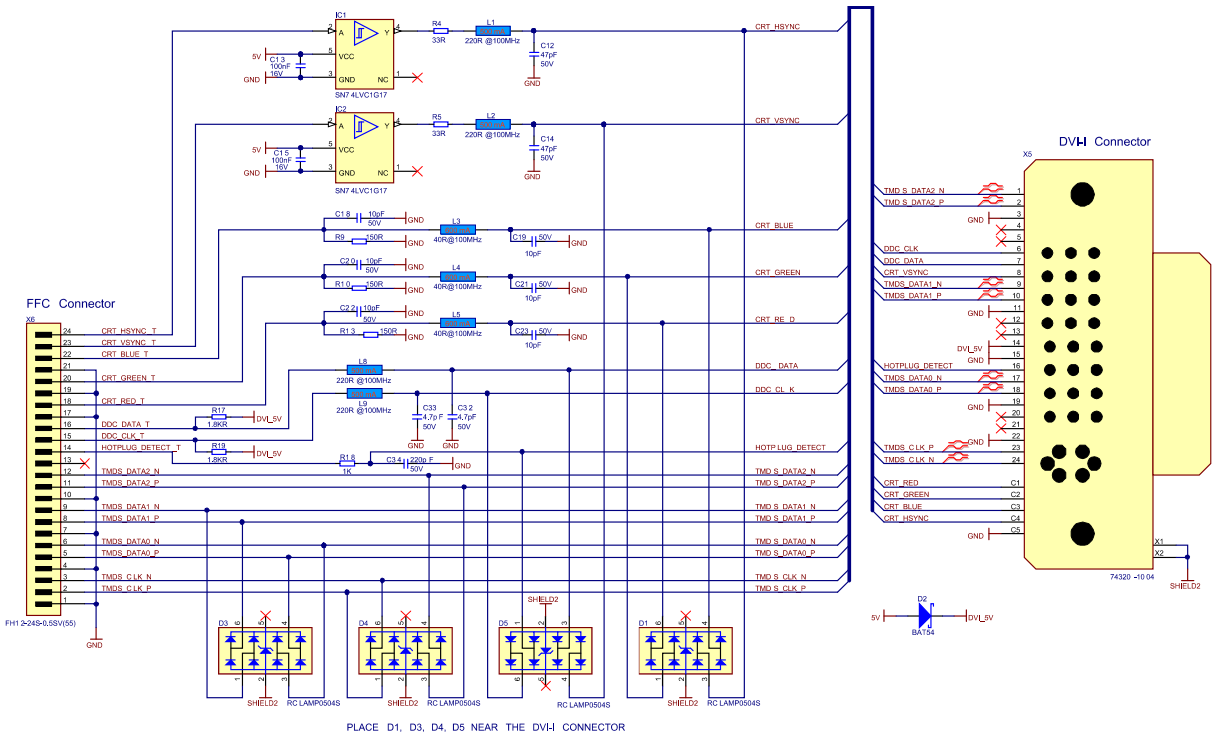

Figure 26: DVI-I Reference Schematic

2.5.2.2 HDMI Schematic Example

The HDMI connector does not feature an Analog VGA interface, but an optional Consumer Electronics Control (CEC) interface is available on the connector. The location of the CEC signal is not standardized on the Colibri modules. Check the datasheet of the modules for more information on the position of the signal. The CEC is a single-wire interface used to control consumer audio and video devices such as television sets or AV receivers. There are many different CEC trade names (VIERA Link, Anynet+, EasyLink, Aquos Link, BRAVIA Link, and others.). The CEC is a 3.3V interface. Nevertheless, it is recommended to add a level shifter from the internal 3.3V logic level. This eliminates problems with displays that pull-up the signal to other voltage levels.

The I^2C signals for the DDC and the hotplug detection (HPD) need to be shifted to/from the 5V logic level of the HDMI to the Colibri level of 3.3V. The HPD has a 100kΩ pull-down resistor already on the baseboard

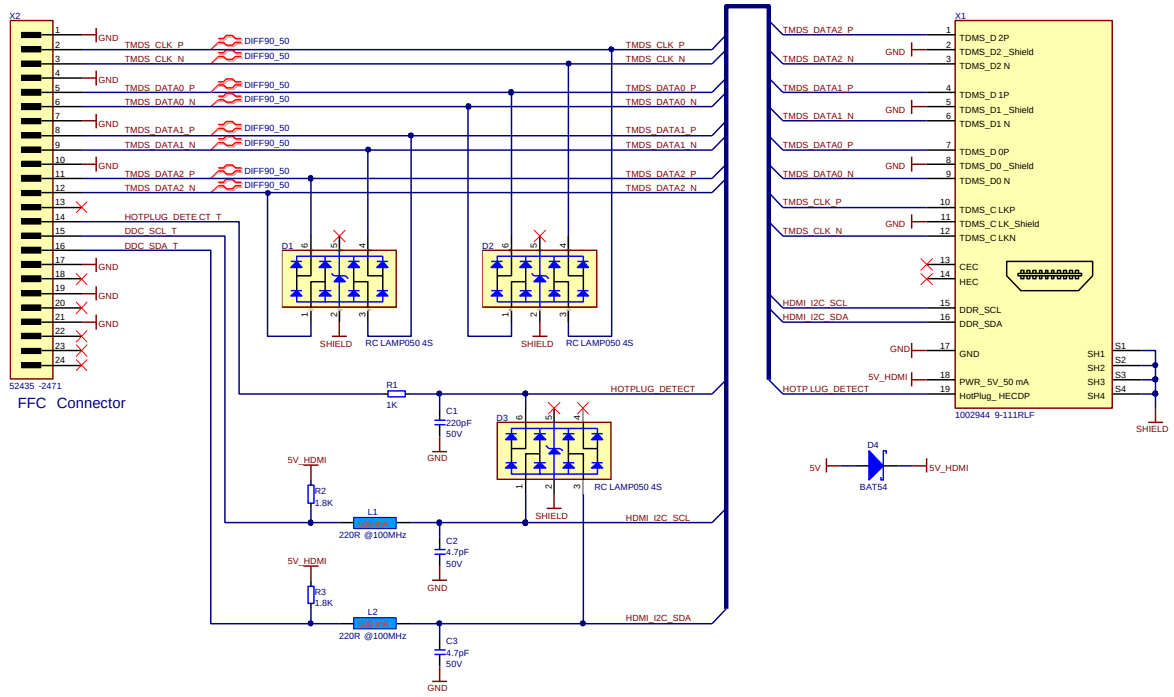

Figure 27: HDMI Reference Schematic

2.5.3 Unused HDMI/DVI Signal Termination

All unused HDMI/DVI signals can be left unconnected. The HPD has a 100kΩ pull-down resistor on the module.

Colibri Pin	Colibri Signal Name	Recommended Termination
2	HDMI_1_CLK_P	Leave NC if not used
3	HDMI_1_CLK_N	Leave NC if not used
5	HDMI_1_DATA0_P	Leave NC if not used
6	HDMI_1_DATA0_N	Leave NC if not used
8	HDMI_1_DATA1_P	Leave NC if not used
9	HDMI_1_DATA1_N	Leave NC if not used
11	HDMI_1_DATA2_P	Leave NC if not used
12	HDMI_1_DATA2_N	Leave NC if not used
14	HDMI_1_HPD	Leave NC if not used, 100kΩ resistor on Colibri module
16	HDMI_DDC_SDA	Add pull-up resistor or disable the I^2C function in the software
15	HDMI_DDC_SCL	Add pull-up resistor or disable the I^2C function in the software

Table 12: Unused HDMI/DVI Signals Termination

2.6 Analog VGA

Some Colibri modules feature a dedicated VGA interface on the HDMI FFC connector. For systems that need to be compatible with a wide range of Colibri modules, it is recommended to use a parallel RGB to VGA DAC instead of the dedicated VGA interface.

2.6.1 VGA Signals

Colibri FFC Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
18	VGA_1_R	O	Analog		Analog red video (0 to 0.7V)
20	VGA_1_G	O	Analog		Analog green video (0 to 0.7V)
22	VGA_1_B	O	Analog		Analog blue video (0 to 0.7V)
24	VGA_1_HSYNC	O	CMOS	3.3V	Horizontal sync
23	VGA_1_VSYNC	O	CMOS	3.3V	Vertical sync
16	HDMI_DDC_SDA	I/O	OD	3.3V/ 5V tolerant	I^2C interface for reading the extended display identification data (EDID) over DDC. Signal shared with the HDMI interface
15	HDMI_DDC_SCL	O	OD	3.3V/ 5V tolerant	

Table 13: VGA Signals

2.6.2 Reference Schematics

The horizontal and vertical sync signals need to be level-shifted on the baseboard. The DDC signals on the FFC connector do not require a level shifter since these signals are 5V tolerant. If a different I^2C interface is used as DDC, the shifters are needed. In the VGA connector standard, the carrier board needs to provide a 5V power supply for the EDID memory on the DDC. This allows the system to read out the EDID information of an attached display even if it is not powered. Unfortunately, some displays source the 5V internally and also provide internal pull-up resistors to the I^2C lines. This can cause back-feeding problems. Therefore we recommend connecting the display and pull-up resistor 5V supply over a diode to the module supply.

It is mandatory to place on every analog RGB signal a 150Ω resistor to the ground. Place this resistor as close to the VGA connector as possible. Before this resistor, the signal trace can be routed with 50Ω impedance. After the resistor, the signal should be routed with a 75Ω impedance. Depending on the layer stack-up, 75Ω traces cannot be reached since the trace width is getting too small. In this case, a lower trace impedance (e.g., 50Ω) can be used, but the trace length should be kept short.

All signals on the VGA D-SUB connector need to be ESD protected. TSR diodes can be used. It is recommended to add a PI-filter to the analog RGB signals. The values for the capacitors and inductors depend on the maximum required display resolution. The PI-filter reduces EMI problems but also limits the maximum bandwidth of the VGA signal.

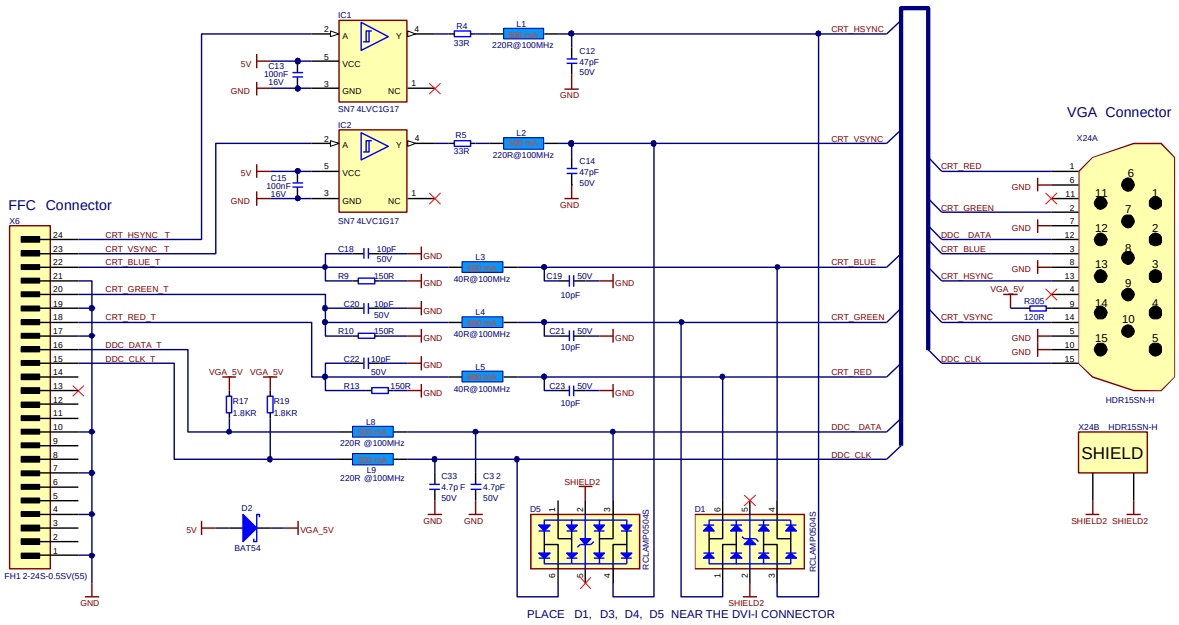

Figure 28: VGA Reference Schematic

2.6.3 Unused VGA Interface Signal Termination

All unused VGA interface signals can be left unconnected.

2.7 Parallel Camera Interface

The Colibri module form factor features an 8-bit parallel camera interface as a standard interface. Depending on the module, there may be additional bits available in the type-specific area. Only the 8-bit YUV and ITU-R BT.656 format mode are intended to keep compatible between Colibri modules. Consult the Colibri datasheets to get more information about the additionally available input modes (e. g., Bayer, RGB, and others.)

2.7.1 Parallel Camera Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
101	CAM_1_Y0/C0	I	CMOS	3.3V	Video input pixel data
103	CAM_1_Y1/C1	I	CMOS	3.3V	
79	CAM_1_Y2/C2	I	CMOS	3.3V	
97	CAM_1_Y3/C3	I	CMOS	3.3V	
67	CAM_1_Y4/C4	I	CMOS	3.3V	
59	CAM_1_Y5/C5	I	CMOS	3.3V	
85	CAM_1_Y6/C6	I	CMOS	3.3V	
65	CAM_1_Y7/C7	I	CMOS	3.3V	
96	CAM_1_PCLK	I	CMOS	3.3V	Video input pixel clock
81	CAM_1_VSYNC	I	CMOS	3.3V	Video input vertical sync
94	CAM_1_HSYNC	I	CMOS	3.3V	Video input horizontal sync
75	CAM_1_MCLK	O	CMOS	3.3V	Master clock output for the camera. Some Camera might do not need this clock since they use other clock sources

Table 14: Parallel Camera Signals

2.7.2 Unused Parallel Camera Interface Signal Termination

All unused parallel camera input signals can be left unconnected if the interface is disabled in software. It depends on the module whether the signals can be used as GPIO when they are not used as a camera interface.

2.8 SD/MMC/SDIO

The Colibri module form factor features one SD/MMC interface as a standard interface. The interface provides up to 4 data bits that can be used for interfacing SD, MMC cards, and SDIO interface peripherals. Depending on the module, there might be additional data signals to get an 8bit interface. MMCplus cards and eMMC memory chips use this bit width. The additional data bits are not intended to be compatible between different Colibri modules.

The SD cards know different bus speed modes. The required signal voltage depends on the bus speed mode. For example, the SDR104 mode requires 1.8V signaling. In the Colibri module definition, all GPIO capable interfaces, including the SD/MMC/SDIO, are defined for 3.3V. Some Colibri modules might be capable of switching the voltages of the SD card interface pins to a 1.8V, but it is not mandatory. Read the related datasheet of the Colibri module.

Even if the bus speed mode requires a signaling voltage of 1.8V, the supply of the card itself is still 3.3V. Pay attention to the SD card signal pull-up resistors on the carrier board. If the carrier board should support the 1.8V mode, the pull-up resistors' voltage also needs to be switchable. Some Colibri modules might allow removing the pull-up resistors on the carrier board and using the internal ones only. In this case, this is the preferred solution. Even if the external pull-up resistors are not mandatory, we recommend adding not-assembled pull-up resistors to the 3.3V rail to be compatible with future modules.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage
Default Speed	25 MHz	12.5 MByte/s	3.3V
High Speed	50 MHz	25 MByte/s	3.3V
SDR12	25 MHz	12.5 MByte/s	1.8V
SDR25	50 MHz	25 MByte/s	1.8V
DDR50	50 MHz	50 MByte/s	1.8V
SDR50	100 MHz	50 MByte/s	1.8V
SDR104	208 MHz	104 MByte/s	1.8V

Table 15: SD Card Bus Speed Modes

2.8.1 SD/MMC/SDIO Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
192	SD_1_DATA0	I/O	CMOS	3.3V	Data signals [3:0], used for SD, MMC, and SDIO interfaces, add external pull-up resistors
49	SD_1_DATA1	I/O	CMOS	3.3V	
51	SD_1_DATA2	I/O	CMOS	3.3V	
53	SD_1_DATA3	I/O	CMOS	3.3V	
190	SD_1_CMD	I/O	CMOS	3.3V	Command signal, add an external pull-up resistor
47	SD_1_CLK	O	CMOS	3.3V	Clock output

Table 16: 4bit SD/MMC/SDIO Signals

2.8.2 Reference Schematics

Even if the selected module does not require pull-up resistors on the data and command lines, it is recommended to place such resistors in the customer design and just not assemble them. This makes sure that the module is compatible with other Colibri modules. There is no dedicated card detect signal available. Any free GPIO capable signal could be used, but we recommend using the signal on Pin 43 (CTRL_WAKE_0) whenever possible. There is also no dedicated write protection signal available on the standard Colibri pinout. Any free GPIO capable signal can be used if the write protection function is required.

2.8.2.1 SD Card Slot Reference Schematics

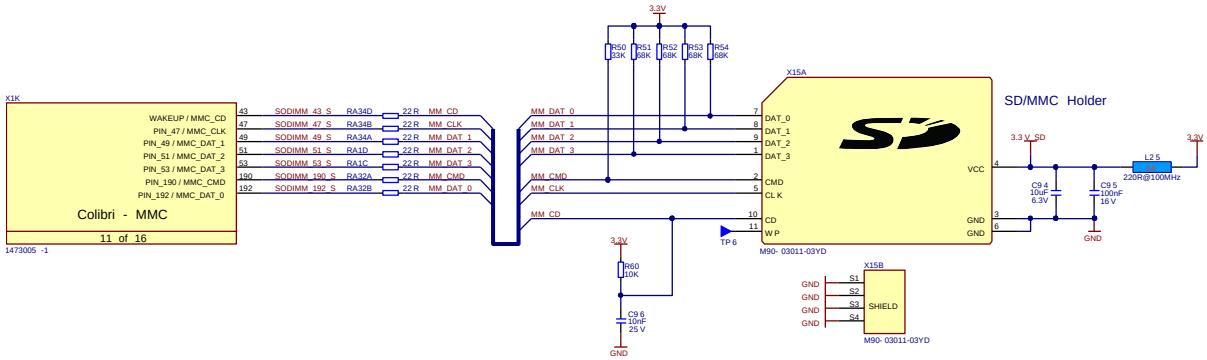

Figure 29: SD Card Slot Reference Schematic

2.8.3 Unused SD/MMC/SDIO Interface Signal Termination

All unused SD interface signals can be left unconnected.

2.9 I²C

The Colibri module form factor features one general-purpose I²C interface. Additionally, some Colibri modules feature a dedicated DDC interface on the HDMI FFC connector.

The I²C, as well as the DDC interfaces, do not feature any pull-up resistors on the module. It is required to add pull-up resistors to the data and clock lines on the carrier board. The pull-up resistor values usually are between 1kΩ and 10kΩ. A small pull-up resistor increases power consumption, while a large resistor could lead to signal quality problems. The optimum size of the resistor depends on the capacitive load on the I²C lines and the required bus speed. 4.7kΩ is a suitable value for many applications.

2.9.1 I²C Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
194	I2C_1_SDA	I/O	OD	3.3V	General-purpose I²C data signal, pull-up resistor required on carrier board
196	I2C_1_SCL	O	OD	3.3V	General-purpose I²C clock signal, pull-up resistor required on carrier board

Table 17: I²C Signals

2.9.2 Real-Time Clock (RTC) recommendation

The RTC on the module is not designed for ultra-low power consumption. Therefore, a standard lithium coin cell battery can drain faster than allowed for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the I²C interface of the module.

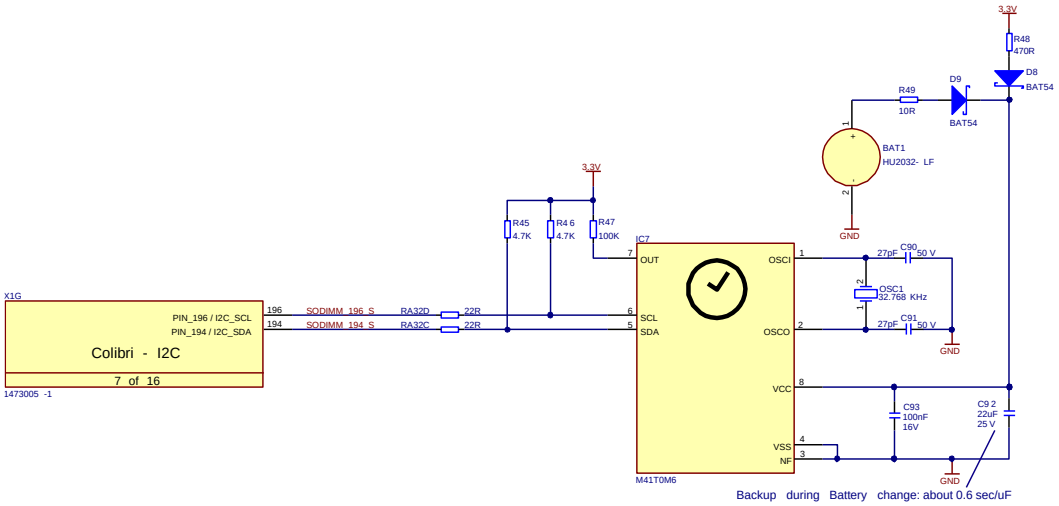

Figure 30: External RTC Reference Schematic

2.9.3 Unused I²C Signal Termination

All unused I²C can be left unconnected if the corresponding I²C port is switched off in software. Otherwise, it is recommended to keep the pull-up resistors available. Unused I²C signals can be configured to be GPIO.

2.10 UART

The Colibri module form factor features three UART interfaces. Even though the UART_A is specified as full-featured UART, some modules might not provide all the control signals. Please read the corresponding datasheet of the module carefully. UART_A is the standard console output interface for the Linux and Windows Embedded Compact operating system. It is desirable to keep at least the RX and TX signals of this port accessible for system debugging.

UART_B features RTS and CTS signals for hardware flow control, while UART_C does not feature any flow control signals. Some modules might provide the additional flow control signals on non-standard pins.

2.10.1 UART Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
33	UART_A_RX	I	CMOS	3.3V	Received Data
35	UART_A_TX	O	CMOS	3.3V	Transmitted Data
27	UART_A_RTS	O	CMOS	3.3V	Request to Send
25	UART_A_CTS	I	CMOS	3.3V	Clear to Send
23	UART_A_DTR	O	CMOS	3.3V	Data Terminal Ready
29	UART_A_DSR	I	CMOS	3.3V	Data Set Ready
37	UART_A_RI	I	CMOS	3.3V	Ring Indicator
31	UART_A_DCD	I	CMOS	3.3V	Data Carrier Detect
36	UART_B_RX	I	CMOS	3.3V	Received Data
38	UART_B_TX	O	CMOS	3.3V	Transmitted Data
34	UART_B_RTS	O	CMOS	3.3V	Request to Send
32	UART_B_CTS	I	CMOS	3.3V	Clear to Send
19	UART_C_RX	I	CMOS	3.3V	Received Data
21	UART_C_TX	O	CMOS	3.3V	Transmitted Data

Table 18: UART Signals

2.10.2 Reference Schematics

2.10.2.1 Full-Featured RS232 Reference Schematics

The RS232 interface can be classified as Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). This classification is inherited from the usage of the interface for modems. The signal direction of these modes is different. Some Colibri modules might allow changing the mode and the data direction, but this is not a mandatory requirement. According to the Colibri specifications, the interface is intended to be used in the DTE configuration.

Signal	Name	Usage	DTE Direction (Colibri standard)	DCE Direction
UART_A_RXD	Received Data	Data from DCE to DTE	Input	Output
UART_A_TXD	Transmitted Data	Data from DTE to DCE	Output	Input
UART_A_RTS	Request to Send	DTE request to DCE be prepared to receive data	Output	Input
UART_A_CTS	Clear to Send	DCE indicates ready to accept data	Input	Output
UART_A_DTR	Data Terminal Ready	DTE indicates presence to DCE	Output	Input
UART_A_DSR	Data Set Ready	DCE is ready to receive commands or data	Input	Output
UART_A_RI	Ring Indicator	DCE announce to have detected an incoming ring signal on the telephone line	Input	Output
UART_A_DCD	Data Carrier Detect	DCE announce to be connected to the telephone line	Input	Output

Table 19: RS232 Signal Modes

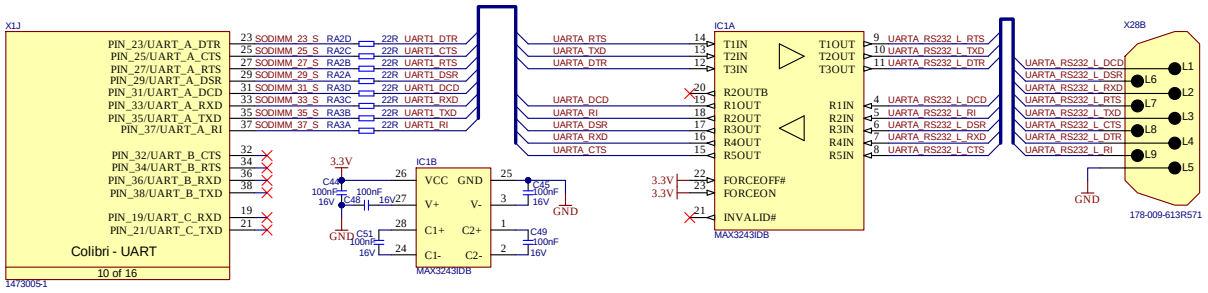

Figure 31: RS232 Reference Schematic

The RS232 interface is prone to backfeed. The idle state of the RS232 signals is between 3V and 15V. If a connected device is powered while the Colibri system is shut down can cause backfeeding through the RS232 transceiver. Therefore, the selection of a non-backfeeding transceiver makes sense in many applications. Often it is hard to judge whether a transceiver is backfeeding or not by simply reading its datasheet. Therefore, Toradex tested a few pin-compatible RS232 transceivers. Please note that the table only shows a limited selection of components, and Toradex does not guarantee correctness.

Part Number	Manufacturer	Backfeeding, according to Toradex tests
SP3243EEA-L	MaxLinear	Yes (negative voltage)
ICL3243EIAZ	Renesas	Yes (negative voltage)
ST3243EBTR	ST	No backfeeding measured
MAX3243IDB	TI	No backfeeding measured
SN65C3243	TI	Yes (positive voltage)
TRS3243EIDBR	TI	No backfeeding measured

Table 20: Tested RS232 Transceivers

2.10.2.2 RS422 Reference Schematics

The RS422 is a full-duplex serial interface with differential pair signals. This allows higher data rates and longer distances as with the RS232. Since the RS422 has separate RX and TX signal pairs, no additional control signals are required for changing the signal direction. This means the RS422 requires only the RX and TX signals of the UART interface. Therefore, it is possible to use any of the three standard UART interfaces of the Colibri standard.

The RS422 specification does not contain a connector. Therefore, there is no standard connector for this interface available. The reference schematic below uses the 9 pin D-sub connector (DE-9). Peripherals might have a different pinout even if they use a DE-9 connector.

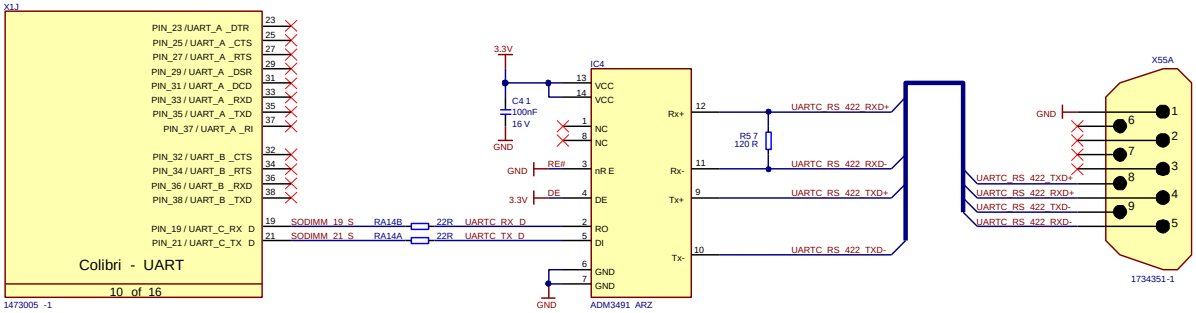

Figure 32: RS422 Reference Schematic

2.10.2.3 RS485 Reference Schematics

The RS485 interface is a half-duplex serial interface with differential pair signals. Instead of two differential pair wires (RS422), only one pair is used for transmitting and receiving the data. The bus allows multi-point connections. An additional control signal is required since the transceiver needs to be set either in the transmitting or receiving mode. It is recommended to use the RTS signal of the corresponding UART interface. The RTS signal is only available on the UART_A and UART_B as a Colibri standard interface. The schematic below inverts the RTS signal for the data enable input of the transceiver. Some modules allow inverting the signal in software. However, it is recommended to use the inverter circuit shown below to maintain compatibility with different modules and drivers provided by Toradex. For some applications, the UART controller should not see the TX message on its RX pins (the echo of the sent message). In this case, the receive enable pin (RE#) can be driven with the RTS signal. This turns off the RX output buffer while sending a message.
Like the RS422, the RS485 specification also does not describe a standard connector. The reference schematic below uses a DE-9 connector which may have a different pinout as some peripheral devices.

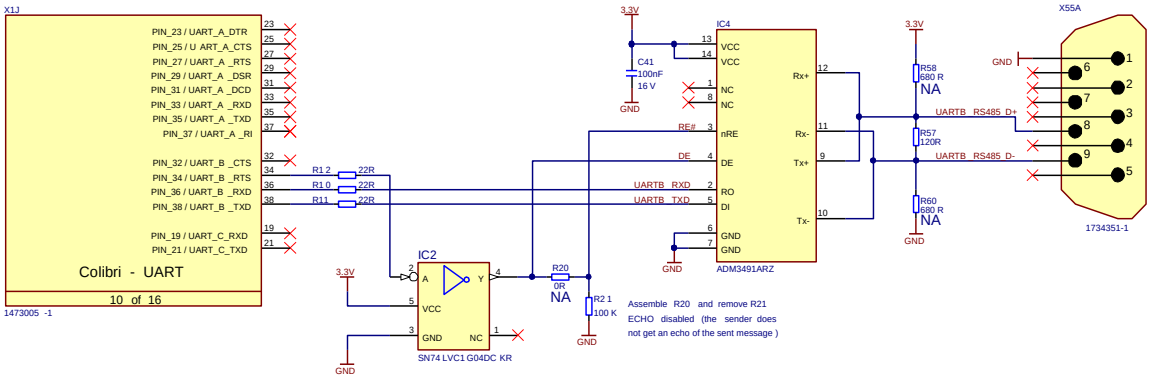

Figure 33: RS485 Reference Schematic

2.10.2.4 IrDA Reference Schematics

IrDA is an optical wireless communication interface. There are different physical layer modulation schemes available. Make sure which modes are supported by the specific Colibri module and the peripheral devices. For compatibility reasons, it is recommended to use UART_C for the IrDA implementation. Some modules only feature the IrDA function on this UART instance.

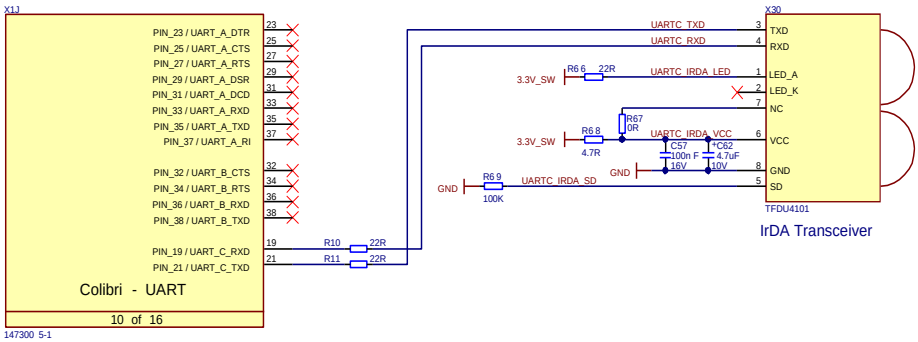

Figure 34: IrDA Reference Schematic

2.10.3 Unused UART Signal Termination

Unused UART interface signals can be left unconnected. For debugging purposes, it is recommended to have at least the UART1_RXD and UART1_TXD signals available.

2.11 SPI

The serial peripheral interface (SPI) bus is a synchronous, full-duplex interface. The Colibri module form factor features one SPI interface. The interface has a chip select signal as a compatible standard. Some modules may feature additional chip select signals or additional SPI interfaces as a secondary function of other pins.

The clock polarity and phase of the SPI bus are not standardized. Some peripherals are latching the data on the positive edge of the clock, while others are latching it at the negative edge. The SPI modes describe these different behaviors. Ensure that the Colibri module and the peripheral device can be set to the same SPI mode.

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock is positive polarity, and the data is latched on the positive edge of the SCK
1	0	1	The clock is positive polarity, and the data is latched on the negative edge of the SCK
2	1	0	The clock is negative polarity, and the data is latched on the positive edge of the SCK
4	1	1	The clock is negative polarity, and the data is latched on the negative edge of the SCK

Table 21: SPI Modes

2.11.1 SPI Signals

The SPI bus consists of one master and one or many slaves. In the Colibri standard, the module is the SPI master. Some modules might allow being also used as SPI slaves. Some modules may provide this function on different, non-standard pins.

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
92	SPI_1_MOSI	O	CMOS	3.3V	Master Output, Slave Input
90	SPI_1_MISO	I	CMOS	3.3V	Master Input, Slave Output
86	SPI_1_CS0	O	CMOS	3.3V	Slave Select
88	SPI_1_CLK	O	CMOS	3.3V	Serial Clock

Table 22: SPI Signals

2.11.2 Unused SPI Signal Termination

Unused SPI signals can be left unconnected.

2.12 CAN

The Colibri form factor does not provide a controller area network (CAN) bus as a standard interface. Some modules feature dedicated CAN interface signals. For the other modules, it is recommended to add a CAN controller with an SPI interface on the carrier board to provide a CAN interface. This section describes how to add a CAN controller to the SPI interface. If you intend to use the dedicated CAN interface signals, please read the Colibri module's datasheet.

2.12.1 Reference Schematics

Besides a controller, the CAN interface requires a transceiver on the carrier board. Usually, the CAN interface needs to be galvanically isolated from the Colibri computer module. There are transceivers with integrated signal isolation couplers and isolated DC/DC converters available (for example, the Analog Devices ADM3053). The other solution is to use separate components for the transceiver, signal coupler, and DC/DC converter. There are different types of connectors used for the CAN interface. The reference schematic below uses a DE-9 connector. Since this is not an official standard, some devices might have a different pinout.

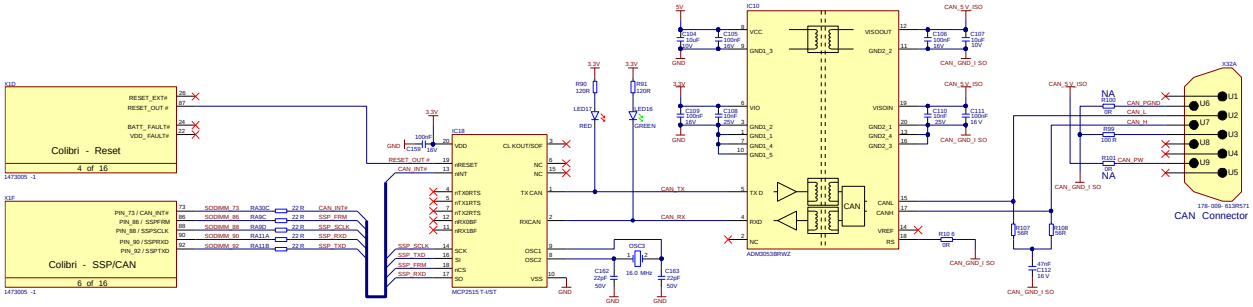

Figure 35: CAN Reference Schematic

2.13 PWM

The Colibri module form factor defines four general-purpose pulse width modulator (PWM) outputs. Please note that two of the four PWM signals are located on pins that are also used for the standard parallel camera interface. These PWM outputs can only be used if the according camera pins are not in use. The maximum output frequency and the available duty cycle steps can also vary between the different Colibri modules.

2.13.1 PWM Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
59	PWM_A	O	CMOS	3.3V	General-purpose PWM output, pin also used for camera interface
28	PWM_B	O	CMOS	3.3V	General-purpose PWM output
30	PWM_C	O	CMOS	3.3V	General-purpose PWM output
67	PWM_D	O	CMOS	3.3V	General-purpose PWM output, pin also used for camera interface

Table 23: PWM Signals

2.13.2 Reference Schematics

The PWM output signals can be used for example, to drive motors, LEDs, robotic servos, or fans. It is possible to get an analog signal with a simple low-pass filter. A widespread usage is driving of the backlight of liquid crystal displays.

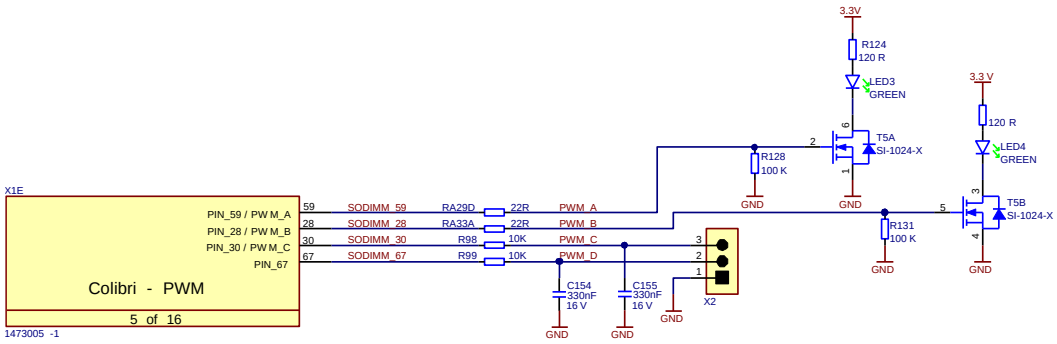

Figure 36: PWM Example Schematic

2.13.3 Unused PWM Signal Termination

Unused PWM signals can be left unconnected.

2.14 Analog Audio

2.14.1 Analog Audio Signals

If only a single channel (mono) line input or headphone output is required, it is recommended to use the left channel.

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
1	ANALOG_AUDIO_MIC_IN	I	Analog	3.3V	Microphone input
3	ANALOG_AUDIO_MIC_GND		Analog		Microphone pseudo-ground
5	ANALOG_AUDIO_LINEIN_L	I	Analog	3.3V	Left line input
7	ANALOG_AUDIO_LINEIN_R	I	Analog	3.3V	Right line input
15	ANALOG_AUDIO_HEADPHONE_L	O	Analog	3.3V	Headphone left output (can also be used as left line output)
17	ANALOG_AUDIO_HEADPHONE_R	O	Analog	3.3V	Headphone right output (can also be used as right line output)
13	ANALOG_AUDIO_HEADPHONE_GND		Analog		Headphone pseudo-ground (do not connect to the ground!)

Table 24: Analog Audio Signals

2.14.2 Reference Schematics

Depending on the module, the headphone output signals can have a DC offset. A standard solution is adding series capacitors to the headphone signal lines. If the headphone output signals are used only as line output signals, 1µF series capacitors are sufficient. If the signals are used for driving headphones, larger capacitors (47µF and more) are recommended. Some Colibri modules provide a virtual headphone ground that can be used instead of the series capacitors to reduce the BOM cost. Please note this solution only works if the attached device is isolated from the module ground. For example, this works perfectly for headphones but does not work for an audio amplifier that uses the same ground as the module.

The line-in and microphone signals do not require serial capacitors since they are already placed on the module. Some microphones (e.g., the widely used electret microphones) require phantom power. The reference schematic below shows a suitable solution for common electret microphone capsules. Please note that some microphones require phantom power on the middle ring of the 3.5mm jack, while others need to be powered over the tip of the 3.5mm jack which is also used for the audio signals. The Colibri modules feature a special analog ground for the microphone. This is a switched ground. Using this ground instead of the regular analog ground allows switching off the phantom power when the microphone is not used.

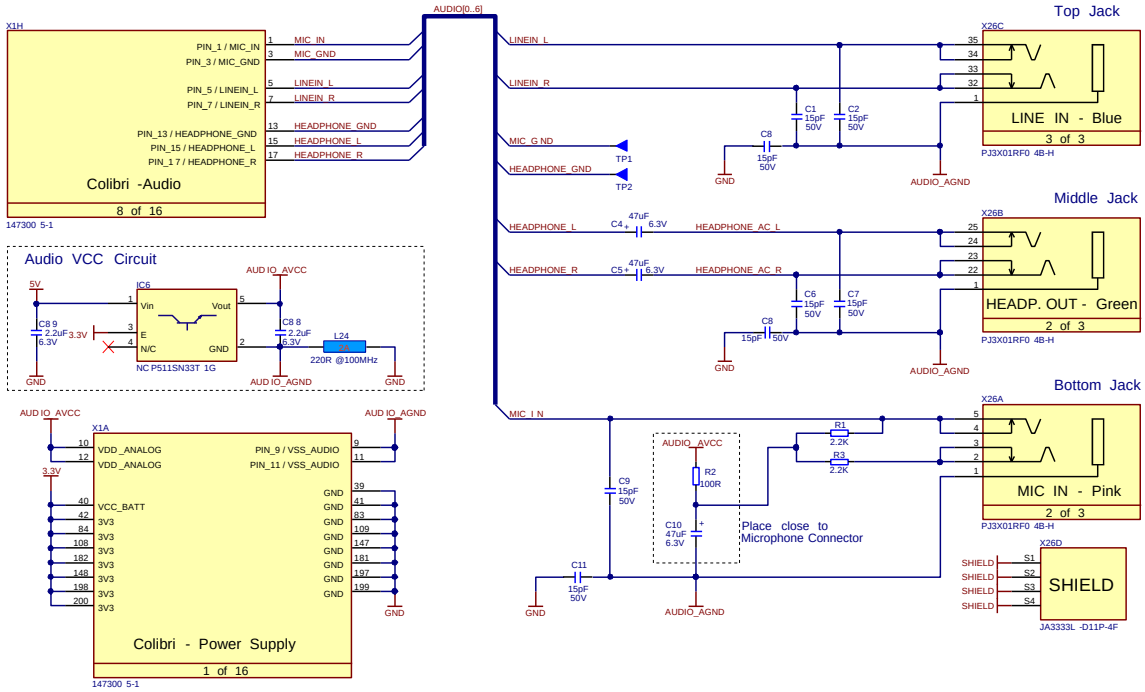

Figure 37: Analog Audio Reference Schematic

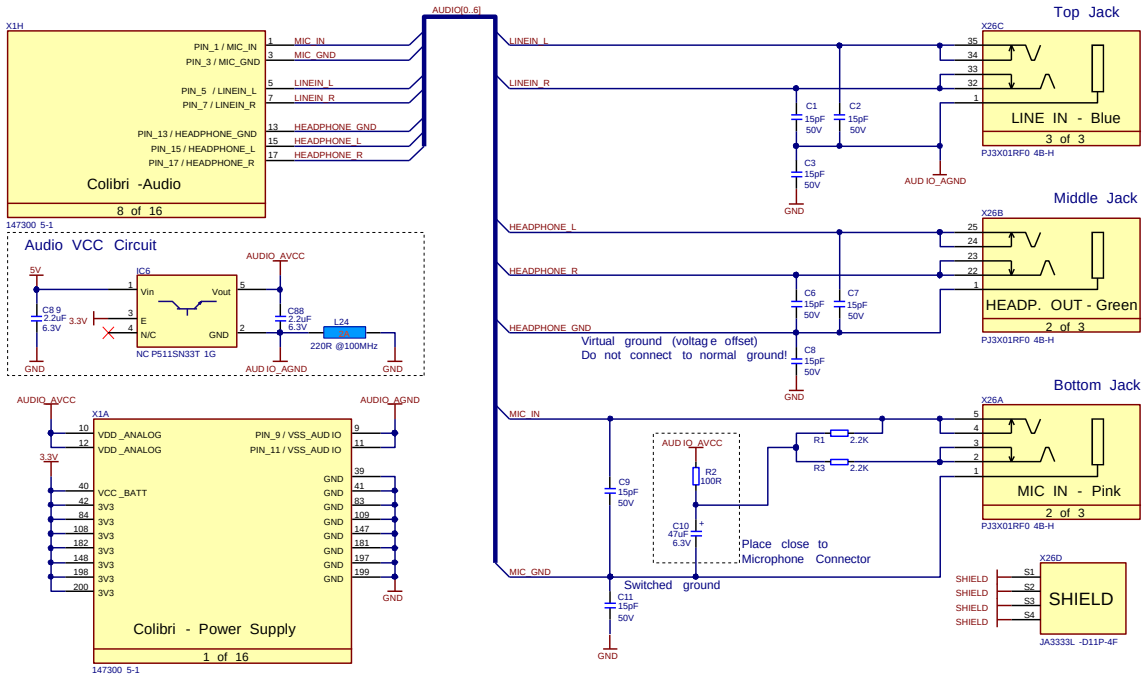

Figure 38: Analog Audio Reference Schematic (using virtual and switched grounds)

2.14.3 Unused Analog Audio Signal Termination

The unused analog audio signals can be left unconnected. Please note, even if the analog audio interface is not used at all, the analog 3.3V power pins of the module (pin 10 and 12) still need to be powered. Alternatively, the analog power can be connected to the digital 3.3V power rail.

2.15 Touch Panel Interface

The Colibri module standard features a touch panel interface for resistive touch screens. This allows integrating a touch screen solution with a minimum amount of components on the carrier board. This standard supports four-wire resistive touch screens. Some modules also support five-wire touch. Read the corresponding datasheet of the module for more information.

2.15.1 Resistive Touch Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
14	TOUCH_4-wire_PX	I/O	Analog	3.3V	X+ (4-wire)
16	TOUCH_4-wire_MX	I/O	Analog	3.3V	X- (4-wire)
18	TOUCH_4-wire_PY	I/O	Analog	3.3V	Y+ (4-wire)
20	TOUCH_4-wire_MY	I/O	Analog	3.3V	Y- (4-wire)

Table 25: Digital Audio Signals

2.15.2 Reference Schematics

To reduce the noise that is picked up by the display or long cables, it is recommended to add capacitors to the touch screen signals. 1nF to 10nF is a good choice. It is also recommended to add clamping diodes to protect the input of the touch screen controller against ESD.

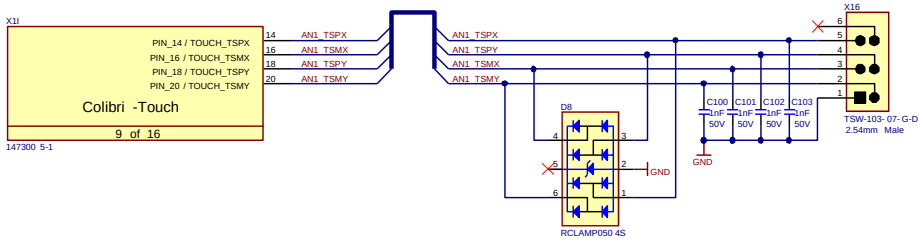

Figure 39: Touch Interface Reference Schematic

2.15.3 Unused Touch Panel Interface Signal Termination

Unused touch panel signals can be left unconnected or pull down the signals individually with 10kΩ resistors. It is recommended to disable the corresponding drivers.

2.16 Analog Inputs

The Colibri modules feature up to four analog input channels. The supported sampling rates and resolution are dependent on the modules. The input voltage range for most modules is from 0V to 3.3V. Please check the related datasheet for the input voltage range. The ADC reference is the analog input voltage rail. The analog input channels are not designed to be used for high precision measurement tasks. The interface can be used for battery voltage monitoring (additional circuit required), ambient light sensors, or simple analog joystick input devices.

2.16.1 Analog Input Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
8	Analog Input <0>	I	Analog	3.3V	ADC input (3.3V max)
6	Analog Input <1>	I	Analog	3.3V	ADC input (3.3V max)
4	Analog Input <2>	I	Analog	3.3V	ADC input (3.3V max)
2	Analog Input <3>	I	Analog	3.3V	ADC input (3.3V max), some modules might use this input for the five-wire resistive touch interface.

Table 26: Analog Input Signals

2.16.2 Unused Analog Inputs Signal Termination

The unused analog input signals can be left unconnected or tied to the ground. It is recommended to disable the corresponding inputs in the driver or disable the whole ADC block if not used.

2.17 Parallel Memory Bus (External Memory Bus)

The Colibri form factor reserves several module edge pins as a parallel memory bus. This bus can be used for interfacing high-speed peripherals like FPGAs, DSPs, Ethernet controllers, CAN, and controllers. The supported data and address width, as well as some control signals, are dependent on the module. Some modules do not even provide a compatible parallel bus on the dedicated signal pins. Carefully check the datasheets of the modules for more information about the supported modes.

Additionally, the Pinout Designer tool can be a valuable source of information. This tool allows comparing the different bus modes and data/address widths. Special care has to be taken if a carrier board is designed for PXA270: Since the Colibri PXA270 uses the parallel memory bus also internally, it is not allowed to use the pins for anything else than for this dedicated function. Proper glue logic is needed or the pins need to be left unconnected.

2.17.1 Memory Bus Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
111	BUS_A00	O	CMOS	3.3V	Address signals. The actual available number of address signals varies by the modules.
113	BUS_A01	O	CMOS	3.3V	
115	BUS_A02	O	CMOS	3.3V	
117	BUS_A03	O	CMOS	3.3V	
119	BUS_A04	O	CMOS	3.3V	
121	BUS_A05	O	CMOS	3.3V	
123	BUS_A06	O	CMOS	3.3V	
125	BUS_A07	O	CMOS	3.3V	
110	BUS_A08	O	CMOS	3.3V	
112	BUS_A09	O	CMOS	3.3V	
114	BUS_A10	O	CMOS	3.3V	

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
116	BUS_A11	O	CMOS	3.3V	
118	BUS_A12	O	CMOS	3.3V	
120	BUS_A13	O	CMOS	3.3V	
122	BUS_A14	O	CMOS	3.3V	
124	BUS_A15	O	CMOS	3.3V	
188	BUS_A16	O	CMOS	3.3V	
186	BUS_A17	O	CMOS	3.3V	
184	BUS_A18	O	CMOS	3.3V	
146	BUS_A19	O	CMOS	3.3V	
144	BUS_A20	O	CMOS	3.3V	
142	BUS_A21	O	CMOS	3.3V	
140	BUS_A22	O	CMOS	3.3V	
138	BUS_A23	O	CMOS	3.3V	
136	BUS_A24	O	CMOS	3.3V	
134	BUS_A25	O	CMOS	3.3V	
149	BUS_D00	I/O	CMOS	3.3V	
151	BUS_D01	I/O	CMOS	3.3V	
153	BUS_D02	I/O	CMOS	3.3V	
155	BUS_D03	I/O	CMOS	3.3V	
157	BUS_D04	I/O	CMOS	3.3V	
159	BUS_D05	I/O	CMOS	3.3V	
161	BUS_D06	I/O	CMOS	3.3V	
163	BUS_D07	I/O	CMOS	3.3V	
165	BUS_D08	I/O	CMOS	3.3V	
167	BUS_D09	I/O	CMOS	3.3V	
169	BUS_D10	I/O	CMOS	3.3V	
171	BUS_D11	I/O	CMOS	3.3V	
173	BUS_D12	I/O	CMOS	3.3V	
175	BUS_D13	I/O	CMOS	3.3V	
177	BUS_D14	I/O	CMOS	3.3V	
179	BUS_D15	I/O	CMOS	3.3V	Data signals. The available data bits vary by the modules. The major part of modules only supports 16-bit data.
150	BUS_D16	I/O	CMOS	3.3V	
152	BUS_D17	I/O	CMOS	3.3V	
154	BUS_D18	I/O	CMOS	3.3V	
156	BUS_D19	I/O	CMOS	3.3V	
158	BUS_D20	I/O	CMOS	3.3V	
160	BUS_D21	I/O	CMOS	3.3V	
162	BUS_D22	I/O	CMOS	3.3V	
164	BUS_D23	I/O	CMOS	3.3V	
166	BUS_D24	I/O	CMOS	3.3V	
168	BUS_D25	I/O	CMOS	3.3V	
170	BUS_D26	I/O	CMOS	3.3V	
172	BUS_D27	I/O	CMOS	3.3V	
174	BUS_D28	I/O	CMOS	3.3V	
176	BUS_D29	I/O	CMOS	3.3V	
178	BUS_D30	I/O	CMOS	3.3V	
180	BUS_D31	I/O	CMOS	3.3V	
126	BUS_DQM0	O	CMOS	3.3V	Byte Enable Mask, corresponds to D[7:0]

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
128	BUS_DQM1	O	CMOS	3.3V	Byte Enable Mask, corresponds to D[15:8]
130	BUS_DQM2	O	CMOS	3.3V	Byte Enable Mask, corresponds to D[23:16]
132	BUS_DQM3	O	CMOS	3.3V	Byte Enable Mask, corresponds to D[31:24]
105	BUS_nCS0	O	CMOS	3.3V	Chip select signals, all required chip select signals should be pulled up on the carrier board.
107	BUS_nCS1	O	CMOS	3.3V	
106	BUS_nCS2	O	CMOS	3.3V	
91	BUS_nOE	O	CMOS	3.3V	Output Enable
99	BUS_nPWE	O	CMOS	3.3V	Buffered Write Enable
89	BUS_nWE	O	CMOS	3.3V	Write Enable
93	BUS_RDnWR	O	CMOS	3.3V	Buffered Write Enable
95	BUS_RDY	I	CMOS	3.3V	Ready/Busy/Wait signal

Table 27: Memory Bus Signals

2.17.2 Unused Memory Bus Signals Termination

All unused memory bus signals can be left unconnected. On the Colibri PXA270, the memory bus interface is also used on the module for connecting the RAM, flash, and Ethernet controller. Therefore, the bus signal pins cannot be used for any other purpose on this module. It might be possible to use the unused bus signals as GPIO or for other alternative functions on other modules.

2.18 GPIO

Many interface pins can also be used as a general-purpose input-output pin (GPIO) for alternative functions. Theoretically, any unused interface pin that serves a GPIO function can be used. Since some interface pins do not provide GPIO functionality on certain Colibri modules, there is a list of preferred GPIO pins. For compatibility reasons, we recommend using the first pin on this list. Please note that there might be additional restrictions in using the GPIO functions on certain modules. For example, two pins share the same GPIO instance and cannot be used independently of each other on some modules. More information can be found in the datasheet of the module.

2.18.1 Preferred GPIO Signals

Colibri Pin	I/O	Type	Power Rail	Description
19, 21, 23, 25, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 78, 79, 80, 81, 82, 85, 86, 88, 90, 92, 95, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 127, 129, 131, 133, 135, 137, 190, 192, 194, 196	I/O	CMOS	3.3V	General-purpose GPIO

Table 28: Dedicated GPIO Signals

2.18.2 Unused GPIO Termination

The GPIO signals do not need to be terminated if they are not in use.

2.19 Module Recovery

Recovery mode is the only officially supported method for flashing the bootloader onto Colibri modules. It is highly recommended to evaluate the need for the in-field recovery and software update functionalities in the context of the end-product at the time of designing the system.

If in-field recovery needs to be supported, it is recommended to define and implement a hardware-based solution for entering into recovery mode. In case the bootloader fails, the hardware-based solution is the only method available for entering into recovery mode.

The procedure for entering into recovery mode depends on the module. On most Colibri modules, there are solder pads that need to be shorted while powering up the main power rail. In addition, some modules provide the option for entering into recovery mode by pulling down the SODIMM pin 91. For these modules, it is advisable to add a push-button or jumper on pin 91. Please check the respective Colibri module datasheets for more details.

If the in-field recovery and software update use cases need to be supported by the end-device, it is highly recommended to make the USBC or UART_A interface available externally on the end-product.

For most Colibri modules, the USBC port (USB OTG) is used in client mode for downloading software from a host computer. Some modules, like the Colibri VFxx, use the UART_A for downloading software in recovery mode. Please check the respective module datasheets for more details.

3 Power Management

3.1 Power Supply Design

All Colibri modules can be powered with a single main power supply powering VCC, AVDD_AUDIO, and VCC_BACKUP. If the Real-Time Clock (RTC) feature is required, a low current backup power supply for the VCC_BACKUP is recommended. For better audio and ADC performance, a separate low-noise supply for the AVDD_AUDIO is recommended. The main power supply input can accept a voltage range between 3.135V and 3.465V (absolute). This allows supplying the module from a 3.3V +/-5% power supply.

The Colibri form factor is specified for a maximum sustained power consumption of up to 10W and a maximum peak power consumption of up to 15W for the SoMs.

The peak/maximum power consumption of individual SoMs depends on the use case, the silicon revision of the SoC, the versions of software components being used, and the ambient temperature, among other factors. For this reason, as a general rule of thumb, we recommend scaling the carrier board power supplies for being able to reliably deliver the maximum peak power consumption specified for Colibri modules in order to ensure compatibility with the broadest range of existing and future Colibri modules.

Do not forget to take the additional power consumption of the carrier board peripheral devices on the module power rail (3.3V) into the power budget. Most of the GPIO-capable I/O pins operate at a 3.3V logic level.

3.2 Power Signals

3.2.1 Digital Supply Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
42, 84,108, 148,182,198, 200	VCC	I	PWR	3.3V	Main power supply input for the module
39, 41, 83, 109,147, 181, 197, 199	GND	I	PWR		Signal and power ground
40	VCC_BACKUP	I	PWR	3.3V	RTC supply, connect this pin to 3.3V even if the internal RTC is not used

Table 29: Digital Supply Signals

3.2.2 Analog Supply Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
10, 12	AVDD_AUDIO	I	PWR	3.3V	Power supply for the analog part of the module
9, 11	VSS_AUDIO	I	PWR		Ground for the analog part of the module

Table 30: Analog Supply Signals

The analog power supply is used on the module for the analog circuits. 3.3 Volt needs to be provided to this input even if the analog part is not used in a design. In this case, the pins can be connected to the main power input of the module. It is recommended for better audio quality to add separate filters to the analog power supply rail. For the best quality, a separate power supply with a linear voltage regulator is recommended.

3.2.3 Power Management Signals

Colibri Pin	Colibri Signal Name	I/O	Type	Power Rail	Description
26	nRESET_EXT (CTRL_RESET_MICO#)	I	CMOS	3.3V	Active-low reset input
87	nRESET_OUT (CTRL_RESET_MOCI#)	O	CMOS	3.3V	Active-low reset output
43	CTRL_WAKE_0	I	CMOS	3.3V	Active-low primary module wake input signal, needs a pull-up resistor on the baseboard if wake function is used
22	nVDD_FAULT	I	Analog		Only available on PXA270, can be left unconnected
22	nGPIO_RESET	I	CMOS	3.3V	Only available on PXA3xx, can be left unconnected
24	nBATT_SENSE	I	Analog		Only available on PXA270 and PXA3xx, can be left unconnected

Table 31: Power Management Signals

To make the direction of the power management signals clear, the ending MICO or MOCI is added. MICO is the abbreviation for "Module Input, Carrier board Output", while MOCI stands for "Module Output, Carrier board Input".

3.3 Power Block Diagram

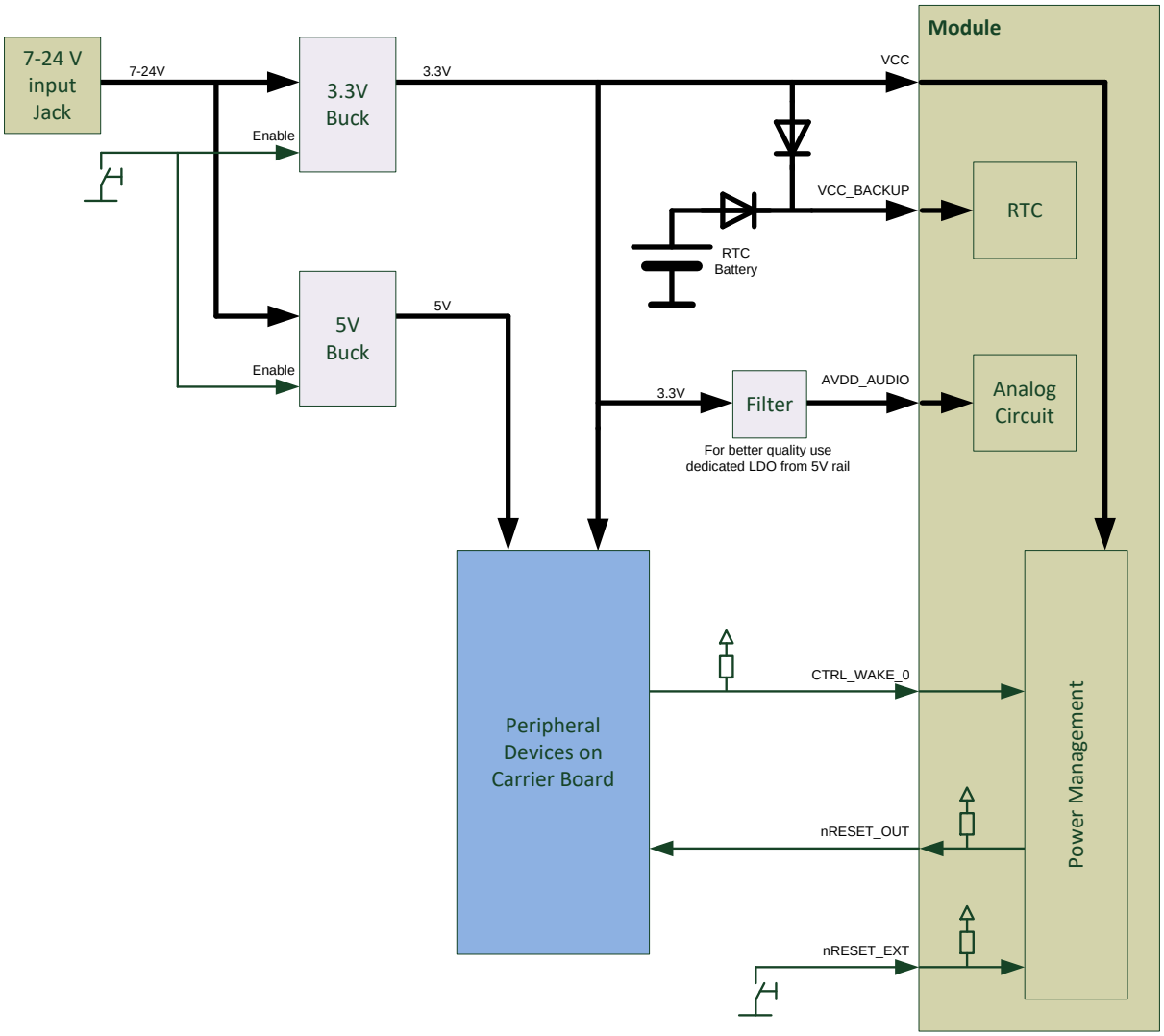

Figure 40: Power Block Diagram

If the internal RTC of the module is not used or the analog audio and resistive touch interface are not required, the carrier board power supply can be further simplified. It is crucial that even if RTC or the analog interfaces are not used, its corresponding supply rails need to be served by the carrier board.

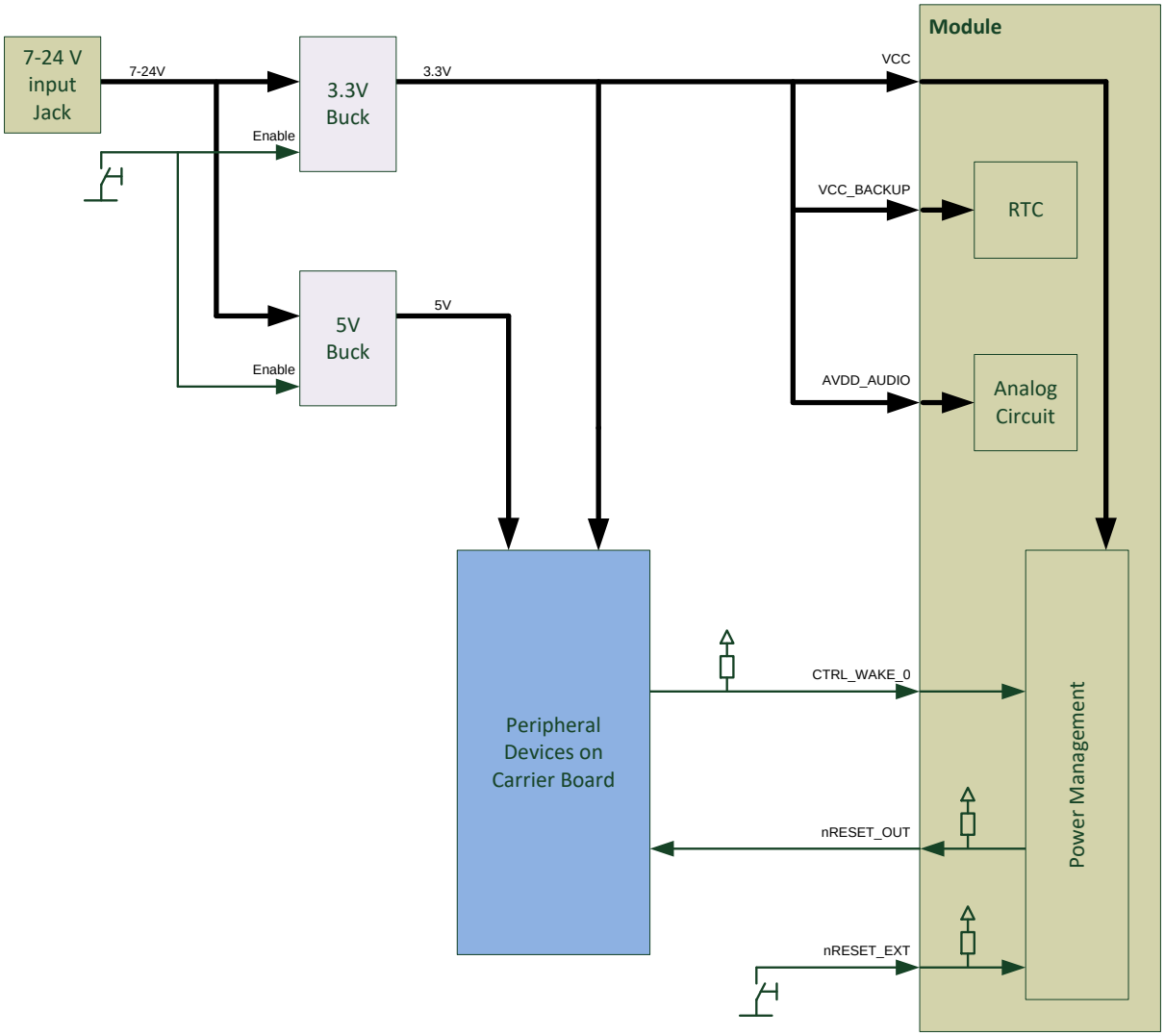

Figure 41: Power Block Diagram (without RTC and analog interfaces)

3.4 Power States

The Colibri module and carrier board have different power states. The table below describes the behavior during different states, and which power rails and peripherals are active. These are just the standard power states. If additional power saving is necessary, it is possible to introduce other states where some of the carrier board peripherals are switched off. In this case, a free GPIO can be used to switch off unused peripheral power rails.

Abbr.	Name	Description	Module	Carrier Board
UPG	Unplugged	No power is applied to the system, except the RTC battery might be available	No main VCC and AVDD_AUDIO applied. Maybe VCC_BACKUP available	No power supply input, RTC battery may be inserted
SUS	Suspend	The system is suspended and waits for wake-up sources to trigger	CPU is suspended, wake-up capable peripherals are running while others might be switched off	Power rails are available on the carrier board. Peripherals might be stopped by software
RUN	Running	System is running	All power rails are available, CPU and peripherals are running	All power rails are available. Peripherals are running
RST	Reset	The system is put in a reset state by holding nRESET low	All power rails are available, CPU and peripherals are in a reset state	All power rails are available. Peripherals are in a reset state

Table 32: Available Colibri Power States

The figure shown below shows a sequence diagram of the different power states. The module automatically goes into the running mode when the main power rail is applied to the module. In the running mode, the system can be set to be suspended by the software. There might be different wake-up sources available. Read the datasheet of the corresponding module for more information about the available wake-up events. All Colibri modules have it in common that the CTRL_WAKE_0 wakes up the module if the signal level goes low. If compatibility between the modules is needed, use this pin as the general wake signal.

Unlike the Apalis module family, the Colibri modules do not provide a shutdown state in which the module can switch off the carrier board peripheral supplies. The Colibri module does not have a dedicated signal for turning off the peripheral supplies. Nevertheless, some modules can be shut down (depending on the used operating system). In the standard carrier board architecture, all power rails remain turned on.

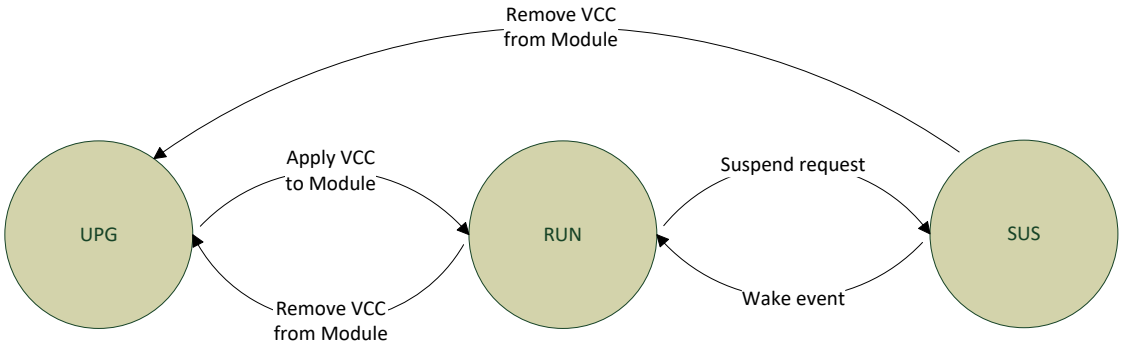

Figure 42: Power State Diagram

3.5 Power-Up Sequence

The Colibri module starts booting as soon as the main voltage rail is applied to the module. The main input voltage must rise monotonically. The RTC rail (VCC_BACKUP) needs to be applied before or together with the main voltage. It is not allowed to apply the analog voltage supply before applying the main voltage.

The peripheral power rails on the carrier board need to be ramped-up in a correct sequence. The sequence starts typically with the highest voltage (e.g., 5V) followed by the lower voltages (e.g., 3.3V, then 1.5V, and so on). Peripherals usually require that a lower voltage rail is never present if a higher rail is missing. Check the datasheet of all peripheral components on the carrier board for proper sequencing.

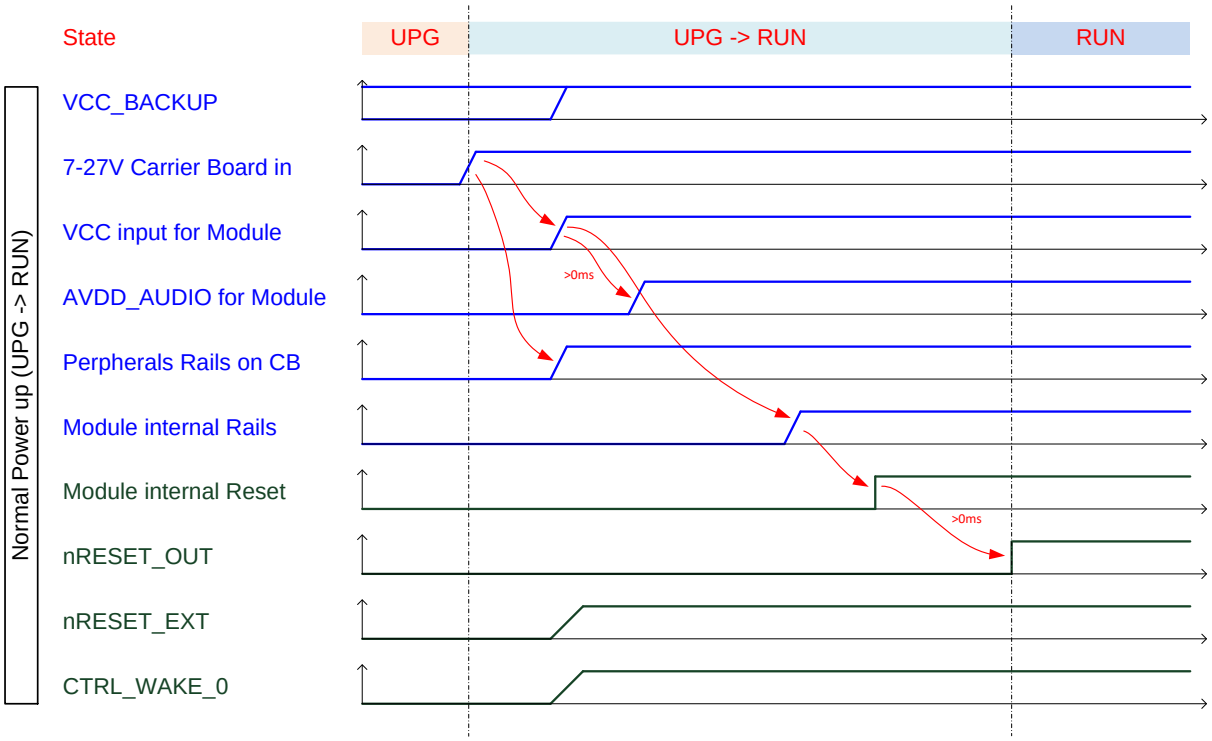

Figure 43: Power-Up Sequence

3.6 Reference Schematics

Place enough power supply bypass capacitors to the voltage inputs of the peripheral devices (see Toradex Layout Design Guide). Place a bypass capacitor to each power input pin of the Colibri module. Be aware of the total capacity on a voltage rail when switching the voltage. If the rails are switched on too fast, the current peaks for charging all the bypass capacitors can be very high. This can produce unacceptable disturbances or can trigger an overcurrent protection circuit. Maybe the switching speed needs to be limited. The following figure shows a simple voltage rail switch circuit. C1 and R1 limit the switching speed. The values need to be optimized according to the requirements. It is recommended to place a bypass capacitor (C2) close to the switching transistor.

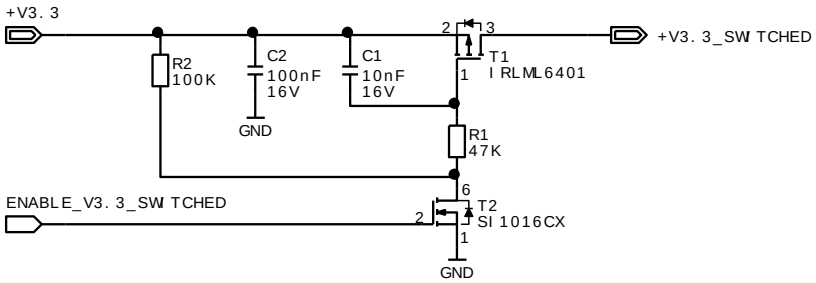

Figure 44: Simple Voltage Switch Circuit

To satisfy the in-rush current during the start-up of a Colibri module, we recommend using bulk capacitors of about **450µF** in total on the main 3.3V power supply.

The nRESET_EXT and nRESET_OUT do not need any pull-up resistors on the carrier board since these resistors are already placed on the module. The CTRL_WAKE_0 requires a pull-up resistor on the carrier board if the wake function is implemented.

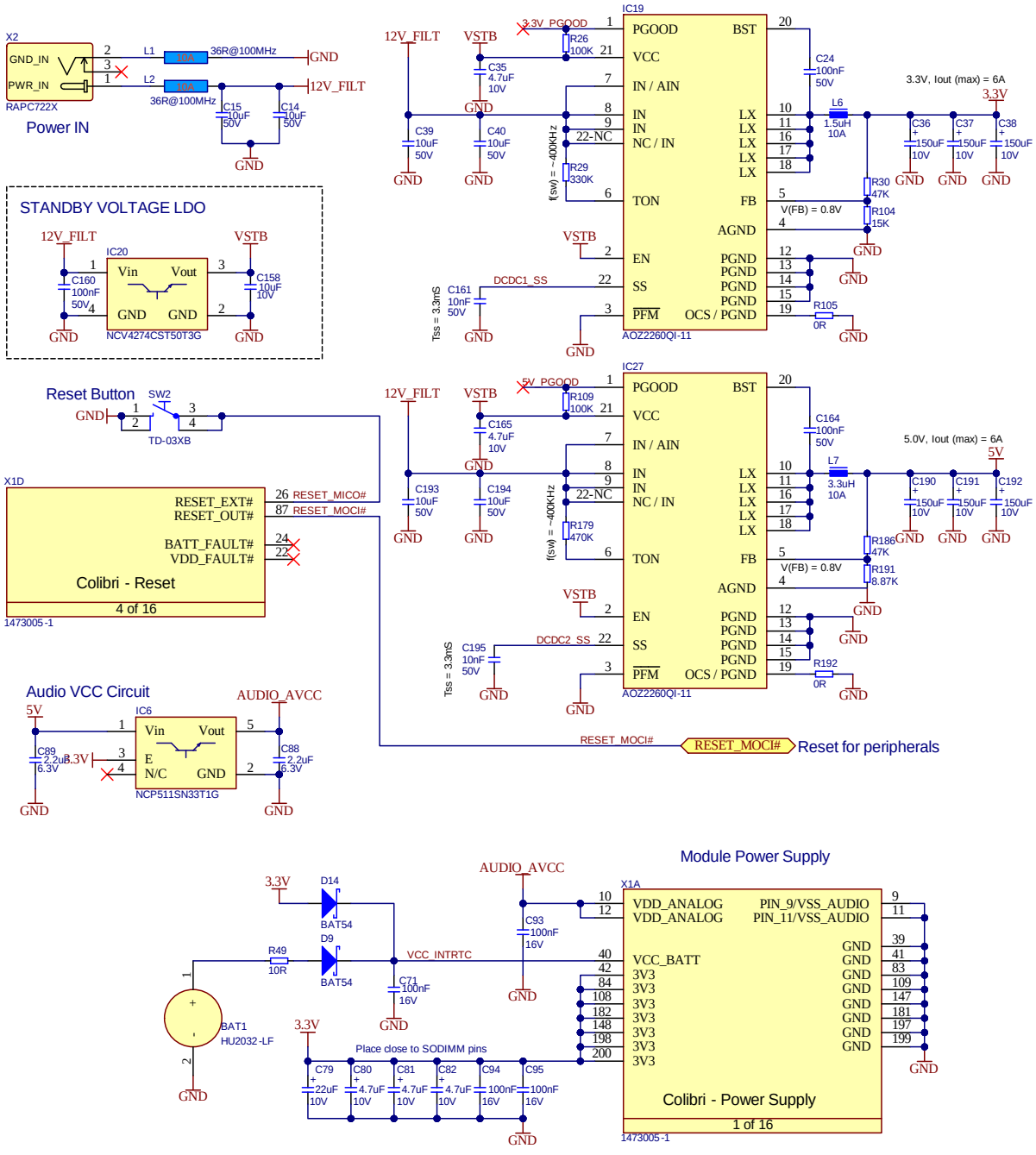

Figure 45: Simple Power Supply Reference Schematic

Please note: Integrated buck converters with a rating of 6A are used in the reference schematics. Converters with a lower current rating are suitable depending on the carrier board power budget.

3.7 Backfeeding

3.7.1 Introduction

Backfeeding is sometimes also called backflow. Backfeeding is an unintentional and irregular flow of current mainly over the signal path. It can happen if interfaces are crossing different power domains. Backfeeding can happen between circuit blocks powered by or switched by different power rails (power domains) and thus transitioning through different power states over time. A domain that is still powered can feed another power domain. This can lead to residual voltages on a power rail that is supposed to be turned off.

The most obvious consequences of backfeeding are increased power consumption, unexpected behaviors, failing power-on resets, and in the worst-case, damages of interfaces. This section discusses why backfeeding occurs, how it can be identified, and potential preventions of backfeeding in a Colibri carrier board design.

Interfaces that are prone to backfeed are UART, RS232, VGA, HDMI, and I2C. Therefore, special attention is required to these interfaces when designing a carrier board for the Colibri module.

3.7.2 What is Backfeeding

Backfeeding is sometimes also called backflow. To understand what backfeeding is, we need to look at the internal circuit of an input pin. Most Colibri module pins (and also peripheral device input pins) feature ESD protection diodes. These protection diodes provide basic protection for electrostatic discharge. Depending on the SoC and peripheral devices, the pins are typically only protected up to 1kV (Human Body Model) or 250V (Charged-Device Model). This means additional ESD protection is still needed for signals that are exposed to the real world. The basic ESD protection is usually accomplished with two (Schottky) diodes. One diode is between the pin and the ground, and a second between the pin and the power rail of the I/O block (IO rail). These diodes are the reason why for a lot of IO pins, the absolute maximum voltage is specified as VDD+0.3V.

Figure 46 shows a typical low-speed SoC input pin with ESD protection diodes. If the IO rail and the peripheral rail are turned on, these ESD diodes are not conducting. The diodes can basically be ignored. There is a small current flowing from the peripheral output to the input buffer of the SoC. This is not backfeeding. This is a regular signal current.

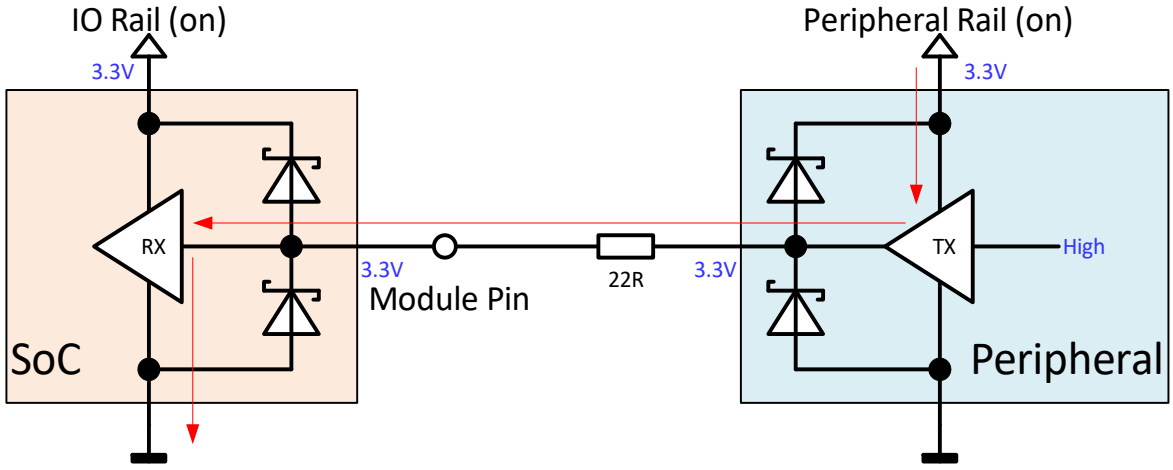

Figure 46: SoC input pin with ESD protection, both power rails on

But what happens if the on-module IO rail is turned off while the peripheral rail is still on and the peripheral signal is set to high? In this situation, there is a non-marginal current from the output buffer of the peripheral interface into the SoC input pin. Since the IO rail is turned off, the upper ESD protection diode of the input pin becomes forward-biased. The current flows through the

diode to the IO rail pin. In other words, the IO rail gets fed through the IO pin. This is called backfeeding. Figure 47 shows a backfeeding path and possible voltage values. Depending on the situation, the backfeeding can reach several milliamperes. Therefore, the output buffer of the peripheral signal already has some voltage drop. In the example, the drop in the buffer is 1V. This means the output voltage is only 2.3V. Some voltage is lost in the series resistor. Therefore, only 2.0V arrives at the SoC input pin. There is a further voltage drop in the ESD protection diode. 0.3V is a typical value for a Schottky type diode. In this example, the backfeeding path lifts the IO rail to 1.7V, even though the power supply is turned off. Of course, the actual resulting IO voltage is heavily dependent on the load on the IO rail and the backfeeding path and the number of pins that are backfeeding.

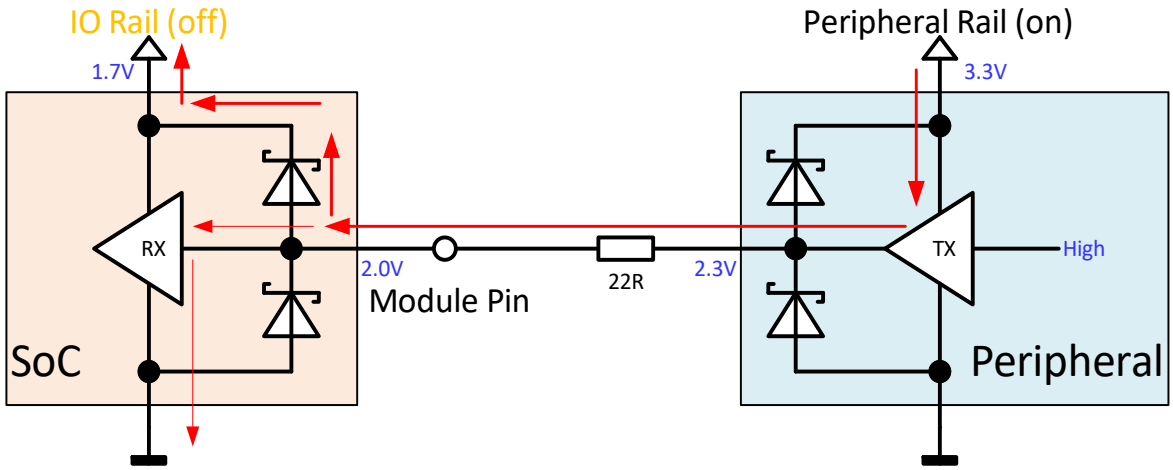

Figure 47: Backfeeding if IO rail is off and the peripheral signal is high

Open drain signals can also cause backfeeding if the pull-up resistor is still powered while the IO rail on the module is off. However, the backfeeding currents are more likely much smaller than with a regular push-pull peripheral output pin. The pull-up resistor value limits the current.

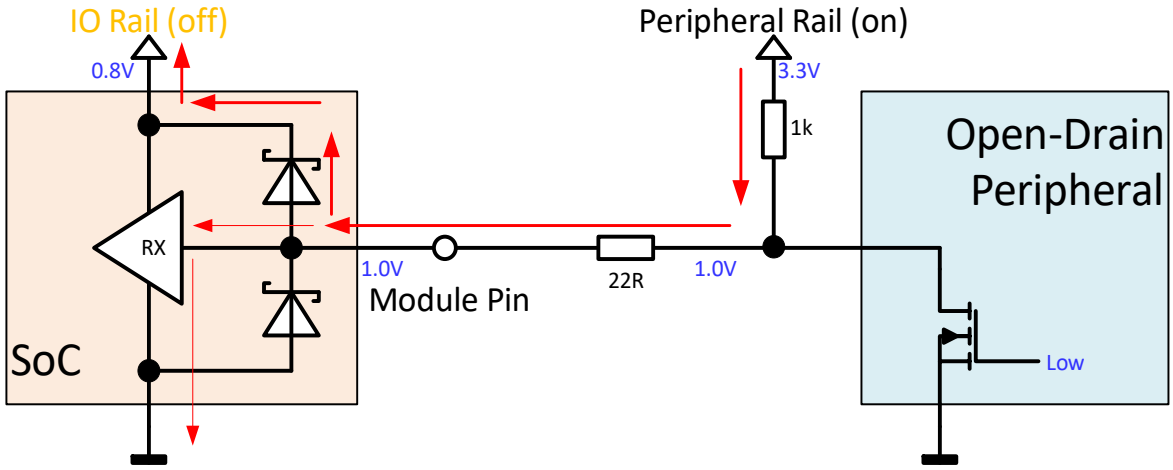

Figure 48: Backfeeding with open-drain signals

Interfaces that are prone to backfeeding are, for example, UART and HDMI. The problem is that the UART signals are high in idle. If the transceiver is not switched off when the module is shut down, there is potential backfeeding. The transition-minimized differential signals (TMDS) of the HDMI interface are terminated to 3.3V at the receiver side (e.g., a display). Therefore, the signals have a DC offset. Even if the module and carrier board are turned-off, the TMDS signals can be lifted to 3.3V by the monitor. If an improper HDMI circuit is used, this can cause backfeeding. The DDC and the hotplug detection signal can cause further backfeeding in combination with an HDMI monitor.

Besides the HDMI DDC, I2C interfaces, in general, can be sources for backfeeding if the pull-up resistor is using a different voltage domain than the module IO rail. Due to the pull-up resistor value, the current usually is smaller than with regular CMOS signals. However, with backfeeding, the amount of interface pins that are backfeeding signals is essential. If a system has many open-drain signals backfeeding, this can still lead to problematic high IO rail voltage.

Backfeeding can also happen in the other direction. For saving energy, unused peripherals are often turned off by switching off their power rails. If the module output signals are still driven high, the module can feed back the peripheral rail.

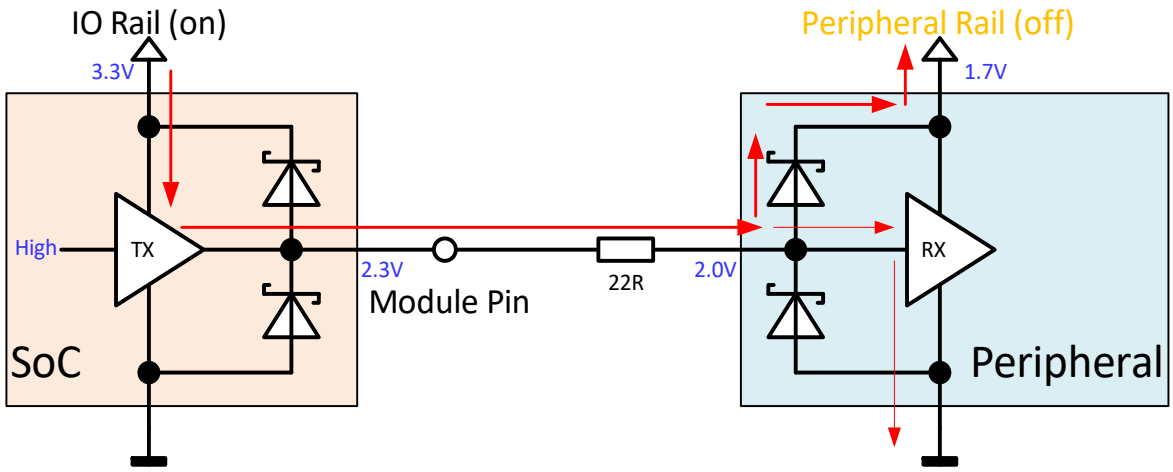

Figure 49: Backfeeding to peripherals

3.7.3 Potential Issues Caused by Backfeeding

In many systems, it is difficult and expensive to avoid backfeeding altogether. Various issues could be caused by backfeeding. For example, the resulting backfeeding current could overload the output driver of the signal that is causing the backfeeding. If the backfeeding path has series resistors, the current might get limited to a non-damaging value. Series resistors also allow for checking the backfeeding current by measuring the voltage drop over the resistor. A high continuous backfeeding current can also damage the ESD protection diode. Standard on-chip ESD protection diodes are characterized to withstand tens of amps for nanoseconds, but not continuously. Continuous current through the protection diode causes power dissipation, which can be above the diode's limits. However, a few milliamperes are usually neither damaging the ESD protection diode nor the output driver. Please check whether there any information available in the SoC and peripheral datasheets.

Even if the resulting input current of a pin is small enough not to damage the ESD protection diode, the absolute maximum input voltage specifications are violated in many cases. An input pin's absolute maximum input voltage is often specified by a similar formula:

$$V_{in\,max} = V_{DD} + 0.3V$$

The ESD protection diode dictates the 0.3V in this formula. According to the device specifications, the input voltage always needs to be small enough for not having the protection diode conducting. This means backfeeding is often per se violating the maximum input voltage specifications. Therefore, the manufacturer does not guarantee that backfeeding is not damaging the device.

Damaged input or output signal paths due to backfeeding current are usually a minor problem. Issues caused by a residual voltage on a turned-off IO rail are often more pronounced. If the IO rail reaches a certain voltage level, other devices on the same rail might show unexpected behavior. Especially if the voltage level reaches the power-on-reset threshold, devices (or blocks of devices) might start to run. This could lead to a higher current draw on the backfeeding path, which could lower the voltage again. This could cause cyclical behavior in which devices are

oscillating between starting and crashing. Such behavior could result in higher overall power consumption or even audible noise of power converters. Some LEDs may slightly light up or start blinking.

Backfeeding can cause latch-up situations. IO blocks can go into unintended states, which might even cause short-circuits that could lead to further chip damages if countermeasures are not taken.

If the IO rail reaches a certain voltage level, it could mean that some power-on-reset circuits are not triggering when fully turning on the power rails since the reset was already released. This can cause devices and peripherals to stay in unintended/unpredictable states and might fail to boot the system. The system could be locked up by backfeeding.

Whether backfeeding is actually causing issues or not depends on the backfeeding current and its residual voltage on the IO rail. It also depends on the specific chip design. The lower the current per backfeeding pin is, the smaller the chance of damage is. The lower the remaining voltage on the IO rail is, the smaller the chance of unexpected behavior is. As a rule of thumb, a few milliamperes are unlikely to cause damages to an IO pin. If the resulting IO rail voltage is below 0.5V, issues are often not to be expected. However, these are just rough numbers. The actual limits are heavily depending on the system and the actual devices in use.

3.7.4 Identify Backfeeding Issues

3.7.4.1 System Design

Ideally, potential backfeeding issues should be identified in the design phase of a carrier board, not in the prototype phase. A power delivery block diagram can help to identify different power domains. A power domain is a group of devices or peripherals which are always in the same power state. Figure 50 shows a simple example of a system block diagram. The Colibri module and the RS232 transceiver are not in the same power domain. The transceiver uses the 3.3V rail, which can still be enabled while on the Colibri module, the IO voltage rails are turned off. However, the behavior of the module IO voltage rail depends on the Colibri module.

In this example, the SD card also has its own power domain since the SODIMM pin 100 might be used for individually control the card power. Also, external devices like a VGA display or the host PC must be considered as separate power domains. These peripheral devices are powered independently from the Colibri carrier board.

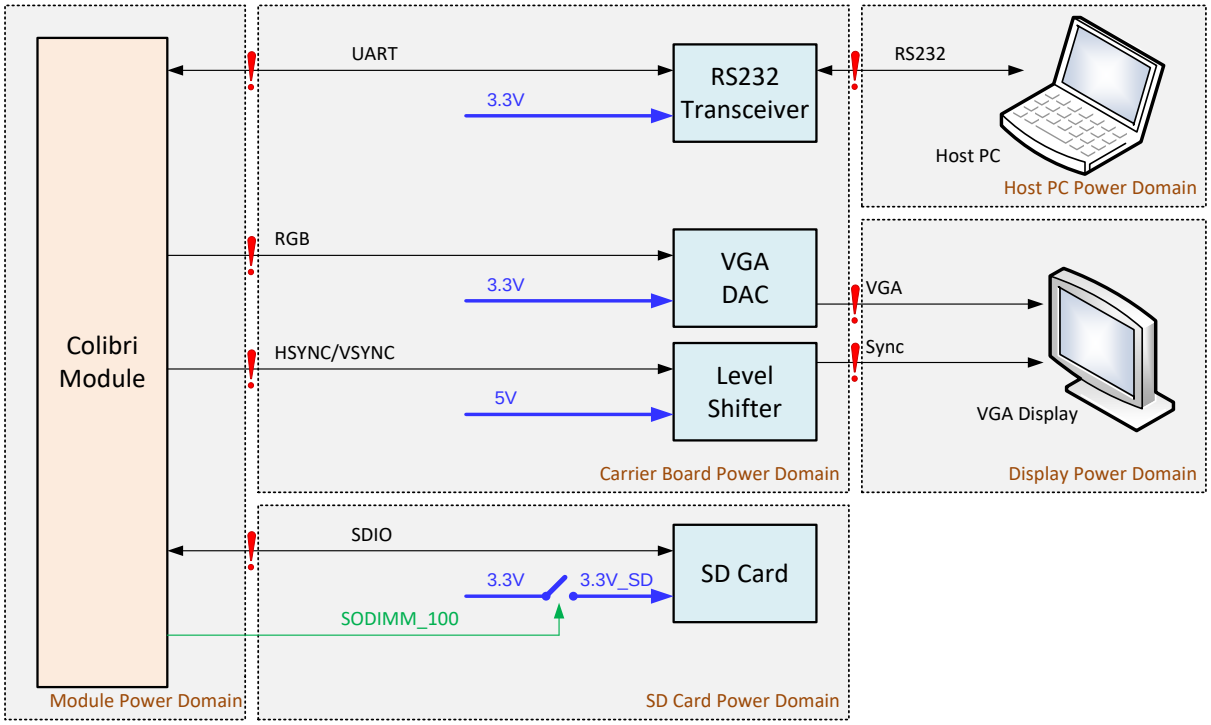

Figure 50: Power Domain Example

Each time a signal crosses the boundaries of power domains, you need to check whether backfeeding could be an issue. For each signal, check whether the output is driven high while the other side's power domain is turned off. In the example above, we need to check whether the software drives and SD card signal driven high or pulled-up while the SD card power rail is turned off. Otherwise, the module can back feed to the card. The signal states of the external devices like the RS232 signals of the host PC or the VGA display's sync signals are hard to control by the Colibri module and the carrier board. Therefore, it might be required to take other countermeasures for preventing the backfeeding of these interfaces.

3.7.4.2 Prototype Testing

For identifying backfeeding on a system with a Colibri module, it is recommended to measure the IO rails of the different power domains in different scenarios. Different scenarios mean testing different power states of the systems with different types of peripheral devices plugged in and turned on. If you can measure any significant residual voltage on an IO rail, further investigations are required for identifying the source of the backfeeding.

The first option is to unplug external peripherals and observe the residual voltage. If the voltage drops, the peripheral signals are likely a source of backfeeding. If you measure residual voltage in one power domain, all the input signals crossing this domain should be checked. Measure the voltage levels on these inputs. A pin that is the source for backfeeding has a higher voltage than the residual voltage on its IO rail. Typically, due to the protection diode in the backfeeding path, the voltage at the input pin is around 200mV to 300mV higher than the residual voltage (see Figure 51)

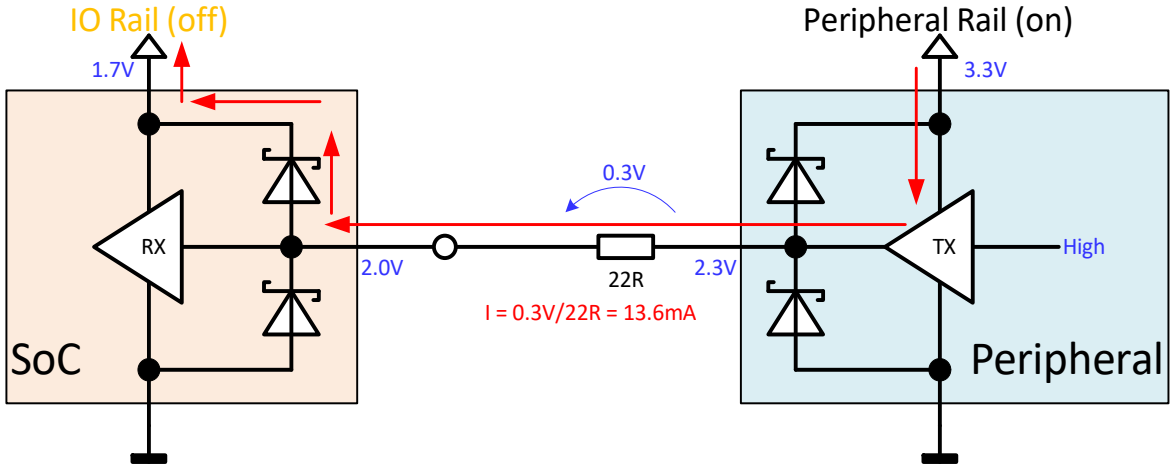

Figure 51: Measuring backfeeding current

If a signal features a series resistor, the voltage drop can be used to measure the backfeeding current. Some signals might not have a series resistor for measuring the current. By adding a load resistor to the backfeeding signal (for example, a 180Ω resistor), the voltage with and without extra load can be measured. This allows to estimate the internal resistance of the driver by using the following formula:

$$R_i \approx \frac{(V_{no\ load} - V_{load}) \cdot R_{load}}{V_{no\ load}}$$

With the help of the estimated internal driver resistance, the backfeeding current on the pin can be estimated by using the following formula ($V_{peripheral\ IO\ rail}$ is the peripheral rail voltage, $V_{backfeeding}$ is the voltage on the signal without the extra load resistor):

$$I_{backfeeding} \approx \frac{(V_{peripheral\ IO\ rail} - V_{backfeeding})}{R_i}$$

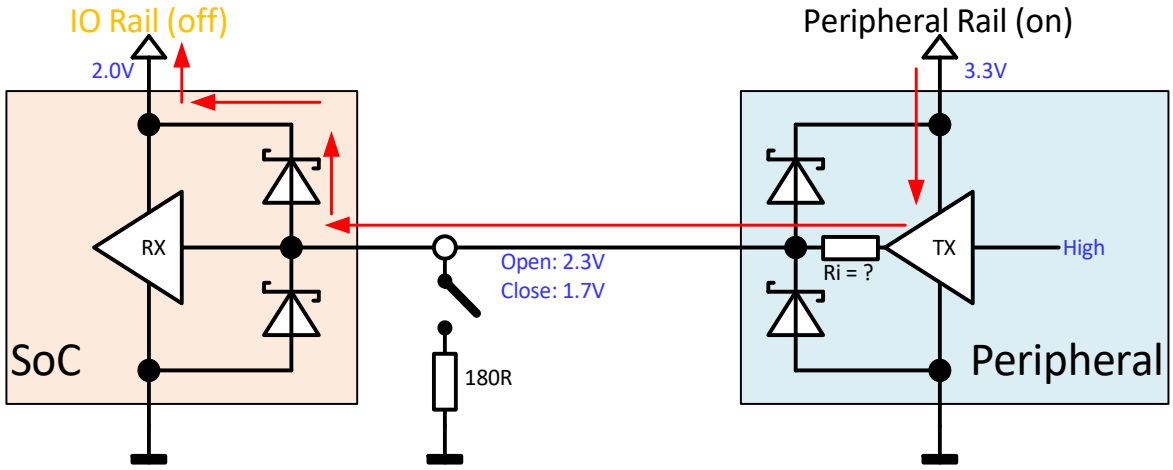

Figure 52: Evaluating the internal resistance of the driver

With the help of these formulas, the measured values in Figure 52 would lead to the following internal resistance and backfeeding current:

$$R_i \approx \frac{(2.3V - 1.7V) \cdot 180\Omega}{2.3V} = 47\Omega$$

$$I_{backfeeding} \approx \frac{(3.3V - 2.3V)}{47\Omega} = 21mA$$

Often it is crucial to know whether all the backfeeding pins are identified, or the search for backfeeding sources must continue. Ideally, you might be able to disconnect individual pins by removing series resistors or a jumper (for example, possible on the Colibri Evaluation Board). Unfortunately, this is not always the case. However, there is another method for estimating the number of backfeeding pins.

By adding a load resistor to the IO rail and observing the residual voltage changes, the total internal resistance of the backfeeding can be estimated. A good value for the load resistor is 100Ω. You might need to select a different value if the voltage is dropping too little or too much. The best values can often be achieved by a voltage drop between 50mV and 100mV. The formula for estimating the internal resistance is the same as used for the individual pin. Assuming the voltage drop over the ESD diode is constant, the diode voltage drop is eliminated from the formula. Please keep in mind that this formula only provides a rough estimated value. There might be devices on the IO rail which behave non-linear to voltage changes. Therefore, the forced voltage change should be kept small for better results.

$$R_{i\,total} \approx \frac{(U_{no\,load} - U_{load}) \cdot R_{load}}{U_{no\,load}}$$

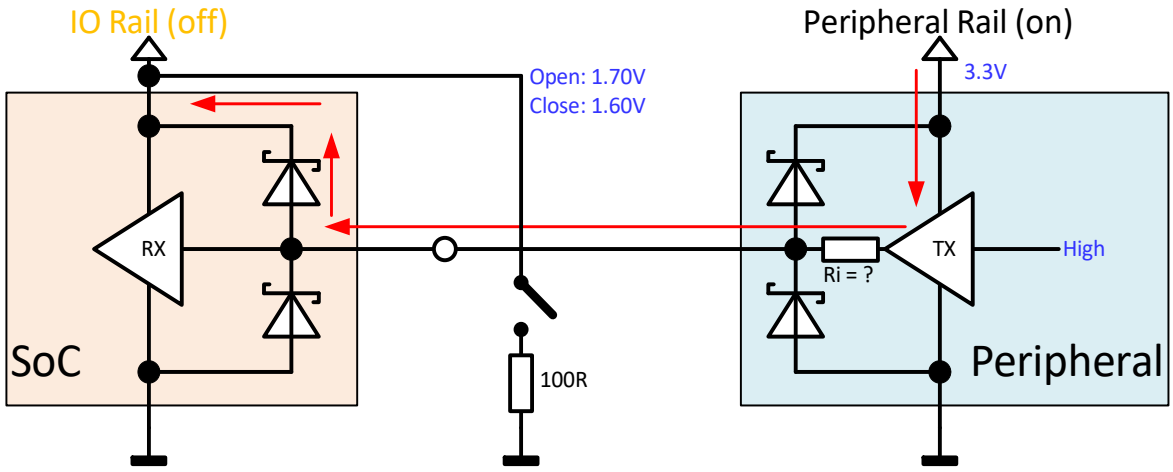

Figure 53: Evaluating the total internal resistance of the backfeeding

Using the numbers in Figure 53 as an example, we get the following total internal resistance:

$$R_{i\,total} \approx \frac{(1.70V - 1.60V) \cdot 100\Omega}{1.70V} = 5.9\Omega$$

The total internal resistance measured on the IO rail can then be compared to the estimated internal resistance of the backfeeding IO pins. If the total resistance is smaller than the combined resistance of the IO pins, there are still other backfeeding sources to be uncovered.

Comparing the results from Figure 52 and Figure 53, we see that the total internal resistance is about eight times smaller than a single signal pin. This means there are probably a total of eight (similar) signal pins that are backfeeding to this IO rail.

3.7.5 Backfeeding Prevention

There are multiple approaches for preventing backfeeding from happening. Some of them are very cost-effective but do not apply to all types of signals or situations. Other solutions are expensive or require extra precious PCB real estate. Therefore, defining the right backfeeding prevention approach is challenging. The following list of potential solutions starts from the cheap and

straightforward approaches and stretches to the complicated and expensive ones. This is not a complete list. There exist other solutions that are not discussed here. Some backfeeding countermeasures are specific to an interface. Therefore, following the reference schematics is advised.

3.7.5.1 Avoid Multiple Power Domains

The best solution for preventing backfeeding is trying to avoid having different power domains. Try to use the same voltage for the IO rail and the peripheral devices. For some Colibri modules, the IO rail is identical to the module's main power supply (VCC). For such modules, it is advised to use the same power source also for the peripherals.

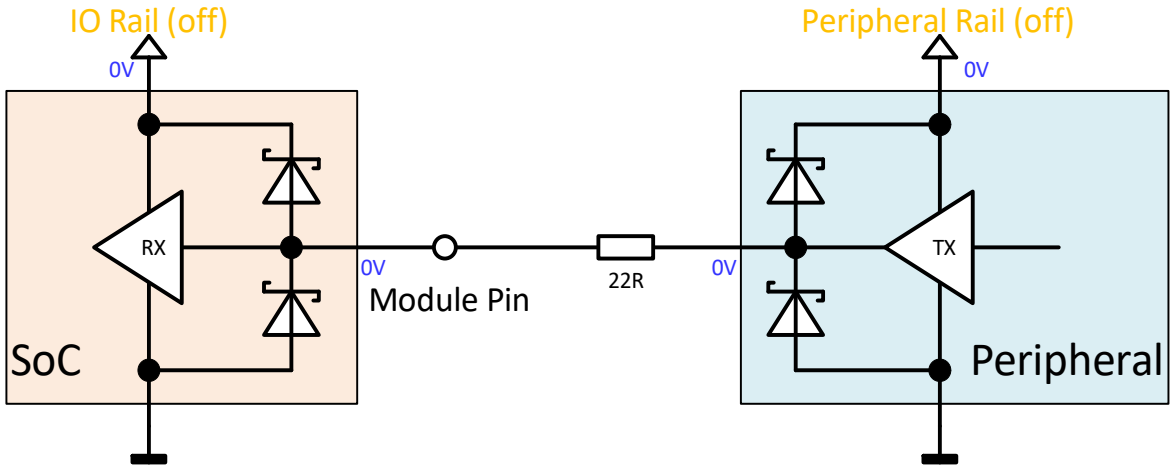

Figure 54: Keep the peripherals on the same Domain

3.7.5.2 Avoid Driving Outputs High

Backfeeding can be prevented by ensuring the output pin is not driven high while the IO rail of the input side is powered off. This is a standard solution for preventing backfeeding from the module to peripheral devices. Before disabling the peripherals' power rails (for example, when going into sleep mode), the software makes sure that the output signals are either driven low or set into a high-Z mode. Some SoC pins have internal pull-up resistors. It is also important to switch off the pull-up resistors and optionally enable the pull-down resistor.

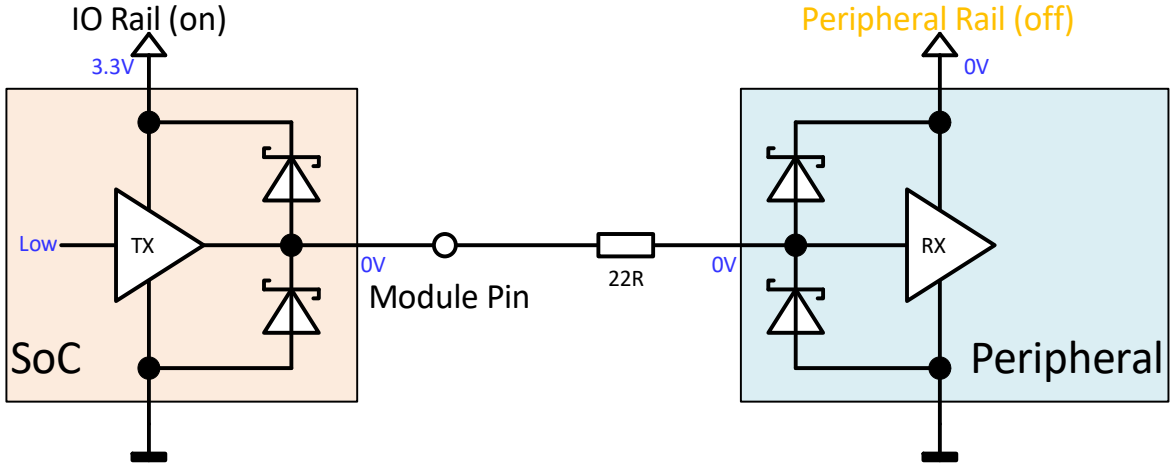

Figure 55: Make sure outputs are not driven high

3.7.5.3 Inputs without Backfeeding Path

Certain interfaces have different input circuits that are not prone to backfeeding or are having backfeeding prevention built-in. Some interfaces use a different ESD protection approach and therefore do not offer a backfeeding path. An example of an interface with built-in backfeeding prevention is the USB interface of the Colibri module. The USB cable can be connected to a powered peripheral or host device, even if the Colibri module is powered off. In this situation, the USB 2.0 data signals could be pulled up to 3.3V on the attached device. The Colibri module already prevents backfeeding over the USB data signals. Therefore, no further backfeeding prevention is required for the data signals on the carrier board.

Whenever you are selecting peripheral devices, it is advised to check whether the input pins of the device have any built-in protection again backfeeding. Using such a device can eliminate complicated external circuits required for backfeeding prevention.

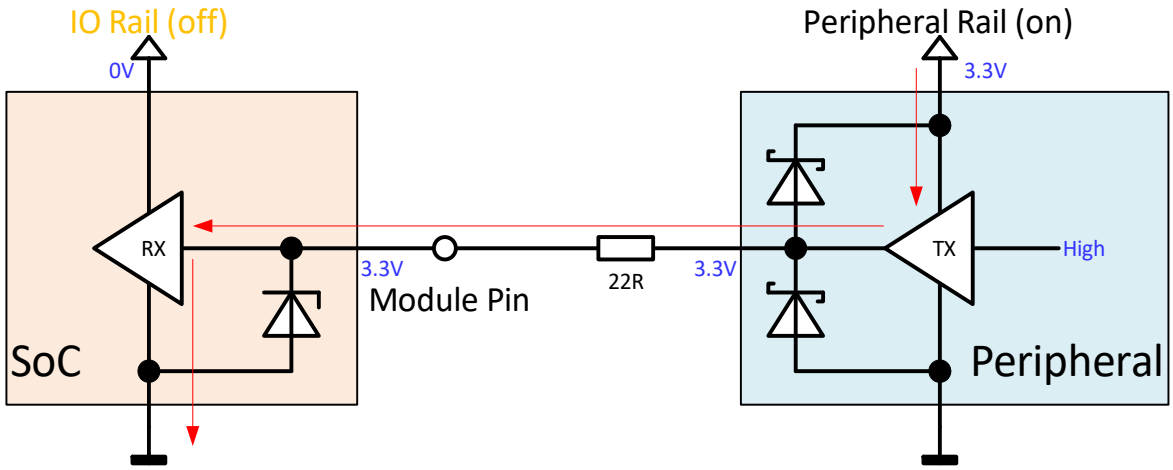

Figure 56: Input without backfeeding path

3.7.5.4 Series Resistor

For low-speed signals, a simple and cost-effective method can be using a higher value series resistor. Of course, this only works if the input impedance is big enough and the parasitic capacity is small enough (in order not to degrade the signal quality). The series resistor does not eliminate backfeeding entirely, but it limits the current and, therefore, also the residual voltage.

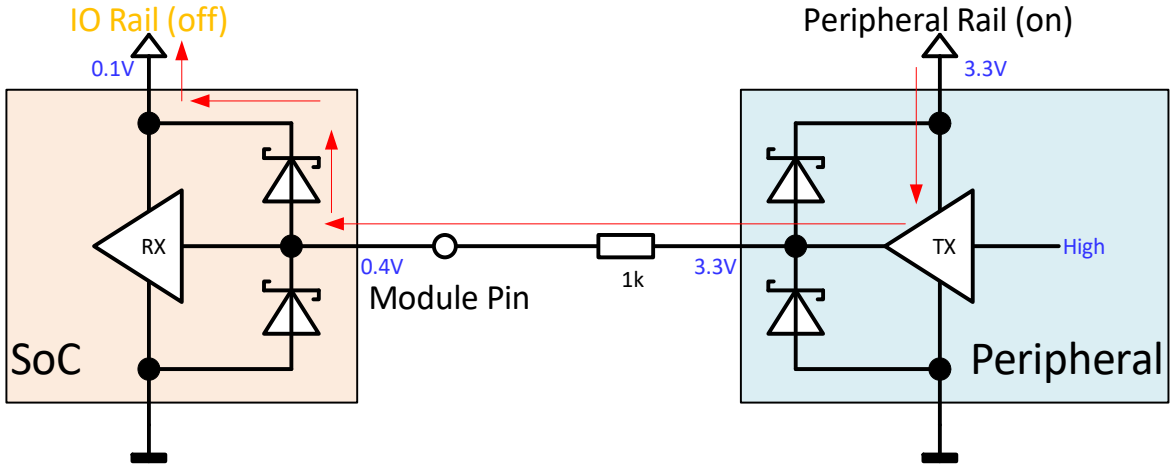

Figure 57: Series resistor for limiting backfeeding

3.7.5.5 Open Drain Signals

When using open-drain signals, it is crucial to use the correct voltage domain for the pull-up resistor. In Figure 48, the peripheral rail is used, and therefore backfeeding occurs. By using the same voltage domain for the pull-up resistor as the input side, backfeeding is eliminated. When using a computer module, using the IO rail might not be feasible. In this case, it might be necessary to use a power rail that switches off together with the on-module IO rail. One option for switching such a rail is using a free module GPIO. Make sure the GPIO is low by adding a pull-down resistor on the carrier board.

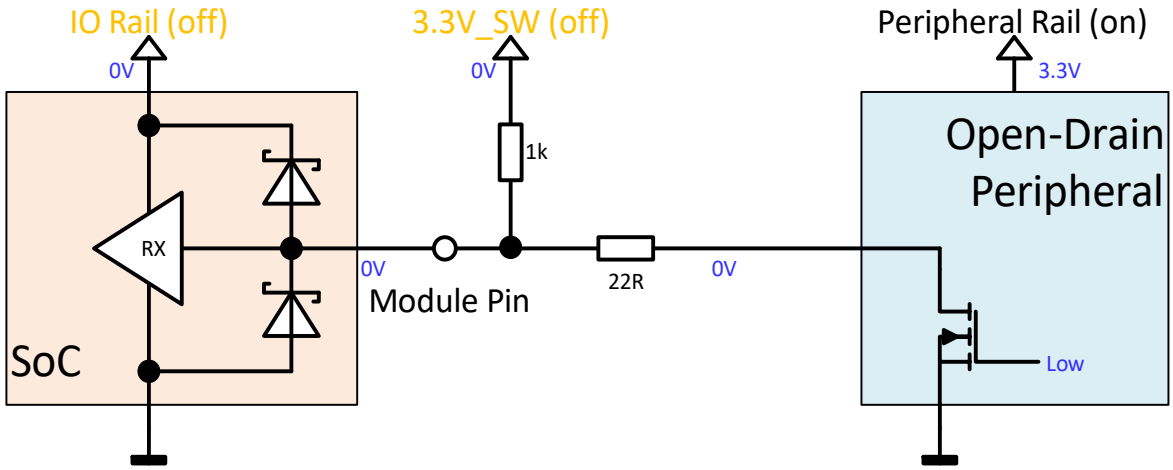

Figure 58: Correct pull-up rail for open-drain signals

Most SoC pins feature configurable internal pull-up resistors. If the pull-up value is strong enough, a good solution is to use these resistors instead of external ones. The internal pull-up resistors are perse on the correct IO rail and therefore are not backfeeding.

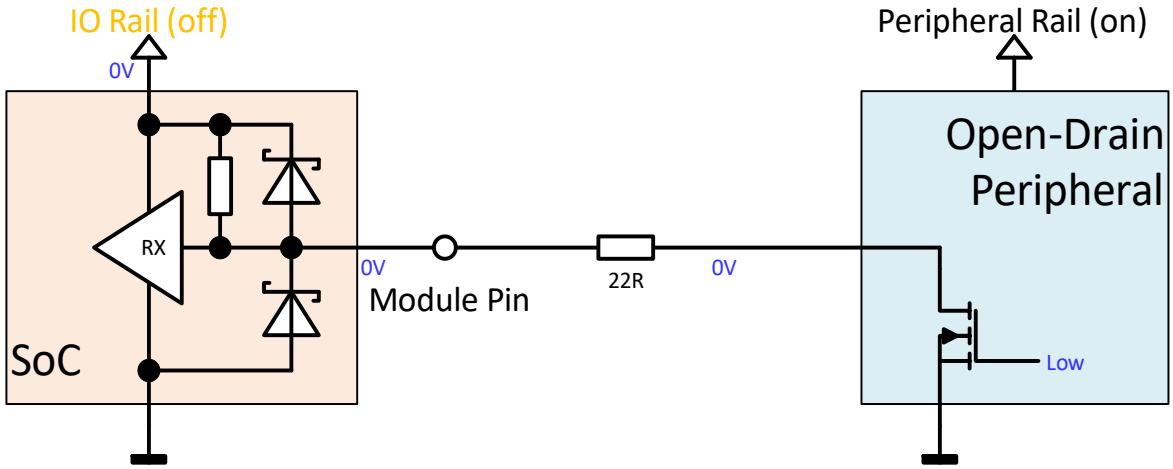

Figure 59: Using internal pull-up resistor

3.7.5.6 Simple FET Circuit for Open-Drain Signals

Sometimes, it is impossible to move the pull-up resistor to the IO rail domain since there is already a pull-up resistor on the peripheral rail. Maybe this pull-up resistor is inside the peripheral device and cannot be switched off. The simple FET circuit in Figure 60 can offer a solution for blocking backfeeding. This circuit also works for bidirectional open-drain signals such as I2C and can be used as a low-cost level shifter.

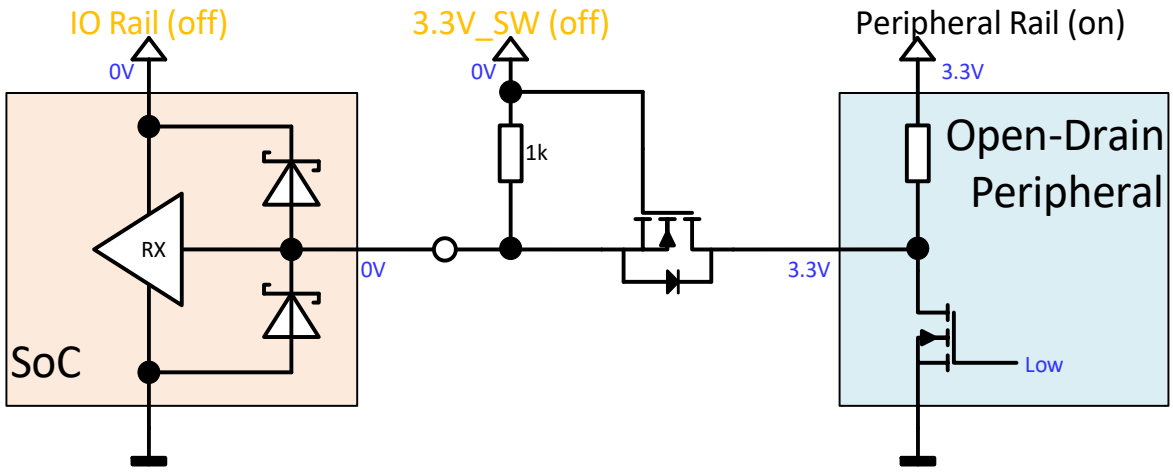

Figure 60: Simple FET circuit for open-drain signals

3.7.5.7 Blocking Diode

Another solution for low-speed signals is to use a diode and a pull-up resistor for blocking backfeeding. The pull-up resistor must be on the same voltage domain as the IO rail of the input side. Most SoC GPIO pins have configurable internal pull-up resistors. This can eliminate the need for an external resistor. The advantage of the internal resistor is that it is using the correct IO rail. The biggest drawback of this solution is that the low level of the signal is increased. Therefore, using a Schottky diode is recommended due to the smaller forward voltage drop. Make sure the specified maximum low level of the input pin is not violated.

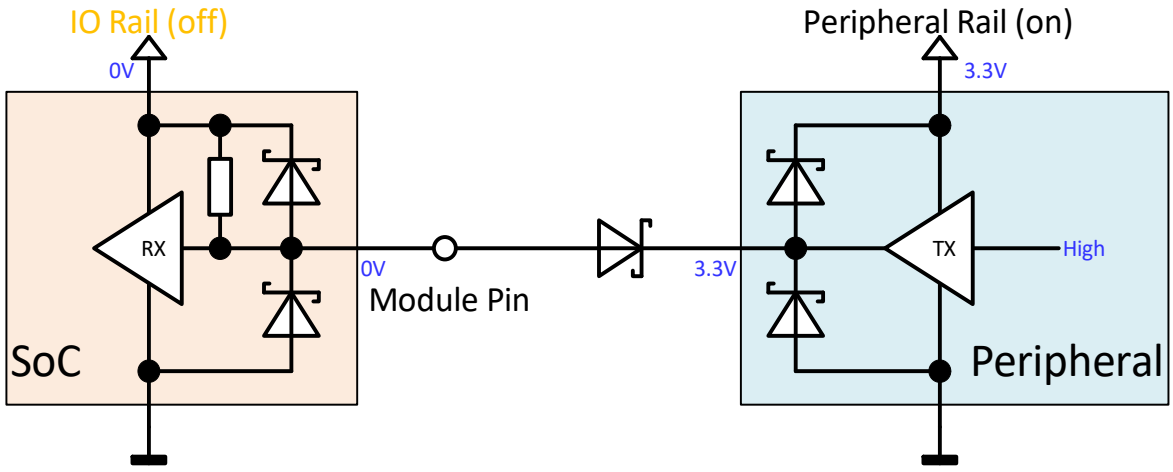

Figure 61: Diode circuit for backfeeding prevention with an on-chip pull-up resistor

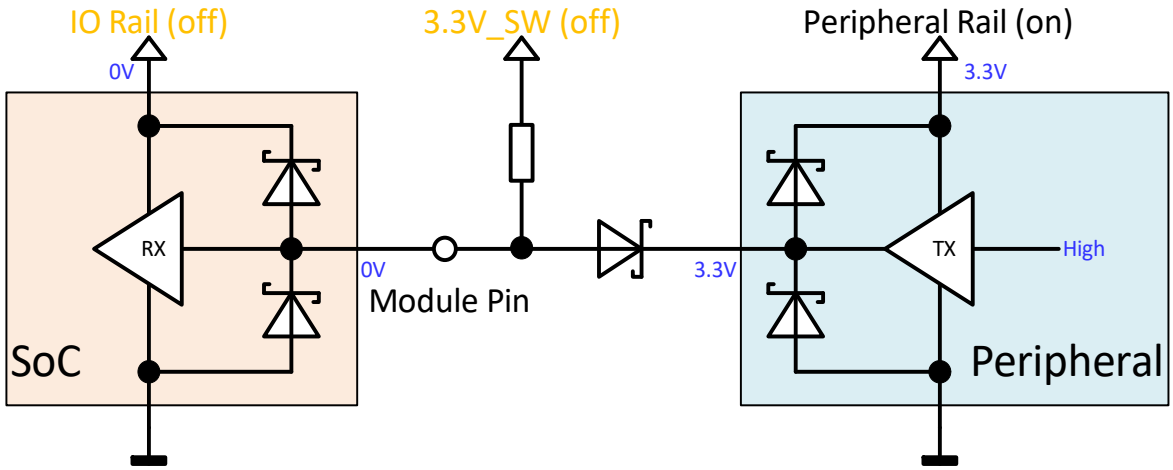

Figure 62: Diode circuit for backfeeding prevention with an external pull-up resistor

3.7.5.8 Capacitive Coupling

Some high-speed signals allow (or require) capacitive coupling. Capacitive coupling blocks all DC current and eliminates backfeeding caused by a DC offset of high-speed signals. Most high-speed interfaces and differential clocks (e.g., LVPECL, CML) use capacitive coupling nowadays. Typical signals using capacitive coupling are PCIe, SATA, DisplayPort, and the SuperSpeed signals of USB.

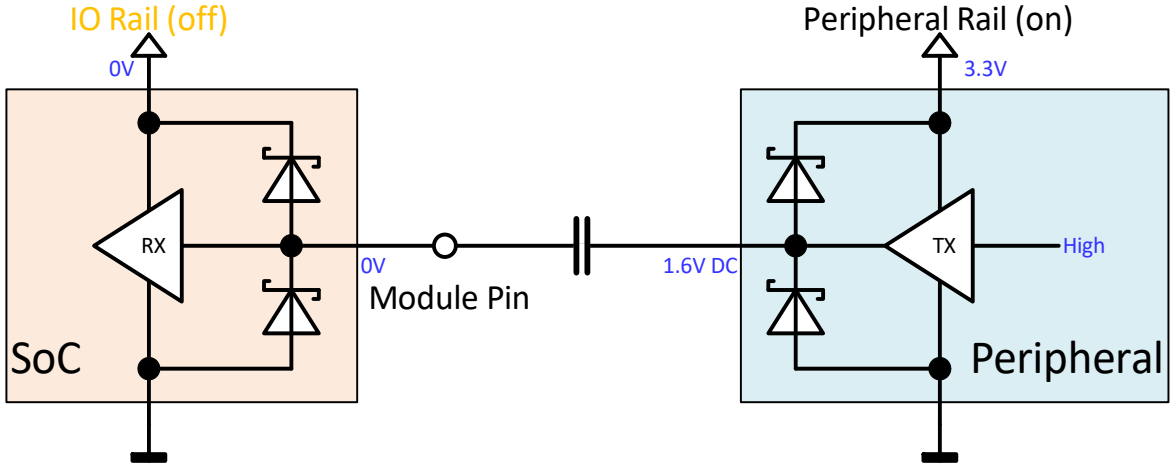

Figure 63: Capacitive coupled signals

3.7.5.9 Non-Backfeeding Buffer

Placing an additional buffer in the signal path can prevent backfeeding. The buffer needs to be powered from the same domain as the rail of the input. If the Colibri module is the signal input, using a power rail that is switched by a module GPIO as the buffer's power supply is advised. Noteworthy, the buffer should not have an ESD protection circuit at its input that allows for backfeeding. Otherwise, the signal would back feed to the module domain, and the whole circuit would lose its purpose.

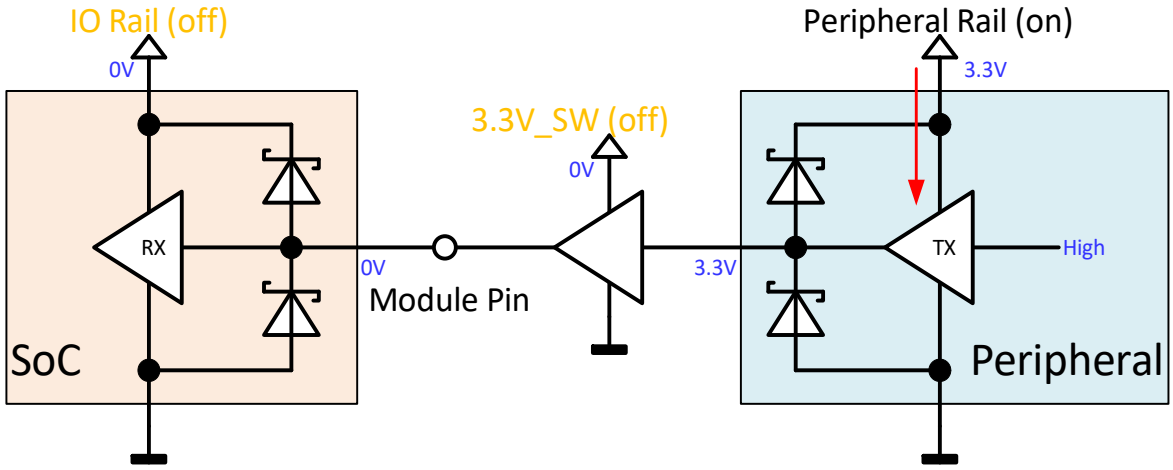

Figure 64: Non-backfeeding buffer

3.7.5.10 Dual-FET circuit

For low-speed signals, two transistors and two resistors can be used for blocking backfeeding. The first transistor is inverting the signal, while the second one makes it an open-drain type. Make sure the pull-up resistors are on the input IO rail. Instead of using two transistors, it might be possible to invert the signal in software and use only a single FET.

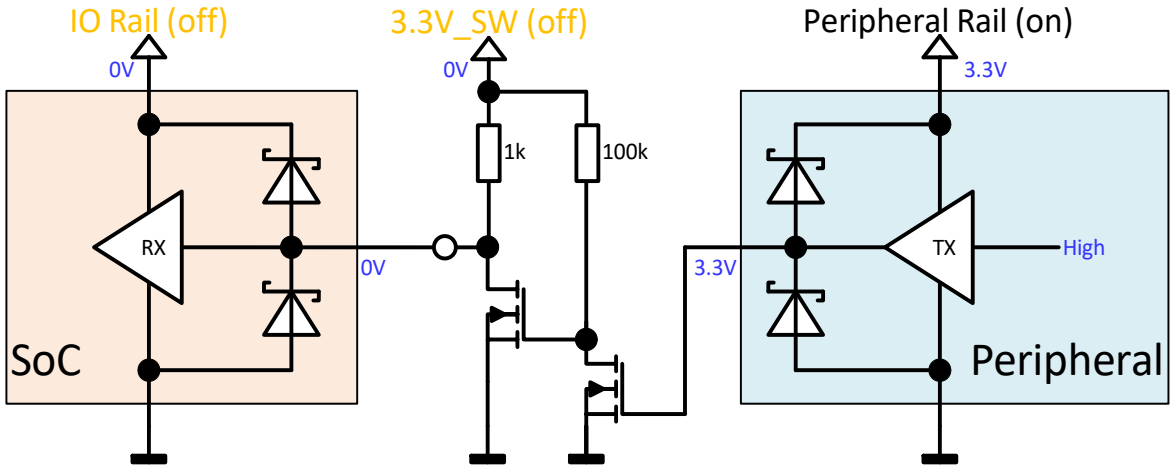

Figure 65: Dual-FET circuit

3.7.5.11 Tristate Buffer

Tristate buffers that feature an output enable control signal can be a solution. For example, RS232 transceivers often feature an output enable signal. The biggest challenge with this solution is to control the output enable signal. Often you cannot directly use the IO rail. If there is backfeeding to the power rail used as the output enable signal, the buffers might never turn off, and therefore the backfeeding remains. Likely another circuit is required for generating a proper output enable signal.

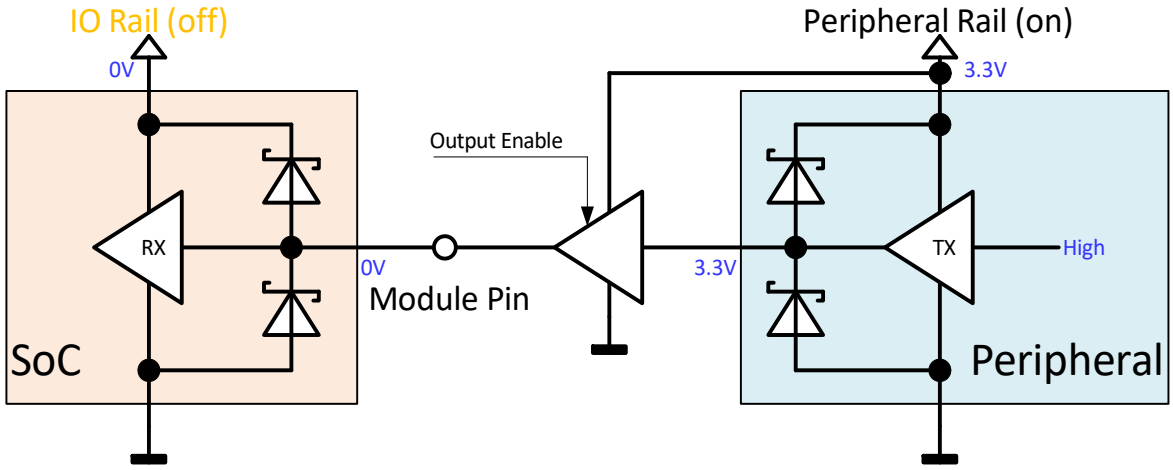

Figure 66: Tristate buffer

3.7.5.12 Level Shifter

Level shifters can be an effective method for preventing backfeeding. Especially if you anyway need a level shifter in the signal path. Even if both sides have the same IO voltage level, a level shifter can still be a good option. It is crucial to select a level shifter that allows both power rails to be switched off individually. Not all level shifters allow that without causing backfeeding. A good candidate for preventing backfeeding is the SN74AVC4T774 from TI. For open-drain signals such as the I2C bus, the FXMA2102L8X from ON Semiconductor prevents backfeeding.

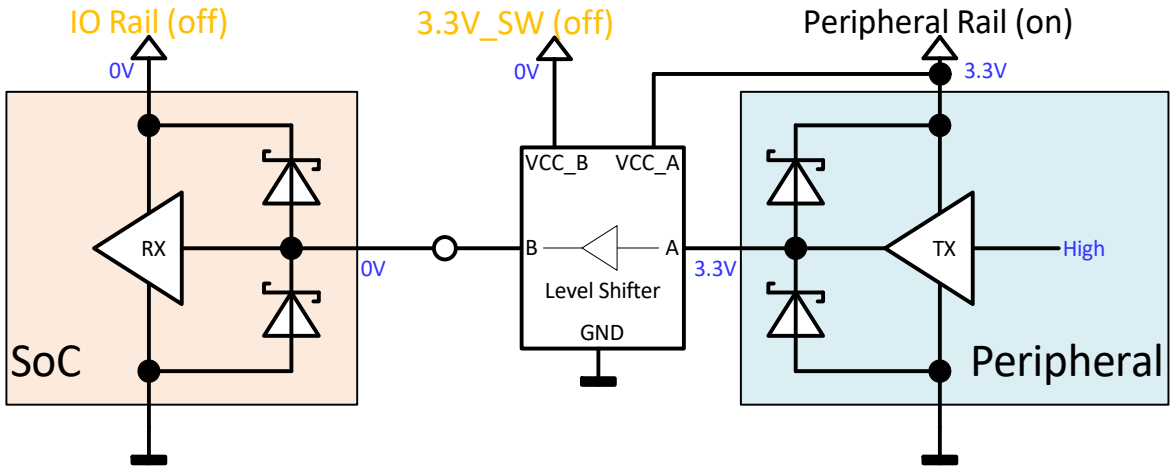

Figure 67: Level shifter for preventing backfeeding

3.7.5.13 Galvanic Isolation

Galvanic isolations in the signal path can be achieved by transformers, optocouplers, or specialized ICs. Especially in harsh environments, galvanic isolation is a preferred method for isolating power domains of different devices. The so-called magnetics inside the Ethernet connector is also a galvanic isolator and prevents backfeeding over the Ethernet cable. Galvanic isolators are also preferred way for protecting different power domains of CAN interfaces.

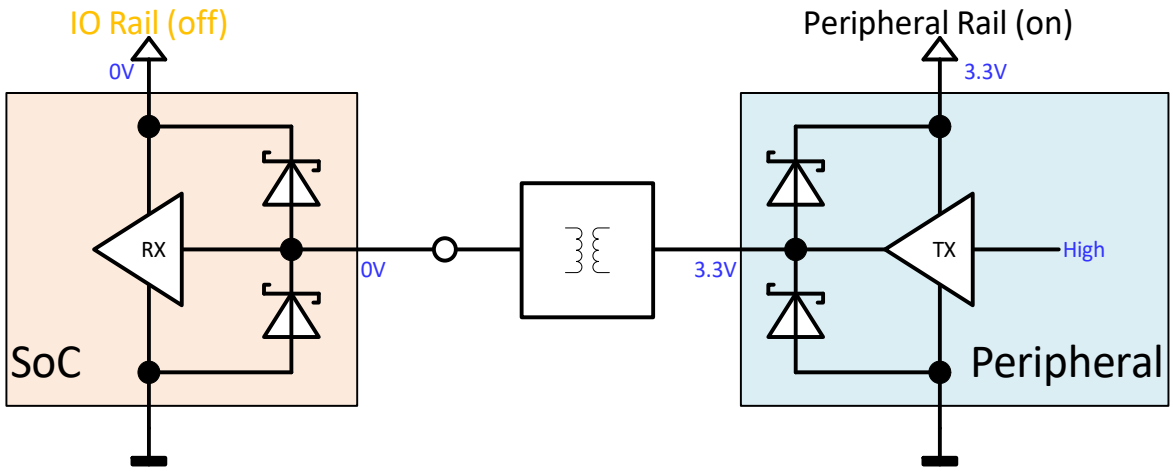

Figure 68: Galvanic isolation between input and output

3.7.5.14 Reverse Current Protection in IO Rail

By placing a diode in the IO rail's power supply, reverse current to other IO rail devices can be prevented. For example, this is a preferred solution for protecting the HDMI CEC signal from backfeeding to the 3.3V rail. However, it is not always a feasible solution due to the forward voltage drop on the IO voltage rail.

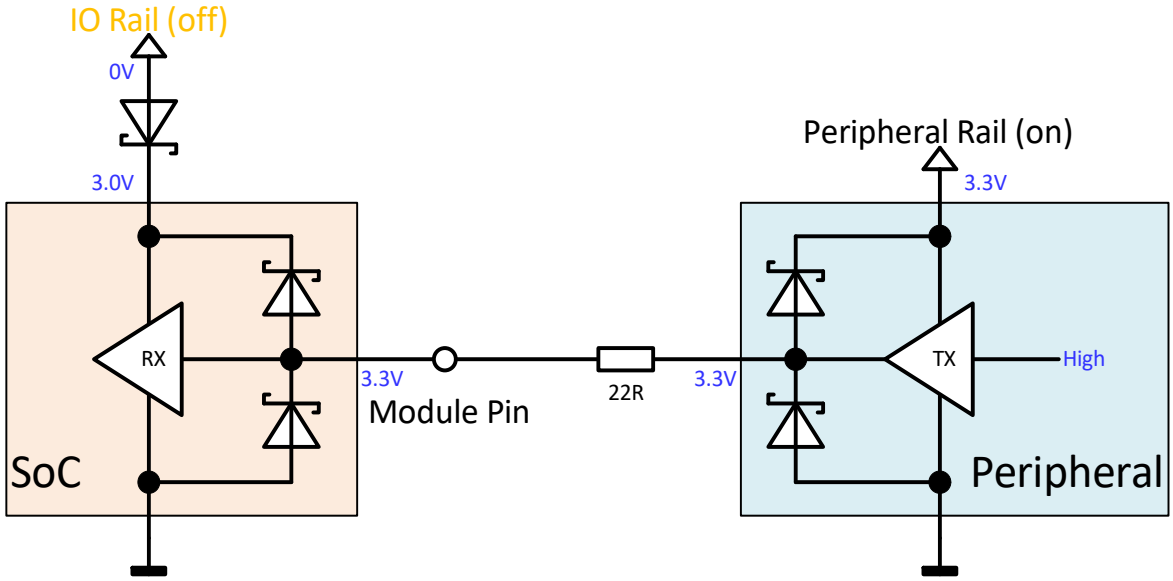

Figure 69: Reverse current protection diode

3.7.5.15 Extra Load on Rail

Suppose the primary issue caused by the residual voltage is an above-threshold voltage compromising the power-on reset or an incorrect device configuration strapped. In that case, a solution might be adding an extra load to the affected rail. Turning this load on only during the power-up sequence is advisable for reducing the extra power consumption. Before implementing this approach, make sure the extra load is not overloading the output driver or the ESD protection diode. Often this method is used in conjunction with other methods described before as an additional fallback solution. For example, the driver should drive output signals low to prevent backfeeding. If the driver fails to set the output signals correctly, the extra load can make sure that the peripheral's power-on reset is still triggering.

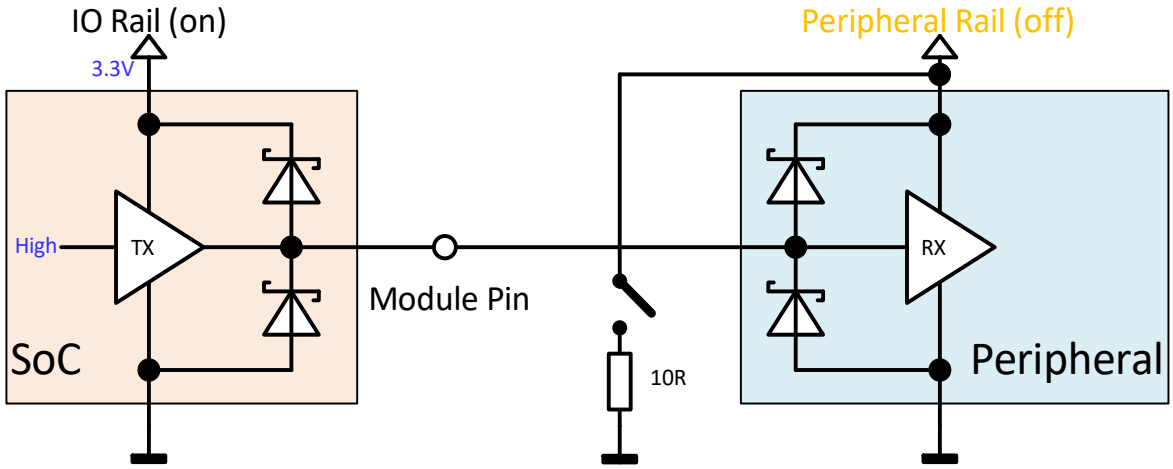

Figure 70: Additional load on peripheral rail

4 Mechanical and Thermal Consideration

4.1 Module Connector

The Colibri modules fit into a regular 2.5V (DDR1) SO-DIMM200 memory socket. Please note there are two versions of the 200-pin SO-DIMM connector available. The Colibri module is only compatible with the variant that is designed for DDR1 modules with 2.5V. The 1.8V DDR2 variant has a different notch position and is therefore not compatible.

There are many suitable connectors from different manufacturers available in different stacking heights. A selection of SO-DIMM200 socket manufacturers is listed below:

CONCRAFT:	http://www.concraft.com.tw/connector_products_ddr.html
Morethanall Co Ltd.:	http://www.morethanall.com
Tyco Electronics (AMP):	http://www.te.com
NEXUS COMPONENTS GmbH:	http://www.nexus-de.com
FCI	http://www.fci.com

4.2 Fixation of the Module

The SO-DIMM connector features a locking mechanism that is reliable for many applications. Additional fixation might be required to ensure the proper connection of the module at high vibration or shock situations. The Colibri module offers different solutions for the fixation.

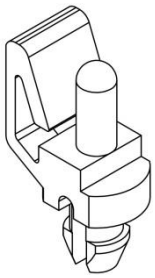

Figure 71: Colibri Fastener

Toradex offers Colibri Fastener for an easy-to-install fixation. Two fasteners are required for holding the module. The fastener supports a SO-DIMM connector height of 5.2mm only. If a connector with a different height is used, another fixation solution is required. Please note, inserting the Colibri module is critical. If done wrong, the Colibri can be damaged due to mechanical stress! More information, including a module inserting guide, can be found here: http://developer.toradex.com/products/colibri-fastener

Figure 72: Colibri Module with Fastener

Instead of using the holes on the module for the fastener, they can also be used for fixing the module with screws. Select a suitable spacer that matches the SO-DIMM connector stacking height. The holes in the module have a diameter of 2.0mm. Therefore, M1.5, M1.6, or M1.8 screws can be used. Please note the maximum allowed head and washer diameter is 6mm.

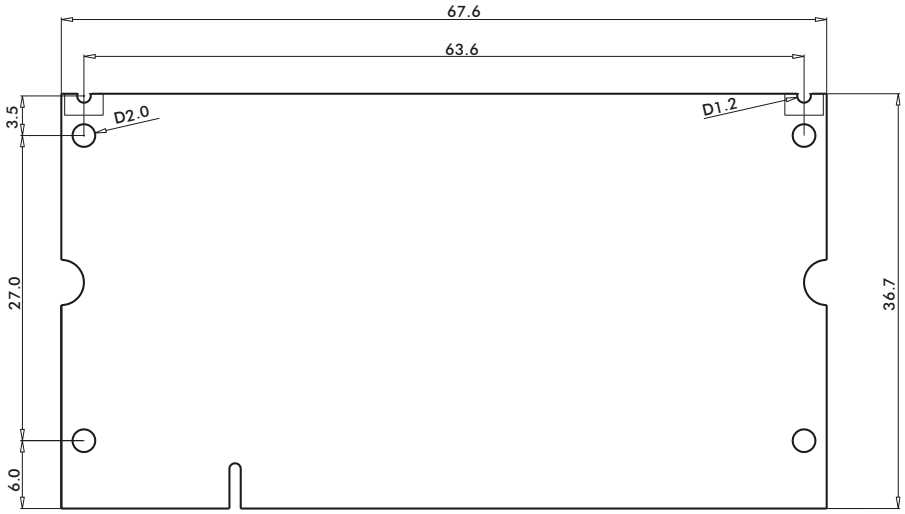

Figure 73: Location of Mounting Holes

The third option is to solder down the module. The modules feature a half-open through-hole solder pad. These holes can be used for soldering the module down with solder pins. Please note the solder pads are connected to the ground plane of the module. Some of the older modules might do not feature the pads. Please contact the Toradex support team for more information.

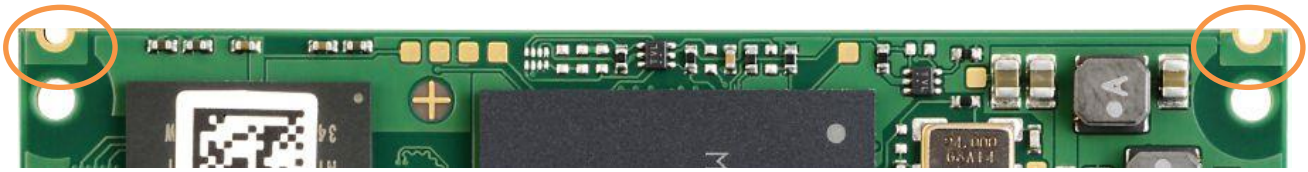

Figure 74: Thru-Hole Solder Pads for Fixation

4.3 Thermal Solution

The Colibri modules are designed to be used without an additional heat spreader or heat sink. Most of the Colibri modules feature a thermal throttling mechanism. The module measures the current temperature of the SoC. If it reaches a critical limit, it starts throttling down the CPU speed or shuts the system entirely down to prevent damages. Please read the corresponding datasheets for more information on thermal behavior.

- If you only use the peak performance for a short time, heat dissipation is less of a problem because most of the modules reduce the power consumption when full performance is not required.
- A lower die temperature also lowers the power consumption due to smaller leakage currents.
- If you need the full CPU/Graphics performance over a long time, make sure that you can dissipate sufficient thermal energy to the environment.

In general, the more effectively the generated thermal energy is transported to the environment, the better performance you get out of the computer module. Therefore, it might be necessary to add a thermal solution. The best solution is to glue a suitable heat sink directly to the top of the SoC. Since the module PCB is only 1mm thick, the board is not very stiff. Applying force to the SoC can bend PCB, which destroys the module. Therefore, pay attention when mounting a thermal solution on the module that the module is not cracked due to bending stress.

4.4 Module Size

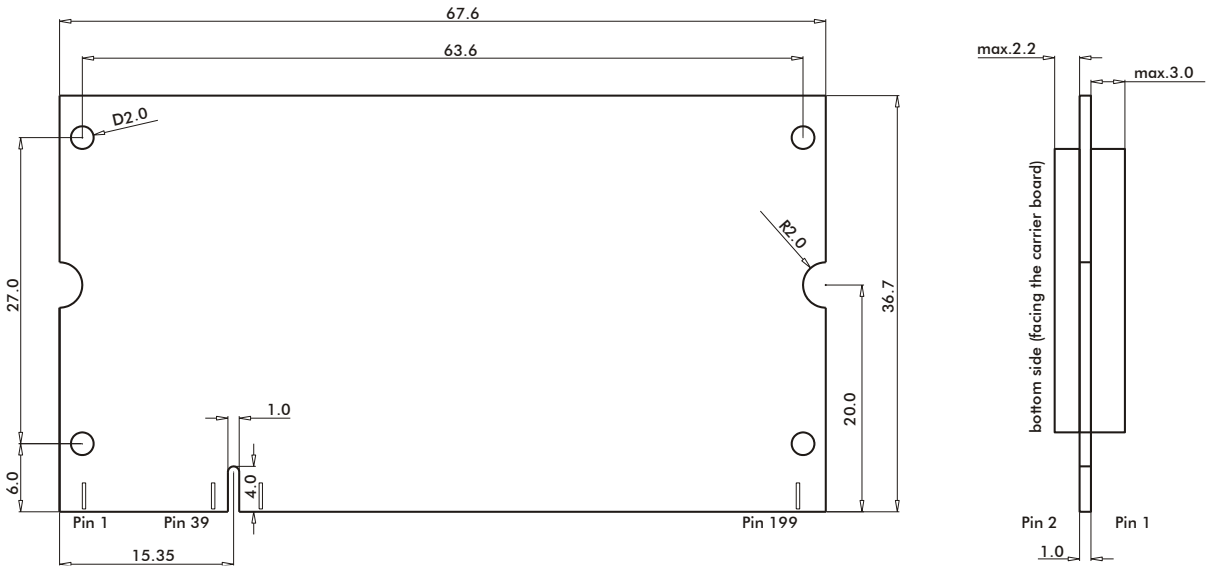

Figure 75: Module Dimensions Top Side (dimensions in mm)

4.5 JTAG Test Pads

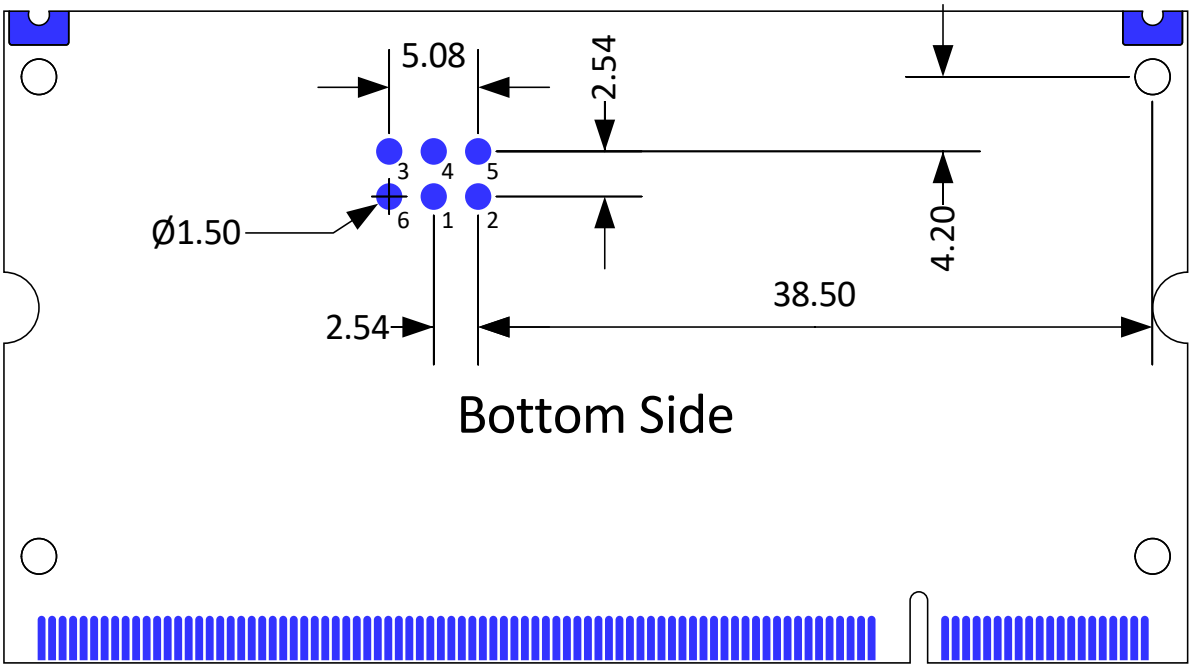

Figure 76: Location of JTAG Test Pads (bottom view, dimensions in mm)

The JTAG interface is not generally required for software development with the Colibri module. There is always the possibility of reprogramming the module using the Recovery Mode over USB or UART. However, for debugging the operating system, especially for real-time operating systems, it might be beneficial having access to the JTAG interface of the SoC.

The JTAG interface is located on test points on the underside of the module. The location is the same for all modules in the Colibri family. There are a total of six test pads, of which five are used for the JTAG interface. The sixth test pad is used for module testing and should be left unconnected on the carrier board. Please note the unusual pin numbering.

Pin Number	Colibri Signal Name	I/O	Type	Power Rail	Description
1	JTAG_TDI	I	CMOS	1.8V/3.3V	Test Data In
2	JTAG_TDO	O	CMOS	1.8V/3.3V	Test Data Out
3	JTAG_TCK	I	CMOS	1.8V/3.3V	Test Clock
4	JTAG_TRST#	I	CMOS	1.8V/3.3V	Test Reset (optional)
5	JTAG_TMS	I	CMOS	1.8V/3.3V	Test Reset (optional)
6					Do not use this pin. The manufacturer uses the test pad for module testing or programming.

Table 33: JTAG Signals

Please pay attention to the interface voltage. Depending on the module, the IO voltage can be 3.3V or 1.8V. It is crucial to use the correct JTAG interface voltage. Carefully read the module datasheet for more information. On the Colibri Evaluation Board version 3.1 and later, there is a jumper for setting the JTAG IO voltage (JP29).

5 Appendix A – Physical Pin Definition and Location

The following table contains information about the standard functions on the module edge connector pins. Not all modules feature the complete set of standard functions. Please read the function lists carefully in the datasheet of the modules. The Toradex Pinout Designer can be a helpful tool for checking the availability of functions on specific modules. It helps to configure the pin muxing. More information and download link can be found here:
http://developer.toradex.com/carrier-board-design/pinout-designer-tool

Module Bottom Side	SO-DIMM Pin		Module Top Side
Analog Input <3>	2	1	Audio Analog Microphone Input
Analog Input <2>	4	3	Audio Analog Microphone GND
Analog Input <1>	6	5	Audio Analog Line-In Left
Analog Input <0>	8	7	Audio Analog Line-In Right
Audio_Analog VDD	10	9	Audio_Analog GND
Audio_Analog VDD	12	11	Audio_Analog GND
Resistive Touch PX	14	13	Audio Analog Headphone GND
Resistive Touch MX	16	15	Audio Analog Headphone Left
Resistive Touch PY	18	17	Audio Analog Headphone Right
Resistive Touch MY	20	19	UART_C RXD
VDD Fault Detect	22	21	UART_C TXD
Battery Fault Detect	24	23	UART_A DTR
nReset In	26	25	UART_A CTS, Keypad_In<0>
PWM<B>	28	27	UART_A RTS
PWM<C>	30	29	UART_A DSR
UART_B CTS	32	31	UART_A DCD
UART_B RTS	34	33	UART_A RXD
UART_B RXD	36	35	UART_A TXD
UART_B TXD	38	37	UART_A RI, Keypad_In<4>
VCC_BATT	40	39	GND
3V3	42	41	GND
LCD RGB DE	44	43	WAKEUP Source<0>, SDCard CardDetect
LCD RGB Data<7>	46	45	WAKEUP Source<1>
LCD RGB Data<9>	48	47	SDCard CLK
LCD RGB Data<11>	50	49	SDCard DAT<1>
LCD RGB Data<12>	52	51	SDCard DAT<2>
LCD RGB Data<13>	54	53	SDCard DAT<3>
LCD RGB PCLK	56	55	PS2 SDA1
LCD RGB Data<3>	58	57	LCD RGB Data<16>
LCD RGB Data<2>	60	59	PWM<A>, Camera Input Data<7>
LCD RGB Data<8>	62	61	LCD RGB Data<17>
LCD RGB Data<15>	64	63	PS2 SCL1
LCD RGB Data<14>	66	65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2
LCD RGB HSYNC	68	67	PWM<D>, Camera Input Data<6>
LCD RGB Data<1>	70	69	PS2 SCL2
LCD RGB Data<5>	72	71	Camera Input Data<0>, LCD Back-Light GPIO
LCD RGB Data<10>	74	73	
LCD RGB Data<0>	76	75	Camera Input MCLK
LCD RGB Data<4>	78	77	
LCD RGB Data<6>	80	79	Camera Input Data<4>
LCD RGB VSYNC	82	81	Camera Input VSYNC
3V3	84	83	GND
SPI CS	86	85	Camera Input Data<8>, Keypad_Out<4>
SPI CLK	88	87	nReset Out
SPI RXD	90	89	nWE
SPI TXD	92	91	nOE

Camera Input HSYNC	94	93	RDnWR
Camera Input PCLK	96	95	RDY
Camera Input Data<1>	98	97	Camera Input Data<5>
Keypad_Out<1>	100	99	nPWE
	102	101	Camera Input Data<2>
	104	103	Camera Input Data<3>
nCS2	106	105	nCS0
3V3	108	107	nCS1
ADDRESS8	110	109	GND
ADDRESS9	112	111	ADDRESS0
ADDRESS10	114	113	ADDRESS1
ADDRESS11	116	115	ADDRESS2
ADDRESS12	118	117	ADDRESS3
ADDRESS13	120	119	ADDRESS4
ADDRESS14	122	121	ADDRESS5
ADDRESS15	124	123	ADDRESS6
DQM0	126	125	ADDRESS7
DQM1	128	127	
DQM2	130	129	USB Host Power Enable
DQM3	132	131	USB Host Over-Current Detect
ADDRESS25	134	133	
ADDRESS24	136	135	SPDIF_IN
ADDRESS23	138	137	USB Client Cable Detect, SPDIF_OUT
ADDRESS22	140	139	USB Host DP
ADDRESS21	142	141	USB Host DM
ADDRESS20	144	143	USB Client DP
ADDRESS19	146	145	USB Client DM
3V3	148	147	GND
DATA16	150	149	DATA0
DATA17	152	151	DATA1
DATA18	154	153	DATA2
DATA19	156	155	DATA3
DATA20	158	157	DATA4
DATA21	160	159	DATA5
DATA22	162	161	DATA6
DATA23	164	163	DATA7
DATA24	166	165	DATA8
DATA25	168	167	DATA9
DATA26	170	169	DATA10
DATA27	172	171	DATA11
DATA28	174	173	DATA12
DATA29	176	175	DATA13
DATA30	178	177	DATA14
DATA31	180	179	DATA15
3V3	182	181	GND
ADDRESS18	184	183	Ethernet Link/Activity Status
ADDRESS17	186	185	Ethernet Speed Status
ADDRESS16	188	187	Ethernet TXO-
SDCard CMD	190	189	Ethernet TXO+
SDCard DAT<0>	192	191	Ethernet GND
I2C SDA	194	193	Ethernet RXI-
I2C SCL	196	195	Ethernet RXI+
3V3	198	197	GND
3V3	200	199	GND

Table 34: Physical Pin Definition and Location