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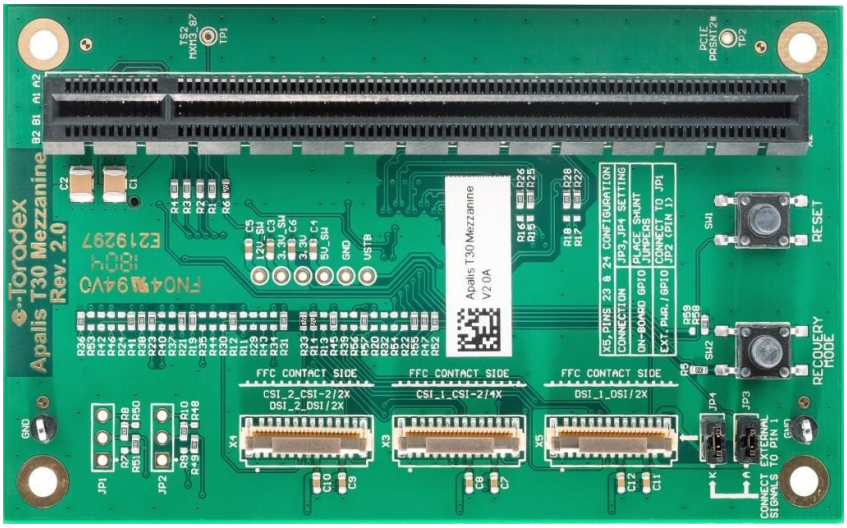
Apalis T30 Mezzanine

Datasheet



Revision History

Date	Doc. Rev.	Board Version	Changes
12-April-18	Rev. 1.0	V2.0	- Initial Release: Preliminary Version
17-May-18	Rev. 1.1	V2.0	- Updated product image on the cover page

Contents

1. Introduction

Apalis T30 Mezzanine is an add-on board for the Apalis Evaluation Board which provides access to the type specific interfaces available on the Apalis T30 module. It allows the user to test and evaluate the type specific features available on the Apalis T30 module.

Since type specific features are dependent on the Apalis module. Specific types of mezzanine boards will be available for each Apalis module. Customers are free to develop their own type specific mezzanine board for prototyping and development purposes. Please refer to the datasheets for the individual Apalis module for more information.

1.1. Reference Documents

For detailed technical information about suitable computer modules, please refer to the documents listed below.

1.1.1 Apalis Computer Modules

An overview of the Apalis product family:

https://www.toradex.com/computer-on-modules/apalis-arm-family

An overview of the Apalis T30 module:

https://www.toradex.com/computer-on-modules/apalis-arm-family/nvidia-tegra-3

http://developer.toradex.com/products/apalis-t30

1.1.2 Toradex Developer Website - Apalis Evaluation Board

http://developer.toradex.com/products/apalis-evaluation-board

1.1.3 Toradex Developer Website - Carrier Board Design

http://developer.toradex.com/carrier-board-design

2. Features

2.1. Overview

The Apalis T30 Mezzanine provides the following features and interfaces:

- 1x x16 (x4 mode) PCI Express connector (X16)
- 2x MIPI CSI (1x Quad-lane or 2x Dual-lane) connector
- 1x MIPI DSI (Dual-lane) connector
- 1x Recovery mode switch
- 1x Reset switch

2.2. Block Diagram

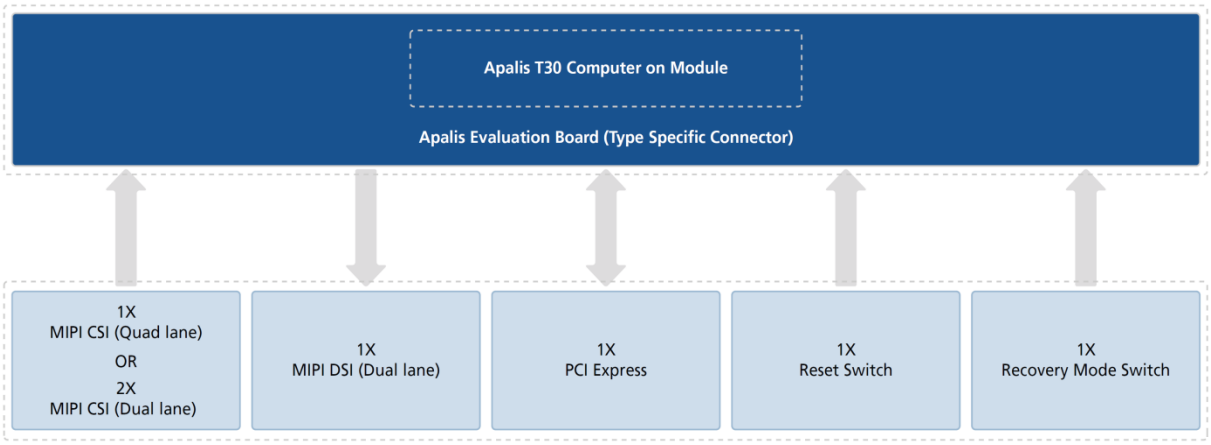


Fig.1 Apalis T30 Mezzanine Board Hardware Architecture

2.3. Physical Drawings

2.3.1 Top Side Connectors

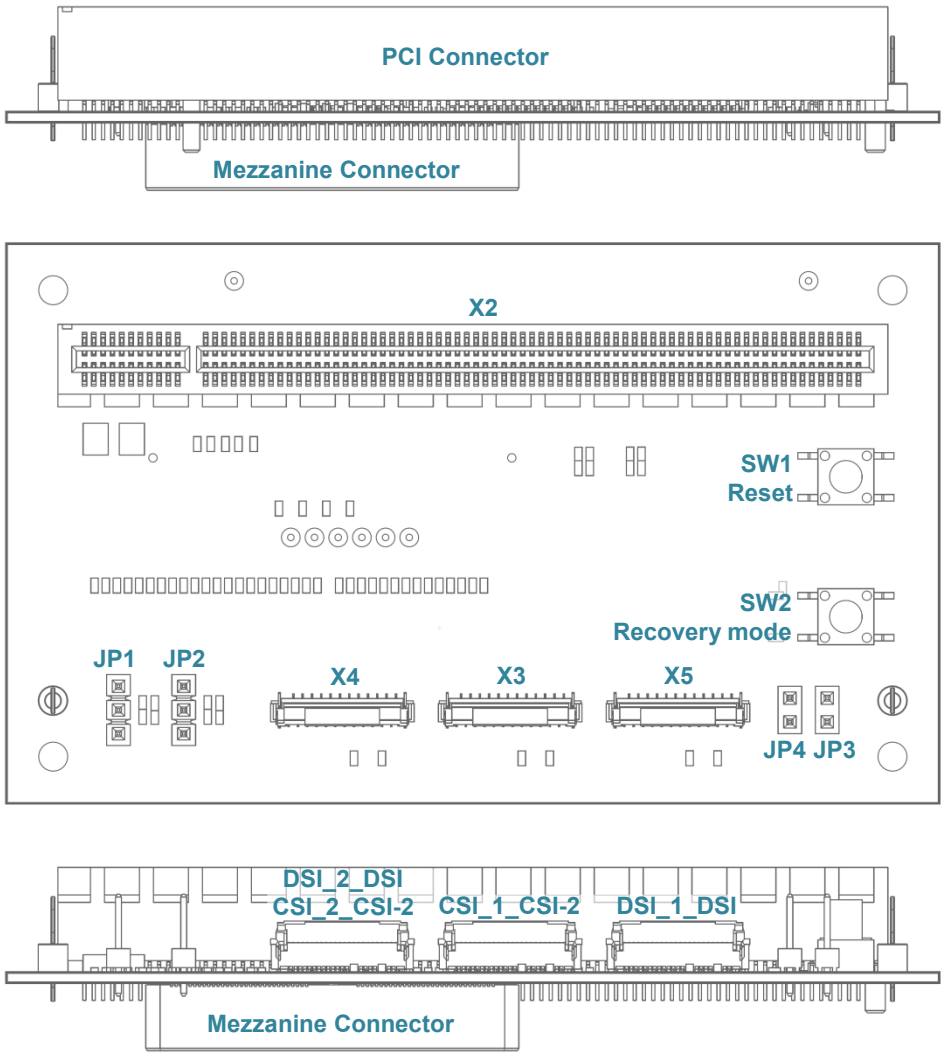


Fig.2 Apalis T30 Mezzanine Board Connectors – Top Side

Ref	Description	Remarks
X2	PCI Connector	x4 PCI lane; x16 Connector
X3	CSI_1 Connector	Quad-lane MIPI CSI-2; CSI_1 Interface
X4	CSI_2 Connector	Dual-lane MIPI CSI-2, CSI_2 Interface / Dual-lane MIPI DSI, DSI_2 Interface
X5	DSI_1 Connector	Dual-lane MIPI DSI, DSI_1 Interface
SW1	Reset Switch	
SW2	Recovery Mode Switch	
JP1	I2C_SDA Jumper	Not assembled
JP2	I2C_SCL Jumper	Not assembled
JP3	DSI_GPIO_BLK_LED_A Jumper (for X2, Pin 23)	
JP4	DSI_GPIO_BLK_LED_K Jumper (for X2, Pin 24)	

2.3.2 Bottom Side Connectors

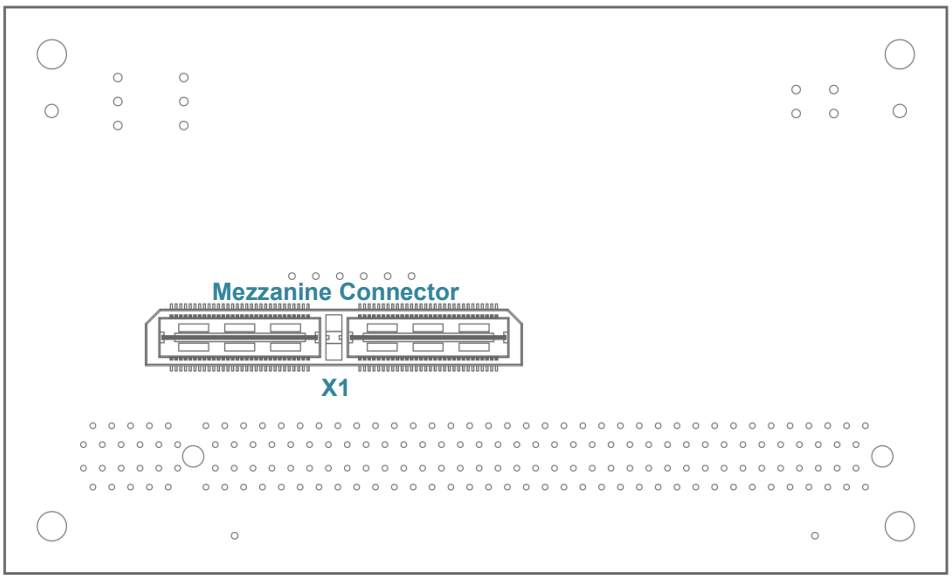


Fig.3 Apalis T30 Mezzanine Board Connectors – Bottom Side

Ref	Description	Remarks
X1	Mezzanine Connector	

3. Interface Description

3.1. Mezzanine Connector (X1)

Manufacturer: Samtec, QTH-060-02-L-D-A

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	VSTB		PWR	+5V	
3	CSI_1_CLK_P	163	I		
4	GND		PWR		
5	CSI_1_CLK_N	161	I		
6	GPIO_MXM3_235	235	I/O	+3.3V	
7	CAM_MEZ_PIN26	159			
8	GPIO_MXM3_233	233	I/O	+3.3V	
9	CSI_1_D1_P	157	I		
10	GPIO_MXM3_231	231	I/O	+3.3V	
11	CSI_1_D1_N	155	I		
12	GPIO_MXM3_229	229	I/O	+3.3V	
13	GND		PWR		
14	GPIO_MXM3_227	227	I/O	+3.3V	
15	CSI_1_D2_P	151	I		
16	GPIO_MXM3_225	225	I/O	+3.3V	
17	CSI_1_D2_N	149	I		
18	GPIO_MXM3_223	223	I/O	+3.3V	
19	GND		PWR		
20	GPIO_MXM3_221	221	I/O	+3.3V	
21	CSI_2_DATA1_P	145	I		
22	GND		PWR		
23	CSI_2_DATA1_N	143	I		
24	CAM_MEZ_PIN24				
25	GND		PWR		
26	CAM_MEZ_PIN26				
27	CSI_2_DATA2_P	139	I		
28	CAM_MEZ_PIN28				
29	CSI_2_DATA2_N	137	I		
30	CAM_MEZ_PIN30				
31	GND		PWR		
32	GND		PWR		
33	CAM_MEZ_PIN24	135			
34	CAM_MCLK	193	O	+3.3V	
35	CSI_2_CLK_P	133	I		
36	GND		PWR		
37	CSI_2_CLK_N	131	I		
38	I2C3_SCL	203	O	+3.3V	
39	GND		PWR		

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
40	GND		PWR		
41	DSI_1_CLK_P	127	O		
42	I2C3_SDA	201	I/O	+3.3V	
43	DSI_1_CLK_N	125	O		
44	5V_SW		PWR	+5V	
45	GND		PWR		
46	5V_SW		PWR	+5V	
47	CAM_MEZ_PIN28	123			
48	5V_SW		PWR	+5V	
49	DSI_1_D1_P	121	O		
50	5V_SW		PWR	+5V	
51	DSI_1_D1_N	119	O		
52	5V_SW		PWR	+5V	
53	GND		PWR		
54	NC				
55	DSI_1_D2_P	115	O		
56	NC				
57	DSI_1_D2_N	113	O		
58	NC				
59	GND		PWR		
60	NC				
61	PCIE_L3_TX_P	109	O		
62	3.3V		PWR	+3.3V	
63	PCIE_L3_TX_N	107	O		
64	3.3V		PWR	+3.3V	
65	GND		PWR		
66	3.3V		PWR	+3.3V	
67	PCIE_L3_RX_P	103	I		
68	3.3V		PWR	+3.3V	
69	PCIE_L3_RX_N	101	I		
70	NC				
71	GND		PWR		
72	3.3V_SW		PWR	+3.3V	
73	CAM_MEZ_PIN30	99			
74	3.3V_SW		PWR	+3.3V	
75	PCIE_L2_TX_P	97	O		
76	3.3V_SW		PWR	+3.3V	
77	PCIE_L2_TX_N	95	O		
78	3.3V_SW		PWR	+3.3V	
79	GND		PWR		
80	NC				
81	PCIE_L2_RX_P	91	I		
82	12V_SW_UNREG_F		PWR	+12V	

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
83	PCIE_L2_RX_N	89	I		
84	12V_SW_UNREG_F		PWR	+12V	
85	GND		PWR		
86	12V_SW_UNREG_F		PWR	+12V	
87	TS2	87			
88	GND		PWR		
89	PCIE_L1_TX_P	85	O		
90	I2C1_SCL	211	O	+3.3V	
91	PCIE_L1_TX_N	83	O		
92	I2C1_SDA	209	I/O	+3.3V	
93	GND		PWR		
94	GPIO_MXM3_138	138	I/O	+3.3V	
95	PCIE_L1_RX_P	79	I		
96	GPIO_MXM3_140	140	I/O	+3.3V	
97	PCIE_L1_RX_N	77	I		
98	GPIO_MXM3_37	37	I/O	+3.3V	
99	GND		PWR		
100	NC				
101	PCIE_L0_TX_P	73	O		
102	RESET_MOCI#	26	O	+3.3V	
103	PCIE_L0_TX_N	71	O		
104	RESET_MICO#	28	I	+3.3V	
105	GND		PWR		
106	GPIO_1	1	I/O	+3.3V	
107	PCIE_L0_RX_P	67	I		
108	GPIO_2	3	I/O	+3.3V	
109	PCIE_L0_RX_N	65	I		
110	GPIO_3	5	I/O	+3.3V	
111	GND		PWR		
112	GPIO_4	7	I/O	+3.3V	
113	RECOVERY_MODE#	63	I		
114	GPIO_5	11	I/O	+3.3V	
115	PCIE_CLK_P	61	O		
116	GPIO_6	13	I/O	+3.3V	
117	PCIE_CLK_N	59	O		
118	GPIO_7	15	I/O	+3.3V	
119	GND		PWR		
120	GPIO_8	17	I/O	+3.3V	
121	GND		PWR		

3.2. PCI Express slot (X2)

Connector type: Molex 87715-9305

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
A1	GND		PWR		
A2	12V_SW_UNREG_F		PWR	+12V	
A3	12V_SW_UNREG_F		PWR	+12V	
A4	GND		PWR		
A5	NC				
A6	NC				
A7	NC				
A8	NC				
A9	3.3V_SW		PWR	+3.3V	
A10	3.3V_SW		PWR	+3.3V	
A11	PCIE1_RESET#	26		+3.3V	
A12	GND		PWR		
A13	PCIE_CLK_P	61	O		
A14	PCIE_CLK_N	59	O		
A15	GND		PWR		
A16	PCIE_L0_RX_N	65	I		
A17	PCIE_L0_RX_P	67	I		
A18	GND		PWR		
A19	NC				
A20	GND		PWR		
A21	PCIE_L1_RX_P	79	I		
A22	PCIE_L1_RX_N	77	I		
A23	GND		PWR		
A24	GND		PWR		
A25	PCIE_L2_RX_P	91	I		
A26	PCIE_L2_RX_N	89	I		
A27	GND		PWR		
A28	GND		PWR		
A29	PCIE_L3_RX_P	103	I		
A30	PCIE_L3_RX_N	101	I		
A31	GND		PWR		
A32	NC				
A33	NC				
A34	GND		PWR		
A35	NC				
A36	NC				
A37	GND		PWR		
A38	GND		PWR		
A39	NC				
A40	NC				
A41	GND		PWR		

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
A42	GND		PWR		
A43	NC				
A44	NC				
A45	GND		PWR		
A46	GND		PWR		
A47	NC				
A48	NC				
A49	GND		PWR		
A50	NC				
A51	GND		PWR		
A52	NC				
A53	NC				
A54	GND		PWR		
A55	GND		PWR		
A56	NC				
A57	NC				
A58	GND		PWR		
A59	GND		PWR		
A60	NC				
A61	NC				
A62	GND		PWR		
A63	GND		PWR		
A64	NC				
A65	NC				
A66	GND		PWR		
A67	GND		PWR		
A68	NC				
A69	NC				
A70	GND		PWR		
A71	GND		PWR		
A72	NC				
A73	NC				
A74	GND		PWR		
A75	GND		PWR		
A76	NC				
A77	NC				
A78	GND		PWR		
A79	GND		PWR		
A80	NC				
A81	NC				
A82	GND		PWR		
B1	12V_SW_UNREG_F		PWR	+12V	
B2	12V_SW_UNREG_F		PWR	+12V	

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
B3	NC				
B4	GND		PWR		
B5	PCIE_SMBCLK	211	O	+3.3V	
B6	PCIE_SMBDAT	209	I/O	+3.3V	
B7	GND		PWR		
B8	3.3V_SW		PWR	+3.3V	
B9	NC				
B10	3.3V_SW		PWR	+3.3V	
B11	PCIE_WAKE#	37	O		
B12	NC				
B13	GND		PWR		
B14	PCIE_L0_TX_N	71	O		
B15	PCIE_L0_TX_P	73	O		
B16	GND		PWR		
B17	PCIE_PRSNT2#				4.7K to +3.3V
B18	GND		PWR		
B19	PCIE_L1_TX_N	83	O		
B20	PCIE_L1_TX_P	85	O		
B21	GND		PWR		
B22	GND		PWR		
B23	PCIE_L2_TX_N	95	O		
B24	PCIE_L2_TX_P	97	O		
B25	GND		PWR		
B26	GND		PWR		
B27	PCIE_L3_TX_N	107	O		
B28	PCIE_L3_TX_P	109	O		
B29	GND		PWR		
B30	NC				
B31	PCIE_PRSNT2#				4.7K to +3.3V
B32	GND		PWR		
B33	NC				
B34	NC				
B35	GND		PWR		
B36	GND		PWR		
B37	NC				
B38	NC				
B39	GND		PWR		
B40	GND		PWR		
B41	NC				
B42	NC				
B43	GND		PWR		
B44	GND		PWR		
B45	NC				

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
B46	NC				
B47	GND		PWR		
B48	PCIE_PRSNT2#				4.7K to +3.3V
B49	GND		PWR		
B50	NC				
B51	NC				
B52	GND		PWR		
B53	GND		PWR		
B54	NC				
B55	NC				
B56	GND		PWR		
B57	GND		PWR		
B58	NC				
B59	NC				
B60	GND		PWR		
B61	GND		PWR		
B62	NC				
B63	NC				
B64	GND		PWR		
B65	GND		PWR		
B66	NC				
B67	NC				
B68	GND		PWR		
B69	GND		PWR		
B70	NC				
B71	NC				
B72	GND		PWR		
B73	GND		PWR		
B74	NC				
B75	NC				
B76	GND		PWR		
B77	GND		PWR		
B78	NC				
B79	NC				
B80	GND		PWR		
B81	PCIE_PRSNT2#				4.7K to +3.3V
B82	NC				

3.3. MIPI CSI Interface

Apalis T30 computer-on-module features 2x Dual-lane or 1x Quad-lane MIPI CSI-2 interface. MIPI CSI signals CSI_2_DATA1_N/P and CSI_2_DATA2_N/P are shared between CSI connectors X3 and X4. Assembly options have been provided to evaluate 2x Dual-lane or 1x Quad-lane MIPI CSI-2 interface.

2x Dual-lane MIPI CSI-2 interfaces are available as default assembly. Please refer to Apalis T30 Mezzanine V2.0 schematics for more details.

3.3.1 CSI Connector (X3)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	CSI_1_D1_N	155	I		
3	CSI_1_D1_P	157	I		
4	GND		PWR		
5	CSI_1_D2_N	149	I		
6	CSI_1_D2_P	151	I		
7	GND		PWR		
8	CSI_1_CLK_N	161	I		
9	CSI_1_CLK_P	163	I		
10	GND				
11	CSI_1_GPIO0_RST	1 / 26 / 221	I/O	+3.3V	
12	CSI_1_MCLK	193	O	+3.3V	
13	CSI_I2C_SCL	203 / 211	I		
14	CSI_I2C_SDA	201 / 209	I/O		
15	3.3V_SW		PWR	+3.3V	
16	CSI_1_D3_N	143	I		
17	CSI_1_D3_P	145	I		
18	GND		PWR		
19	CSI_1_D4_N	137	I		
20	CSI_1_D4_P	139	I		
21	5V_SW		PWR	+5V	
22	CSI_1_GPIO1	3 / 225	I/O	+3.3V	
23	CSI_1_GPIO2	5 / 229	I/O	+3.3V	
24	CSI_1_GPIO3	7 / 13	I/O	+3.3V	

3.3.2 CSI Connector (X4)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	CSI_2_D1_N	143	I		
3	CSI_2_D1_P	145	I		
4	GND		PWR		
5	CSI_2_D2_N	137	I		
6	CSI_2_D2_P	139	I		
7	GND		PWR		
8	CSI_2_CLK_N	131	I		
9	CSI_2_CLK_P	133	I		
10	GND				
11	CSI_2_GPIO0_RST	1 / 26 / 138 / 227	I/O	+3.3V	
12	CSI_2_MCLK	193	O	+3.3V	
13	CSI_I2C_SCL	203 / 211	I		
14	CSI_I2C_SDA	201 / 209	I/O		
15	3.3V_SW		PWR	+3.3V	
16	NC		I		
17	NC		I		
18	GND		PWR		
19	NC		I		
20	NC		I		
21	5V_SW		PWR	+5V	
22	CSI_2_GPIO1	3 / 17 / 37	I/O	+3.3V	
23	CSI_2_GPIO2	5 / 11 / 223	I/O	+3.3V	
24	CSI_2_GPIO3	7 / 13 / 15	I/O	+3.3V	

As default assembly, I2C3 bus has been connected to the MIPI CSI connectors. Following table describes the assembly options available on the Apalis T30 Mezzanine V2.0 with respect of the MIPI CSI interface I2C bus selection:

Solution Selected	Assembly Options	Assembled components on Apalis T30 Mezzanine V2.0	PCB Side
I2C1	Assemble components R7 and R9 Disassemble components R8 and R10	R8, R10	Top
I2C3	Assemble components R8 and R10 Disassemble components R7 and R9	R8, R10	Top

Please refer to Apalis T30 Mezzanine V2.0 assembly drawing for the position of the components.

Jumpers JP1 and JP2 can also be used for MIPI CSI interface I2C bus selection. Jumpers JP1 and JP2 are not assembled by default. Please refer to Apalis T30 Mezzanine V2.0 schematics for more details.

3.4. MIPI DSI

3.4.1 DSI Connector (X4)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	DSI_1_D1_N	119	O		
3	DSI_1_D1_P	121	O		
4	GND		PWR		
5	DSI_1_D2_N	113	O		
6	DSI_1_D2_P	115	O		
7	GND		PWR		
8	DSI_1_CLK_N	125	O		
9	DSI_1_CLK_P	127	O		
10	GND				
11	DSI_RESET	1 / 26 / 221	O		
12	DSI_BLK_ON	15 / 235	O		
13	DSI_I2C_SCL	211 / 203	I		
14	DSI_I2C_SDA	209 / 201	I/O		
15	3.3V_SW		PWR	+3.3V	
16	NC				
17	NC				
18	GND		PWR		
19	NC				
20	NC				
21	5V_SW		PWR	+5V	
22	DSI_BLK_PWM	233 / 17			
23	DSI_GPIO_BLK_LED_A	227 / 231			
24	DSI_GPIO_BLK_LED_K	223 / 225			

As default assembly, I2C1 bus has been connected to the MIPI DSI connector. Following table describes the assembly options available on the Apalis T30 Mezzanine V2.0 with respect of the MIPI DSI interface I2C bus selection:

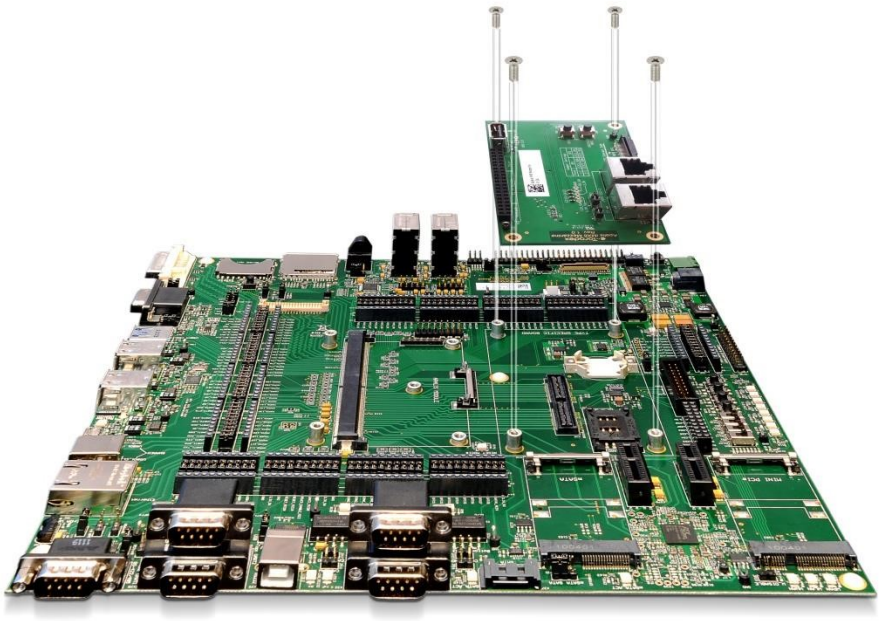
Solution Selected	Assembly Options	Assembled components on Apalis T30 Mezzanine V2.0	PCB Side
I2C1	Assemble components R49 and R51 Disassemble components R48 and R50	R49, R51	Top
I2C3	Assemble components R48 and R50 Disassemble components R49 and R51	R49, R51	Top

Please refer to Apalis T30 Mezzanine V2.0 assembly drawing for the position of the components.

Jumpers JP3 and JP4 are connected to pins 23 and 24 of the connector X5 respectively. If the jumpers JP3 and JP4 are short circuited using shunt jumpers, default GPIO signals connected to jumpers JP3 and JP4 will be available at pins 23 and 24 of connector X5. In-case customer wants to connect external power or I/O, they can remove the shunt jumpers from jumpers JP3 and JP4 and then connect external power or I/O to pin 1 of the jumpers JP3 and JP4 using jumper wires.

4. Assembly

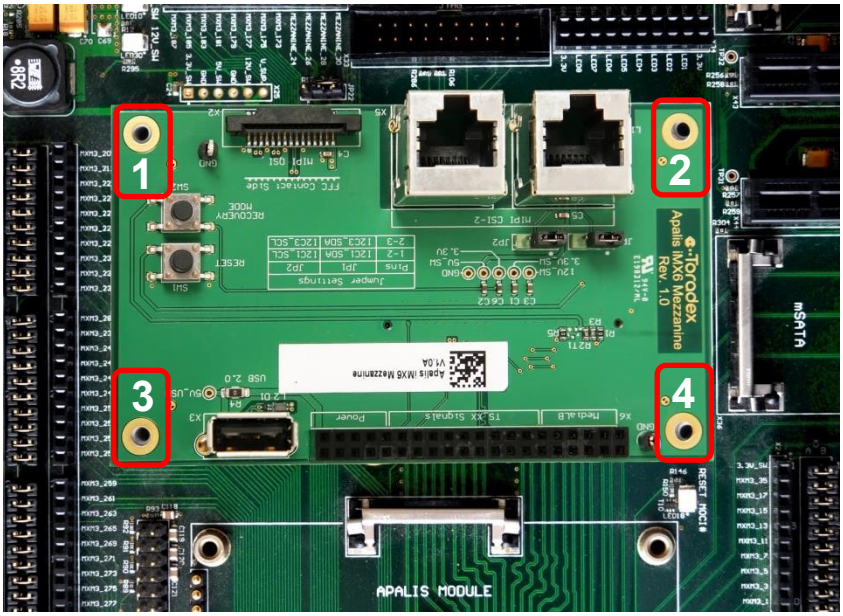
The illustration shown below represents how to attach the Apalis T30 Mezzanine to the Apalis Carrier Board. *Please note that Apalis iMX6 Mezzanine V1.0A board is used for illustration, actual product may look different from the images shown below:*



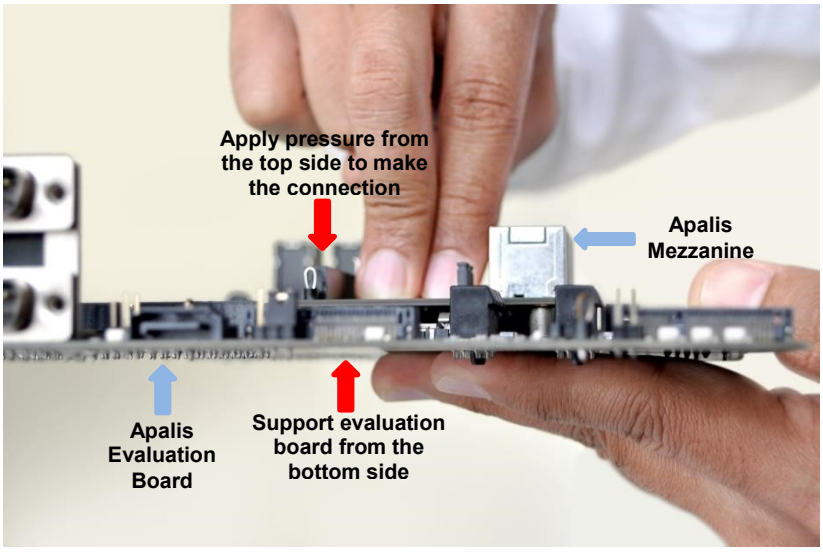
4.1. Assembly Procedure

The following procedure demonstrates how to attach the Apalis T30 Mezzanine to the Apalis Evaluation Board. Please read the instructions carefully to ensure that the connectors or circuit board does not get damaged. Necessary precautions should be taken to avoid the electrostatic charge.

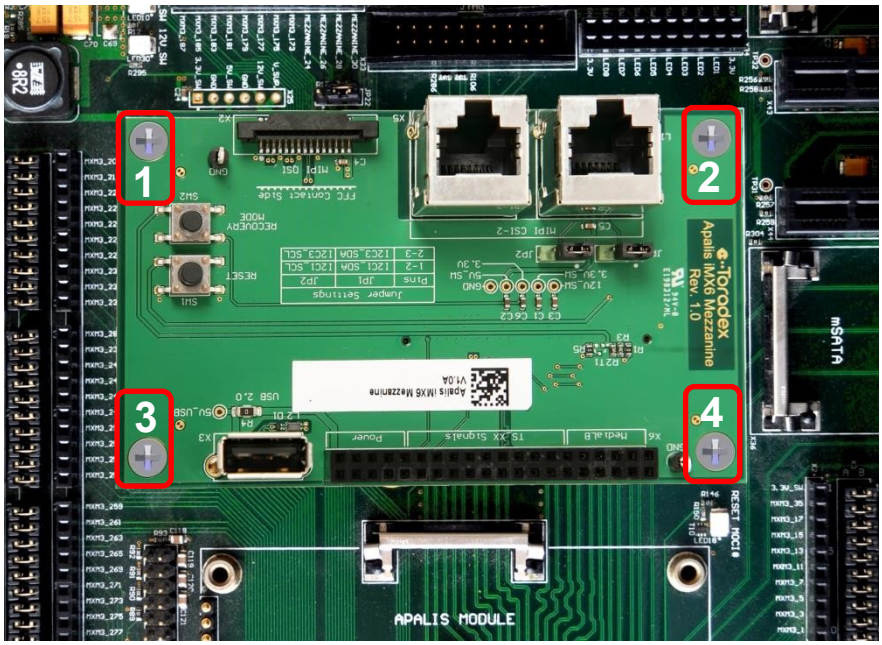
1. Carefully align the mounting holes {1}, {2}, {3}, and {4} on the mezzanine to be in-line with the fasteners available on the Apalis Evaluation board. Place the mezzanine on the Apalis Evaluation Board.



2. As shown in the image below, support the Apalis Evaluation Board from the bottom side, place the fingers just beneath the Apalis Mezzanine mating connector. Apply pressure on the Apalis T30 Mezzanine from the top to make the proper connection. This procedure ensures that the Apalis Evaluation Board PCB does not flex or bent while connecting the Apalis T30 Mezzanine.



3. Optional: Use 4 units of M3 screws to affix the mezzanine together with the Apalis Evaluation Board.



4. Done. The Apalis T30 Mezzanine is now firmly connected to the Apalis Evaluation Board.

5. Temperature Range

5.1. Operating Temperature Range

- -40 °C to +85 °C

6. Mechanical Data

6.1. Dimensions - Top Side

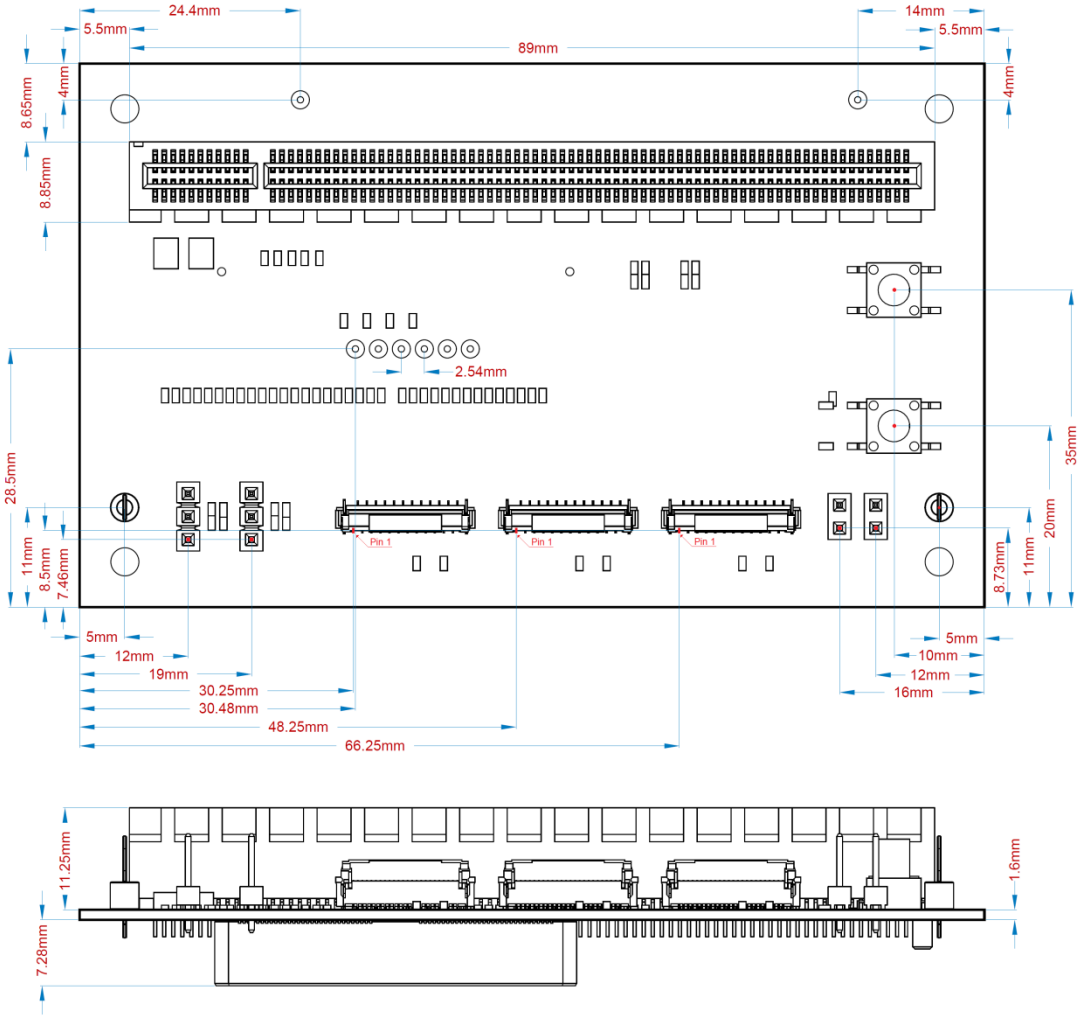


Fig.4 Apalis T30 Mezzanine Board Mechanical Drawing – Top Side
All dimensions in millimetres (mm)

6.2. Dimensions - Bottom Side

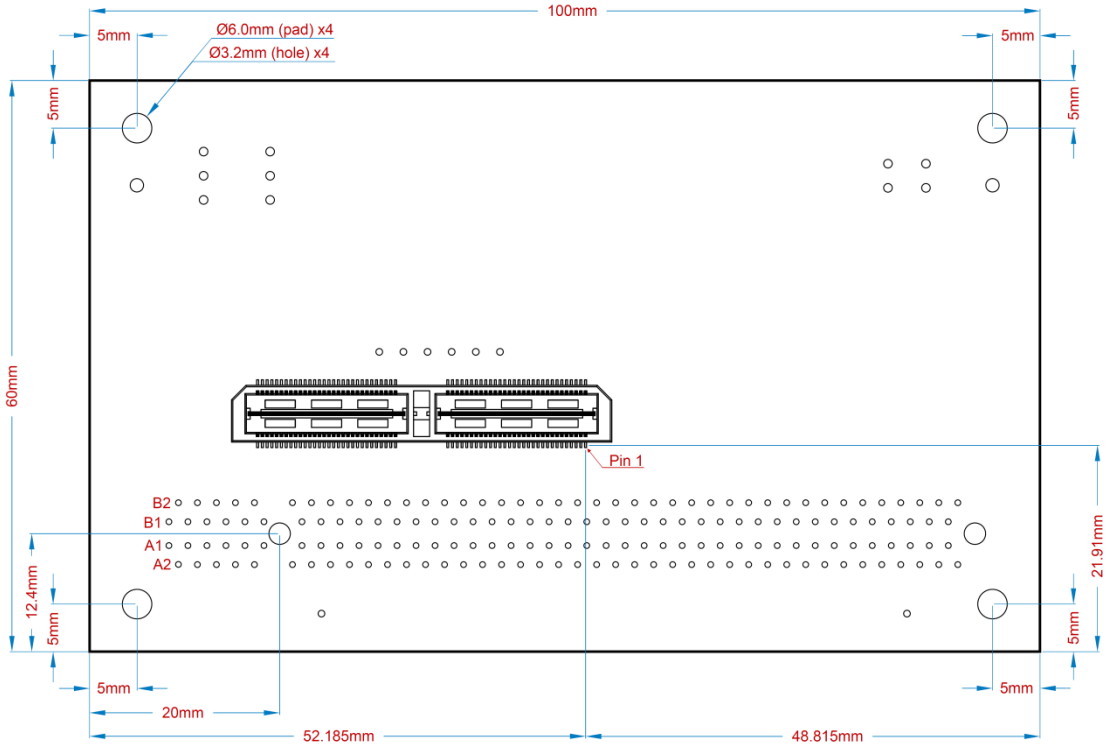


Fig.5 Apalis T30 Mezzanine Board Mechanical Drawing – Bottom Side
All dimensions in millimetres (mm)

7. Design Data

The design data for the Toradex carrier board and adapter board are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the adapter board design data, please use the web-link below:

http://developer.toradex.com/carrier-board-design/reference-designs

8. Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Materials, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance