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Apalis T30

Datasheet

Revision History

Date	Doc. Rev.	Apalis T30 Version	Changes
24-Jan-2013	Rev. 1.0	V1.0	Initial Release: Preliminary version
11-Apr-2014	Rev. 1.1	V1.0	Minor corrections
04-Jul-2014	Rev. 1.2	V1.0	Update section 1.4 with a comparison between different module versions Update size of RAM and Flash Clarifications of the table in section 1.5 Correction of used SPI instance for CAN controller 1 in Table 5-39 Add new section 5.11 Controller Area Network (CAN) Add typical power consumption numbers
14-Aug-2014	Rev. 1.3	V1.1	Product version updated.
27-Nov-2014	Rev. 1.4	V1.1	Section 9.7 renamed and updated Information added to the speed limit of MCP2515 (section 5.11) Electrical Characteristics updated (section 9.2) Additional information to RTC added (section 5.8.1) Known issues updated (section 8)
03-Feb-2015	Rev. 1.5	V1.1	Add additional information to UHS-I capability of MMC1 interface (section 5.14)
21-Mar-2016	Rev. 1.6	V1.1	Thermal Specification (section 9.6): Minor corrections
14-Feb-2017	Rev. 1.7	V1.1	Revision History: Updated document revision and product version details Updated broken web-links (section 1.5) Changed heading (section 1.5.7) Corrected typing error (section 5.8.1)
08-Oct-2018	Rev. 1.8	V1.1	Section 1.4.2: adding flash memory endurance remark Section 3.2: rename DAP1_RESET to DAP1_RESET# Section 5.1.3 clarify RESET_MOCI# behavior during power-up Section 5.15: correct SGTL500 pin number for AAP1_HP_L Section 5.16.2: rename DAP1_RESET to DAP1_RESET# Section 9.2: update RTC current consumption Section 9.6: clarify thermal behavior
30-Sep-2020	Rev. 1.9	V1.1	Section 9.4.1: Update the MXM3 connector
08-Feb-2021	Rev. 1.10	V1.2	Section 1.6: Update reference document links Update Figure 3 and Figure 4 Section 8: Clarify RTC issue Section 9.2: Rename section and remove power consumption measurements Minor changes
02-May-2022	Rev. 2.0	V1.2	Section 1.1: Add purpose of the datasheet Section 9.3: Add power consumption section. Change contact email address to support@toradex.com Minor changes
19-Oct-2022	Rev. 2.1	V1.2	Section 5.1.3: Clarified reset behavior

Contents

1. Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the Apalis T30 module. For information on the actual features supported by software, please refer to the relevant SoM product page on the Toradex Developer website: https://developer.toradex.com/products/apalis-t30.

1.2 Hardware

The Apalis T30 is a computer module based on the NVIDIA© Tegra 3 embedded System-on-Chip (SoC). The Cortex A9 quad-core CPU peaks up to 1.4 GHz Single Core / 1.3 GHz Quad-Core. The module delivers very high CPU and graphic performance with minimum power consumption.

The Apalis T30 incorporates DVFS (Dynamic Voltage and Frequency Switching) and Thermal Throttling, enabling the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption.

The integrated NVIDIA Graphics enables visually rich, smooth, and fast user interfaces.

The module targets a wide range of applications, including Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment System, POS, Data Acquisition, Thin Clients, Robotics, Gaming, and much more

It offers a wide range of interfaces from simple GPIOs, industry-standard I2C and SPI buses to high-speed USB 2.0 interfaces and high-speed PCI Express and SATA. The HDMI and dual-channel LVDS interfaces make it very easy to connect large, full HD and beyond resolution displays.

The Apalis T30 module encapsulates the complexity associated with modern-day electronic design, such as high-speed impedance-controlled layouts with high component density utilizing blind and buried via technology. This allows the customer to create a carrier board that implements the application-specific electronics, which is generally much less complicated. The Apalis T30 module takes this one step further and implements an interface pinout, which allows direct connection of real-world I/O ports without needing to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high speed. These serial technologies use impedance controlled differential pairs, as it allows them to easily route such interfaces to standard connectors in a simple, robust fashion.

1.3 Software

The Apalis T30 comes pre-installed with a Windows Embedded Compact 7 Operating System. Embedded Linux based around NVIDIA's "Linux for Tegra" is also available.

Toradex works with partners in case you require another Operating System. For more information, contact our support.

1.4 Main Features

1.4.1 CPU

	Apalis T30 2GB	Apalis T30 1GB IT Apalis T30 1GB
NVIDIA SoC	T30MQS	T30MQS
CPU Cores	4+1	4+1
L1 Instruction Cache (each core)	32KByte	32KByte
L1 Data Cache (each core)	32KByte	32KByte
L2 Cache (shared by cores)	1MByte	1MByte
NEON MPE	✓	✓
Maximum CPU frequency (single-core mode)	1.4GHz	1.4GHz
Maximum CPU frequency (quad-core mode peak performance, time and temperature limited)	1.3GHz	1.3GHz

1.4.2 Memory

	Apalis T30 2GB	Apalis T30 1GB IT Apalis T30 1GB
DDR3 RAM Size	2GByte	1GByte
DDR3 RAM Speed (max)	1600MT/s	1600MT
DDR3 RAM Memory Width	32bit	32bit
eMMC NAND Flash (8bit) [2]	8GByte [1]	4GByte

[1] Early samples were equipped with only 2Gbyte.
[2] eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear-leveling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.4.3 Interfaces

	Apalis T30 2GB	Apalis T30 1GB IT Apalis T30 1GB
LCD RGB 24bit (2048 x 1536)	1	1
Single/dual channel LVDS 18/24bit, colour mapping configurable (1920x1440)	1	1
HDMI 1.4a 1080p60 (1920x1080) (3D Video Format support)	1	1
VGA Analogue Video (1920x1200)	1	1
MIPI DSI	2x 2 Data Lanes*	2x 2 Data Lanes*
Resistive Touch Screen	4 Wire	4 Wire
Analogue Audio Headphone out	1 (Stereo)	1 (Stereo)
Analogue Audio Line in	1 (Stereo)	1 (Stereo)
Analogue Audio Mic in	1 (Mono)	1 (Mono)
HD Audio /I^{2}S	1+1*	1+1*
S/PDIF	1 in / 1 out	1 in / 1 out
Parallel Camera Interface (8/10 bit)	1	1

	Apalis T30 2GB	Apalis T30 1GB IT Apalis T30 1GB
MIPI CSI-2	2x 2 Data Lanes*/ 1x 4 Data Lanes*	2x 2 Data Lanes*/ 1x 4 Data Lanes*
I^2C	3+1*	3+1*
SPI	2+2*	2+2*
UART	4+1*	4+1*
SD/SDIO/MMC	2+1* (2x8Bit + 1x4Bit)	2+1* (2x8Bit + 1x4Bit)
GPIO	8+121*	8+121*
USB 2.0 high speed OTG (host/device)	1	1
USB 2.0 high-speed host	2	2
PCIe (Gen 1.0)	5 Lane (1 x1 +1 x4*)	5 Lane (1 x1 +1 x4*)
Serial ATA II (3Gbit/s)	1	1
One-Wire	1*	1*
Keypad	8x16 Matrix*	8x16 Matrix*
PWM	4	4
Analogue Inputs	4	4
CAN	2	2
10/100/1000 MBit/s Ethernet	1	1
Ethernet Controller	Intel I210	Intel I211
IEEE1588 Precision Clock	✓	✓
Manageability	✓	-

*These interfaces are available on pins that are not defined as standard interfaces in the Apalis architecture. The pins are either located in the Type-specific area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. For more information, please check the list of Type-specific interfaces in section 1.5 and the description of the associated interface in section 5

1.4.4 HD Video Decode

- ✓ H.264 (Baseline Profile, Main Profile, High Profile) —1080p@30, 1080p@48, 1080p60
- ✓ WMV9 VC-1 (Simple, Main and Advanced Profiles) — 1080p@30, 1080i@60
- ✓ MPEG-4 (Simple + B frames) — 1080p@30
- ✓ MPEG-2 (Main Profile) — 1080p@30, 1080i@60
- ✓ H.263 (Profile 0) — 1080p@30
- ✓ DivX 4/5/6 (Home Theatre Profile) — 1080p@30
- ✓ XviD — 1080p/30Mbps
- ✓ JPEG up to 120 MPixel per second

1.4.5 HD Video Encode

- ✓ H.264 (Baseline Profile) — 1080p/30Mbps
- ✓ MPEG-4 (Simple Profile) — 1080p@24
- ✓ H.263 (Profile 0) — 1080p@24
- ✓ JPEG up to 120 MPixel per second

1.4.6 Ultra-low Power NVIDIA GeForce GPU

- ✓ OpenGL® ES 1.1 and 2.0 (depending on the driver)
- ✓ Dual-Core (2 fragment shader pipe, vertex shader pipe)
- ✓ OpenGL ES Shader Performance 16 GFLOPS
- ✓ Programmable pixel shader
- ✓ Programmable vertex and lighting
- ✓ Antialiasing: 5x VCAA, 4xFSAA, or both
- ✓ 2K x 2K texture and 4K x 4K render resolutions supported
- ✓ Advanced 2D and vector engine

1.4.7 3D Vision (Support requires additional license and royalty fee)

- ✓ Automatic Stereo
- ✓ Built-in (native) pixel Interleaving support
- ✓ 3D Video and Photo Capture
- ✓ 3D Video and Photo Playback
- ✓ HDMI 1.4a Frame packing 1080p24

1.4.8 Digital Audio Decode

- ✓ AAC-LC, AAC, AAC+, eAAC+
- ✓ WMA7/8/9, WMA Lossless, WMA Pro LBR 10,
- ✓ MP3
- ✓ AC3
- ✓ MPEG2
- ✓ WAVE

1.4.9 Digital Audio Encode

- ✓ AAC-LC
- ✓ AMR-WB / AMR-NB

1.4.10 Timers

- ✓ 10 timers
- ✓ 1 Microsecond resolution
- ✓ Watchdog function

1.4.11 Supported Operating Systems

- ✓ Windows Embedded Compact 7
- ✓ Embedded Linux based on Linux For Tegra
- ✓ Contact Toradex for Android
- ✓ Other operating systems are available through 3rd party companies

1.5 Interface Overview

The table in Figure 1 shows the interfaces supported on the Apalis® T30 module and whether an interface is provided on standard or Type-specific pins. The PCI-Express interface is an example of an interface that uses standard and Type-specific pins – one lane is provided as part of the standard interface pinout. The additional four lanes are Type-specific.

Some interfaces are available as an alternate function of a pin. This function can only be used if the primary function of the pin is not used. Check section 4.4 for a list of all alternate functions of the MXM3 pins.

Feature	Apalis®™ T30	Standard	Type-Specific	Alternate Function
4 Wire Resistive Touch	1	1		
Analogue Inputs	4	4		
Analogue Audio	1	1		
CAN	2	1		
CSI (Dual Lane)	2		2	
DSI	2		1	1
Dual-Channel LVDS Display (1x Single or 1x Dual)	1	1		
Gigabit Ethernet	1	1		
GPIO	129	8	6	115
HDA	2	1		1
HDMI (TDMS)	1	1		
I2C	4	3		1
I2S (multiplexed with HDA)	2	1		1
Parallel Camera (8/10bit)	1	1 (8bit)	(additional bits)	
Parallel LCD (24 bit)	1	1		
PCI-Express (lane count)	5	1 (1 Port)	4 (1 Port)	
PWM	4	4		
SATA	1	1		
SD/SDIO/MMC	3	2 (1x 8bit +1x 4bit)	1 (8bit)	
S/PDIF	1	1		
SPI	4	2		2
UART	5	4		1
USB	3 (USB 2.0)	3		
VGA	1	1		
One-Wire	1			1

Figure 1: Apalis® T30 Module Interfaces

1.6 Reference Documents

1.6.1 NVIDIA Tegra T30

You can find the details about the T30 system on a chip (SoC) in the Datasheet and Technical Reference Manual provided by NVIDIA. (Registration required)

https://developer.nvidia.com/tegra-3-technical-reference-manual

1.6.2 Ethernet Controller

Apalis T30 uses the Intel I210-AT Gigabit Ethernet Controller Chip

https://ark.intel.com/content/www/us/en/ark/products/64400/intel-ethernet-controller-i210-at.html

1.6.3 Audio Codec

Apalis T30 uses the NXP/Freescale SGTL5000 Audio Codec.
https://www.nxp.com/products/audio-and-radio/audio-converters/ultra-low-power-audio-codec:SGTL5000 http://www.nxp.com/products/media-and-audio-processing/data-converters/audio-converters/audio-codec/ultra-low-power-audio-codec:SGTL5000

1.6.4 Touch Screen Controller / ADC

Apalis T30 uses the STMicroelectronics STMPE811 Touchscreen Controller.
https://www.st.com

1.6.5 Apalis Carrier Board Design Guide

This document provides additional information about the Apalis form factor. A custom carrier board should follow the Apalis Carrier Board Design Guide to make the board compatible with the Apalis module family. Please study this document in detail before starting your carrier board design.

https://developer.toradex.com/carrier-board-design/carrier-board-design-guides

1.6.6 Toradex Developer Center

You can find much additional information in the Toradex Developer Center, updated regularly with the latest product support information. Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information is valid or relevant for the Apalis T30.

https://developer.toradex.com

1.6.7 Apalis Carrier Board Schematics

We provide the completed schematics plus the Altium project file, including library symbols and IPC-7351 compliant footprints for the Apalis Evaluation Board and other carrier boards free of charge. This is a great help when designing your own Carrier Board.

https://developer.toradex.com/carrier-board-design/reference-designs

1.6.8 Layout Design Guide

This document contains information about high-speed layout design and additional information that helps to get the carrier board layout the first time right.

http://docs.toradex.com/102492-layout-design-guide.pdf

1.6.9 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparing the interfaces of different modules.

http://developer.toradex.com/knowledge-base/pinout-designer

2. Architecture Overview

2.1 Block Diagram

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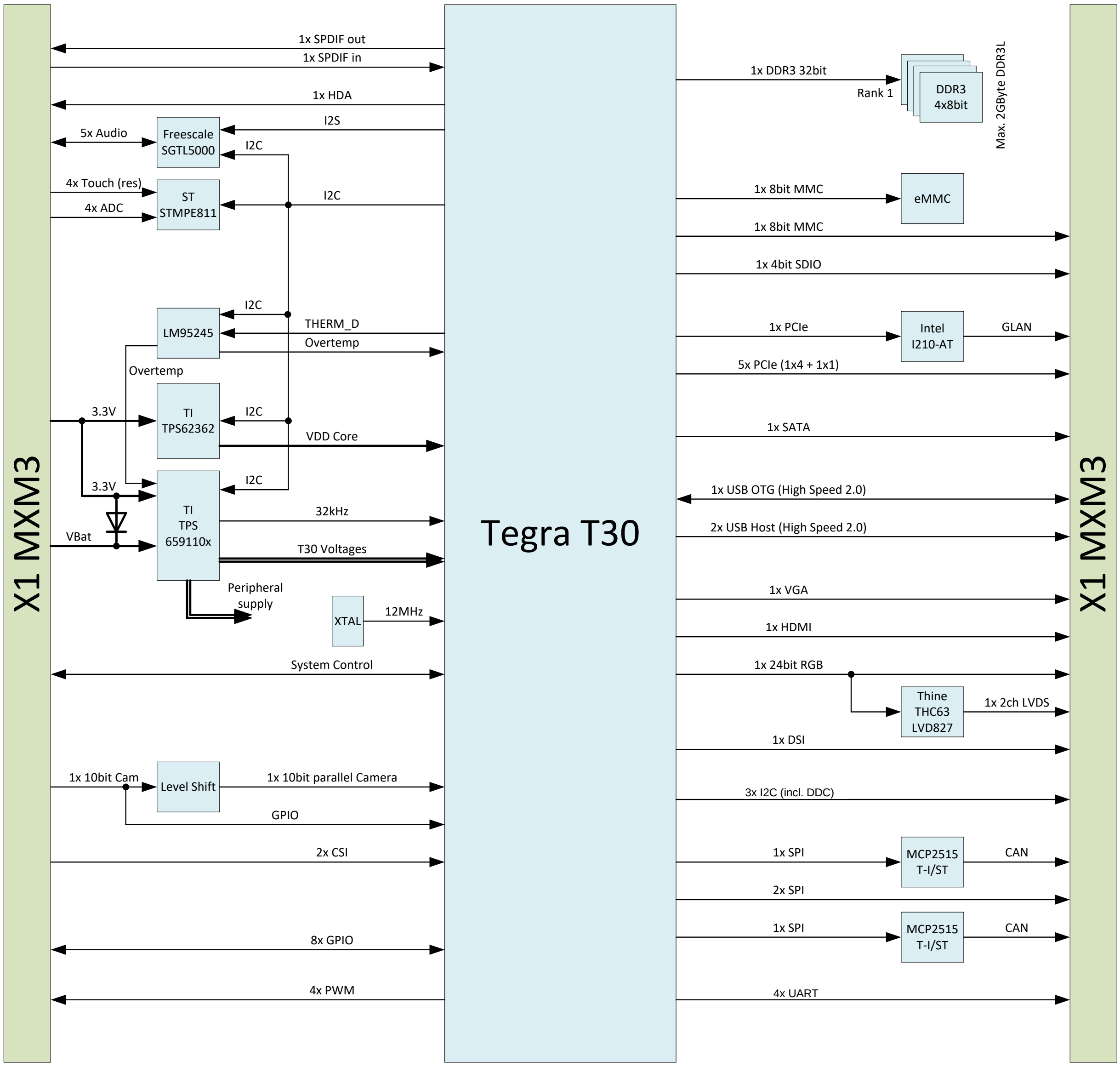

Figure 2 Apalis T30 Block Diagram

3. Apalis T30 Connectors

3.1 Pin Numbering

The diagrams in figures Figure 3 and Figure 4 show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema. Pins on the top side of the module have an even number, and pins on the bottom side have an odd number.

The pin number increases linearly as a multiple of the pitch – that is, pins that are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins that do not exist due to the connector notch are also accounted for (pins 166 through 172).

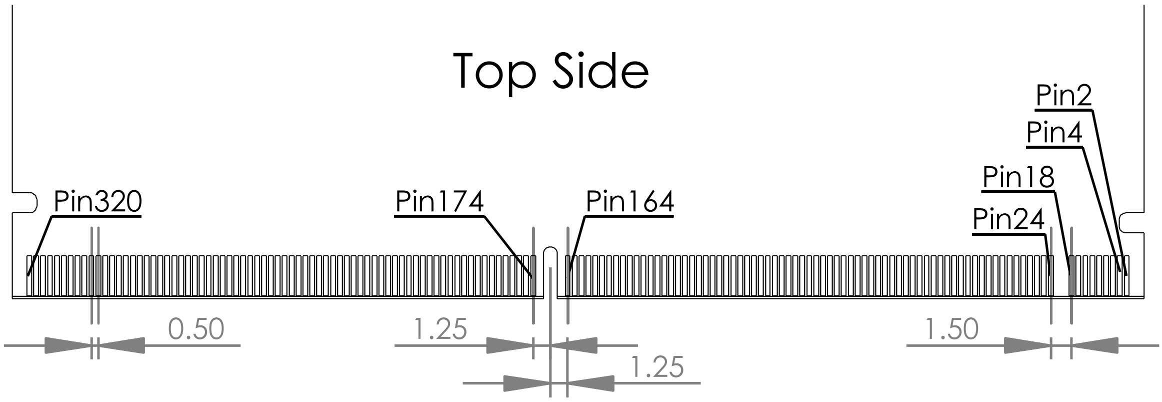

Figure 3: Pin numbering schema on the top side of the module (top view)

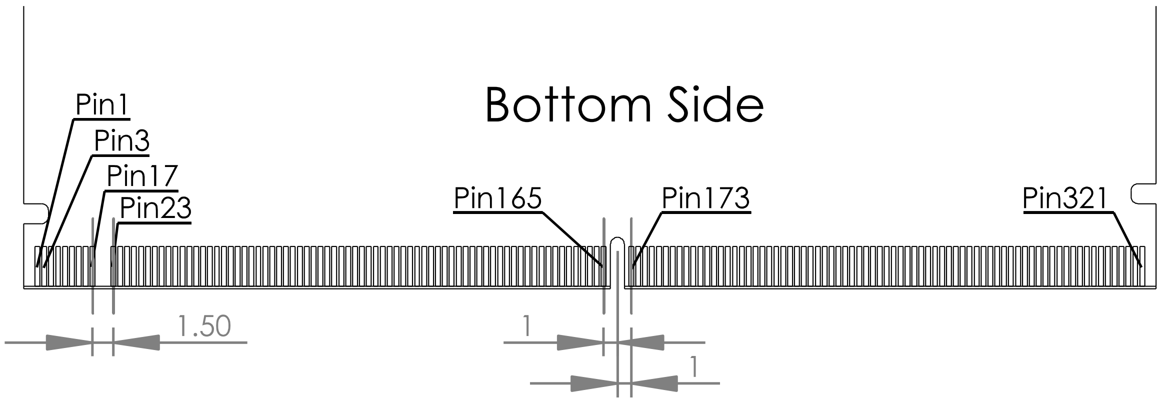

Figure 4: Pin numbering schema on the bottom side of the module (bottom view)

3.2 Assignment

The following table describes the MXM3 connector pinout. It should be noted that some of the pins are multiplexed; this means there is more than one Tegra pin connected to one module edge connector pin. For example, KB_ROW0 and VI_D2 are both assigned to MXM3 pin 187. Care should be taken to ensure that multiplexed Tegra pins are tri-stated when they are not being used (e.g., if Tegra pins A and pin B are tied to the same MXM3 pin, then if you are driving Tegra pin A, pin B should be tri-stated). Additional information can be found in chapter 4.1: Function Multiplexing.

Some pins are shaded dark grey as Type-specific interfaces. These pins might not be compatible with other modules in the Apalis family. Please be aware that you might lose compatibility with other Apalis modules on your carrier board if you make use of these interfaces. It should be noted that Type-specific interfaces are kept standard across modules that share such interfaces where possible. For example, suppose both module A and module B have three additional PCI-Express lanes available in the same configurations as a Type-specific interface. In that case, they shall be assigned to the same pins in the Type-specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the Type-specific interface.

- X1: Pin number on the MXM3 module edge connector (X1).
- Apalis Signal Name: The name of the signal according to the Apalis form factor definition. This name corresponds to the default usage of the pin. Most of the pins also have an alternative function. However, to be compatible with other Apalis modules, only the default function should be used, and the carrier board should be implemented according to the Apalis Carrier Board Design Guide.
- Tegra 3 Pin Name: The name of the pin of the Tegra chip.

Table 3-1 X1 Connector

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes	X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
1	GPIO1	KB_ROW10		2	PWM1	GPIO_PU6	
3	GPIO2	KB_ROW11		4	PWM2	GPIO_PU5	
5	GPIO3	KB_ROW12		6	PWM3	GPIO_PU4	
7	GPIO4	KB_ROW13		8	PWM4	GPIO_PU3	
9	GND			10	VCC		
11	GPIO5	KB_ROW14		12	CAN1_RX		MCP2515 Pin20
13	GPIO6	KB_COL0 / OWR	Multiplexed	14	CAN1_TX		MCP2515 Pin19
15	GPIO7	KB_ROW15		16	CAN2_RX		MCP2515 Pin20
17	GPIO8	KB_COL1		18	CAN2_TX		MCP2515 Pin19
23	GND			24	POWER_ENABLE_MOCI		PWR Management
25	SATA1_RX+	SATA_L0_RXP		26	RESET_MOCI#	GMI_RST_N	PWR Management
27	SATA1_RX-	SATA_L0_RXN		28	RESET_MICO#		PWR Management
29	GND			30	VCC		
31	SATA1_TX-	SATA_L0_TXN		32	ETH1_MDI2+		I210 Pin 32
33	SATA1_TX+	SATA_L0_TXP		34	ETH1_MDI2-		I210 Pin 34
35	SATA1_ACT#	PEX_L0_PRSNT_N		36	VCC		
37	WAKE1_MICO	GPIO_PV1		38	ETH1_MDI3+		I210 Pin 38
39	GND			40	ETH1_MDI3-		I210 Pin 40
41	PCIE1_RX-	PEX_L4_RXN		42	ETH1_ACT		I210 Pin 42
43	PCIE1_RX+	PEX_L4_RXP		44	ETH1_LINK		I210 Pin 44
45	GND			46	ETH1_CTREF		NC

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
47	PCIE1_TX-	PEX_L4_TXN	
49	PCIE1_TX+	PEX_L4_TXP	
51	GND		
53	PCIE1_CLK-	PEX_CLK2N	
55	PCIE1_CLK+	PEX_CLK2P	
57	GND		
59	TS_DIFF1-	PEX_CLK1N	Type-specific
61	TS_DIFF1+	PEX_CLK1P	Type-specific
63	TS_1	GMI_OE_N	Type-specific
65	TS_DIFF2-	PEX_L0_RXN	Type-specific
67	TS_DIFF2+	PEX_L0_RXP	Type-specific
69	GND		
71	TS_DIFF3-	PEX_L0_TXN	Type-specific
73	TS_DIFF3+	PEX_L0_TXP	Type-specific
75	GND		
77	TS_DIFF4-	PEX_L1_RXN	Type-specific
79	TS_DIFF4+	PEX_L1_RXP	Type-specific
81	GND		
83	TS_DIFF5-	PEX_L1_TXN	Type-specific
85	TS_DIFF5+	PEX_L1_TXP	Type-specific
87	TS_2	KB_COL7	Type-specific
89	TS_DIFF6-	PEX_L2_RXN	Type-specific
91	TS_DIFF6+	PEX_L2_RXP	Type-specific
93	GND		
95	TS_DIFF7-	PEX_L2_TXN	Type-specific
97	TS_DIFF7+	PEX_L2_TXP	Type-specific
99	TS_3	VI_D11 / KB_COL5	Multiplexed, Type-specific
101	TS_DIFF8-	PEX_L3_RXN	Type-specific
103	TS_DIFF8+	PEX_L3_RXP	Type-specific
105	GND		
107	TS_DIFF9-	PEX_L3_TXN	Type-specific
109	TS_DIFF9+	PEX_L3_TXP	Type-specific
111	GND		
113	TS_DIFF10-	DSI_D2AN	Type-specific
115	TS_DIFF10+	DSI_D2AP	Type-specific
117	GND		

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
48	ETH1_MDI0-		I210 Pin 57
50	ETH1_MDI0+		I210 Pin 58
52	VCC		
54	ETH1_MDI1-		I210 Pin 54
56	ETH1_MDI1+		I210 Pin 55
58	VCC		
60	USBO1_VBUS	USB1_VBUS	
62	USBO1_SSRX+		NC
64	USBO1_SSRX-		NC
66	VCC		
68	USBO1_SSTX+		NC
70	USBO1_SSTX-		NC
72	USBO1_ID	ACC1_DETECT	
74	USBO1_D+	USB1_DP	
76	USBO1_D-	USB1_DN	
78	VCC		
80	USBH2_D+	USB2_DP	
82	USBH2_D-	USB2_DN	
84	USBH_EN	PEX_L0_RST_N	
86	USBH3_D+	USB3_DP	
88	USBH3_D-	USB3_DN	
90	VCC		
92	USBH4_SSRX-		NC
94	USBH4_SSRX+		NC
96	USBH_OC#	PEX_L0_CLKREQ_N	
98	USBH4_D+		NC
100	USBH4_D-		NC
102	VCC		
104	USBH4_SSTX-		NC
106	USBH4_SSTX+		NC
108	VCC		
110	UART1_DTR	ULPI_DATA7	
112	UART1_TXD	ULPI_DATA0	
114	UART1_RTS	ULPI_DATA3	
116	UART1_CTS	ULPI_DATA2	
118	UART1_RXD	ULPI_DATA1	

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes	X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
119	TS_DIFF11-	DSI_D1AN	Type-specific	120	UART1_DSR	ULPI_DATA6	
121	TS_DIFF11+	DSI_D1AP	Type-specific	122	UART1_RI	ULPI_DATA4	
123	TS_4	VI_D10 / KB_COL6	Multiplexed, Type-specific	124	UART1_DCD	ULPI_DATA5	
125	TS_DIFF12-	DSI_CLKAN	Type-specific	126	UART2_TXD	ULPI_CLK	
127	TS_DIFF12+	DSI_CLKAP	Type-specific	128	UART2_RTS	ULPI_STP	
129	GND			130	UART2_CTS	ULPI_NXT	
131	TS_DIFF13-	CSI_CLKBN	Type-specific	132	UART2_RXD	ULPI_DIR	
133	TS_DIFF13+	CSI_CLKBP	Type-specific	134	UART3_TXD	UART2_TXD	
135	TS_5	VI_D0 / KB_ROW8	Multiplexed, Type-specific	136	UART3_RXD	UART2_RXD	
137	TS_DIFF14-	CSI_D2BN	Type-specific	138	UART4_TXD	UART3_TXD	
139	TS_DIFF14+	CSI_D2BP	Type-specific	140	UART4_RXD	UART3_RXD	
141	GND	_GND		142	GND		
143	TS_DIFF15-	CSI_D1BN	Type-specific	144	MMC1_D2	SDMMC3_DAT2	
145	TS_DIFF15+	CSI_D1BP	Type-specific	146	MMC1_D3	SDMMC3_DAT3	
147	GND	_GND		148	MMC1_D4	SDMMC3_DAT4	
149	TS_DIFF16-	CSI_D2AN	Type-specific	150	MMC1_CMD	SDMMC3_CMD	
151	TS_DIFF16+	CSI_D2AP	Type-specific	152	MMC1_D5	SDMMC3_DAT5	
153	GND	_GND		154	MMC1_CLK	SDMMC3_CLK	
155	TS_DIFF17-	CSI_D1AN	Type-specific	156	MMC1_D6	SDMMC3_DAT6	
157	TS_DIFF17+	CSI_D1AP	Type-specific	158	MMC1_D7	SDMMC3_DAT7	
159	TS_6	VI_D1 / KB_ROW9	Multiplexed, Type-specific	160	MMC1_D0	SDMMC3_DAT0	
161	TS_DIFF18-	CSI_CLKAN	Type-specific	162	MMC1_D1	SDMMC3_DAT1	
163	TS_DIFF18+	CSI_CLKAP	Type-specific	164	MMC1_CD#	GPIO_PV3	
165	GND	_GND					
173	CAM1_D7	VI_D9 / KB_ROW7	Multiplexed	174	VCC_BACKUP		
175	CAM1_D6	VI_D8 / KB_ROW6	Multiplexed	176	SD1_D2	SDMMC1_DAT2	
177	CAM1_D5	VI_D7 / KB_ROW5	Multiplexed	178	SD1_D3	SDMMC1_DAT3	
179	CAM1_D4	VI_D6 / KB_ROW4	Multiplexed	180	SD1_CMD	SDMMC1_CMD	
181	CAM1_D3	VI_D5 / KB_ROW3	Multiplexed	182	GND		
183	CAM1_D2	VI_D4 / KB_ROW2	Multiplexed	184	SD1_CLK	SDMMC1_CLK	
185	CAM1_D1	VI_D3 / KB_ROW1	Multiplexed	186	SD1_D0	SDMMC1_DAT0	
187	CAM1_D0	VI_D2 / KB_ROW0	Multiplexed	188	SD1_D1	SDMMC1_DAT1	
189	GND	_GND		190	SD1_CD#	CLK2_REQ	

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
191	CAM1_PCLK	VI_PCLK / KB_COL2	Multiplexed
193	CAM1_MCLK	CAM_MCLK	
195	CAM1_VSYNC	VI_VSYNC / KB_COL3	Multiplexed
197	CAM1_HSYNC	VI_HSYNC / KB_COL4	Multiplexed
199	GND		
201	I2C3_SDA (CAM)	CAM_I2C_SDA	
203	I2C3_SCL (CAM)	CAM_I2C_SCL	
205	I2C2_SDA (DDC)	DDC_SDA	
207	I2C2_SCL (DDC)	DDC_SCL	
209	I2C1_SDA	GEN1_I2C_SDA	
211	I2C1_SCL	GEN1_I2C_SCL	
213	GND		
215	SPDIF1_OUT	SPDIF_OUT	
217	SPDIF1_IN	SPDIF_IN	
219	GND		
221	SPI1_CLK	SPI1_SCK	
223	SPI1_MISO	SPI1_MISO	
225	SPI1_MOSI	SPI1_MOSI	
227	SPI1_CS	SPI1_CS0_N	
229	SPI2_MISO	LCD_SDIN	
231	SPI2_MOSI	LCD_SDOUT	
233	SPI2_CS	LCD_CS0_N	
235	SPI2_CLK	LCD_SCK	
237	GND		
239	BKL1_PWM	UART3_RTS_N	
241	GND		
243	LCD1_PCLK	LCD_PCLK	
245	LCD1_VSYNC	LCD_VSYNC	
247	LCD1_HSYNC	LCD_HSYNC	
249	LCD1_DE	LCD_DE	
251	LCD1_R0	LCD_D22	
253	LCD1_R1	LCD_D23	
255	LCD1_R2	LCD_D12	
257	LCD1_R3	LCD_D13	
259	LCD1_R4	LCD_D14	
261	LCD1_R5	LCD_D15	

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
192	GND		
194	DAP1_MCLK	CLK2_OUT	
196	DAP1_D_OUT	DAP1_DOUT	
198	DAP1_RESET#	CLK1_REQ	
200	DAP1_BIT_CLK	DAP1_SCLK	
202	DAP1_D_IN	DAP1_DIN	
204	DAP1_SYNC	DAP1_FS	
206	GND		
208	VGA1_R	VDAC_R	
210	VGA1_G	VDAC_G	
212	VGA1_B	VDAC_B	
214	VGA1_HSYNC	CRT_HSYNC	
216	VGA1_VSYNC	CRT_VSYNC	
218	GND		
220	HDMI1_CEC	HDMI_CEC	
222	HDMI1_TXD2+	HDMI_TXD2P	
224	HDMI1_TXD2-	HDMI_TXD2N	
226	GND		
228	HDMI1_TXD1+	HDMI_TXD1P	
230	HDMI1_TXD1-	HDMI_TXD1N	
232	HDMI1_HPD	HDMI_INT	
234	HDMI1_TXD0+	HDMI_TXD0P	
236	HDMI1_TXD0-	HDMI_TXD0N	
238	GND		
240	HDMI1_TXC+	HDMI_TXCP	
242	HDMI1_TXC-	HDMI_TXCN	
244	GND		
246	LVDS1_A_CLK-		THC63LVD827 Pin B4
248	LVDS1_A_CLK+		THC63LVD827 Pin A4
250	GND		
252	LVDS1_A_TX0-		THC63LVD827 Pin B1
254	LVDS1_A_TX0+		THC63LVD827 Pin A1
256	GND		
258	LVDS1_A_TX1-		THC63LVD827 Pin B2
260	LVDS1_A_TX1+		THC63LVD827 Pin A2
262	USBO1_OC#	GEN2_I2C_SDA	

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
263	LCD1_R6	LCD_D16	
265	LCD1_R7	LCD_D17	
267	GND		
269	LCD1_G0	LCD_D20	
271	LCD1_G1	LCD_D21	
273	LCD1_G2	LCD_D6	
275	LCD1_G3	LCD_D7	
277	LCD1_G4	LCD_D8	
279	LCD1_G5	LCD_D9	
281	LCD1_G6	LCD_D10	
283	LCD1_G7	LCD_D11	
285	GND		
287	LCD1_B0	LCD_D18	
289	LCD1_B1	LCD_D19	
291	LCD1_B2	LCD_D0	
293	LCD1_B3	LCD_D1	
295	LCD1_B4	LCD_D2	
297	LCD1_B5	LCD_D3	
299	LCD1_B6	LCD_D4	
301	LCD1_B7	LCD_D5	
303	AGND		
305	AN1_ADC0		STMPE811 Pin8
307	AN1_ADC1		STMPE811 Pin9
309	AN1_ADC2		STMPE811 Pin11
311	AN1_TSWIP_ADC 3		STMPE811 Pin12
313	AGND		
315	AN1_TSPX		STMPE811 Pin13
317	AN1_TSMX		STMPE811 Pin16
319	AN1_TSPY		STMPE811 Pin15
321	AN1_TSMY		STMPE811 Pin1

X1	Apalis Signal Name	Tegra 3 Pin Name	Notes
264	LVDS1_A_TX2-		THC63LVD827 Pin B3
266	LVDS1_A_TX2+		THC63LVD827 Pin A3
268	GND		
270	LVDS1_A_TX3-		THC63LVD827 Pin B5
272	LVDS1_A_TX3+		THC63LVD827 Pin A5
274	USBO1_EN	GEN2_I2C_SCL	
276	LVDS1_B_CLK-		THC63LVD827 Pin B9
278	LVDS1_B_CLK+		THC63LVD827 Pin A9
280	GND		
282	LVDS1_B_TX0-		THC63LVD827 Pin B6
284	LVDS1_B_TX0+		THC63LVD827 Pin A6
286	BKL1_ON	GPIO_PV2	
288	LVDS1_B_TX1-		THC63LVD827 Pin B7
290	LVDS1_B_TX1+		THC63LVD827 Pin A7
292	GND		
294	LVDS1_B_TX2-		THC63LVD827 Pin B8
296	LVDS1_B_TX2+		THC63LVD827 Pin A8
298	GND		
300	LVDS1_B_TX3-		THC63LVD827 Pin C8
302	LVDS1_B_TX3+		THC63LVD827 Pin C9
304	AGND		
306	AAP1_MICIN		SGTL5000 Pin 10
308	AGND		
310	AAP1_LIN_L		SGTL5000 Pin 9
312	AAP1_LIN_R		SGTL5000 Pin 8
314	AVCC		
316	AAP1_HP_L		SGTL5000 Pin 4
318	AAP1_HP_R		SGTL5000 Pin 1
320	AVCC		

4. I/O Pins

4.1 Function Multiplexing

Most of the NVIDIA Tegra Processors I/O pins have up to four special functions. They can be used as "regular" GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O).
For example, the Tegra Pin on connector X1, pin 134, has the primary function UART2-TXD, but can also provide the following alternative functions: SPDIF1.C-IN, UART1.C-RTS_N, or SPI4.B-SCK.

The default setting for this pin is the primary function UART2-TXD. It is strongly recommended to use a pin for a function that is compatible with the Apalis standard. This guarantees the best compatibility with the standard software and with the other modules in the Apalis family.

All the pins in the Tegra family are organized into supply domain groups. The alternative functions can be changed individually by pin. The following pad control register can only be changed per group and not per pin:

- HSM High-Speed Mode (Enable/Disable)
- SCHMT Schmitt Trigger (Enable/Disable)
- LPMD Low Power Mode
- DRVDN/UP Drive Down / Up
- SLWR/SLWF Slew Falling Rising

Most of the alternative functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In some cases, the available alternative functions of certain pins on the Tegra device were constrained; to allow maximum flexibility; some of these pins are paired and share the same MXM3 pin. As previously mentioned, ensure that the pair's unused pin is tri-stated to avoid undesired behavior or hardware damage.

The following module connector pins are connected to more than one pin on the Tegra T30:

Table 4-1 Apalis T30 Multiplexed Pins

MXM3 Pin #	Tegra Pin 1	Tegra Pin 2	Remarks
13	KB_COL0	OWR	
99	VI_D11	KB_COL5	Due to the unidirectional level shifter, VI_D11 can only be used as input. Use KB_COL5 if general-purpose output functionality is needed. See also Figure 5.
123	VI_D10	KB_COL6	Due to the unidirectional level shifter, VI_D10 can only be used as input. Use KB_COL6 if general-purpose output functionality is needed. See also Figure 5.
135	VI_D0	KB_COL8	Due to the unidirectional level shifter, VI_D0 can only be used as input. Use KB_COL8 if general-purpose output functionality is needed. See also Figure 5.
159	VI_D1	KB_ROW9	Due to the unidirectional level shifter, VI_D1 can only be used as input. Use KB_ROW9 if general-purpose output functionality is needed. See also Figure 5.
173	VI_D9	KB_ROW7	Due to the unidirectional level shifter, VI_D9 can only be used as input. Use KB_ROW7 if general-purpose output functionality is needed. See also Figure 5.
175	VI_D8	KB_ROW6	Due to the unidirectional level shifter, VI_D8 can only be used as input. Use KB_ROW8 if general-purpose output functionality is needed. See also Figure 5.

MXM3 Pin #	Tegra Pin 1	Tegra Pin 2	Remarks
177	VI_D7	KB_ROW5	Due to the unidirectional level shifter, VI_D7 can only be used as input. Use KB_ROW5 if general-purpose output functionality is needed. See also Figure 5.
179	VI_D6	KB_ROW4	Due to the unidirectional level shifter, VI_D6 can only be used as input. Use KB_ROW4 if general-purpose output functionality is needed. See also Figure 5.
181	VI_D5	KB_ROW3	Due to the unidirectional level shifter, VI_D5 can only be used as input. Use KB_ROW3 if general-purpose output functionality is needed. See also Figure 5.
183	VI_D4	KB_ROW2	Due to the unidirectional level shifter, VI_D4 can only be used as input. Use KB_ROW2 if general-purpose output functionality is needed. See also Figure 5.
185	VI_D3	KB_ROW1	Due to the unidirectional level shifter, VI_D3 can only be used as input. Use KB_ROW1 if general-purpose output functionality is needed. See also Figure 5.
187	VI_D2	KB_ROW0	Due to the unidirectional level shifter, VI_D2 can only be used as input. Use KB_ROW0 if general-purpose output functionality is needed. See also Figure 5.
191	VI_PCKL	KB_COL2	Due to the unidirectional level shifter, VI_PCKL can only be used as input. Use KB_COL2 if general-purpose output functionality is needed. See also Figure 5.
195	VI_VSYNC	KB_COL3	Due to the unidirectional level shifter, VI_VSYNC can only be used as input. Use KB_COL3 if general-purpose output functionality is needed. See also Figure 5.
197	VI_HSYNC	KB_COL4	Due to the unidirectional level shifter, VI_HSYNC can only be used as input. Use KB_COL4 if general-purpose output functionality is needed. See also Figure 5.

In the table in chapter 4.4, you find a list of all pins which have alternative functions. There you can find which alternative functions are available for each individual pin.

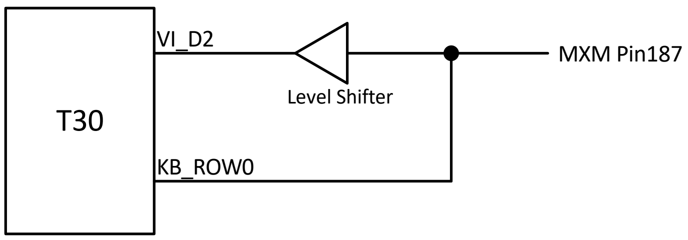

Figure 5 Parallel camera input level shifter circuit

The backlight PWM output signal on the module connector Pin 239 is connected to the UART3_RTS_N pin of the Tegra T30 and over a tri-state buffer to GPIO3 output of the TI 65911 power management IC. Both outputs can be configured to generate a PWM signal. Since the Tegra UART3_RTS_N pin internally uses the same PWM generator as used for the module connector pin 8, it is recommended to use the PWM signal generated in the power management IC. In this case, the UART3_RTS_N pin should be configured as high-impedance to avoid short circuits. The UART3_CTS_N pin of Tegra T30 controls the tri-state buffer for GPIO3. Disable the buffer's output by driving this pin high if the UART3_RTS_N pin is used to output the signal to the backlight PWM.

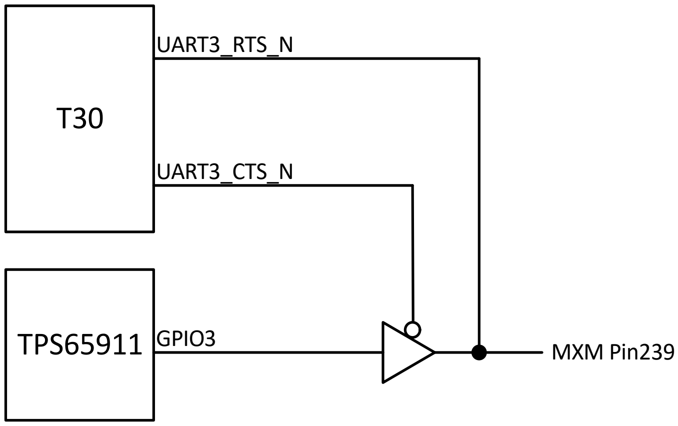

Figure 6 Backlight PWM output circuit

4.2 Pin Control

The Tegra T30 pins connected to the MXM3 module connector are available in three different pad types. The following table describes the differences between the types:

Abbr.	Pad type	Input buffer	Output buffer	Nominal pull strength	Slew rate control	Drive strength control
ST	Standard	Schmitt / CMOS	Push- Pull	50kΩ or 100kΩ	2-bits, up & down	5-bits, up & down LPMD
DD	Dual driver	Schmitt / CMOS	Push-Pull / Open-Drain	50kΩ	2-bits, up & down	5-bits, up & down LPMD
CZ	Controlled output impedance	Schmitt / CMOS	Push- Pull	15kΩ	2-bits, up & down	7-bits, up & down
OD	Open drain	Schmitt / CMOS	Open-Drain	100kΩ down only	2-bits, down only	5-bits, down only LPMD
LV	Low voltage only camera interface	CMOS (level Shifter)	-	-	-	-

For each GPIO pin, the following controls can be changed individually if the function is available for this pad type:

- Output Enable Control: Normal I/O or tri-state
- Pull-up/down Control: Normal, pull up or pull
- Alternative Function Selection: Up to 4 special functions are available per pin.

If the following functions are available for this pad type, they can only be set for a whole pad group:

- High-Speed Mode (Enable/Disable)
- Schmitt Trigger (Enable/Disable)
- Low Power Mode (LPMD)
- Drive strength control down / up
- Slew rate control falling/rising

4.3 Pin Reset Status

After a reset, the pins can be in different modes. Most of them are tri-stated, pulled up, or pulled low. A few are driven low or high. Please check the table in chapter 4.4 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

4.4 List Functions

Below you find a list of all the Tegra pins which are available on the MXM3 module connector. It shows what alternative functions are available for each pin. The default function (marked in yellow) is the configuration used to ensure compatibility with the Apalis form factor. For most of the pins, the default function is the primary function, but for some, it is an alternative function of the T30. To be compatible with the Apalis module family, only use the pin in the highlighted default function or GPIO. The other functions are not guaranteed to be compatible with other Apalis modules.

The list also contains the Tegra GPIO name and the pin's state immediately after reset (power on or software reset).

Reset Status	Description
z:	Tristate
pd:	Pull Down
pu:	Pull Up
pd+pu:	Pulled Up and Pulled Down (due multiplexed pins)
0:	Drive Low
1:	Drive High

Function Short Forms	
UART:	Serial Ports (Universal Asynchronous Receiver/Transmitter)
VI:	Video Interface (Camera Interface)
SPDIF:	S/PDIF (Sony-Philips Digital Interface I/O)
SDIO:	Secure Card I/O (SD, MMC, CE-ATA, eMMC)
HSMM:	High Speed (SD, MMC, CE-ATA, eMMC)
SPI:	Serial Peripheral Interface Bus
GMI:	General Memory Interface
LCD:	The parallel display interface
TWC:	Three Wire Interface
OWR:	One Wire Interface
DAP:	Digital Audio Port (I2S)
PMFM:	Pulse Width Modulation

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res KΩ	Pad Ctrl Group
1	KB_ROW10	KBC-ROW10		SDMMC2.A-SCLK		GPIO-S.02	pd	ST	50	aocfg2
3	KB_ROW11	KBC-ROW11		SDMMC2.A-CMD		GPIO-S.03	pd	ST	50	aocfg2
5	KB_ROW12	KBC-ROW12		SDMMC2.A-DAT0		GPIO-S.04	pd	ST	50	aocfg2
7	KB_ROW13	KBC-ROW13		SDMMC2.A-DAT1		GPIO-S.05	pd	ST	50	aocfg2
11	KB_ROW14	KBC-ROW14		SDMMC2.A-DAT2		GPIO-S.06	pd	ST	50	aocfg2
13	KB_COL0	KBC-COL0		TRACE-DATA0		GPIO-Q.00	pu	ST	100	aocfg2
	OWR	OWR-IO	CEC-IO				z	OD	100	owrcfg
15	KB_ROW15	KBC-ROW15		SDMMC2.A-DAT3		GPIO-S.07	pd	ST	50	aocfg2
17	KB_COL1	KBC-COL1		TRACE-DATA1		GPIO-Q.01	pu	ST	100	aocfg2
25	SATA_L0_RXP	SATA_L0_RXP								
27	SATA_L0_RXN	SATA_L0_RXN								
31	SATA_L0_TXN	SATA_L0_TXN								
33	SATA_L0_TXP	SATA_L0_TXP								
35	PEX_L0_PRSNT_N	PEX0-PRSNT_N	HDA.C-SYNC			GPIO-DD.00	z	ST	100	gpvcfg
37	GPIO_PV1					GPIO-V.01	z	ST	100	uabcfg
41	PEX_L4_RXN	PEX_L4_RXN								

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res KΩ	Pad Ctrl Group
43	PEX_L4_RXP	PEX_L4_RXP								
47	PEX_L4_TXN	PEX_L4_TXN								
49	PEX_L4_TXP	PEX_L4_TXP								
53	PEX_CLK2N	PEX_CLK2N								
55	PEX_CLK2P	PEX_CLK2P								
59	PEX_CLK1N	PEX_CLK1N								
61	PEX_CLK1P	PEX_CLK1P								
63	GMI_OE_N		NAND-RE_N	GMI-OE_N		GPIO-I.01	1	ST	100 [1)]	atcfg2
65	PEX_L0_RXN	PEX_L0_RXN								
67	PEX_L0_RXP	PEX_L0_RXP								
71	PEX_L0_TXN	PEX_L0_TXN								
73	PEX_L0_TXP	PEX_L0_TXP								
77	PEX_L1_RXN	PEX_L1_RXN								
79	PEX_L1_RXP	PEX_L1_RXP								
83	PEX_L1_TXN	PEX_L1_TXN								
85	PEX_L1_TXP	PEX_L1_TXP								
87	KB_COL7	KBC-COL7		TRACE-DATA7		GPIO-Q.07	pu	ST	100	aocfg2
89	PEX_L2_RXN	PEX_L2_RXN								
91	PEX_L2_RXP	PEX_L2_RXP								
95	PEX_L2_TXN	PEX_L2_TXN								
97	PEX_L2_TXP	PEX_L2_TXP								
99	KB_COL5	KBC-COL5		TRACE-DATA5		GPIO-Q.05	pu	ST	100	aocfg2
	VI_D11			VI-D11			pd	LV	15	vicfg1
101	PEX_L3_RXN	PEX_L3_RXN								
103	PEX_L3_RXP	PEX_L3_RXP								
107	PEX_L3_TXN	PEX_L3_TXN								
109	PEX_L3_TXP	PEX_L3_TXP								
113	DSI_D2AN	DSI_D2AN								
115	DSI_D2AP	DSI_D2AP								
119	DSI_D1AN	DSI_D1AN								
121	DSI_D1AP	DSI_D1AP								
123	KB_COL6	KBC-COL6		TRACE-DATA6		GPIO-Q.06	pu	ST	100	aocfg2
	VI_D10			VI-D10			pd	LV	15	vicfg1
125	DSI_CLKAN	DSI_CLKAN								
127	DSI_CLKAP	DSI_CLKAP								
131	CSI_CLKBN	CSI_CLKBN								
133	CSI_CLKBP	CSI_CLKBP								
135	KB_ROW8	KBC-ROW8		SDMMC2.A-DAT6		GPIO-S.00	pd	ST	50	aocfg2
	VI_D0			VI-D0			pd	LV	15	vicfg1
137	CSI_D2BN	CSI_D2BN								
139	CSI_D2BP	CSI_D2BP								
143	CSI_D1BN	CSI_D1BN								
145	CSI_D1BP	CSI_D1BP								
149	CSI_D2AN	CSI_D2AN								
151	CSI_D2AP	CSI_D2AP								
155	CSI_D1AN	CSI_D1AN								
157	CSI_D1AP	CSI_D1AP								
159	KB_ROW9	KBC-ROW9		SDMMC2.A-DAT7		GPIO-S.01	pd	ST	50	aocfg2
	VI_D1			VI-D1			pd	LV	15	vicfg1
161	CSI_CLKAN	CSI_CLKAN								
163	CSI_CLKAP	CSI_CLKAP								
173	KB_ROW7	KBC-ROW7		SDMMC2.A-DAT5		GPIO-R.07	pd	ST	50	aocfg1
	VI_D9			VI-D9			pd	LV	15	vicfg1
175	KB_ROW6	KBC-ROW6		SDMMC2.A-DAT4		GPIO-R.06	pd	ST	50	aocfg1
	VI_D8			VI-D8			pd	LV	15	vicfg1
177	KB_ROW5	KBC-ROW5		TRACE-CTL	OWR-PCTLZ	GPIO-R.05	pd	ST	100	aocfg1
	VI_D7			VI-D7			pd	LV	15	vicfg1
179	KB_ROW4	KBC-ROW4		TRACE-CLK		GPIO-R.04	pd	ST	100	aocfg1
	VI_D6			VI-D6			pd	LV	15	vicfg1
181	KB_ROW3	KBC-ROW3				GPIO-R.03	pd	ST	100	aocfg1
	VI_D5			VI-D5			pd	LV	15	vicfg1
183	KB_ROW2	KBC-ROW2				GPIO-R.02	pd	ST	100	aocfg1
	VI_D4			VI-D4			pd	LV	15	vicfg1

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res KΩ	Pad Ctrl Group
185	KB_ROW1	KBC-ROW1				GPIO-R.01	pd	ST	100	aocfg1
	VI_D3			VI-D3			pd	LV	15	vicfg1
187	KB_ROW0	KBC-ROW0				GPIO-R.00	pd	ST	100	aocfg1
	VI_D2			VI-D2			pd	LV	15	vicfg1
191	KB_COL2	KBC-COL2		TRACE-DATA2		GPIO-Q.02	pu	ST	100	aocfg2
	VI_PCLK			VI-CLK			pd	LV	15	vicfg1
193	CAM_MCLK			CLK-VI_MCLK	SDMMC4.B-SCLK	GPIO-CC.00	pu	ST	50	gmgcfg
195	KB_COL3	KBC-COL3		TRACE-DATA3		GPIO-Q.03	pu	ST	100	aocfg2
	VI_VSYNC			VI-VSYNC			pd	LV	15	vicfg1
197	KB_COL4	KBC-COL4		TRACE-DATA4		GPIO-Q.04	pu	ST	100	aocfg2
	VI_HSYNC			VI-HSYNC			pd	LV	15	vicfg1
201	CAM_I2C_SDA		I2C3.A-DAT		SDMMC4.B-DAT2	GPIO-BB.02	z	DD	50	gmecfg
203	CAM_I2C_SCL		I2C3.A-CLK		SDMMC4.B-DAT1	GPIO-BB.01	z	DD	50	gmecfg
205	DDC_SDA	I2C4-DAT				GPIO-V.05	z	OD	100	ddccfg
207	DDC_SCL	I2C4-CLK				GPIO-V.04	z	OD	100	ddccfg
209	GEN1_I2C_SDA	I2C1-DAT				GPIO-C.05	z	DD	50	dbgcfg
211	GEN1_I2C_SCL	I2C1-CLK				GPIO-C.04	z	DD	50	dbgcfg
215	SPDIF_OUT	SPDIF1.A-OUT			SDMMC2.C-DAT2	GPIO-K.05	pu	ST	50	dap1cfg
217	SPDIF_IN	SPDIF1.A-IN	HDA.B-RESET		SDMMC2.C-DAT3	GPIO-K.06	pu	ST	50	dap1cfg
221	SPI1_SCK	SPI2.E-SCK	SPI1.B-SCK		GMI-A26	GPIO-X.05	pu	ST	100	spicfg
223	SPI1_MISO		SPI1.B-MISO			GPIO-X.07	pd	ST	100	spicfg
225	SPI1_MOSI	SPI2.E-MOSI	SPI1.B-MOSI		GMI-A25	GPIO-X.04	pu	ST	100	spicfg
227	SPI1_CS0_N	SPI2.E-CS1_N	SPI1.B-CS0_N		GMI-A27	GPIO-X.06	pu	ST	100	spicfg
229	LCD_SDIN	LCD0-SDI	LCD1-SDI	SPI5.A-MISO		GPIO-Z.02	pu	ST	100	lcdcfg1
231	LCD_SDOUT	LCD0-SDA	LCD1-SDA	SPI5.A-MOSI		GPIO-N.05	pu	ST	100	lcdcfg1
233	LCD_CS0_N	LCD0-CS_N	LCD1-CS_N	SPI5.A-CS2_N		GPIO-N.04	pu	ST	100	lcdcfg1
235	LCD_SCK	LCD0-SCK	LCD1-SCK	SPI5.A-SCK		GPIO-Z.04	pu	ST	100	lcdcfg1
239	UART3_RTS_N [4]	UART3-RTS_N	PWFM-PWM0 [3]	GMI-A4		GPIO-C.00	pu	ST	100	uart3cfg
243	LCD_PCLK	LCD0.A-PCLK	LCD1.A-PCLK			GPIO-B.03	pd	ST	100	lcdcfg2
245	LCD_VSYNC	LCD0.A-VSYNC	LCD1.A-VSYNC			GPIO-J.04	pu	ST	100	lcdcfg2
247	LCD_HSYNC	LCD0.A-HSYNC	LCD1.A-HSYNC			GPIO-J.03	pu	ST	100	lcdcfg2
249	LCD_DE	LCD0.A-DE	LCD1.A-DE			GPIO-J.01	pd	ST	100	lcdcfg2
251	LCD_D22	LCD0-DI	LCD1-DI			GPIO-M.06	pd	ST	100	lcdcfg2
253	LCD_D23	LCD0-PP	LCD1-PP			GPIO-M.07	pd	ST	100	lcdcfg2
255	LCD_D12	LCD0-D12	LCD1-D12			GPIO-F.04	pd	ST	100	lcdcfg2
257	LCD_D13	LCD0-D13	LCD1-D13			GPIO-F.05	pd	ST	100	lcdcfg2
259	LCD_D14	LCD0-D14	LCD1-D14			GPIO-F.06	pd	ST	100	lcdcfg2
261	LCD_D15	LCD0-D15	LCD1-D15			GPIO-F.07	pd	ST	100	lcdcfg2
263	LCD_D16	LCD0-D16	LCD1-D16			GPIO-M.00	pd	ST	100	lcdcfg2
265	LCD_D17	LCD0-D17	LCD1-D17			GPIO-M.01	pd	ST	100	lcdcfg2
269	LCD_D20	LCD0-VP1	LCD1-VP1			GPIO-M.04	pd	ST	100	lcdcfg2
271	LCD_D21	LCD0-HP0	LCD1-HP0			GPIO-M.05	pd	ST	100	lcdcfg2
273	LCD_D6	LCD0-D6	LCD1-D6			GPIO-E.06	pd	ST	100	lcdcfg2
275	LCD_D7	LCD0-D7	LCD1-D7			GPIO-E.07	pd	ST	100	lcdcfg2
277	LCD_D8	LCD0-D8	LCD1-D8			GPIO-F.00	pd	ST	100	lcdcfg2
279	LCD_D9	LCD0-D9	LCD1-D9			GPIO-F.01	pd	ST	100	lcdcfg2
281	LCD_D10	LCD0-D10	LCD1-D10			GPIO-F.02	pd	ST	100	lcdcfg2
283	LCD_D11	LCD0-D11	LCD1-D11			GPIO-F.03	pd	ST	100	lcdcfg2
287	LCD_D18	LCD0-HP1	LCD1-HP1			GPIO-M.02	pd	ST	100	lcdcfg2
289	LCD_D19	LCD0-HP2	LCD1-HP2			GPIO-M.03	pd	ST	100	lcdcfg2
291	LCD_D0	LCD0-D0	LCD1-D0			GPIO-E.00	pd	ST	100	lcdcfg2
293	LCD_D1	LCD0-D1	LCD1-D1			GPIO-E.01	pd	ST	100	lcdcfg2
295	LCD_D2	LCD0-D2	LCD1-D2			GPIO-E.02	pd	ST	100	lcdcfg2
297	LCD_D3	LCD0-D3	LCD1-D3			GPIO-E.03	pd	ST	100	lcdcfg2
299	LCD_D4	LCD0-D4	LCD1-D4			GPIO-E.04	pd	ST	100	lcdcfg2
301	LCD_D5	LCD0-D5	LCD1-D5			GPIO-E.05	pd	ST	100	lcdcfg2
2	GPIO_PU6	PWFM-PWM3	UART1.B-DSR_N	GMI-A12		GPIO-U.06	z	ST	100	dbgcfg
4	GPIO_PU5	PWFM-PWM2	UART1.B-RI_N	GMI-A11		GPIO-U.05	z	ST	100	dbgcfg
6	GPIO_PU4	PWFM-PWM1	UART1.B-DTR_N	GMI-A10		GPIO-U.04	z	ST	100	dbgcfg
8	GPIO_PU3	PWFM-PWM0 [3]	UART1.B-RTS_N	GMI-A9		GPIO-U.03	z	ST	100	dbgcfg
26	GMI_RST_N	NAND-BSY3	NAND-CLE	GMI-RST_N [2]		GPIO-I.04	0	ST	100 [2]	atcfg2
60	USB1_VBUS	USB1_VBUS								

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res KΩ	Pad Ctrl Group
72	ACC1_DETECT	ACC1_DETECT								
74	USB1_DP	USB1_DP								
76	USB1_DN	USB1_DN								
80	USB2_DP	USB2_DP								
82	USB2_DN	USB2_DN								
84	PEX_L0_RST_N	PEX0-RST_N	HDA.C-SDI			GPIO-DD.01	z	ST	100	gpvcfg
86	USB3_DP	USB3_DP								
88	USB3_DN	USB3_DN								
96	PEX_L0_CLKREQ_N	PEXCLK0-CLKREQ_N	HDA.C-SDO			GPIO-DD.02	z	ST	100	gpvcfg
110	ULPI_DATA7	SPI2.A-CS1_N		UART1.A-DTR_N	ULPI-DATA7	GPIO-O.00	pu	ST	100	uabcfg
112	ULPI_DATA0	SPI3.E-MOSI		UART1.A-TXD	ULPI-DATA0	GPIO-O.01	pu	ST	100	uaacfg
114	ULPI_DATA3	SPI3.E-CS1_N		UART1.A-RTS_N	ULPI-DATA3	GPIO-O.04	pu	ST	100	uaacfg
116	ULPI_DATA2	SPI3.E-SCK		UART1.A-CTS_N	ULPI-DATA2	GPIO-O.03	pu	ST	100	uaacfg
118	ULPI_DATA1	SPI3.E-MISO		UART1.A-RXD	ULPI-DATA1	GPIO-O.02	pu	ST	100	uaacfg
120	ULPI_DATA6	SPI2.A-SCK		UART1.A-DSR_N	ULPI-DATA6	GPIO-O.07	pu	ST	100	uabcfg
122	ULPI_DATA4	SPI2.A-MOSI		UART1.A-RI_N	ULPI-DATA4	GPIO-O.05	pu	ST	100	uabcfg
124	ULPI_DATA5	SPI2.A-MISO		UART1.A-DCD_N	ULPI-DATA5	GPIO-O.06	pu	ST	100	uabcfg
126	ULPI_CLK	SPI1.A-MOSI		UART4.A-TXD	ULPI-CLOCK	GPIO-Y.00	z	ST	100	udacfg
128	ULPI_STP	SPI1.A-CS0_N		UART4.A-RTS_N	ULPI-STP	GPIO-Y.03	z	ST	100	udacfg
130	ULPI_NXT	SPI1.A-SCK		UART4.A-CTS_N	ULPI-NXT	GPIO-Y.02	z	ST	100	udacfg
132	ULPI_DIR	SPI1.A-MISO		UART4.A-RXD	ULPI-DIR	GPIO-Y.01	z	ST	100	udacfg
134	UART2_TXD	UART2-TXD	SPDIF1.C-IN	UART1.C-RTS_N	SPI4.B-SCK	GPIO-C.02	pu	ST	100	uart2cfg
136	UART2_RXD	UART2-RXD	SPDIF1.C-OUT	UART1.C-CTS_N	SPI4.B-MOSI	GPIO-C.03	pu	ST	100	uart2cfg
138	UART3_TXD	UART3-TXD		GMI-A2		GPIO-W.06	pu	ST	100	uart3cfg
140	UART3_RXD	UART3-RXD		GMI-A3		GPIO-W.07	pu	ST	100	uart3cfg
144	SDMMC3_DAT2		PWFM-PWM1	SDMMC3-DAT2		GPIO-B.05	pu	CZ	15	sdio3cfg
146	SDMMC3_DAT3		PWFM-PWM0	SDMMC3-DAT3		GPIO-B.04	pu	CZ	15	sdio3cfg
148	SDMMC3_DAT4	PWFM-PWM1		SDMMC3-DAT4		GPIO-D.01	pu	CZ	15	sdio2cfg
150	SDMMC3_CMD	UART1.E-RXD	PWFM-PWM3	SDMMC3-CMD		GPIO-A.07	pu	CZ	15	sdio3cfg
152	SDMMC3_DAT5	PWFM-PWM0		SDMMC3-DAT5		GPIO-D.00	pu	CZ	15	sdio2cfg
154	SDMMC3_CLK	UART1.E-TXD	PWFM-PWM2	SDMMC3-SCLK		GPIO-A.06	pu	CZ	15	sdio3cfg
156	SDMMC3_DAT6	SPDIF1.B-IN		SDMMC3-DAT6		GPIO-D.03	pu	CZ	15	sdio2cfg
158	SDMMC3_DAT7	SPDIF1.B-OUT		SDMMC3-DAT7		GPIO-D.04	pu	CZ	15	sdio2cfg
160	SDMMC3_DAT0			SDMMC3-DAT0		GPIO-B.07	pu	CZ	15	sdio3cfg
162	SDMMC3_DAT1			SDMMC3-DAT1		GPIO-B.06	pu	CZ	15	sdio3cfg
164	GPIO_PV3					GPIO-V.03	z	ST	100	uabcfg
176	SDMMC1_DAT2	SDMMC1-DAT2		UART5.A-RXD		GPIO-Y.05	pu	CZ	15	sdio1cfg
178	SDMMC1_DAT3	SDMMC1-DAT3		UART5.A-TXD		GPIO-Y.04	pu	CZ	15	sdio1cfg
180	SDMMC1_CMD	SDMMC1-CMD				GPIO-Z.01	pu	CZ	15	sdio1cfg
184	SDMMC1_CLK	SDMMC1-SCLK				GPIO-Z.00	pu	CZ	15	sdio1cfg
186	SDMMC1_DAT0	SDMMC1-DAT0		UART5.A-RTS_N		GPIO-Y.07	pu	CZ	15	sdio1cfg
188	SDMMC1_DAT1	SDMMC1-DAT1		UART5.A-CTS_N		GPIO-Y.06	pu	CZ	15	sdio1cfg
190	CLK2_REQ	CLK-DAP_MCLK2_REQ				GPIO-CC.05	z	ST	100	cdev2cfg
194	CLK2_OUT	CLK-EXTCLK2				GPIO-W.05	pd	ST	100	cdev2cfg
196	DAP1_DOUT	I2S0-SDATA_OUT	HDA.A-SDO	GMI-D30	SDMMC2.C-DAT1	GPIO-N.02	pd	ST	50	dap1cfg
198	CLK1_REQ	CLK-DAP_MCLK1_REQ	HDA.A-RESET			GPIO-EE.02	z	ST	100	cdev1cfg
200	DAP1_SCLK	I2S0-SCLK	HDA.A-BCLK	GMI-D31	SDMMC2.C-SCLK	GPIO-N.03	pd	ST	50	dap1cfg
202	DAP1_DIN	I2S0-SDATA_IN	HDA.A-SDI	GMI-D29	SDMMC2.C-DAT0	GPIO-N.01	pd	ST	50	dap1cfg
204	DAP1_FS	I2S0-LRCK	HDA.A-SYNC	GMI-D28	SDMMC2.C-CMD	GPIO-N.00	pd	ST	50	dap1cfg
208	VDAC_R	VDAC_R								
210	VDAC_G	VDAC_G								
212	VDAC_B	VDAC_B								
214	CRT_HSYNC	TVO-HSYNC				GPIO-V.06	pu	ST	100	crtcfg
216	CRT_VSYNC	TVO-VSYNC				GPIO-V.07	pu	ST	100	crtcfg
220	HDMI_CEC	CEC-IO				GPIO-EE.03	z	DD	50	ceccfg
222	HDMI_TXD2P	HDMI_TXD2P								
224	HDMI_TXD2N	HDMI_TXD2N								
228	HDMI_TXD1P	HDMI_TXD1P								
230	HDMI_TXD1N	HDMI_TXD1N								
232	HDMI_INT					GPIO-N.07	z	OD	100	lcdcfg2
234	HDMI_TXD0P	HDMI_TXD0P								

X1 Pin	Tegra Pin Name	Primary Function	Alt 1	Alt 2	Alt 3	GPIO	Reset state	Pad Type	Pull Res KΩ	Pad Ctrl Group
236	HDMI_TXD0N	HDMI_TXD0N								
240	HDMI_TXCP	HDMI_TXCP								
242	HDMI_TXCN	HDMI_TXCN								
262	GEN2_I2C_SDA	I2C2-DAT		GMI-CS7_N		GPIO-T.06	z	DD	50	atcfg5
274	GEN2_I2C_SCL	I2C2-CLK		GMI-CS6_N		GPIO-T.05	z	DD	50	atcfg5
286	GPIO_PV2	OWR-PCTLZ				GPIO-V.02	z	ST	100	uabcfg

1) This pin features an additional external pull up resistor (94kOhm) on the module. For more information about this pin, see also the chapter "Recovery Mode."
2) This pin works as a reset output for the carrier board. The pin is driven low during the reset of the Tegra. Afterward, it goes high (see section 5.1.3). The pin features an additional external pull up resistor (10kOhm) on the module.
3) The Tegra T30 UART3_RTS_N (Pin 239) and GPIO_PU3 (Pin 8) use the same PWM source (PWFM_PWM0). Only one or the other can be used at the same time.
4) The MXM3 pin 239 is connected additionally to GPIO3 output of the power management IC TPS65911 over a tri-state buffer. The buffer state is controlled over the UART3_CTS_N signal of the T30 (Figure 6 and section 4.1)

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
10, 30, 36, 52, 58, 66, 78, 90, 102, 108	VCC	I	3.3V main power supply	If possible, use decoupling capacitors on all pins.
9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298	GND	I	Digital Ground	
174	VCC_BACKUP	I/O	RTC Power supply can be connected to a backup battery.	It can be left unconnected if the internal RTC is not used.

5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
314, 320	AVCC	I	3.3V Analogue supply	Connect this pin to a 3.3V supply. For better Audio accuracy, we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec.
303, 313, 304, 308	AGND	I	Analogue Ground	Connect this pin to GND. For better Audio accuracy, we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Apalis T30.

5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
28	RESET_MICO#	I	Reset Input	This pin is low active and resets the Apalis module. This pin is connected to the power management IC.
26	RESET_MOCI#	O	Reset Output	This pin is active low. This pin is driven low at boot up. There is a 10k Ohm pullup on this pin.
24	POWER_ENABLE_MOCI	O	Signal for the carrier board to enable the peripheral voltage rails	More information about the required power management on the carrier board can be found in the Apalis Carrier Board Design Guide

On the Apalis T30, the RESET_MICO# (pin 28) performs a cold reset of the module. This means that all the SoM power supplies are turned off when the reset is asserted. The Software initiated reset cycle, on the other hand, implements a module warm reset in which all the power rails are kept on.

The GMI_RST_N pin of the SoC is used as RESET_MOCI#. During the power-up sequence, this pin is driven low. After the power-up sequence has been completed (around 6ms after the main power rail has applied to the module), the pin is released. This release is not software controlled and cannot be adjusted. Since the PCIe specification requires a longer reset time, the standard Toradex BSP executes another reset for around 100ms during the boot sequence. This happens around 5s after the main power rail is applied to the module and is fully controlled by software.

5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. All GPIO pins can be used as an interrupt source.

5.2.1 Wakeup Source

Certain pins can be used to wake up the Apalis module from a suspended state. There is on-chip de-glitch logic, which can be de-activated if required. A signal pulse of at least 46µs is required to wake up the system. It is possible to configure the wake-up level.
In the Apalis module standard, pin 37 is the default wakeup source. Only this pin is guaranteed to be wakeup compatible with other Apalis modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Apalis modules.

Table 5-4 Wakeup Pins

X1 Pin#	Wakeup Source	Remarks
1	WAKE9	
2	WAKE7	
4	WAKE6	
5	WAKE25	
7	WAKE26	
11	WAKE28	
15	WAKE29	
37	WAKE1	Default Apalis wake-up source
60	WAKE19	
72	WAKE21	
114	WAKE32	
122	WAKE0	
135	WAKE27	
162	WAKE3	
185	WAKE2	
188	WAKE13	
196	WAKE30	
203	WAKE36	
232	WAKE4	
	WAKE24	Touch pen down interrupt signal of STMPE811
	WAKE14	Wake signal of Ethernet controller I210-AT

The touch pen down interrupt signal of the touch controller is connected to the WAKE24 source and can also wake up the system. The wake signal of the Ethernet controller is connected to the WAKE14 source.

5.3 Ethernet

The Apalis Module features a 10/100/1000 Mbit Ethernet interface. The MAC/PHY is integrated into the module. Therefore only the magnetics are required on the carrier board. The Intel I210-AT Gigabit Ethernet Controller chip is connected over PCIe lane 5 to the Tegra T30

Table 5-5 Ethernet Pins

X1 Pin #	Apalis Signal Name	I210-AT Signal Name	I/O	Description	Remarks
50	ETH1_MDI0+	MDI_0_P	I/O	Media Dependent Interface	100BASE-TX: Transmit +
48	ETH1_MDI0-	MDI_0_N	I/O	Media Dependent Interface	100BASE-TX: Transmit -
56	ETH1_MDI1+	MDI_1_P	I/O	Media Dependent Interface	100BASE-TX: Receive +
54	ETH1_MDI1-	MDI_1_N	I/O	Media Dependent Interface	100BASE-TX: Receive -
32	ETH1_MDI2+	MDI_2_P	I/O	Media Dependent Interface	100BASE-TX: Unused
34	ETH1_MDI2-	MDI_2_N	I/O	Media Dependent Interface	100BASE-TX: Unused
38	ETH1_MDI3+	MDI_3_P	I/O	Media Dependent Interface	100BASE-TX: Unused
40	ETH1_MDI3-	MDI_3_N	I/O	Media Dependent Interface	100BASE-TX: Unused
46	ETH+_CTREF	NC	O	Center tap supply	I210 does not need a center tap supply
42	ETH1_ACT	LED1	O	LED indication output	The mode can be configured individually
44	ETH1_LINK	LED2	O	LED indication output	The mode can be configured individually

The Intel I210-AT does not require a central tap supply on the magnetics. Nevertheless, follow the Apalis Carrier Board Design Guide and connect the magnetics center tap to pin 46 of the Apalis module. This guarantees the full compatibility to Apalis modules, which require a center tap supply.

If only fast Ethernet is required, 10/100Mbit magnetics with only 2 lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

5.4 USB

The Apalis module form factor features up to four USB interfaces, two USB 3.0 SuperSpeed (backward compatible), and two USB 2.0 High-Speed interfaces. The NVIDIA Tegra T30 features only three USB 2.0 High Speed (480 Mbit) interfaces. Therefore, the Apalis T30 module does not provide any signals on the USBH4 interface. All three USB interfaces can be configured as host or client.

Since the necessary control signals are only available for the USBO1 interface, only this one is OTG compatible. USBO1 can also be used for the USB recovery mode. See section 6, "Recovery Mode" for more information. If the USB recovery mode is used, the USBO1_VBUS (pin 60) needs to be connected to a 5V rail. This can be either a 5V rail of the carrier board or sourced over the USB cable from the host device. Suitable circuits can be found in the Apalis Carrier Board Design Guide or the evaluation board schematics.

5.4.1 USB Data Signal

Table 5-6 USBO1 Data Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
74	USBO1_D+	USB1_DP	I/O	Positive Differential USB Signal, OTG capable
76	USBO1_D-	USB1_DN	I/O	Negative Differential USB Signal, OTG capable
62	USBO1_SSRX+	NC	I	Not connected
64	USBO1_SSRX-	NC	I	Not connected
68	USBO1_SSTX+	NC	O	Not connected
70	USBO1_SSTX-	NC	O	Not connected

Table 5-7 USBH2 Data Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
80	USBH2_D+	USB2_DP	I/O	Positive Differential USB Signal, Host and Client capable
82	USBH2_D-	USB2_DN	I/O	Negative Differential USB Signal, Host and Client capable

Table 5-8 USBH3 Data Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
86	USBH3_D+	USB3_DP	I/O	Positive Differential USB Signal, Host and Client capable
88	USBH3_D-	USB3_DN	I/O	Negative Differential USB Signal, Host and Client capable

Table 5-9 USBH4 Data Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
98	USBH4_D+	NC	I/O	Not connected
100	USBH4_D-	NC	I/O	Not connected
94	USBH4_SSRX+	NC	I	Not connected
92	USBH4_SSRX-	NC	I	Not connected
106	USBH4_SSTX+	NC	O	Not connected
104	USBH4_SSTX-	NC	O	Not connected

5.4.2 USB Control Signals

Table 5-10 USB OTG Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
72	USBO1_ID	ACC1_DETECT	I	Use this pin to detect the ID pin if you use USB OTG
60	USBO1_VBUS	USB1_VBUS	I	Use this pin to detect if VBUS is present (5V USB supply). This pin is 5V tolerant and can be connected directly to the USB supply.

If you use the USB Host function, you need to provide the 5V USB supply voltage on your carrier board for the interfaces. The Apalis T30 provides additional signals for controlling the USB supply. We recommend using the following pins to guarantee the best possible compatibility. However, if required, you can use other GPIOs or not use the signals at all. The USBH2 and USBH3 interfaces share the bus power control signals, whereas USBO1 has its dedicated control signals.

Table 5-11 USB Power Control Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
274	USBO1_EN	GEN2_I2C_SCL	O	This pin enables the external USB voltage supply for the USBO1 interface
262	USBO1_OC#	GEN2_I2C_SDA	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBO1 interface
84	USBH_EN	PEX_L0_RST_N	O	This pin enables the external USB voltage supply for the USBH2 and USBH3 interfaces
96	USBH_OC#	PEX_L0_CLKREQ_N	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBH2 and USBH3 interfaces

5.5 Display

The Apalis T30 has two independent display controllers. Each of the two display controllers shares access to the various output ports. There is only one instance of the parallel LCD (shared with the LVDS interface), HDMI, and up to two DSI outputs. Only one display controller can access one of these outputs at any given time. If you are using a smart display (displays with an internal frame-buffer), it is possible to use both display controllers on the parallel display interface.

Features for each display controller include:
- Three display windows (primary frame-buffer and 2 overlays)
- Hardware surface blending
- Hardware cursor
- Fully programmable display timing and resolution

5.5.1 Parallel RGB LCD interface

The Apalis T30 provides a parallel LCD interface on the MXM3 connector. It supports up to 24-bit colors per pixel. The 24bit color mapping is guaranteed to be compatible with other Apalis modules. R7, G7, and B7 are the most significant bits (MSBs). R0, G0, and B0 are the least significant bits (LSBs) for the respective colors. To ensure compatibility between modules, the display interface should always be used in 24-bit mode. To use displays that require fewer bits (e.g., 18 or 16-bit displays), do not connect the bottom n LSBs for each color, where n is the number of signals not required for a specific color. For instance, to connect an 18-bit display, R0, R1, G0, G1 B0, and B1 remain unused. R2, G2, and B2 become the LSBs for this configuration.

It is also possible to use this interface for a smart display. If you use 18bit or less, you can use the other bits for a smart display. However, only a few special cases make sense to use such a smart display.

Since the LVDS interface uses the same parallel RGB signals, only the LVDS or the parallel RGB interface can be used at any one time.

Features
- Up to QXGA (2048x1536) resolution
- Up to 24-bit color
- Supports parallel TTL displays and smart displays
- Max pixel clock 165MHz

The following list details the most common color configurations.

Table 5-12 Colour Configuration

X1 Pin#	Apalis Signal Name	T30 Signal Name	THC63LVD827 Signal Name	24 bit RGB	18 bit RGB	16 bit RGB
251	LCD1_R0	LCD_D22	R10	R0		
253	LCD1_R1	LCD_D23	R11	R1		
255	LCD1_R2	LCD_D12	R12	R2	R0	
257	LCD1_R3	LCD_D13	R13	R3	R1	R0
259	LCD1_R4	LCD_D14	R14	R4	R2	R1
261	LCD1_R5	LCD_D15	R15	R5	R3	R2
263	LCD1_R6	LCD_D16	R16	R6	R4	R3
265	LCD1_R7	LCD_D17	R17	R7	R5	R4
269	LCD1_G0	LCD_D20	G10	G0		
271	LCD1_G1	LCD_D21	G11	G1		
273	LCD1_G2	LCD_D6	G12	G2	G0	G0
275	LCD1_G3	LCD_D7	G13	G3	G1	G1
277	LCD1_G4	LCD_D8	G14	G4	G2	G2
279	LCD1_G5	LCD_D9	G15	G5	G3	G3
281	LCD1_G6	LCD_D10	G16	G6	G4	G4
283	LCD1_G7	LCD_D11	G17	G7	G5	G5
287	LCD1_B0	LCD_D18	B10	B0		
289	LCD1_B1	LCD_D19	B11	B1		
291	LCD1_B2	LCD_D0	B12	B2	B0	
293	LCD1_B3	LCD_D1	B13	B3	B1	B0
295	LCD1_B4	LCD_D2	B14	B4	B2	B1
297	LCD1_B5	LCD_D3	B15	B5	B3	B2
299	LCD1_B6	LCD_D4	B16	B6	B4	B3
301	LCD1_B7	LCD_D5	B17	B7	B5	B4

Table 5-13 Additional Display Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
249	LCD1_DE	LCD_DE	O	Data Enable (other names: Output Enable) For Passive Displays, you can use this pin as Bias/Modulation pin
243	LCD1_PCLK	LCD_PCLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)
247	LCD1_HSYNC	LCD_HSYNC	O	Horizontal Sync (other names: Line Clock, L_LCKL_A0)
245	LCD1_VSYNC	LCD_VSYNC	O	Vertical Sync (other names: Frame Clock, L_FCLK)
239	BKL1_PWM	UART3_RTSN	O	Backlight PWM (Shared with GPIO3 of power management IC, see Figure 6 in section 4.1)
286	BKL1_ON	GPIO_PV2	O	Enable signal for the backlight.
205	I2C2_SDA	DDC_SDA	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	DDC_SCL	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

5.5.2 LVDS

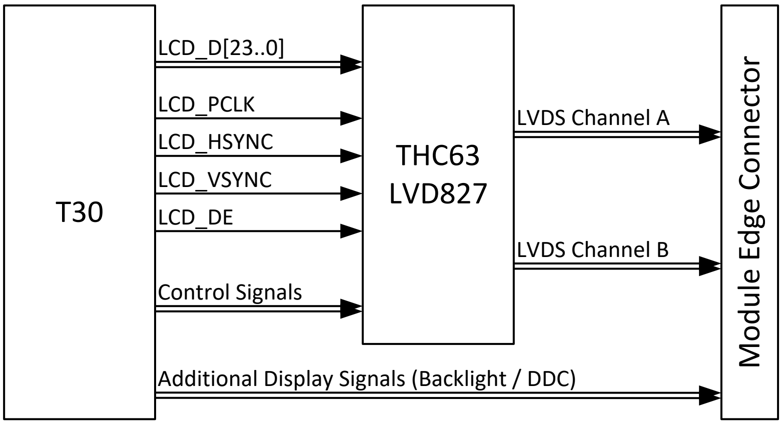

Figure 7: LVDS Block diagram

The LVDS interface (official name: FPD-Link/FlatLink) serializes the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to 7 parallel signals. For an 18-bit RGB interface, including the control signals (Display Enable, Vertical, and Horizontal Synch), each FPD_Link/FlatLink channel requires three LVDS data pairs. The additional color bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two color mapping standards for the 24-bit interface. The less common "24 bit / 18 bit compatible" (JEIDA format) standard packs the two low significant bits of each color into the fourth LVDS pair. This standard is backward compatible with the 18bit mode. It is possible to connect an 18-bit display to a 24-bit interface or vice versa. The more common 24-bit color mapping standard (VESA format) serializes each color's two most significant bits into the fourth LVDS pair. This mode is not backward compatible. Therefore, only 24bit displays can be connected to a 24-bit host with this color mapping. The LVDS interface of Apalis T30 is configurable to support different color mappings and depths. This ensures compatibility with 18bit and 24bit displays with both kinds of color mappings.

A single channel LVDS interface can provide resolutions up to 1280 x 1024 pixels (depending on available displays). For higher resolutions, a second LVDS channel is needed. The odd bits are transmitted in the first channel, and the even bits are transmitted in the second channel. The LVDS converter can transmit the parallel RGB signals into a single or dual-channel LVDS interface. Hence, a wide range of display resolutions is supported by the Apalis T30 LVDS interface.

Table 5-14 LVDS interface signals

X1 Pin#	Apalis Signal Name	THC63LVD827 Signal Name	I/O	Description
246	LVDS1_A_CLK-	TCLK1-	O	LVDS Clock out for channel A (odd pixels/single channel)
248	LVDS1_A_CLK+	TCLK1+	O	
252	LVDS1_A_TX0-	TA1-	O	LVDS data lane 0 for channel A (odd pixels/single channel)
254	LVDS1_A_TX0+	TA1+	O	
258	LVDS1_A_TX1-	TB1-	O	LVDS data lane 1 for channel A (odd pixels/single channel)
260	LVDS1_A_TX1+	TB1+	O	
264	LVDS1_A_TX2-	TC1-	O	LVDS data lane 2 for channel A (odd pixels/single channel)
266	LVDS1_A_TX2+	TC1+	O	
270	LVDS1_A_TX3-	TD1-	O	LVDS data lane 3 for channel A (odd pixels/single channel; unused for 18bit)
272	LVDS1_A_TX3+	TD1+	O	
276	LVDS1_B_CLK-	TCLK2-	O	LVDS Clock out for channel B (even pixels/unused for the single-channel)
278	LVDS1_B_CLK+	TCLK2+	O	

X1 Pin#	Apalis Signal Name	THC63LVD827 Signal Name	I/O	Description
282	LVDS1_B_TX0-	TA2-	O	LVDS data lane 0 for channel B (odd pixels/unused for the single-channel)
284	LVDS1_B_TX0+	TA2+	O	
288	LVDS1_B_TX1-	TB2-	O	LVDS data lane 1 for channel B (odd pixels/unused for the single-channel)
290	LVDS1_B_TX1+	TB2+	O	
294	LVDS1_B_TX2-	TC2-	O	LVDS data lane 2 for channel B (odd pixels/unused for the single-channel)
296	LVDS1_B_TX2+	TC2+	O	
300	LVDS1_B_TX3-	TD2-	O	LVDS data lane 3 for channel B (odd pixels/unused for single-channel; unused for 18-bit)
302	LVDS1_B_TX3+	TD2+	O	

Table 5-15 Additional Display Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
239	BKL1_PWM	UART3_RTSN	O	Backlight PWM (Shared with GPIO3 of power management IC, see Figure 6 in section 4.1)
286	BKL1_ON	GPIO_PV2	O	Enable signal for the backlight.
205	I2C2_SDA	DDC_SDA	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	DDC_SCL	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

Table 5-16 THC63LVD827 control signals

THC63LVD827 Signal Name	T30 Signal Name	Pull Resistor	Description
MODE	GPIO_PBB0	L	Single/Dual channel mode. H: Single channel LVDS out (Figure 9) L: Dual channel LVDS out (Figure 8)
MAP	GPIO_PBB7	L	Colour mapping H: 24 bit / 18 bit compatible (JEIDA format, Figure 10) L: Common 24-bit color mode (VESA format, Figure 11)
6B/8B#	GPIO_PBB3	L	18-bit / 24-bit mode select H: 18-bit (6 bit per colour) mode (Figure 12) L: 24-bit (8 bit per colour) mode
O/E	GPIO_PBB4	L	Output enable H: LVDS output enabled L: LVDS output disabled (all outputs are Hi-Z)
PDWN#	GPIO_PBB5	L	Power down H: Normal operation L: Power down, all outputs are Hi-Z, and all circuits are in stand-by mode with minimum current consumption.
RS	GPIO_PCC1	H	LVDS swing mode H: 350mV (standard LVDS value) L: 200mV (reduced swing reduces EMI and power consumption, suitable for short cables)
R/F#	GPIO_PBB6	H	Input clock triggering edge select H: Rising edge (the preferred setting for Apalis T30) L: Falling edge
DDR#	GPIO_PCC2	H	Double edge clock input H: DDR disabled (the preferred setting for Apalis T30) L: DDR enabled (RGB input is sampled on both edges of the pixel clock)

The THC63LVD827 features pull up and down resistors on the control signals. This guarantees a defined value for the signals during startup. The table contains the direction of the pull resistor.

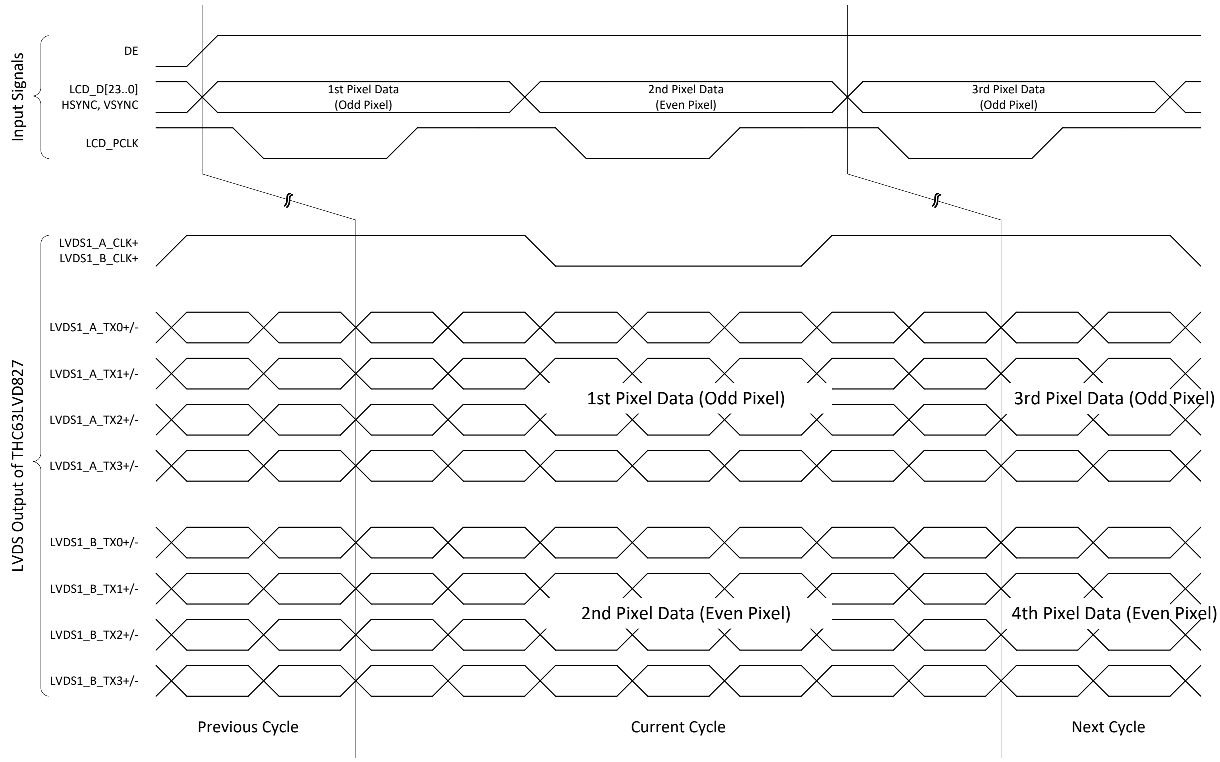

Figure 8: Dual Channel Mode (MODE = L)

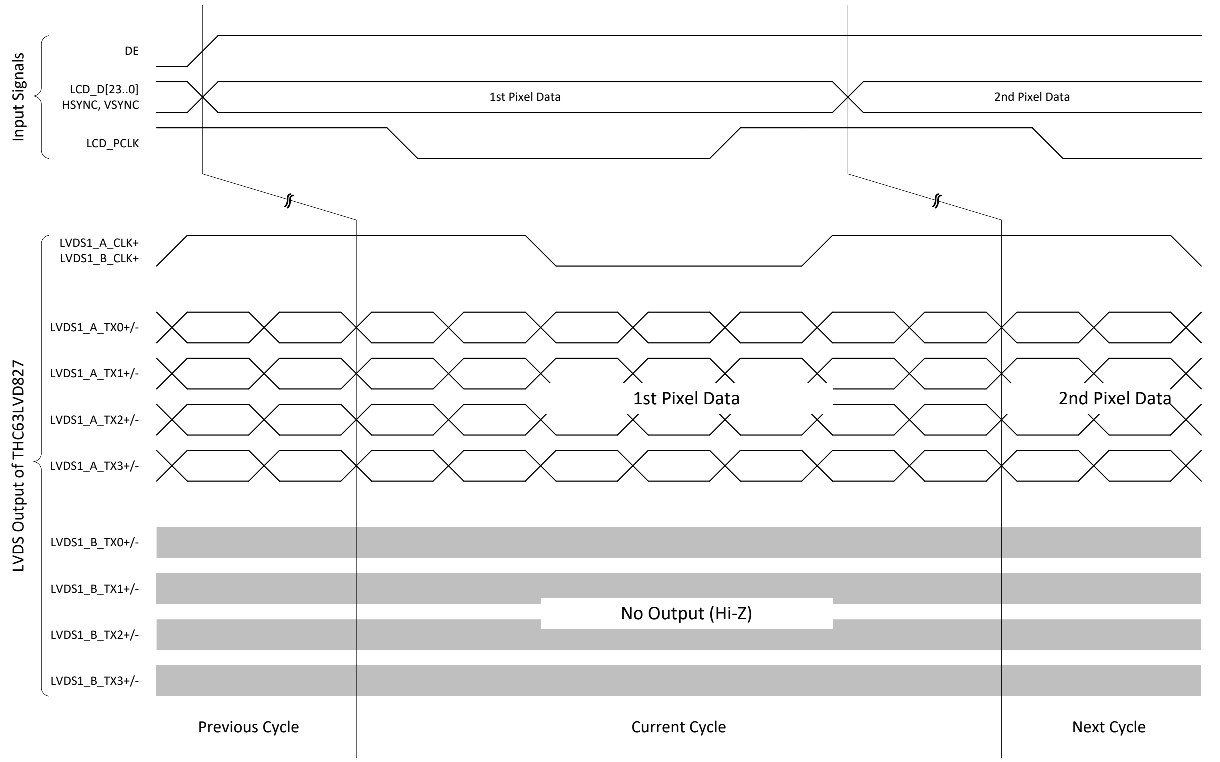

Figure 9: Single Channel Mode (MODE = H)

Figure 10 shows the LVDS output signals for the "24-bit /18-bit Compatible Color Mapping" (JEIDA format). The RGB bits' names correspond to the color names in the "**24-bit RGB**" column in Table 5-12. To enable this mode, the Tegra T30 needs to be configured in 24-bit RGB mode, and the LVDS converter control signal MAP needs to be set high, while the 6B/8B# signal needs to be low.

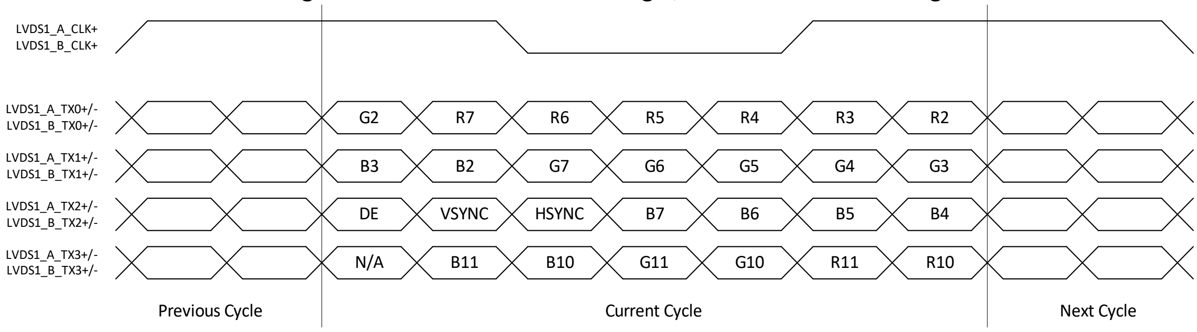

Figure 10: 24-bit / 18-bit Compatible Color Mapping (MAP = H; 6B/8B# = L)

Figure 11 shows the LVDS output signals for the common 24-bit color mapping (VESA format). The RGB bits' names correspond to the color names in the "**24-bit RGB**" column in Table 5-12. The Tegra T30 needs to be configured in 24-bit RGB mode, and the LVDS converter control signal MAP and 6B/8B# needs to be low to enable this mode.

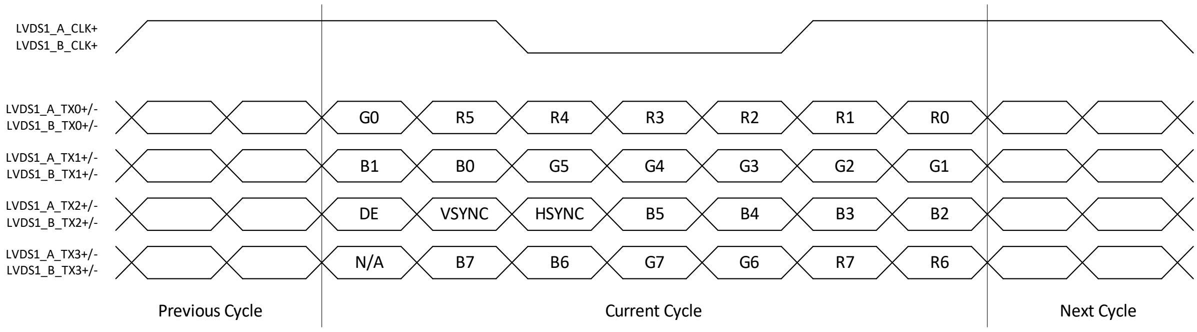

Figure 11: Common 24-bit VESA Color Mapping (MAP = L; 6B/8B# = L)

Figure 12 shows the LVDS output signals for the 18-bit interface. The RGB bits' names correspond to the color names in the "**18-bit RGB**" column in Table 5-12. To enable this mode, the Tegra T30 needs to be configured in either a 24 bit or 18-bit RGB mode, and the LVDS converter control signal MAP and 6B/8B# needs to be high.

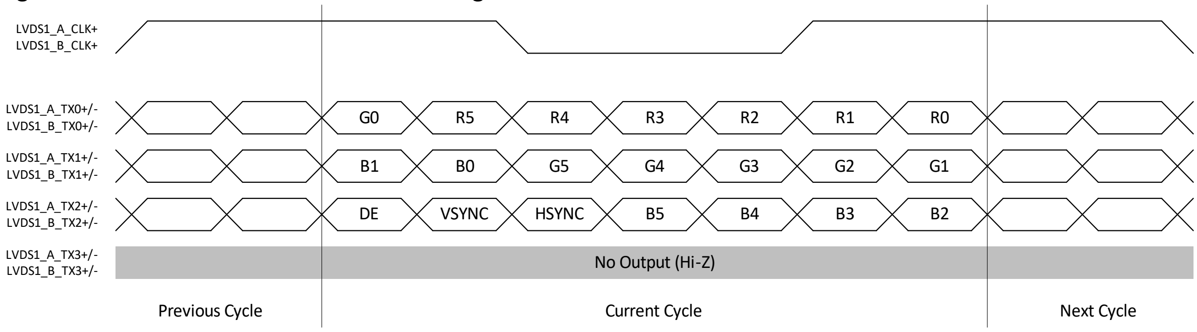

Figure 12: 18-bit Mode (MAP = H; 6B/8B# = H)

5.5.3 HDMI

HDMI provides a unified method of transferring video and audio data over a TMDS compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI standard.

Features
- HDMI 1.4a up to 1080p60
- Supports digital sound
- High-bandwidth Content Protection (HDCP) with internal SecureROM (license needed)

Table 5-17 HDMI Interface Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
240	HDMI1_TXC+	HDMI_TXCP	O	HDMI Differential Clock
242	HDMI1_TXC-	HDMI_TXCN	O	
234	HDMI1_TXD0+	HDMI_TXD0P	O	HDMI Differential Data, Lane 0
236	HDMI1_TXD0-	HDMI_TXD0N	O	
228	HDMI1_TXD1+	HDMI_TXD1P	O	HDMI Differential Data, Lane 1
230	HDMI1_TXD1-	HDMI_TXD1N	O	
222	HDMI1_TXD2+	HDMI_TXD2P	O	HDMI Differential Data, Lane 2
224	HDMI1_TXD2-	HDMI_TXD2N	O	
220	HDMI1_CEC	HDMI_CEC	I/O	HDMI Consumer Electronics Control.
232	HDMI1_HPD	HDMI_INT	I	Hot Plug Detect

Table 5-18 Additional Display Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
205	I2C2_SDA	DDC_SDA	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	DDC_SCL	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

5.5.4 Analog VGA

The analog VGA interface can be used to connect a standard VGA monitor. It supports analog VGA (analog RGB) and S-Video TV-out. The board support package (BSP) provided by Toradex only supports the VGA output. The Windows CE and Linux BSP do not support the composite TV, component TV, and S-Video TV output.

Features
- Up to WUXGA (1920x1200) resolution

Table 5-19 VGA Interface Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
208	VGA1_R	VDAC_R	O	Analogue Red Signal
210	VGA1_G	VDAC_G	O	Analogue Green Signal
212	VGA1_B	VDAC_B	O	Analogue Blue Signal
214	VGA1_HSYNC	CRT_HSYNC	O	Horizontal Sync needs a 5V level shifter
216	VGA1_VSYNC	CRT_VSYNC	O	Vertical Sync needs a 5V level shifter

Table 5-20 Additional Display Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
205	I2C2_SDA	DDC_SDA	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	DDC_SCL	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

5.5.5 Display Serial Interface (DSI)

The Tegra T30 supports up to two dual-lane MIPI DSI interfaces to connect compatible displays. The second DSI uses the interface of the CSI B interface pin. Each data lane is capable of up to 1Gbps data rate. Lane 1 of each interface is bidirectional (high speed out, low power/speed in from display). The interface uses the MIPI D-PHY for the physical interface.

The DSI signals are located in the Type-specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules are compatible with this interface. If you plan to use the DSI interface, please be aware that other Apalis modules might not be compatible with your carrier board.

Since the DSI is a high-speed interface, some additional layout requirements need to be met on the carrier board. These requirements are not detailed in the Apalis Carrier Board Design Guide as the interface is Type-specific.

Table 5-21 DSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	500MHz (1GT/S per data lane)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-22 DSI interface signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	DSI Signal Name	I/O	Description
127	TS_DIFF12+	DSI_CLKAP	DSI1_CLK+	O	DSI clock for interface 1
125	TS_DIFF12-	DSI_CLKAN	DSI1_CLK-	O	
121	TS_DIFF11+	DSI_D1AP	DSI1_D1+	I/O	DSI data lane 1 for interface 1
119	TS_DIFF11-	DSI_D1AN	DSI1_D1-	I/O	
115	TS_DIFF10+	DSI_D2AP	DSI1_D2+	O	DSI data lane 2 for interface 1
113	TS_DIFF10-	DSI_D2AN	DSI1_D2-	O	
133	TS_DIFF13+	CSI_CLKBP	DSI2_CLK+	O	DSI clock for interface 2 (Shared with CSI interface 2)
131	TS_DIFF13-	CSI_CLKBN	DSI2_CLK-	O	
145	TS_DIFF15+	CSI_D1BP	DSI2_D1+	I/O	DSI data lane 1 for interface 2 (Shared with CSI interface 2)
143	TS_DIFF15-	CSI_D1BN	DSI2_D1-	I/O	
139	TS_DIFF14+	CSI_D2BP	DSI2_D2+	O	DSI data lane 2 for interface 2 (Shared with CSI interface 2)
137	TS_DIFF14-	CSI_D2BN	DSI2_D2-	O	

Table 5-23 Additional Display Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
239	BKL1_PWM	UART3_RTSN	O	Backlight PWM (Shared with GPIO3 of power management IC, see Figure 6 in section 4.1)
286	BKL1_ON	GPIO_PV2	O	Enable signal for the backlight.
205	I2C2_SDA	DDC_SDA	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	DDC_SCL	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

5.6 PCI Express

The NVIDIA Tegra T30 features 6 PCI Express (PCIe) lanes that can be used for up to 3 separate PCIe interfaces (Links). As PCIe lane 5 is used internally for the Intel I210-AT Gigabit Ethernet Controller, only 5 PCIe lanes for 2 interfaces are available on the module edge connector. Lane 4 can only be used as a single-lane x1 PCIe interface and is available on the standard Apalis pinout. If you only require a single PCIe x1 interface, then this lane should be used as it is guaranteed to be compatible with other Apalis modules.

Lane 0 to 3 can only be used as a single interface in an x1, x2, or x4 combination. Lanes 0 to 3 are located in the Type-specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules are compatible with this interface. If you plan on using the second PCI interface, please be aware that your carrier board may not be compatible with all Apalis modules.

The PCIe is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 5-24 Apalis standard PCI Interface Signals (x1)

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
55	PCIE1_CLK+	PEX_CLK2P	O	Reference clock differential pair
53	PCIE1_CLK-	PEX_CLK2N	O	
49	PCIE1_TX+	PEX_L4_TXP	O	Lane 4 transmit data
47	PCIE1_TX-	PEX_L4_TXN	O	
43	PCIE1_RX+	PEX_L4_RXP	I	Lane 4 receive data
41	PCIE1_RX-	PEX_L4_RXN	I	

Table 5-25 Type-specific PCI Interface Signals (x4)

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
61	TS_DIFF1+	PEX_CLK1P	O	Reference clock differential pair Type-specific
59	TS_DIFF1-	PEX_CLK1N	O	
73	TS_DIFF3+	PEX_L0_TXP	O	Lane 0 transmit data Type-specific
71	TS_DIFF3-	PEX_L0_TXN	O	
67	TS_DIFF2+	PEX_L0_RXP	I	Lane 0 receive data Type-specific
65	TS_DIFF2-	PEX_L0_RXN	I	
85	TS_DIFF5+	PEX_L1_TXP	O	Lane 1 transmit data Type-specific
83	TS_DIFF5-	PEX_L1_TXN	O	
79	TS_DIFF4+	PEX_L1_RXP	I	Lane 1 receive data Type-specific
77	TS_DIFF4-	PEX_L1_RXN	I	
97	TS_DIFF7+	PEX_L2_TXP	O	Lane 2 transmit data Type-specific
95	TS_DIFF7-	PEX_L2_TXN	O	
91	TS_DIFF6+	PEX_L2_RXP	I	Lane 2 receive data Type-specific
89	TS_DIFF6-	PEX_L2_RXN	I	
109	TS_DIFF9+	PEX_L3_TXP	O	Lane 3 transmit data Type-specific
107	TS_DIFF9-	PEX_L3_TXN	O	
103	TS_DIFF8+	PEX_L3_RXP	I	Lane 3 receive data Type-specific
101	TS_DIFF8-	PEX_L3_RXN	I	

Table 5-26 Additional PCIe Control Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
37	WAKE1_MICO	GPIO_PV1	I	General-purpose wake signal
26	RESET_MOCI#	GMI_RST_N	O	General reset output
209	I2C1_SDA	GEN1_I2C_SDA	I/O	Some PCIe devices need the SMB interface for special configurations. I2C1 should be used if the interface is necessary
211	I2C1_SCL	GEN1_I2C_SCL	O	

5.7 SATA

The Serial ATA (SATA) interface can be used to attach, for example, an external hard drive, SSD, or an mSATA SSD. The interface is a single Gen 2 SATA link with a maximum transfer rate of 3Gb/s. SATA is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information

Table 5-27 Apalis standard PCI Interface Signals (x1)

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
33	SATA1_TX+	SATA_L0_TXP	O	SATA transmit data Series decoupling capacitors are provided on the module
31	SATA1_TX-	SATA_L0_TXN	O	
25	SATA1_RX+	SATA_L0_RXP	I	SATA receive data Series decoupling capacitors are provided on the module
27	SATA1_RX-	SATA_L0_RXN	I	
35	SATA1_ACT#	GPIO_PV1	O	SATA activity indicator

5.8 I²C

The NVIDIA Tegra T30 offers five I²C controllers. They implement the I²C V2.1 specification. All can be used as master or slave. Port 0 is used for power management and is not available externally. Port 1 is available as a general-purpose I²C on the module connector. Port 3 is intended to be used in combination with the camera interface but can also be used for other general purposes. Port 4 is typically used as the DDC or EDID interface. Port 1, 3, and 4 are available on the module edge connector at the dedicated I²C pins, according to the Apalis standard. I²C Port 2 is also available at the module edge connector, but only as an alternative function for some pins. It is not guaranteed that other Apalis modules provide an I²C interface on the same pins. Therefore, I²C Port 2 should only be used if a fourth I²C interface is required, and compatibility with other Apalis modules is not mandatory.

Features:
- Supports standard and fast mode of operation (0-400 kHz) and high-speed mode (3.4 MHz).
- Independent Master Controller and Slave Controller
- Master supports the clock stretching by the slave
- Supports one to eight-byte burst data transfers
- 7-bit or 10-bit addressing
- Fully programmable 7-bit or 10-bit address for the slave
- Supports general call addressing
- Supports Recognition and Transfer of data to peripherals that do not send an acknowledge
- Master supports packet-based DMA
- Supports 4kByte of transfer in packet mode (can be extended by using multiple packets)
- Clock Low Timeout (SMB Bus)

Many low-speed devices use I²C interfaces such as RTCs or sensors, but they are commonly used to configure other devices such as cameras or displays. The I2C Bus can also be used to communicate with SMB Bus devices.

Table 5-28 I²C Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	I²C Port	Description
209	I2C1_SDA	GEN1_I2C_SDA	1	Generic I²C
211	I2C1_SCL	GEN1_I2C_SCL		
201	I2C3_SDA (CAM)	CAM_I2C_SDA	3	I²C port for the camera interface can also be used for other purposes
203	I2C3_SCL (CAM)	CAM_I2C_SCL		
205	I2C2_SDA (DDC)	DDC_SDA	4	I²C port for the DDC interface can also be used for other purposes
207	I2C2_SCL (DDC)	DDC_SCL		
262	USBO1_OC#	GEN2_I2C_SDA	2	Not compatible with Apalis standard
274	USBO1_EN	GEN2_I2C_SCL		

5.8.1 Real-Time Clock (RTC) recommendation

The Apalis module features two RTC circuits. One is located in the power management IC (PMIC), while the other is located inside the SoC. If one of the internal RTC is used, it is recommended to use the one in the PMIC since the other one is not powered with the RTC battery rail. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for timekeeping. As long as the main power supply is provided to the module, the RTC is sourced from this rail. If the RTC needs to be retained even without the primary module voltage, a coin cell must be applied to the VCC_BACKUP (pin 174) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section 9.1). Therefore, a standard lithium coin cell battery can be drain faster than required for certain designs. If a rechargeable RTC battery is not a solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the module's I2C1 interface and leave the VCC_BACKUP pin unconnected. A suitable reference schematic can be found in the schematic diagram of the Apalis evaluation board.

5.9 UART

The Apalis T30 provides up to five serial UART interfaces. Four of them are available on dedicated UART pins as defined in the Apalis standard. The fifth UART is only available as an alternative function on the SDIO interface. It is not guaranteed that other Apalis modules support a UART as an alternative function on the SDIO port. Therefore, the fifth UART should only be used if compatibility with other Apalis modules is not mandatory.

The Tegra T30 UART1 (provided as Apalis UART1 interface) is the only full-featured UART and is used as a standard debug interface for the Toradex Linux and Windows Embedded Compact images. It is desirable to keep this port accessible for system debugging. The Tegra T30 UART2 (provided as Apalis UART3 interface) can be used as a VFIR (Very Fast Infra-Red) interface.

UART Features
- Support 16450 and 16550 compatible modes
- 16 byte FIFO
- Up to 4 Mbaud
- Word length 5 to 8 bit, optional parity, one or two stop bits
- Auto sense baud detection

VFIR Features
- Supports up to IrDA version 1.4 with 16Mbit/s
- 32bit x 16 deep FIFO

Table 5-29 UART1 Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 UART	I/O	Description
112	UART1_TXD	ULPI_DATA0	UART1.A-TXD	O	Transmit Data
118	UART1_RXD	ULPI_DATA1	UART1.A-RXD	I	Receive Data
114	UART1_RTS	ULPI_DATA3	UART1.A-RTS_N	O	Request to Send
116	UART1_CTS	ULPI_DATA2	UART1.A-CTS_N	I	Clear to Send
110	UART1_DTR	ULPI_DATA7	UART1.A-DTR_N	O	Data Terminal Ready
120	UART1_DSR	ULPI_DATA6	UART1.A-DSR_N	I	Data Set Ready
122	UART1_RI	ULPI_DATA4	UART1.A-RI_N	I	Ring Indicator
124	UART1_DCD	ULPI_DATA5	UART1.A-DCD_N	I	Data Carrier Detect

Table 5-30 UART2 Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 UART	I/O	Description
126	UART2_TXD	ULPI_CLK	UART4.A-TXD	O	Transmit Data
132	UART2_RXD	ULPI_DIR	UART4.A-RXD	I	Receive Data
128	UART2_RTS	ULPI_STP	UART4.A-RTS_N	O	Request to Send
130	UART2_CTS	ULPI_NXT	UART4.A-CTS_N	I	Clear to Send

Table 5-31 UART3 Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 UART	I/O	Description
134	UART3_TXD	UART2_TXD	UART2-TXD	O	Transmit Data
136	UART3_RXD	UART2_RXD	UART2-RXD	I	Receive Data

Table 5-32 UART4 Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 UART	I/O	Description
138	UART4_TXD	UART3_TXD	UART3-TXD	O	Transmit Data
140	UART4_RXD	UART3_RXD	UART3-RXD	I	Receive Data

Table 5-33 Signal Pins of additional UART Port

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 UART	I/O	Description
178	SD1_D3	SDMMC1_DAT3	UART5.A-TXD	O	Transmit Data
176	SD1_D2	SDMMC1_DAT2	UART5.A-RXD	I	Receive Data
186	SD1_D0	SDMMC1_DAT0	UART5.A-RTS_N	O	Request to Send
188	SD1_D1	SDMMC1_DAT1	UART5.A-CTS_N	I	Clear to Send

This UART port is only available as an alternative function on the SDIO port signals. Compatibility with other Apalis modules cannot be guaranteed, as it is not part of the Apalis module specification.

5.10 SPI

The Tegra T30 has 6 SPI controllers, of which 5 are used externally or internally. According to the Apalis module standard, two SPI interfaces are available at the dedicated SPI pins of the module connector. Two other SPI interfaces are used for internal communication with the CAN interface. One of the CAN SPI ports can be configured to be accessible as a secondary function of the UART1 pins of the module edge connector if this CAN interface is not used. A fifth SPI port is available as an alternative function on the remaining UART1 pins. Since these two SPI channels are only available as alternative functions, compatibility with other Apalis modules is not guaranteed. Please first use the dedicated Apalis SPI ports before using the ones on the UART1 pins.

These SPI ports operate at up to 50 Mbps and provide full-duplex, synchronous, serial communication between the Apalis module and internal or external peripheral devices. Each SPI port consists of four signals; clock, chip select (frame), data in, and data out. In the NVIDIA documentation, SPI is also referred to as SLINK.

Features:
- Up to 50 Mbps
- 32bit x 32 deep FIFO
- Packet size 1-32 bit
- Packed mode with 8 or 16bit packet size
- Receive-compare mode where the controller checks for a particular pattern in the incoming data stream before transferring the data to the FIFO
- Simultaneous receive and transmit

Each SPI channel supports four different modes of the SPI protocol:

Table 5-34 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock is positive polarity, and the data is latched on the positive edge of SCK
1	0	1	The clock is positive polarity, and the data is latched on the negative edge of SCK
2	1	0	The clock is negative polarity, and the data is latched on the positive edge of SCK
4	1	1	The clock is negative polarity, and the data is latched on the negative edge of SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCDs require to be configured over SPI before being driven via the RGB or LVDS interface.

Table 5-35 Apalis SPI Port 1 (T30 SPI Controller 1) Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SPI Controller	I/O	Description
225	SPI1_MOSI	SPI1_MOSI	SPI1.B-MOSI	O	Master Output, Slave Input
223	SPI1_MISO	SPI1_MISO	SPI1.B-MISO	I	Master Input, Slave Output
227	SPI1_CS	SPI1_CS0_N	SPI1.B-CS0_N	O	Slave Select
221	SPI1_CLK	SPI1_SCK	SPI1.B-SCK	O	Serial Clock

Table 5-36 Apalis SPI Port 2 (T30 SPI Controller 5) Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SPI Controller	I/O	Description
231	SPI2_MOSI	LCD_SDOUT	SPI5.A-MOSI	O	Master Output, Slave Input
229	SPI2_MISO	LCD_SDIN	SPI5.A-MISO	I	Master Input, Slave Output
233	SPI2_CS	LCD_CS0_N	SPI5.A-CS2_N	O	Slave Select
235	SPI2_CLK	LCD_SCK	SPI5.A-SCK	O	Serial Clock

Table 5-37 T30 SPI Port 3 on non-standard Apalis Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SPI Controller	I/O	Description
112	UART1_TXD	ULPI_DATA0	SPI3.E-MOSI	O	Master Output, Slave Input
118	UART1_RXD	ULPI_DATA1	SPI3.E-MISO	I	Master Input, Slave Output
114	UART1_RTS	ULPI_DATA3	SPI3.E-CS1_N	O	Slave Select
116	UART1_CTS	ULPI_DATA2	SPI3.E-SCK	O	Serial Clock

This SPI port is only available as an alternative function of the UART1 signals. This might not be compatible with other Apalis modules since it is not part of the Apalis module specification.

Table 5-38 SPI Port 2 on non-standard Apalis Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SPI Controller	I/O	Description
122	UART1_RI	ULPI_DATA4	SPI2.A-MOSI	O	Master Output, Slave Input
124	UART1_DCD	ULPI_DATA5	SPI2.A-MISO	I	Master Input, Slave Output
110	UART1_DTR	ULPI_DATA7	SPI2.A-CS1_N	O	Slave Select
120	UART1_DSR	ULPI_DATA6	SPI2.A-SCK	O	Serial Clock

This SPI port is only available as an alternative function on the UART1 signals. This might not be compatible with other Apalis modules, since it is not part of the Apalis module specification.

Table 5-39 SPI Interface for CAN Controller 1

CAN Controller Signal Name	T30 Signal Name	T30 SPI Controller	I/O	Description
SI	SPI2_MOSI	SPI6-MOSI	O	Master Output, Slave Input
SO	SPI2_MISO	SPI6-MISO	I	Master Input, Slave Output
CS#	SPI2_CS0_N	SPI6-CS0	O	Slave Select
SCK	SPI2_SCK	SPI6-SCK	O	Serial Clock
INT#	SPI2_CS1_N	GPIO-W.02	I	Interrupt

Table 5-40 SPI Interface for CAN Controller 2

CAN Controller Signal Name	T30 Signal Name	T30 SPI Controller	I/O	Description
SI	GMI_A17	SPI4.C-MOSI	O	Master Output, Slave Input
SO	GMI_A18	SPI4.C-MISO	I	Master Input, Slave Output
CS#	GMI_A19	SPI4.C-CS1_N	O	Slave Select
SCK	GMI_A16	SPI4.C-SCK	O	Serial Clock
INT#	SPI2_CS2_N	GPIO-W.03	I	Interrupt

5.11 Controller Area Network (CAN)

The Apalis T30 features two CAN interfaces. These interfaces are provided by two MCP2515 CAN controllers with SPI interfaces. It implements the CAN protocol according to the CAN 2.0B specifications with bit rates up to 1Mb/s. For more information about the SPI interfaces for the CAN controllers, see section 5.10.

The MCP2515 provides only a buffer for a maximum of two CAN messages. The system may lose messages if the CAN bus runs at high speed and three or more messages are transmitted over the

CAN bus in short intervals. Contact the Toradex support team for more information about the limitation of the MCP2515 CAN controller.

Table 5-41 CAN Signal Pins

X1 Pin#	Apalis Signal Name	MCP2515 Pin Number	MCP2515 Pin Name	I/O	Description
14	CAN1_TX	19	TXCAN	O	CAN port 1 transmit pin
12	CAN1_RX	20	RXCAN	I	CAN port 1 receive pin
18	CAN2_TX	19	TXCAN	O	CAN port 2 transmit pin
16	CAN2_RX	20	RXCAN	I	CAN port 2 receive pin

5.12 PWM (Pulse Width Modulation)

The Apalis T30 features a four-channel Pulse Width Modulator (PWM). The duty cycle has an 8-bit resolution (it can be set to a value between 0 and 255 in steps of 1/256). The maximum output frequency is 187.5 kHz.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights, or servo motors.

The Apalis standard defines a fifth dedicated PWM output for the display backlight. As the Tegra T30 features only four PWM controllers, the backlight PWM can be selected to be provided by the power management IC (PMIC) or share the Tegra T30 PWM4 output (see Figure 6 and section 4.1.)

Table 5-42 PWM Interface Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 PWM Controller	I/O	Remarks
2	PWM1	GPIO_PU6	PWFM-PWM3	O	
4	PWM2	GPIO_PU5	PWFM-PWM2	O	
6	PWM3	GPIO_PU4	PWFM-PWM1	O	
8	PWM4	GPIO_PU3	PWFM-PWM0	O	Shared PWM controller with BKL1_PWM
239	BKL1_PWM	UART3_RTS_N	PWFM-PWM0	O	Shared Tegra PWM controller with PWM4 Alternative output from PMIC

5.13 OWR (One-Wire)

The One Wire Controller (OWR) implements a device communications bus system that provides low-speed data, signaling, and power over a single wire. The OWR uses two signals for this - one for ground and the other for power and data.

On the Apalis T30, the one-wire protocol is primarily intended for communication with battery controller chips. The OWR is multiplexed with the GPIO6 interface on the module and is not part of the Apalis module specification. Therefore, compatibility with other Apalis modules is not guaranteed.

Features
- FIFO depth of 32 x 32 bits
- Hard-wired implementation of the one-wire protocol to eliminate the need for an external bridge chip
- 1 MHz device clock required
- Supports de-glitch
- Supports Byte transfer or 1-Bit transfer

- Supports the following commands: Read ROM, Skip ROM, Read Memory, Read Status, Read Data/Generate 8-bit CRC, Write Memory, Write Status
- Supports CRC 8/16-bit implementation
- Supports different battery devices, up to a memory size of 256KB in byte transfer
- Generic controller support with device Maxim DS2784

Table 5-43 OWR Data Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
13	GPIO6	OWR	I/O	Multiplexed with KB_COL0 pin of T30

5.14 SD/MMC

The Tegra T30 provides 4 SDIO interfaces; one is used internally for the eMMC Flash, and the other 3 are available on the module edge connector Pins. To ensure carrier board design compatibility with other Apalis modules, it is recommended to use only the two SD/MMC interfaces available at the pins defined in the Apalis standard. The third SD/MMC interface is available as an alternative function at two different pin locations.

The interfaces can interface with SD Memory Cards, SDIO, MMC, CE-ATA cards, and eMMC devices. The controllers can act as both master and slave simultaneously.

Features
- Supports SD Memory Card Specification 3.0
- Supports SDIO Card Specification Version 3.0
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Support SPI mode
- The IO voltage is 3.3V on the SODIMM pins.
- MMC1 interface supports 3.3V and 1.8V IO voltage mode (supports up to UHS-I)
- Other SD/MMC interfaces support 3.3V (default and high-speed mode only)

Tegra SDIO interface	Max Bus Width	Description
1	4bit	Apalis Standard SD1 interface, only 3.3V IO voltage
2	4/8bit	Available as a secondary function, not compatible with Apalis standard, only 3.3V IO voltage
3	8bit	Apalis Standard MMC1 interface, 3.3V/1.8V IO voltage, UHS-I capable
4	8bit	Connected to internal eMMC. Not available at the module edge connector

According to the Apalis module specification, the SD/MMC interface's IO voltage level supports only a 3.3V logic level. Therefore, the SD interfaces are limited to default or high-speed mode. UHS-I modes are not supported. Nevertheless, the MMC1 interface (Tegra SDMMC3 interface) can switch to the 1.8V IO level. This allows using the interface in UHS-I mode with higher speed. Please note that this IO voltage level is not mandatory in the Apalis module specification, and therefore other modules might not support this mode. Pay attention to the SD card signal's pull up resistors on the carrier board. If the MMC1 interface is used in the 1.8V mode, it is recommended to remove the carrier board's pull-up resistors. The Tegra features internal pull-up resistors, which can be used instead.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Supported Interfaces
Default Speed	25 MHz	12.5 MByte/s	3.3V	All
High Speed	50 MHz	25 MByte/s	3.3V	All
SDR12	25 MHz	12.5 MByte/s	1.8V	MMC1 only
SDR25	50 MHz	25 MByte/s	1.8V	MMC1 only
DDR50	50 MHz	50 MByte/s	1.8V	MMC1 only
SDR50	100 MHz	50 MByte/s	1.8V	MMC1 only
SDR104	208 MHz	104 MByte/s	1.8V	MMC1 only

Table 5-44 Apalis MMC1 Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SD/MMC Controller	I/O	Description
150	MMC1_CMD	SDMMC3_CMD	SDMMC3-CMD	I/O	Command
160	MMC1_D0	SDMMC3_DAT0	SDMMC3-DAT0	I/O	Serial Data 0
162	MMC1_D1	SDMMC3_DAT1	SDMMC3-DAT1	I/O	Serial Data 1
144	MMC1_D2	SDMMC3_DAT2	SDMMC3-DAT2	I/O	Serial Data 2
146	MMC1_D3	SDMMC3_DAT3	SDMMC3-DAT3	I/O	Serial Data 3
148	MMC1_D4	SDMMC3_DAT4	SDMMC3-DAT4	I/O	Serial Data 4
152	MMC1_D5	SDMMC3_DAT5	SDMMC3-DAT5	I/O	Serial Data 5
156	MMC1_D6	SDMMC3_DAT6	SDMMC3-DAT6	I/O	Serial Data 6
158	MMC1_D7	SDMMC3_DAT7	SDMMC3-DAT7	I/O	Serial Data 7
154	MMC1_CLK	SDMMC3_CLK	SDMMC3-SCLK	O	Serial Clock
164	MMC1_CD#	GPIO_PV3	GPIO-V.03	I	Card Detect (standard GPIO)

Table 5-45 Apalis SD1 Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SD/MMC Controller	I/O	Description
184	SD1_CLK	SDMMC1_CLK	SDMMC1-SCLK	O	Serial Clock
186	SD1_D0	SDMMC1_DAT0	SDMMC1-DAT0	I/O	Serial Data 0
188	SD1_D1	SDMMC1_DAT1	SDMMC1-DAT1	I/O	Serial Data 1
176	SD1_D2	SDMMC1_DAT2	SDMMC1-DAT2	I/O	Serial Data 2
178	SD1_D3	SDMMC1_DAT3	SDMMC1-DAT3	I/O	Serial Data 3
180	SD1_CMD	SDMMC1_CMD	SDMMC1-CMD	I/O	Command
190	SD1_CD#	CLK2_REQ	GPIO-CC.05	I	Card Detect (standard GPIO)

Table 5-46 Instance A of T30 SD/MMC Controller 2 on non-standard Apalis Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SD/MMC Controller	I/O	Description
1	GPIO1	KB_ROW10	SDMMC2.A-SCLK	I/O	Serial Clock
5	GPIO3	KB_ROW12	SDMMC2.A-DAT0	I/O	Serial Data 0
7	GPIO4	KB_ROW13	SDMMC2.A-DAT1	I/O	Serial Data 1
11	GPIO5	KB_ROW14	SDMMC2.A-DAT2	I/O	Serial Data 2
15	GPIO7	KB_ROW15	SDMMC2.A-DAT3	I/O	Serial Data 3
175	CAM1_D6	KB_ROW6	SDMMC2.A-DAT4	I/O	Serial Data 4
173	CAM1_D7	KB_ROW7	SDMMC2.A-DAT5	I/O	Serial Data 5
135	TS_5	KB_ROW8	SDMMC2.A-DAT6	I/O	Serial Data 6
159	TS_6	KB_ROW9	SDMMC2.A-DAT7	I/O	Serial Data 7
3	GPIO2	KB_ROW11	SDMMC2.A-CMD	O	Command

This 8bit instance of the SD/MMC Controller 2 is available as an alternative function on GPIO and camera interface signals. This might not be compatible with other Apalis modules, as it is not part of the Apalis module specification. For the card-detect, any free GPIO can be used.

Table 5-47 Instance C of T30 SD/MMC Controller 2 on non-standard Apalis Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 SD/MMC Controller	I/O	Description
204	DAP1_SYNC	DAP1_FS	SDMMC2.C-CMD	I/O	Command
202	DAP1_D_IN	DAP1_DIN	SDMMC2.C-DAT0	I/O	Serial Data 0
196	DAP1_D_OUT	DAP1_DOUT	SDMMC2.C-DAT1	I/O	Serial Data 1
215	SPDIF1_OUT	SPDIF_OUT	SDMMC2.C-DAT2	I/O	Serial Data 2
217	SPDIF1_IN	SPDIF_IN	SDMMC2.C-DAT3	I/O	Serial Data 3
200	DAP1_BIT_CLK	DAP1_SCLK	SDMMC2.C-SCLK	O	Serial Clock

This alternative 4bit instance of the SD/MMC Controller 2 is available as an alternative function on digital audio and SPDIF interface signals. This might not be compatible with other Apalis modules, as it is not part of the Apalis module specification. For the card-detect, any free GPIO can be used.

5.15 Analog Audio

The Apalis T30 offers analog Audio input and output channels. On the module, a Freescale SGTL5000 chip handles the analog audio interface. The SGTL5000 is connected to I2S controller 2 with the Tegra T30. Please consult the Freescale SGTL5000 datasheet for more information.

Table 5-48 Analogue Audio Interface Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Pin on the SGTL5000 (20pin QFN)
306	AAP1_MICIN	Analogue Input	Microphone input	10
310	AAP1_LIN_L	Analogue Input	Left Line Input	9
312	AAP1_LIN_R	Analogue Input	Right Line Input	8
316	AAP1_HP_L	Analogue Output	Headphone Left Output	4
318	AAP1_HP_R	Analogue Output	Headphone Right Output	1

5.16 Digital Audio

The Apalis module standard provides one digital audio interface. The interface can be used as Intel® High-Definition Audio (also known as HD Audio, HDA, or Azalia) or as I²S (also known as Inter-IC Sound, Integrated Interchip Sound, or IIS). The interfaces can connect an additional external audio codec that can provide up to 7.1 channel audio. Please be aware that some Apalis modules may only provide HD Audio or I²S on this interface.

5.16.1 I²S

Features
- PCM, Network, and TDM mode Support
- Master or Slave
- Supports I2S, RJM, LJM, and DSP mode data formats
- Maximum device clock of 24 MHz

Table 5-49 Digital Audio port used as I²S

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 I²S Port Names	I/O	Description
202	DAP1_D_IN	DAP1_DIN	I2S0-SDATA_IN	I	Data Input to T30
196	DAP1_D_OUT	DAP1_DOUT	I2S0-SDATA_OUT	O	Data Output from T30
204	DAP1_SYNC	DAP1_FS	I2S0-LRCK	I/O	Field Select
200	DAP1_BIT_CLK	DAP1_SCLK	I2S0-SCLK	I/O	Serial Clock
194	DAP1_MCLK	CLK2_OUT	CLK-EXTCLK2	O	External Peripheral Clock

For controlling the I²S codec, an additional I²C interface is required. Toradex recommends using the generic I²C interface I2C1. Some codecs need an external master reference clock. It is recommended to use the DAP1_MCLK output.

5.16.2 HD Audio

Features
- Maximum HDA Bit clock frequency 24MHz
- Data Rate SDO 48Mb/s (DDR)
- Data Rate SDI 24Mb/s
- Configuration / device organization: 1 load

Table 5-50 Digital Audio port used as HD Audio

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 I²C Port Names	I/O	Description
198	DAP1_RESET#	CLK1_REQ	HDA.A-RESET	O	HD Audio Reset
202	DAP1_D_IN	DAP1_DIN	HDA.A-SDI	I	HD Audio Serial Input to T30
196	DAP1_D_OUT	DAP1_DOUT	HDA.A-SDO	O	HD Audio Serial Output from T30
204	DAP1_SYNC	DAP1_FS	HDA.A-SYNC	I/O	HD Audio Sync
200	DAP1_BIT_CLK	DAP1_SCLK	HDA.A-BCLK	I/O	HD Audio Bit Clock

The HD Audio interface does not need an additional I²C for the control communication. The codec is controlled over the HD Audio interface itself. The HD Audio codec does not require a master reference clock. Please take care of the pin naming of some codecs. Some devices, such as Realtek ALC889, name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host and not to the signal direction.

5.17 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of the serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard. This controller can be used for stereo only; multi-channel audio uses the HDA controller.

Features:

- Supports 5 data formats
    - 16-bit
    - 20-bit
    - 24-bit
    - Raw
    - 16-bit packed
- Supports "auto-lock" mode to automatically detect "spdifin" sample rate and lock onto the data stream.
- Supports override mode to provide a manual control to sample "spdifin" data stream.

Table 5-51 S/PDIF Data Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
215	SPDIF1_OUT	SPDIF_OUT	O	Serial data output
217	SPDIF1_IN	SPDIF_IN	I	Serial data input

5.18 Touch Panel Interface

The Apalis T30 offers a 4-wire resistive touch interface. The ST Microelectronics STMPE811 provides the touch interface. The Microelectronics STMPE811 is connected with the Tegra T30 via the power management I²C interface (Port 0).
Please consult the Microelectronics STMPE811 documentation for more information.

Table 5-52 Touch Interface Pins

X1 Pin #	Signal Name	Pin on the STMPE811	I/O	Description
315	AN1_TSPX	13	Analogue Input	X+ (4-wire)
317	AN1_TSMX	16	Analogue Input	X- (4-wire)
319	AN1_TSPY	15	Analogue Input	Y+ (4-wire)
321	AN1_TSMY	1	Analogue Input	Y- (4-wire)

5.19 Analogue Inputs

The ST Microelectronics STMPE811 provides the 4 analog input channels. Please consult the ST Microelectronics STMPE811 documentation for more information. All AD inputs are protected with a 10k Ohm series resistor between the module edge connector pins and the ADC.

Features
- 12-bit ADC
- 0 to 3.3V rail to rail

Table 5-53 Analogue Inputs Pins

X1 Pin #	Signal Name	Pin on the STMPE811	I/O	Description
305	AN1_ADC0	8	Analogue Input	ADC input (3.3V max)
307	AN1_ADC1	9	Analogue Input	ADC input (3.3V max). This ADC pin is pulled to GND (10k Ohm) for 6µs while booting.
309	AN1_ADC2	11	Analogue Input	ADC input (3.3V max)
311	AN1_TSWIP_ADC3	12	Analogue Input	ADC input (3.3V max).

5.20 Camera Interface

5.20.1 Parallel Camera Interface

The Video Capture and Imaging Subsystem (VI) can receive data from TV decoder chips, CMOS sensors, and other devices. It supports advanced processing features with its multi-stage pipeline, from lens correction through to color space conversion. Among other functions, this subsystem removes common artifacts of digital CMOS image sensors and lenses from the raw data. It interpolates alternating, one-color-per-pixel Bayer-formatted data into full RGB color signals.

All of the camera interface pins are multiplexed with other Tegra T30 pins. If you use the camera interface, make sure the multiplexed pins are tri-stated. Additional information can be found in chapter 4.1 Function Multiplexing.

Features
- Raw (Bayer), RGB, YUV input up to 12 Megapixels
- 8/10bit parallel video interface
- ITU-R 8bit
- Max pixel clock input 120 MHz
- Max Master clock output (Camera input clock) 80MHz

Only the 8-bit YUV mode is guaranteed to be compatible with other Apalis modules. The additional signal bits for the 10 and 12bit interface are located on the Type-specific area. Other Apalis modules may have different signals on these pins. Even if the additional signal pins are available on another module, the color mapping for 10/12bit input is not guaranteed to be compatible.

Table 5-54 Camera Interface Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
187	CAM1_D0	VI_D2	I	Camera pixel data 0 (8bit _YUV)
185	CAM1_D1	VI_D3	I	Camera pixel data 1 (8bit _YUV)
183	CAM1_D2	VI_D4	I	Camera pixel data 2 (8bit _YUV)
181	CAM1_D3	VI_D5	I	Camera pixel data 3 (8bit _YUV)
179	CAM1_D4	VI_D6	I	Camera pixel data 4 (8bit _YUV)
177	CAM1_D5	VI_D7	I	Camera pixel data 5 (8bit _YUV)
175	CAM1_D6	VI_D8	I	Camera pixel data 6 (8bit _YUV)
173	CAM1_D7	VI_D9	I	Camera pixel data 7 (8bit _YUV)
191	CAM1_PCLK	VI_PCLK	I	Camera pixel clock
195	CAM1_VSYNC	VI_VSYNC	I	Camera vertical sync
197	CAM1_HSYNC	VI_HSYNC	I	Camera horizontal sync
135	TS_5	VI_D0	I	Additional Camera pixel data (Type-specific)
159	TS_6	VI_D1	I	Additional Camera pixel data (Type-specific)
123	TS_4	VI_D10	I	Additional Camera pixel data (Type-specific)
99	TS_3	VI_D11	I	Additional Camera pixel data (Type-specific)

Table 5-55 Additional Camera Interface Signals (shared with CSI)

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
193	CAM1_MCLK	CAM_MCLK	O	Master clock output for the camera (shared with CSI)
201	I2C3_SDA (CAM)	CAM_I2C_SDA	I/O	Camera control I^2C (shared with CSI)
203	I2C3_SCL (CAM)	CAM_I2C_SCL	O	Camera control I^2C (shared with CSI)

Table 5-56 Camera Interface Color Pin Mapping

X1 Pin#	Apalis Signal Name	T30 Signal Name	YUV 8bit	Bayer 8bit	Bayer 10bit	Bayer 12bit
135	TS_5	VI_D0		GND	D0	D2
159	TS_6	VI_D1		GND	D1	D3
187	CAM1_D0	VI_D2	D0	D0	D2	D4
185	CAM1_D1	VI_D3	D1	D1	D3	D5
183	CAM1_D2	VI_D4	D2	D2	D4	D6
181	CAM1_D3	VI_D5	D3	D3	D5	D7
179	CAM1_D4	VI_D6	D4	D4	D6	D8
177	CAM1_D5	VI_D7	D5	D5	D7	D9
175	CAM1_D6	VI_D8	D6	D6	D8	D10
173	CAM1_D7	VI_D9	D7	D7	D9	D11
123	TS_4	VI_D10				
99	TS_3	VI_D11				

5.20.2 Camera Serial Interface (CSI)

The Tegra T30 supports two dual-lane or one quad lane MIPI CSI2 interface for connecting compatible cameras. For the quad lane configuration, the two dual-lane interfaces are combined. The second dual-lane CSI interface is shared with the second DSI interface. The interface uses the MIPI D-PHY for the physical interface.

The CSI signals are located in the Type-specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules are compatible with this interface. If you plan to use the CSI interface, please be aware that other modules may not be compatible with your carrier board.

As the CSI is a high-speed interface, some additional layout requirements are needed to be followed on the carrier board. These requirements are not defined in the Apalis Carrier Board Design Guide as this interface is Type-specific.

Table 5-57 CSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	500MHz (1GT/S per data lane)
Configuration /Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-58 Dual Lane CSI interface signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	CSI Signal Name	I/O	Description
163	TS_DIFF18+	CSI_CLKAP	CSI1_CLK+	I	CSI clock for interface 1
161	TS_DIFF18-	CSI_CLKAN	CSI1_CLK-	I	
157	TS_DIFF17+	CSI_D1AP	CSI1_D1+	I/O	CSI data lane 1 for interface 1
155	TS_DIFF17-	CSI_D1AN	CSI1_D1-	I/O	
151	TS_DIFF16+	CSI_D2AP	CSI1_D2+	I	CSI data lane 2 for interface 1
149	TS_DIFF16-	CSI_D2AN	CSI1_D2-	I	
133	TS_DIFF13+	CSI_CLKBP	CSI2_CLK+	I	CSI clock for interface 2 (Shared with DSI interface 2)
131	TS_DIFF13-	CSI_CLKBN	CSI2_CLK-	I	
145	TS_DIFF15+	CSI_D1BP	CSI2_D1+	I/O	CSI data lane 1 for interface 2 (Shared with DSI interface 2)
143	TS_DIFF15-	CSI_D1BN	CSI2_D1-	I/O	
139	TS_DIFF14+	CSI_D2BP	CSI2_D2+	I	CSI data lane 2 for interface 2 (Shared with DSI interface 2)
137	TS_DIFF14-	CSI_D2BN	CSI2_D2-	I	

Table 5-59 Quad Lane CSI interface signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	CSI Signal Name	I/O	Description
163	TS_DIFF18+	CSI_CLKAP	CSI1_CLK+	I	CSI clock for interface 1
161	TS_DIFF18-	CSI_CLKAN	CSI1_CLK-	I	
157	TS_DIFF17+	CSI_D1AP	CSI1_D1+	I/O	CSI data lane 1 for interface 1
155	TS_DIFF17-	CSI_D1AN	CSI1_D1-	I/O	
151	TS_DIFF16+	CSI_D2AP	CSI1_D2+	I	CSI data lane 2 for interface 1
149	TS_DIFF16-	CSI_D2AN	CSI1_D2-	I	
145	TS_DIFF15+	CSI_D1BP	CSI1_D3+	I	CSI data lane 3 for interface 1 (Shared with DSI interface 2)
143	TS_DIFF15-	CSI_D1BN	CSI1_D3-	I	
139	TS_DIFF14+	CSI_D2BP	CSI1_D4+	I	CSI data lane 4 for interface 1 (Shared with DSI interface 2)
137	TS_DIFF14-	CSI_D2BN	CSI1_D4-	I	

Table 5-60 Additional Camera Interface Signals (shared with parallel camera)

X1 Pin#	Apalis Signal Name	T30 Signal Name	I/O	Description
193	CAM1_MCLK	CAM_MCLK	O	Master clock output for the camera (shared with parallel camera)
201	I2C3_SDA (CAM)	CAM_I2C_SDA	I/O	Camera control I²C (shared with parallel camera)
203	I2C3_SCL (CAM)	CAM_I2C_SCL	O	Camera control I²C (shared with parallel camera)

5.21 Clock Output

The Apalis T30 provides up to two external clock outputs on the module edge connector. One output is dedicated to the camera interface, while the other is for the digital audio interface. If the clock outputs are not needed for the interfaces, they can also be used as general-purpose clock outputs.

Available Clock Frequencies: should be validated

Care must be taken when changing PLL frequencies; these PLLs are also used internally in the Tegra T30.

Table 5-61 Clock Output Signal Pins

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 Clock Name	I/O	Description
194	DAP1_MCLK	CLK2_OUT	CLK_EXTCLK2	O	Clock output for the digital audio interface, see section 5.16
193	CAM1_MCLK	CAM_MCLK	CLK-VI_MCLK	O	Clock output for the parallel and serial camera interface, see section 5.20

5.22 Keypad

You can use any free GPIOs to realize a Matrix keypad interface. Additionally, the Tegra T30 features a keyboard controller. As the keyboard controller is only available as an alternative function on specific pins, this interface is not compatible with other Apalis modules. It can only be used if the required pins are not occupied by their primary function.

The Tegra keyboard controller eliminates the requirement for de-bounce capacitors and pull-up resistors. It can handle up to two buttons pressed without the need of de-ghosting diodes. If the diodes are available, any combination of pressed keys can be detected. The row and column pins can be configured for a keyboard matrix of up to 16 by 8.

There are some restrictions if the Tegra T30 keyboard controller is used:

- ROW0 must always be enabled
- The rows must be used consecutively with no holes. Use ROW0 and ROW1 instead of ROW0 and ROW2. If a row is skipped, the keyboard works properly in the normal mode, but the wakeup does not work from keys located after the hole.
- All keys with wake-up capability must be located in the same columns. The keys which should not wake up the system need to be in different columns.

Table 5-62 Keyboard Matrix Interface Signals

X1 Pin#	Apalis Signal Name	T30 Signal Name	T30 Keypad Signal	Primary Apalis Function
187	CAM1_D0	KB_ROW0	KBC-ROW0	Parallel Camera Interface
85	CAM1_D1	KB_ROW1	KBC-ROW1	Serial Camera Interface
183	CAM1_D2	KB_ROW2	KBC-ROW2	Serial Camera Interface
181	CAM1_D3	KB_ROW3	KBC-ROW3	Serial Camera Interface
179	CAM1_D4	KB_ROW4	KBC-ROW4	Serial Camera Interface
177	CAM1_D5	KB_ROW5	KBC-ROW5	Serial Camera Interface
175	CAM1_D6	KB_ROW6	KBC-ROW6	Serial Camera Interface
173	CAM1_D7	KB_ROW7	KBC-ROW7	Serial Camera Interface
135	TS_5	KB_ROW8	KBC-ROW8	Serial Camera Interface, Type-specific
159	TS_6	KB_ROW9	KBC-ROW9	Serial Camera Interface, Type-specific
1	GPIO1	KB_ROW10	KBC-ROW10	Apalis GPIO
3	GPIO2	KB_ROW11	KBC-ROW11	Apalis GPIO
5	GPIO3	KB_ROW12	KBC-ROW12	Apalis GPIO
7	GPIO4	KB_ROW13	KBC-ROW13	Apalis GPIO
11	GPIO5	KB_ROW14	KBC-ROW14	Apalis GPIO
15	GPIO7	KB_ROW15	KBC-ROW15	Apalis GPIO
13	GPIO6	KB_COL0	KBC-COL0	Apalis GPIO
17	GPIO8	KB_COL1	KBC-COL1	Apalis GPIO
191	CAM1_PCLK	KB_COL2	KBC-COL2	Serial Camera Interface
195	CAM1_VSYNC	KB_COL3	KBC-COL3	Serial Camera Interface
197	CAM1_HSYNC	KB_COL4	KBC-COL4	Serial Camera Interface
99	TS_3	KB_COL5	KBC-COL5	Serial Camera Interface, Type-specific
123	TS_4	KB_COL6	KBC-COL6	Serial Camera Interface, Type-specific
87	TS_2	KB_COL7	KBC-COL7	Type-specific

5.23 JTAG

The JTAG interface is not normally required for software development with the Apalis T30. There is always the possibility of reprogramming the module via the Recovery Mode. For flashing the module in recovery mode and debug reasons, it is strongly recommended that the USBO1 interface is accessible even if not needed in the final system. Additional, UART1 should also be accessible.

The JTAG interface is located as test points on the bottom side of the module. The Apalis specifications standardize the location. The reference voltage for the interface is 3.3V.

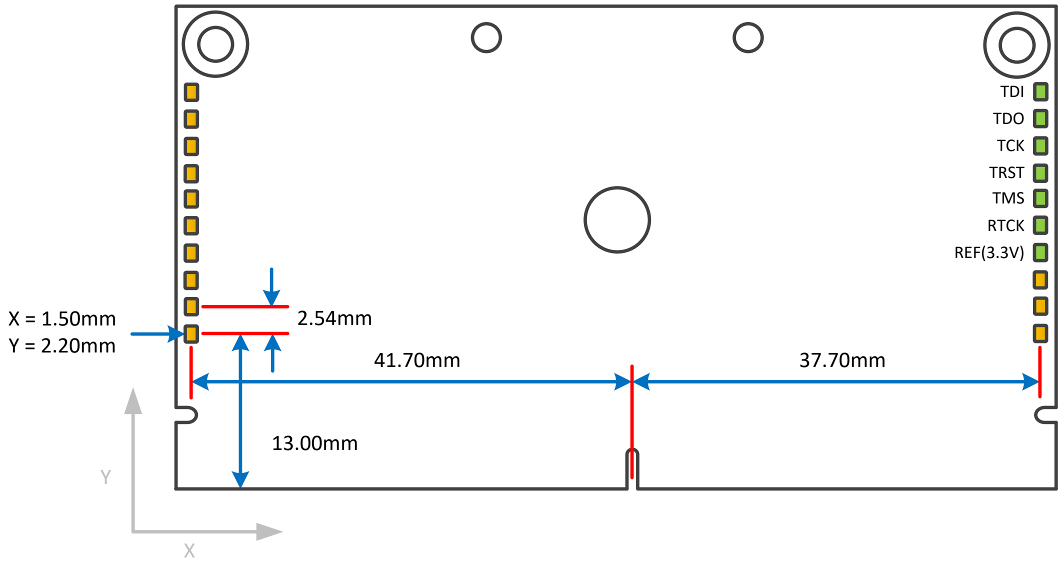

Figure 13 JTAG test point location on the bottom side of the module

6. Recovery Mode

The recovery mode can be used for downloading new software to the Apalis T30 even if the bootloader is no longer capable of booting the module. In the standard development process, this mode is not needed. When the module is in recovery mode, the USBO1 interface connects it to a host computer. The NVFlash tool can be used to re-program the module. You can find additional information in our Developer Center: http://developer.toradex.com.

The recovery mode pads need to be shorted during the initial power on or reset of the module to enter recovery mode. Figure 14 shows the location of the pads that need to be shorted for entering the recovery mode.

It is also possible to enter the recovery mode by pulling down pin 63 of the module edge connector (TS_1) with a 10kΩ resistor while booting. This pin is located in the Type-specific area. It is not guaranteed that other Apalis modules can be put into recovery mode in the same way.

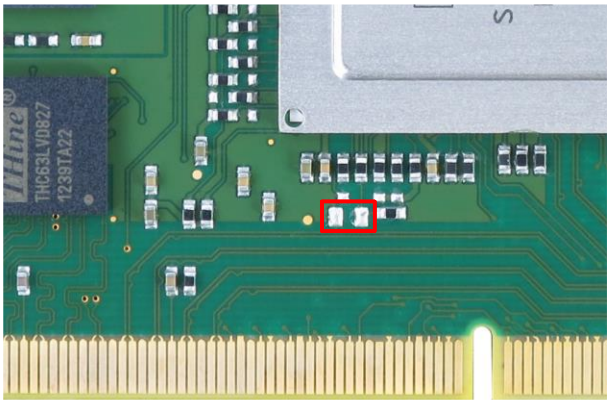

Figure 14 Location of recovery mode pads

7. Suspend

In the suspend state, the CPU is powered off, but the RAM is still powered. It is very fast for the system to wake up from this state. You can use several pins as wake-up sources. Please see chapter 5.2.1 for more information about possible wakeup sources.

For the pin behavior, see the NVIDIA Tegra 3 datasheet.

8. Known Issues

- If a voltage is applied to the analog input AN1_ADC1 (pin 307) during the module's power-up, it can cause problems that the ADC and touch controller STMPE811 is strapped wrongly and therefore not accessible. It is recommended to avoid applying any voltages on the AN1_ADC1 during the power-up of the modules. The other ADC inputs do not have this limitation.
- The current consumption on the RTC battery rail (VCC_BATT) can reach up to 240 µA on earlier modules (Apalis T30 V1.1A and older) if the primary voltage rail (3V3) is not applied. Even though the current consumption is reduced to 56 µA on newer versions of the module, it is recommended to use an external ultra-low power RTC device if the system time needs to be retained without the primary voltage rail. See also section 5.8.1.

9. Technical Specifications

9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_VCC	Main power supply	-0.3	3.63	V
Vmax_AVCC	Analog power supply	-0.3	3.6	V
Vmax_VCC_BACKUP	RTC power supply	-0.3	5.5	V
Vmax_IO	IO pins with GPIO function	-0.5	3.63	V
Vmax_AN1	ADC and touch analog input	-0.3	3.9	V
Vmax USBO1_VBUS	Input voltage at USBO1_VBUS	-0.5	6.0	V

9.2 Recommended Operating Conditions

Table 9-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
VCC	Main power supply	3.135	3.3	3.465	V
AVCC	Analogue power supply	3.0	3.3	3.6	V
VCC_BACKUP	RTC power supply	2.2	3.3	3.6	V

9.3 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Apalis product family. Following those recommendations ensures that the carrier board being designed is compatible with all existing and future Apalis modules. Please refer to the Apalis Family Specification or the Apalis Carrier Board Design Guide for details.

For designing carrier boards for a particular Apalis module only, please consult our Developer Website for module-specific power consumption information. However, please note that scaling the carrier board power supplies for a particular module only may cause compatibility issues with other existing and future modules within the Apalis family. For designing carrier boards specifically for the Apalis T30, please consult our Developer Website for module-specific power consumption information.

9.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Apalis module. This specification can be found in the Apalis Carrier Board Design Guide.

9.5 Mechanical Characteristics

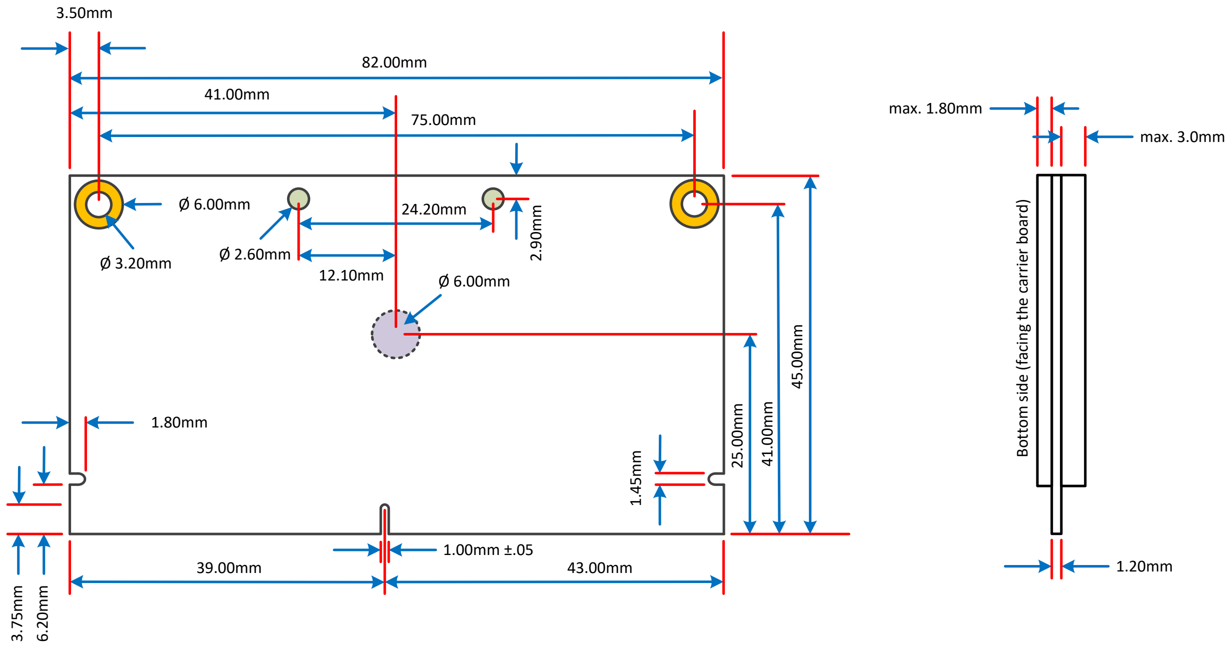

Figure 15 Mechanical dimensions of the Apalis module (top view)
Tolerance for all measures: +/- 0.1mm

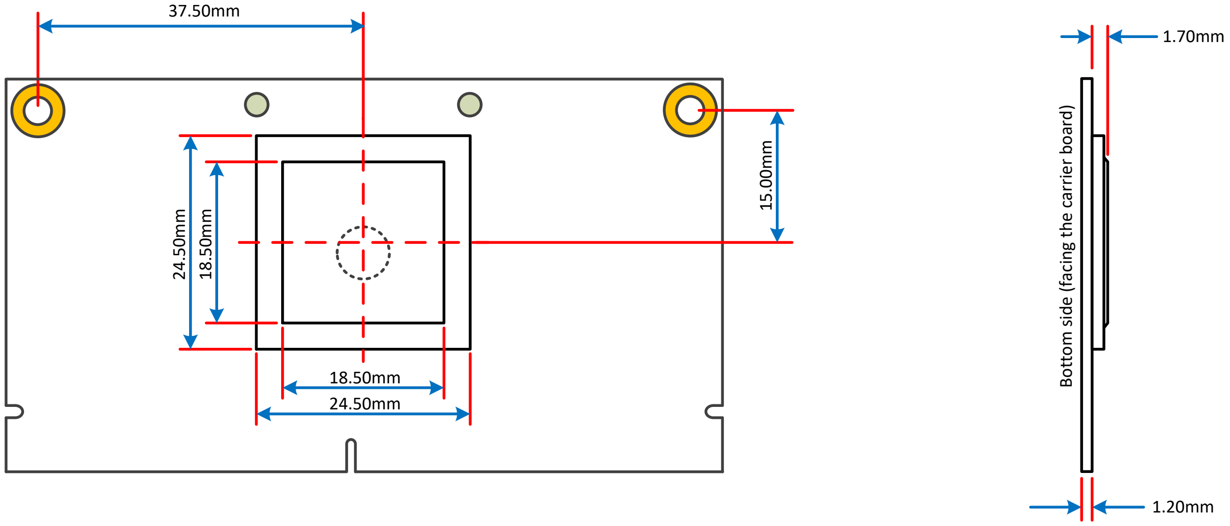

Figure 16 Mechanical position of Tegra T30 SoC (top view)
Tolerance for all measures: +/- 0.1mm

9.5.1 Sockets for the Apalis Modules

The Apalis module uses the MXM3 (Mobile PCI-Express Module) edge connector. This connector is available from different manufacturers in different board-to-board stacking height from 2.3mm to 11.1mm. Toradex recommends using the JAE MM70-314B1-2-R300, which has a board-to-board height of 3.0mm. This stacking height allows using the MXM SnapLock (TM) system to fix the module to the carrier board.

You can refer to a list of other MXM3 connectors on the developer website. Please also check the Apalis Carrier Board Design Guide for more information on recommended sockets and footprints.

9.6 Thermal Specification

Table 9-3 1.1 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Apalis T30	Operating temperature range[1]	0		70	°C
Apalis T30 IT	Operating temperature range[1]	-40		85	°C
Apalis T30 Apalis T30 IT	Storage Temperature (SoC limits the lower temperature, eMMC flash memory the upper)	-40		85	°C
Apalis T30	Operation temperature as sensed form Thermal Diode	-20		90	°C
Apalis T30 IT	Operation temperature as sensed form Thermal Diode	-40		105	°C
Apalis T30 Apalis T30 IT	Thermal Design Power at max Temperature Tegra Chip and DDR RAM		5		W
Apalis T30 Apalis T30 IT	Thermal Resistance Junction-to-Ambient, Tegra Chip only. (Theta-JA) [2]		11.6		°C/W
Apalis T30 Apalis T30 IT	Thermal Resistance Junction-to-Case, Tegra Chip only. (Theta-JC) [2]		1.18		°C/W
Apalis T30 Apalis T30 IT	Thermal Resistance Junction-to-Top of Package, Tegra Chip only, (Psi-JT) [2]		0.89		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC Board, as defined by JEDEC Standard JESD51-9. Test Boards for Area Array Surface Mount Package Thermal Measurements were used for thermal modeling to determine thermal performance. Ambient Temp 55° Celsius, No Airflow

The Apalis T30 incorporates DVFS (Dynamic Voltage and Frequency Switching) and Thermal Throttling, enabling the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. This allows the Apalis T30 to deliver higher performance at lower average power consumption compared to other solutions.

General Consideration Regarding the Thermal Behavior

- The power consumption and, therefore, the generated heat are heavily dependent on the currently running software. Therefore, it is impossible to provide a general guideline on which cooling solution is required at which ambient temperature.
- If you need the full CPU/graphics performance over a long time, we recommend adding a cooling solution.
- Toradex provides a heatsink for the Apalis T30. This solution can be used passively as well as in combination with a fan. More information can be found here: https://developer.toradex.com/products/apalis-heatsink
- If you only use the peak performance for a short time, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- The SoC silicon temperature has a significant impact on power consumption, which amplifies any cooling solution's effect. The more effective the thermal solution is at dissipating heat, the more performance you can get out of the Apalis T30 Module.
- A lower die temperature also lowers power consumption due to smaller leakage currents.
- Due to production variations, not all T30 SoC consumes the same power. Especially in idle, the power consumption can vary between different SoC. This means even modules from the same production batch can have a different temperature behavior. This is normal and often called “Silicon Lottery”.

9.6.1 Temperature Monitoring

The Apalis T30 modules come with an LM95245 temperature monitoring chip.
The LM95245 monitors two temperatures

- Local: temperature of the temperature sensor chip
- Remote: temperature of the T30 silicon

Beside the I^2C bus, the LM95245 features two outputs that get active if any temperature rises above a programmable threshold:

- nOS: This is a simple digital IO that can be monitored by the operating system. The reaction to this signal depends on the software.
- nT_CRIT: This output is hard wired to the power supply and turns off the CPU power rails if it becomes active.

After power-up, all temperature thresholds are at their default values:

LM95245 output	Remote (T30)	Local (LM95245)	Unit
nT_CRIT	110	85	°C
nOS	85	85	°C

These threshold temperatures are adjusted while booting the operating system. Please refer to the documentation on http://developer.toradex.com/knowledge-base/apalis-colibri-t30-temperature-monitoring for details.

The default values remain active until the operating system has booted. At very high temperatures, the thermal monitor may shut down the power supplies before the OS can increase the nT_CRIT temperature threshold.

9.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at http://www.toradex.com/support/product-compliance

DISCLAIMER: