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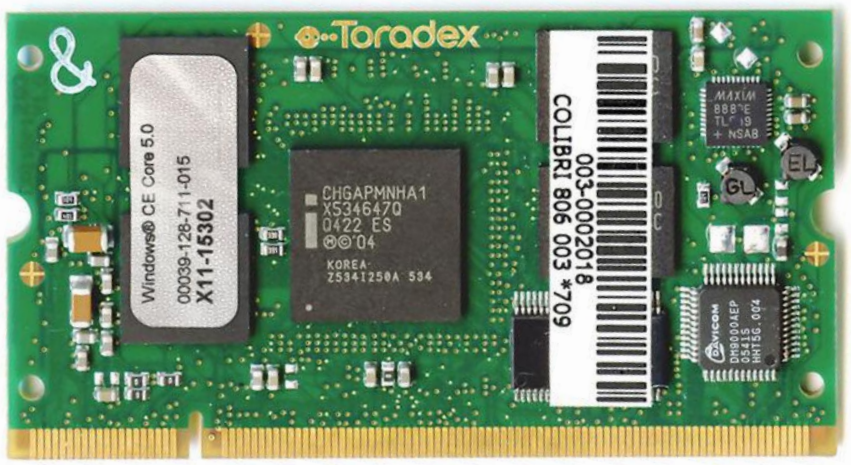
Colibri XScale® PXA3xx

CPLD Description



Revision history

Date	Doc. Rev.	Changes
25-Nov-08	Rev. 1.0	Initial Release
23-Mar-10	Rev. 1.1	-Update Bootloader to CPLD Matching Table -Update chapter 1.1 with the new Bootloader behavior
20-Dec-10	Rev. 1.2	-Update Bootloader to CPLD Matching Table -Added block diagram -Added Timing settings
24-Oct-11	Rev. 1.3	-Updated disclaimer
13-Apr-12	Rev. 1.4	-Added required register settings in order to program CPLD (chapter 2.1.1)

Contents

1. Introduction 4
1.1 CPLD Firmware 4
1.2 Bootloader to CPLD Matching Table 4
2. CPLD Register Description 5
2.1 External Chip Selects 5
MEM Ctrl Signals 7

1. Introduction

The Colibri PXA3xx modules contain a CPLD for different purposes. There is also more information about the CPLD on our developer website (http://developer.toradex.com).

1.1 CPLD Firmware

The Colibris are delivered with a CPLD firmware version which fits the installed boot loader. The CPLD Firmware is included in the bootloader and we do also provide the firmware as bin files together with the newest Win CE Image updates. Make sure the Boot loader version and the CPLD firmware version fits together, please see also the table in chapter 1.2.

You can use the Update Tool to check the firmware version.
To do an update you use the CPLD file provided in the Win CE Updates files on our server. The update with the Win CE Update tool works the same way than a Win CE update.
Alternative you can also use the bootloader to do the update. In this case press “p” in the boot loader menu.

Before you read the firmware version or perform a CPLD update, make sure you don’t interference with the SODIMM pins 88, 90 and 92.
The Colibri drives pin 88 and pin 92. Pin 90 is used as an input. (On the Evaluation board this pins are not used by default.)

The change log for the CPLD firmware can be found in the bootloader change log file.
For more information about the bootloader and the Update Tool visit our developer website (http://developer.toradex.com).

1.1.1 Bootloader Version 3.2 and older

In bootloader versions 3.2 and older the CPLD firmware gets automatically updated if the firmware version in the bootloader is newer. In the opposite a downgrade is not performed automatically but can be done manually. There is an unambiguous relation between bootloader version and CPLD firmware version (See table below). To update the CPLD version just install the corresponding bootloader and the update is done the first time the new bootloader is started.
To downgrade the CPLD version, install the corresponding bootloader version and press “p” in the bootloader menu.
Bootloader versions 3.2 and older are checking the CPLD firmware version on every start of the system. Make sure this doesn’t interference with your HW on SODIMM pins 88, 90, and 92

1.2 Bootloader to CPLD Matching Table

This table contains release versions only (no Beta versions).

Bootloader Version	CPLD Version
V 3.0	V 1.3
V 3.1	V 1.3
V 3.2	V 1.5
V 3.3	V 1.5
V 3.4	V 1.6
V 3.5	V 1.6
V 3.6	V 1.6
V 3.7 and newer	V 1.8

2. CPLD Register Description

2.1 External Chip Selects

2.1.1 All CPLD Firmware Versions

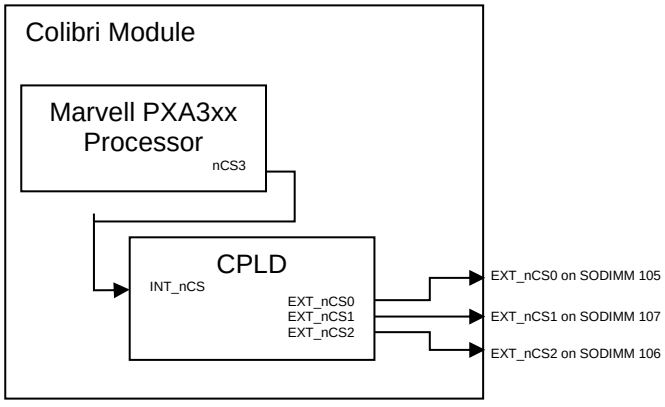
On the Colibri PXA3xx modules there is only one chip-select signal available. This CS is spitted into three address spaces. This is done via CPLD on the modules. Those CS are available on the SODIMM pins 105, 106 and 107. You have to enable them by writing the CPLD CS_CTRL register. All the EXT_nCSx have the same behavior (timings, VLIO, SRAM, etc.). You can change them by modifying the PXA3xx nCS3 registers (e.g. CSADRCFG3, MSC1, etc.).
Set all the GPIOs that are multiplexed with these signals to input before enabling the CS.
All CS are disabled after Reset.

PXA3xx Timing settings
To be able to program the on-module CPLD the following settings need to be met:
PXA register CSADRCFG3 (0x4A00_008C): 0x0032489
PXA register MSC1 (0x4A00_000C): 0x0009nnnn (do not change the n bits)
There are many other combinations which will work. We recommend do use the above settings in order to program the CPLD. After programming it, you are free to adjust the CSADDRCFG3 and MSC1 registers according to your needs except for the ALT bits in register CSADDRCFG3 which has to be set to 3 (0b11) all the time.
Please also visit our developer website (http://developer.toradex.com).

2.1.2 CPLD Firmware Version 1.5 and higher

To connect an AAD-multiplexed device on the DFI bus the corresponding EXT_nCSx_EC_EN (early chip-select enable) has to be set.
If the early chip-select feature is enabled the EXT_nCSx will be asserted simultaneously with the nCS3 of the PXA processor. This is needed if the external device is an AAD-device that does the demultiplexing of the data-address bus by itself.
If the early chip-select feature is disabled, the EXT_nCSx is asserted after the first address phase on the AAD-bus. This is the default behavior of the Colibri and should be used for normal (discrete address and data lines) devices.

2.1.3 Block diagram



2.1.4 EXT_nCSx memory map

0x1780_0000	CPLD Register block (8MB)
0x1700_0000	EXT_nCS2 (8MB)
0x1600_0000	EXT_nCS1 (16MB)
0x1400_0000	EXT_nCS0 (32MB)

2.1.5 CPLD CS_CTRL register (0x1780_0000, write only (read prohibited), 16Bit access only)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_nCS2_EC_DIS	EXT_nCS1_EC_DIS	EXT_nCS0_EC_DIS	res	res	EXT_nCS2_DIS	EXT_nCS1_DIS	EXT_nCS0_DIS	EXT_nCS2_EC_EN	EXT_nCS1_EC_EN	EXT_nCS0_EC_EN	res	res	EXT_nCS2_EN	EXT_nCS1_EN	EXT_nCS0_EN

Bit	Name	Description
15	EXT_nCS2_EC_DIS	Disable the early chip-select feature for EXT_nCS2(default) (Supported in CPLD V 1.5 or higher)
14	EXT_nCS1_EC_DIS	Disable the early chip-select feature for EXT_nCS1(default) (Supported in CPLD V 1.5 or higher)
13	EXT_nCS0_EC_DIS	Disable the early chip-select feature for EXT_nCS0(default) (Supported in CPLD V 1.5 or higher)
12	res	Reserved
11	res	Reserved
10	EXT_nCS2_DIS	Disable the EXT_nCS2 (on SODIMM PIN 106) (default)
9	EXT_nCS1_DIS	Disable the EXT_nCS1 (on SODIMM PIN 107) (default)
8	EXT_nCS0_DIS	Disable the EXT_nCS0 (on SODIMM PIN 105) (default)
7	EXT_nCS2_EC_EN	Enable the early chip-select feature for EXT_nCS2 (Supported in CPLD V 1.5 or higher)
6	EXT_nCS1_EC_EN	Enable the early chip-select feature for EXT_nCS1 (Supported in CPLD V 1.5 or higher)
5	EXT_nCS0_EC_EN	Enable the early chip-select feature for EXT_nCS0 (Supported in CPLD V 1.5 or higher)
4	res	Reserved
3	res	Reserved
2	EXT_nCS2_EN	Enable the EXT_nCS2 (on SODIMM PIN 106)
1	EXT_nCS1_EN	Enable the EXT_nCS1 (on SODIMM PIN 107)
0	EXT_nCS0_EN	Enable the EXT_nCS0 (on SODIMM PIN 105)

MEM Ctrl Signals

The Signals nPREG, nPCE1, nPCE2, nPXCVREN for PCMCIA functionality are provided on Colibri PXA320 via the CPLD. The Toradex WinCE driver for PCMCIA takes care about these signals.
RdnWE and nOE (on SODIMM pin 97) are provided on all Colibri PXA3xx via the CPLD on the Colibri module. To enable them you have to write the CPLD MEM_CTRL register.
Set all the GPIOs that are multiplexed with these signals to input before enabling the signals. There are a few GPIO's with no alternate function GPIO. Set the alternate function to 7 to tristate them. See the Colibri PXA datasheet for more details.

All the signals are disabled by default (reset).

Please also visit our developer website (http://developer.toradex.com).

2.1.6 CPLD MEM_CTRL register (0x1780_0004, write only(read prohibited), 16Bit access only)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	res	res	res	res	res	nOE_DIS	RDnWR_DIS	CF_DIS	res	res	res	res	res	nOE_EN	RDnWR_EN	CF_EN

Bit	Name	Description
15:11	res	Reserved
10	nOE_DIS	Write this bit to 0x1 to disable the nOE signal on SODIMM pin 97.
9	RDnWR_DIS	Write this bit to 0x1 to disable the RDnWR signal from PXA.
8	CF_DISABLE	Write this bit to 0x1 to disable the PCMCIA control signals.
7:3	res	Reserved
2	nOE_EN	Write this bit to 0x1 to enable the nOE signal on SODIMM pin 97. (Compatible to nPOE mapping on Colibri PXA270)
1	RDnWR_EN	Write this bit to 0x1 to enable the RDnWR signal from PXA.
0	CF_ENABLE	Write this bit to 0x1 to enable the PCMCIA control signals.